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Quasi-Resonant Control DC/DC converter and Power Factor Correction converter IC for AC/DC Converter

BM1051F

●General Description

BM1051F is compounded LSI of Power Factor Correction converter (PFC) for harmonic solution and DC/DC converter (DC/DC). Because DC/DC operates on Quasi-resonant method, DC/DC contributes to Low EMI.
BM1051F built in a HV starter circuit that tolerates 650V. Because of putting the current sense resistors externally both the PFC part and the DC/DC part, IC enables power supply design free.

In the PFC part, IC adopts peak current control operation. Suitable application is proposed by a various protection circuit, such as the multiplier with a revision circuit on the AC voltage falls, the load regulation revision circuit, and the maximum power feed-forward circuit, etc.

The Quasi-resonant system of a DC/DC part contributes to low EMI because PFC operates by soft switching.
A burst mode is built in, so the power is reduced at light load. Various protection functions, such as a soft start function, a burst function, an over-current limiting for every cycle, overvoltage protection, and over current protection, are built in. The pin for communicated control with a controller and the external stop pin are prepared; it proposes the system that can be adapted for various applications.

●Basic specifications

- Operating Power Supply Voltage Range:
  VCC：8.0 to 24.0V
- Operating Current:
  QR ON (PFC OFF)：1.20mA(pulse on)
  QR ON (PFC OFF)：1.00mA(pulse off)
  QR ON (PFC ON)：1.80mA(pulse on)
- Oscillation Frequency QR part :120kHz(FB=2.0V typ)
- Operating Temperature: -40℃ to +85℃

●Typical Application Circuit(s)

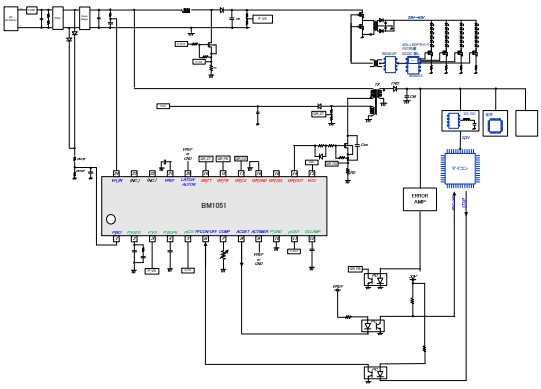

Figure 1. Application circuit

●Features

- Quasi-resonant circuit + PFC circuit
- Built-in HV Starter circuit
- Low consumption current (typ.10uA) when starter circuit is OFF.
- Quasi resonant circuit
  Max operating frequency(120kHz)
  Frequency reduction function
  Over-current limiting variable function
  Pulse-by-pulse over-current protection circuit
  Built-in Soft start
  Voltage protection function (brown out) during low input
  ZT pin Over Voltage Protection
  Output overload protection (auto recovery /latch switching enabled)
  250nsec Leading-Edge Blanking
- Power Factor Correction circuit
  Peak current control (65kHz)
  Per-cycle over current protection circuit
  Maximum power revision
  the multiplier with a revision circuit when the AC voltage falls
  the load change measure circuit
- Selectable protection method by LATCH/AUTOR terminal.
  LATCH/AUTOR=H : Latch
  LATCH/AUTOR=L : Auto recovery
- External stop function (COMP pin)
- AC input voltage stop detected function (ACDET)
- Built-in PFC stop terminal (PFCON/OFF)

●Package(s)

SOP24	15.0mm×5.40mm	×1.80mm	pitch1.27mm	
	(Typ.)	(Typ.)	(TYP.)	(TYP.)

●Applications

TV, AC adapters, printers, LED lighting

○Product structure：Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays

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●Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Rating	Unit	Conditions
Maximum applied voltage 1	V_{max1}	650	V	VH_IN
Maximum applied voltage 2	V_{max2}	30	V	VCC, QR_SEL
Maximum applied voltage 3	V_{max3}	5.5	V	P_BO, P_VSEO, P_VS, P_BOPK P_CS,PFCON/OFF,COMP, ACDET, ACTIMER,QR_CS, QR_ZT, QR_FB,LATCH/AUTOR, VREF
Maximum applied voltage 4	V_{max4}	15	V	GCLAMP, P_OUT, QR_OUT
output peak current 1	I_{OH}	-0.5	A	QR_OUT, P_OUT
output peak current 2	I_{OL}	1.0	A	QR_OUT, P_OUT
QR_ZT pin current 1	I_{SZT1}	-2.0	mA	
QR_ZT pin current 2	I_{SZT2}	3.0	mA	
Allowable dissipation	P_d	687.6 (Note1)	mW	
Operating temperature range	T_{opr}	-40 ～ +85	°C	
Maximum junction temperature	T_{jmax}	150	°C	
Storage temperature range	T_{str}	-55 ～ +150	°C	

(Note1) When mounted (on 70 mm × 70 mm, 1.6 mm thick, glass epoxy on single-layer substrate).
Reduce to 5.5 mW/°C when Ta = 25°C or above.

●Operating Conditions (Ta = 25℃)

Parameter	Symbol	Rating	Unit	Conditions
Power supply voltage range 1	VCC	8.0～24.0	V	VCC
Power supply voltage range 2	VH_IN	80～600	V	VH_IN
Power supply voltage range 3	P_BO	0.0～1.8	V	P_BO

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●**Electrical Characteristics (Unless otherwise noted, Ta=25, VH_IN=320Vdc, VCC=12V)**

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[Circuit current]						
Circuit current (ON) 1	I_{ON1}	0.700	1.200	1.700	mA	VCC=12.0V (QR=ON, PFC=OFF) QR_FB=1.0V (during pulse operation)
Circuit current (ON) 2	I_{ON2}	0.700	1.000	1.300	mA	VCC=12.0V (QR =ON, PFC=OFF) QR_FB=VREF (during pulse operation when OFF)
Circuit current (ON) 3	I_{ON3}	0.800	1.800	2.800	mA	VCC=12.0V (QR =ON, PFC=ON) QR_FB=1.0V (during pulse operation)
[Start circuit Block]						
Start current 1	I_{START1}	0.100	0.500	1.000	mA	VCC= 0V
Start current 2	I_{START2}	1.000	3.000	5.000	mA	VCC=10V
OFF Current	I_{START3}	-	10	16	uA	Input current from VH_IN terminal after releasing UVLO
VH voltage switched start current	V_{SC}	0.400	0.800	1.400	V	
[VREF Block]						
VREF output voltage	V_{REF1}	3.500	4.000	4.500	V	
VREF output capacitor	C_{REF}	0.68	1.00	2.20	uF	
GCLAMP voltage 1	GCL1	11.0	12.5	14.0	V	VCC=15V
GCLAMP voltage 2	GCL2	11.0	12.5	14.0	V	VCC=22V
VREF UVLO 1	V_{RUVLO1}	77.5 (3.100V)	87.5 (3.500V)	97.5 (3.900V)	%	When VREF rise The ratio of VREF pin voltage.
VREF UVLO 2	V_{RUVLO2}	52.5 (2.100V)	62.5 (2.500V)	72.5 (2.900V)	%	When VREF drop The ratio of VREF pin voltage.
VREF UVLO hysteresis	V_{RUVLO3}	-	25 (1.000V)	-	%	$V_{RUVLO3}= V_{RUVLO1}- V_{RUVLO2}$
VCC UVLO voltage 1	V_{UVLO1}	12.50	13.50	14.50	V	VCC rise
VCC UVLO voltage 2	V_{UVLO2}	6.00	7.00	8.00	V	VCC drop
VCC UVLO hysteresis	V_{UVLO3}	-	6.50	-	V	$V_{UVLO3}= V_{UVLO1}- V_{UVLO2}$
VCC OVP voltage 1	V_{OVP1}	24.0	27.0	30.0	V	VCC rise
VCC OVP voltage 2	V_{OVP2}	20.0	23.0	26.0	V	VCC drop
VCC OVP hysteresis	V_{OVP3}	-	4.0	-	V	$V_{OVP3}= V_{OVP1} - V_{OVP2}$
Brown out detection voltage 1	V_{BO1}	0.350	0.400	0.450	V	P_BO rise
Brown out detection voltage 2	V_{BO2}	-	0.200	-	V	P_BO drop
Brown out hysteresis	V_{BO3}	-	0.200	-	V	$V_{BO3} = V_{BO1} - V_{BO2}$
Brown out detection delay time 1	T_{BO1}	21.8	32.0	42.2	ms	Times until ACDET logic change (ACTIMER=L)
Brown out detection delay time 2	T_{BO2}	87.0	128.0	169.0	ms	Times until ACDET logic change (ACTIMER=H)
Brown out detection delay time 3	T_{BO3}	170	250	330	ms	Times until PFC and QR stop

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●**Electrical Characteristics (Unless otherwise noted ,Ta=25,VH_IN=320Vdc,VCC=12V)**

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[ACDET pin characteristics]						
ACDET pin ON resister	R_{ACDET}	50	100	200	Ω	
[ACTIMER pin characteristics]						
ACTIMER pin input L level	$V_{ACTIMEL}$	-	-	0.3	V	
ACTIMER pin input H level	$V_{ACTIMEH}$	1.2	-	-	V	
ACTIMER pin pull-down resistor	$R_{ACTIMEH}$	165	330	500	kΩ	
[PFCON/OFF pin characteristics]						
PFCON/OFF pin input L level	$V_{PON/OFFL}$	-	-	0.3	V	PFC = ON
PFCON/OFF pin input H level	$V_{PON/OFFH}$	1.2	-	-	V	PFC = OFF
PFCON/OFF pin pull-down resistor	$R_{PON/OFFH}$	50	100	150	kΩ	
PFCON/OFF pin timer time	$T_{PFCON/OFF}$	0.50	1.50	3.00	ms	
[LATCH/AUTOR pin characteristics]						
LATCH/AUTOR pin input L level	V_{MODEL}	-	-	0.3	V	
LATCH/AUTOR pin input H level	V_{MODEH}	1.2	-	-	V	
LATCH/AUTOR pin pull-down resistor	R_{MODEH}	50	100	150	kΩ	
[COMP pin characteristics]						
COMP pin detection voltage	V_{COMP}	0.370	0.500	0.630	V	
COMP pin pull-up resistor	R_{COMP}	19.4	25.9	32.3	kΩ	
External Thermistor resistor	R_T	3.32	3.70	4.08	kΩ	
Latch release voltage （VCC pin voltage）	$V_{LATCHOFF}$	-	V_{UVLO2} -0.5	-	V	
Latch mask time	T_{COMP}	70	150	240	us	

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●**Electrical Characteristics (Unless otherwise noted Ta=25, VH_IN=320Vdc, VCC=12V)**

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[Quasi-resonant Control Block]						
[Quasi-resonant DC/DC converter Block (turn off)]						
QR_FB pin pull-up resistance	R_{FB}	15	20	25	kΩ	
CS over-current detect voltage 1A	V_{lim1A}	0.950	1.000	1.050	V	I_{zt}<1.0mA
CS over-current detect voltage 1B	V_{lim1B}	0.630	0.700	0.770	V	I_{zt}>1.0mA
CS over-current detect voltage 1C	V_{lim1C}	-	0.250	-	V	I_{zt}<1.0mA
CS over-current detect voltage 1D	V_{lim1D}	-	0.750	-	V	I_{zt}<1.0mA
CS over-current detect voltage 2A	V_{lim2A}	-	0.150	-	V	QR_FB=0.3V (I_{zt}<1.0mA)
CS switched ZT current	I_{ZT}	0.800	1.000	1.200	mA	
CS Leading Edge Blanking time	T_{LEB}	-	0.250	-	us	
Turn off time	T_{OFF}	-	0.250	-	us	*1
Minimum ON width	T_{min}	-	0.500	-	us	$T_{LEB}+T_{OFF}$
[Quasi-resonant DC/DC converter Block (turn on)]						
Maximum operating frequency 1	F_{SW1}	106	120	134	KHz	QR_FB=2.00V
Maximum operating frequency 2	F_{SW2}	24	30	36	KHz	QR_FB=0.50V
Frequency reduction start FB voltage	V_{FBSW1}	1.15	1.250	1.350	V	
Frequency reduction end FB voltage	V_{FBSW2}	0.35	0.50	0.65	V	
Voltage gain	AV_{CS}	1.70	2.00	2.30	V/V	⊿V (QR_FB)/⊿V (QR_CS)
ZT comparator voltage 1	V_{ZT1}	60	100	140	mV	QR_ZT drop
ZT comparator voltage 2	V_{ZT2}	300	400	500	mV	QR_ZT rise
ZT trigger timeout period	T_{ZTOUT}	-	15	-	us	Count from final ZT trigger
[Quasi-resonant DC/DC converter protection functions]						
Soft start time1	T_{SS1}	0.60	1.00	1.40	ms	
Soft start time2	T_{SS2}	2.60	4.00	5.40	ms	
FB OLP Voltage 1a	V_{FOLP1A}	2.5	2.8	3.1	V	Operate QR_FB rise
FB OLP Voltage 1b	V_{FOLP1B}	-	2.6	-	V	Operate QR_FB drop
FB OLP Voltage 2a	V_{FOLP2A}	3.3	3.6	3.9	V	Switched latch / Auto recovery rise
FB OLP Voltage 2b	V_{FOLP2B}	-	3.4	-	V	Switched latch / Auto recovery drop
FB OLP mode switched external connected resistor	R_{FOLP2}	90	100	110	kΩ	QR_FB pin external resistance value (during latch mode)
FB OLP timer	T_{FOLP}	44	64	84	ms	
ZT OVP Voltage	V_{ZTL}	3.2	3.5	3.8	V	
[QR_OUT pin]						
QR_OUT pin PMOS ON resistor	R_{POUT}	5	15	30	Ω	
QR_OUT pin NMOS ON resistor	R_{NOUT}	2	5	10	Ω	
[QR_SEL pin]						
QR_SEL pin Ron	R_{MASK}	-	150	-	Ω	

*1 Pulse is applied to QR_CS pin
*2 Pulse is applied to QR_ZT pin

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●**Electrical Characteristics (Unless otherwise noted Ta=25, VH_IN=320Vdc, VCC=12V)**

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[Power Factor Correction（PFC）controller block]						
[Power Factor Correction (PFC) Gm amplifier block]						
P_VS pin pull-up current	I_{P_VS}	-	0.50	-	uA	
Gm amplifier normal voltage	V_{VSAMP}	2.460	2.500	2.540	V	
Gm amplifier trans-conductance	V_{VSGM}	30.8	44.0	57.2	uS	
Maximum Gm amplifier source current	I_{VSAMP1}	15	25	35	uA	P_VS=1.0V
Maximum Gm amplifier sink current	I_{VSAMP2}	24	40	56	uA	P_VS=3.5V
[Power Factor Correction (PFC) input voltage monitor block]						
P_BO input voltage range	V_{P_BOIN}	0.000	-	1.800	V	
P_BO pin leak current	I_{BOLEAK}	-1.00	0.00	1.00	uA	
[Power Factor Correction (PFC) input voltage peak detect block]						
P_BOPK max charge current	$I_{BOPKCHG}$	36	72	144	uA	
P_BOPK max discharge current	$I_{BOPKDIS}$	0.1	0.2	0.4	uA	
[Power Factor Correction (PFC) multiplier block]						
Multiplier constant	K_{MULTI}	0.37	0.54	0.71		
P_VSEO stop voltage 1	V_{VSEO1}	181	226	271	mV	BOPK=0.56V
P_VSEO stop voltage 2	V_{VSEO2}	88	128	168	mV	BOPK=1.30V
[Power Factor Correction (PFC) Oscillation frequency block]						
PFC Oscillation frequency	F_{PSW1}	60	65	70	KHz	
Minimum Pulse width	T_{min}	-	500	-	ns	
Maximum DUTY	D_{max}	90.0	94.0	98.0	%	
[Power Factor Correction (PFC) Driver block]						
P_OUT pin PMOS ON resistor	RP_{POUT}	5	15	30	Ω	
P_OUT pin NMOS ON resistor	RP_{NOUT}	2	5	10	Ω	

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●**Electrical Characteristics (Unless otherwise noted Ta=25, VH_IN=320Vdc, VCC=12V)**

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[Power Factor Correction (PFC) controller block]						
[Power Factor Correction (PFC) protection function block]						
Leading Edge Blanking time	T_{PLEB}	-	250	-	ns	
P_CS over current limit voltage 1	V_{PCS1}	0.93	1.16	1.40	V	P_BOPK=0.56V
P_CS over current limit voltage 2	V_{PCS2}	0.48	0.60	0.72	V	P_BOPK=1.30V
P_VS short protection voltage	V_{P_SHORT}	0.200 (-92%)	0.300 (-88%)	0.400 (-84%)	V	Figure of () is comparison with P_VS standard voltage 2.5V
QR power-limit P_VS voltage1	V_{PFCON}	1.800 (-28%)	2.000 (-20%)	2.200 (-12%)	V	Figure of () is the ratio of P_VS standard voltage 2.5V
QR power limit P_VS voltage2	V_{PFCOFF}	1.100 (-56%)	1.250 (-50%)	1.400 (-44%)	V	Figure of () is the ratio of P_VS standard voltage 2.5V
P_VS QR power limit hysteresis	V_{PFCHYS}	-	0.750 (30%)	-	V	Figure of () is the ratio of P_VS standard voltage 2.5V
P_VS gain rise voltage	V_{PGUP}	2.050 (-18%)	2. 250 (-10%)	2.450 (-2%)	V	Figure of () is the ratio of P_VS standard voltage 2.5V
P_VS gain fall voltage	V_{POVP1}	-	2.625 (+5%)	-	V	Figure of () is the ratio of P_VS standard voltage 2.5V
P_VS over voltage protection voltage	V_{POVP2}	-	2.725 (+9%)	-	V	Figure of () is the ratio of P_VS standard voltage 2.5V
P_VS over voltage protection timer	T_{POVP2}	16	32	48	ms	The time to detect P_VS over voltage protection

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●**PIN Configure**

Table 1. I/O Pin Functions

NO	PIN	I/O	Function	ESD protection system	
				VCC	GND
1	P_BO	I	Input AC Voltage monitor pin	○	○
2	P_VSEO	I/O	PFC gm amplifier output pin	○	○
3	P_VS	I	PFC Output voltage monitor pin	○	○
4	P_BOPK	O	Connected capacitor to the pin	○	○
5	P_CS	I	PFC Coil current monitor pin	○	○
6	PFCON/OFF	I	PFC ON/OFF control input pin	○	○
7	COMP	I	External latch stop pin	○	○
8	ACDET	O	Input AC voltage state communication pin	○	○
9	ACTIMER	I	Brown out detection time setting input pin	○	○
10	GND	I/O	GND	○	-
11	P_OUT	O	PFC Output drive pin	○	○
12	GCLAMP	I/O	Gate H level clamp pin	○	○
13	VCC	I/O	Power supply pin	-	○
14	QR_OUT	O	Quasi-resonant Output drive pin	○	○
15	QR_SEL	O	Quasi-resonant Mask pin	-	○
16	GND	I/O	GND	○	-
17	QR_CS	I	Quasi-resonant Over current detected pin	○	○
18	QR_FB	I	Quasi-resonant Feedback detected pin	○	○
19	QR_ZT	I	Quasi-resonant Zero cross detected pin	-	○
20	LATCH/AUTOR	I	Protection mode switched input pin	○	○
21	VREF	O	Internal power supply pin	○	○
22	-	-	-	-	-
23	-	-	-	-	-
24	VH_IN	I	AC Input voltage applied pin	-	○

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●I/O Equivalent Circuit Diagram

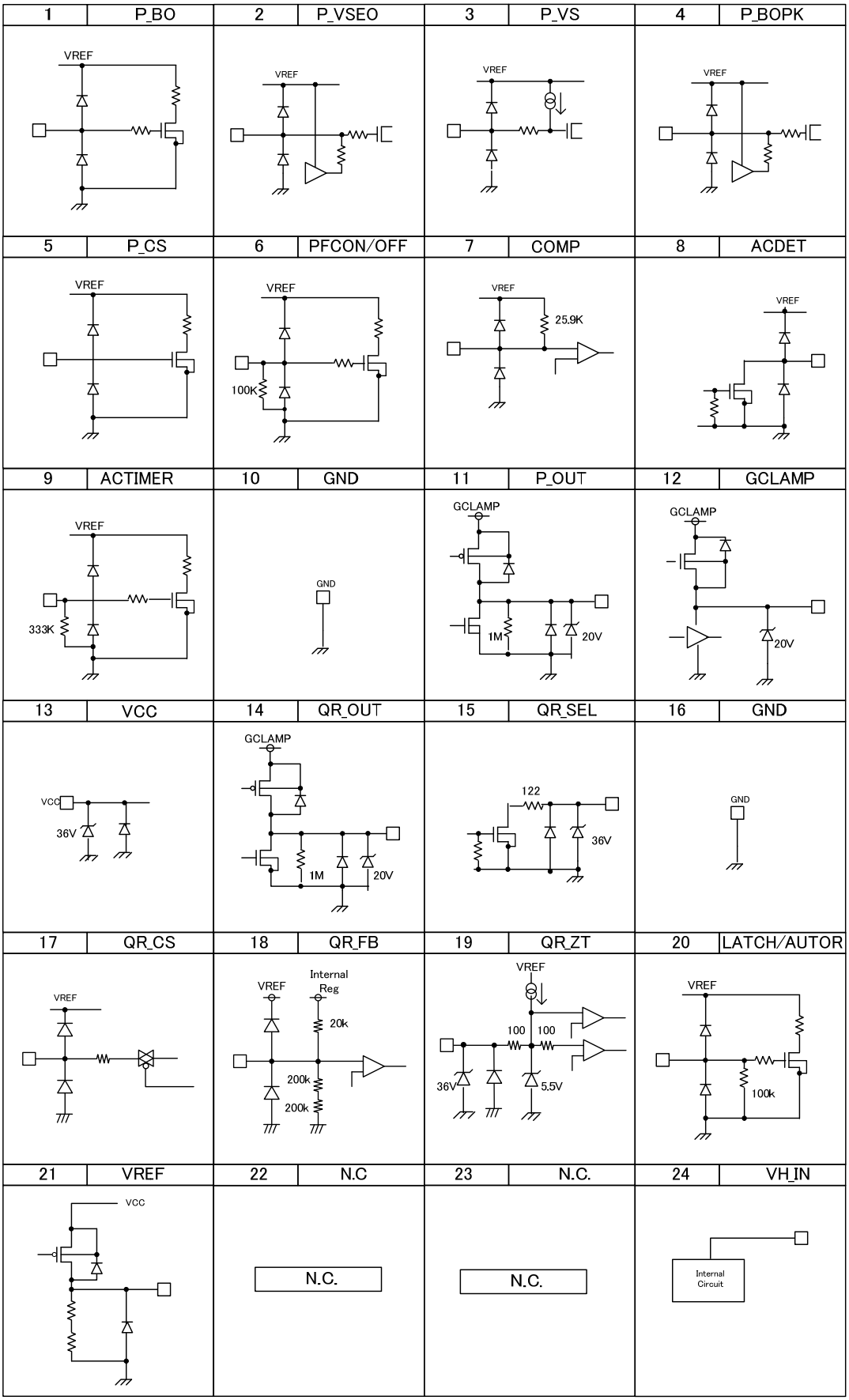

Figure 2. I/O Equivalent Circuit Diagram

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●Block Diagram

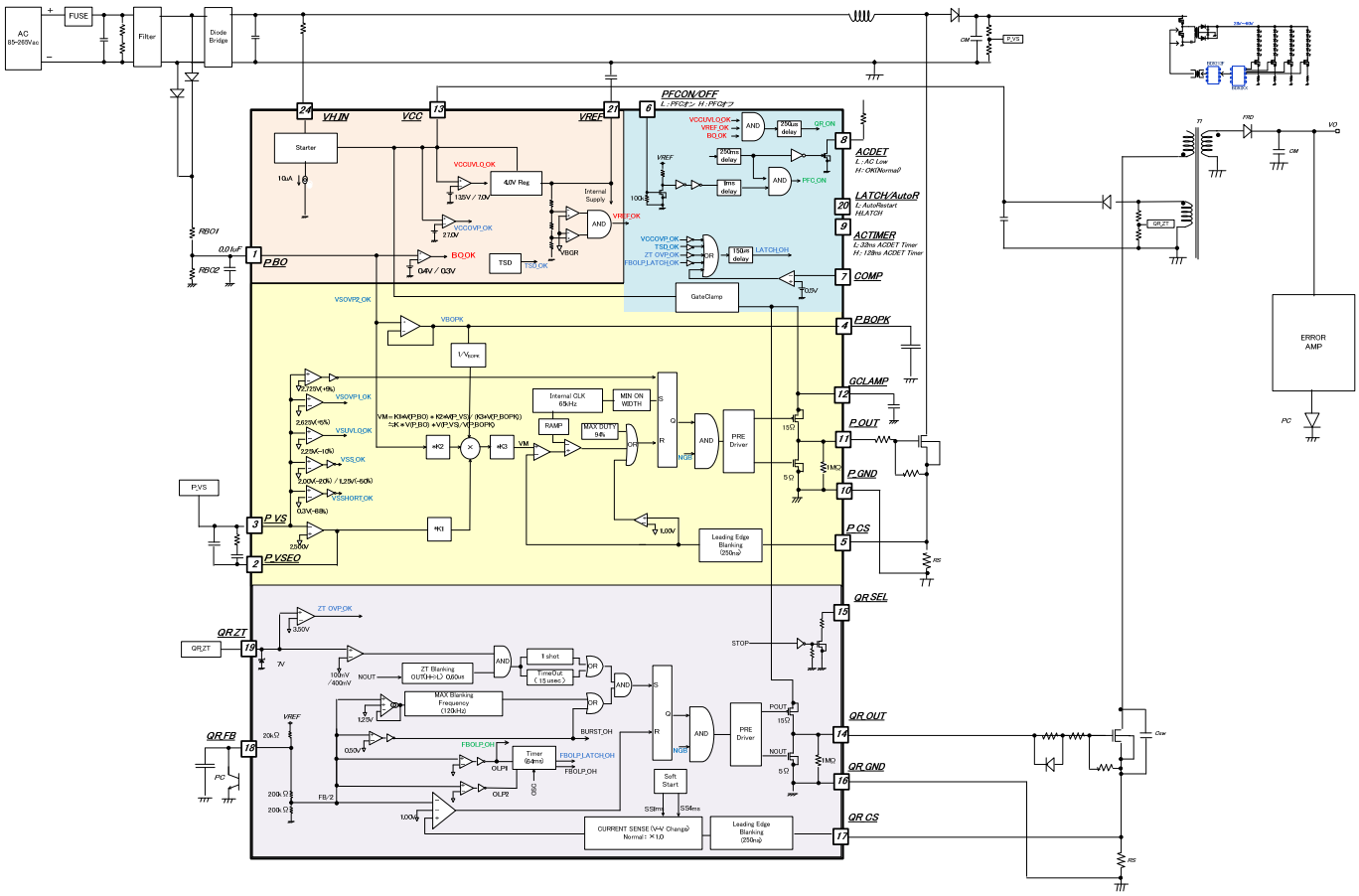

Figure 3. Block Diagram

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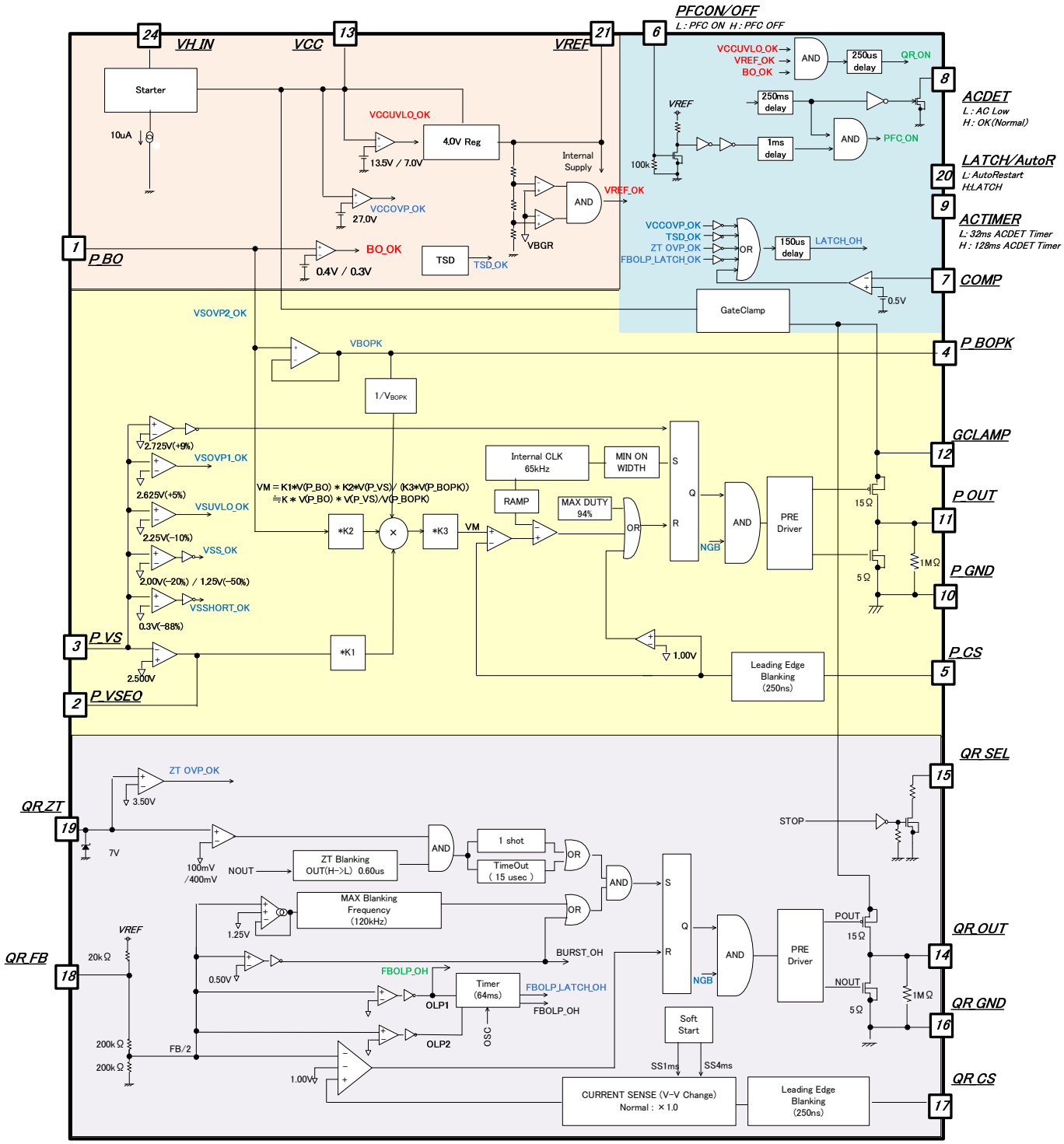

Figure 3-2. Block Diagram

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●**Explanation of each block**

(1) Starter block (24pin)

BM1051F built in the starter circuit that withstands 650V. For that, application used the IC is enabled faster start time and low standby power. After start-up, consumption power is idling current I_{START3} (typ=10uA) only.

Reference of start-up time is shown in Figure 4.

It can start-up less than 0.1sec when C_{VCC}=10uF.

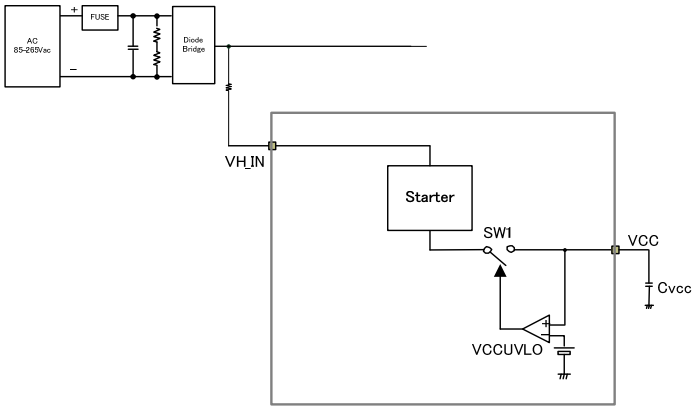

Figure 4. Start Circuit Block Diagram

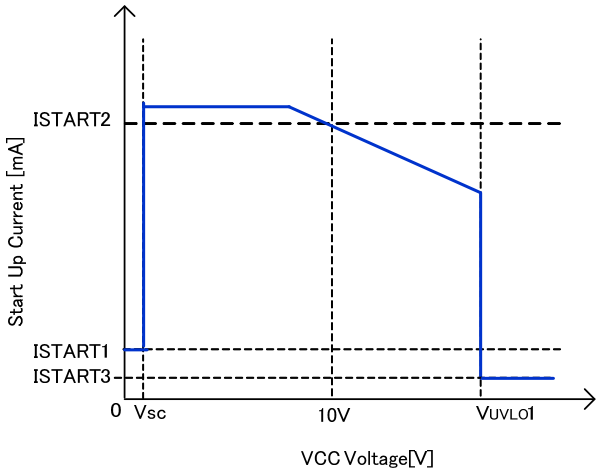

Figure 5. Start-up current vs VCC voltage

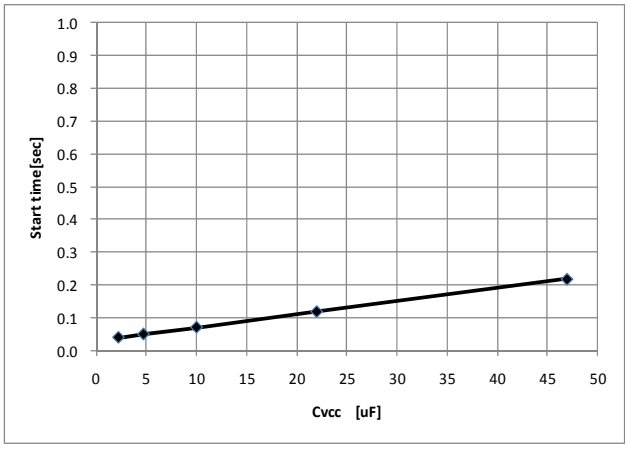

Figure 6. Start time vs C_{VCC} (Reference values)

*Start current flows from VH_IN pin to VCC pin.

ex) When V_{ac}=100V; consumption power of start-up circuit only.
PVH＝100V*√2*10uA=1.41mW

ex) When V_{ac}=240V; consumption power of start-up circuit only.
PVH＝240V*√2*10uA=3.38mW

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(2) Start sequence

The start sequence of IC operates DC/DC part, next PFC part (See the figure 7).

A : Input voltage VH is applied.

B : Charge current flows from VH_IN pin to the VCC pin capacitor. Then VCC pin voltage rises.

C : Monitor the AC voltage by P_BO pin. And confirm normal state by releasing brown out.

D :When V_{UVLO1} (typ=13.5V) < VCC pin, release the inside UVLO and ON the inside regulator VREF.

E : When V_{RUVLO1} (typ=87.5%) < VREF pin, release the inside VREFUVLO.

F : If the 'E' state continues constant period, DC/DC part starts because it recognizes normal state.
When the switching starts, VOUT voltage rises.
When the DC/DC start-up, please set external parts to be regulated output voltage within the T_{FOLP} period (64ms .typ).

[QR start-up operation]

G: This IC adjusts over current limiter of DC/DC by operation of soft start 1 against over voltage and current rising.
That term continues T_{ss1} (typ=1ms).

H: This IC adjusts over current limiter of DC/DC by operation of soft start 2 against over voltage and current rising.
Soft start 2 operation continues power limiter operation until P_VS pin voltage > V_{PFCON} (2.00V typ) and T_{SS2} (typ=4ms) .
This IC operates the state that maximum power of QR is 50% at this state.

I: If secondary voltage is setting value, QR_FB pin voltage is constant value corresponded load by current from photo coupler.
At normal state, QR_FB voltage is QR_FB<$V_{FBOLP1B}$ (2.60V typ).

[PFC start up operation]

J: At the point in I time, This IC recognizes that the part of DC/DC operation is normal, Part of PFC starts operation.

K: If P_VS pin voltage is upper V_{P_SHORT} (typ = 0.3V), this IC judges short detection normal.

L: P_VSEO voltage rises from 0V to prevent from over rising voltage and current at PFC part.
At this time P_OUT pin DUTY increase from 0% with P_VSEO voltage increasing.

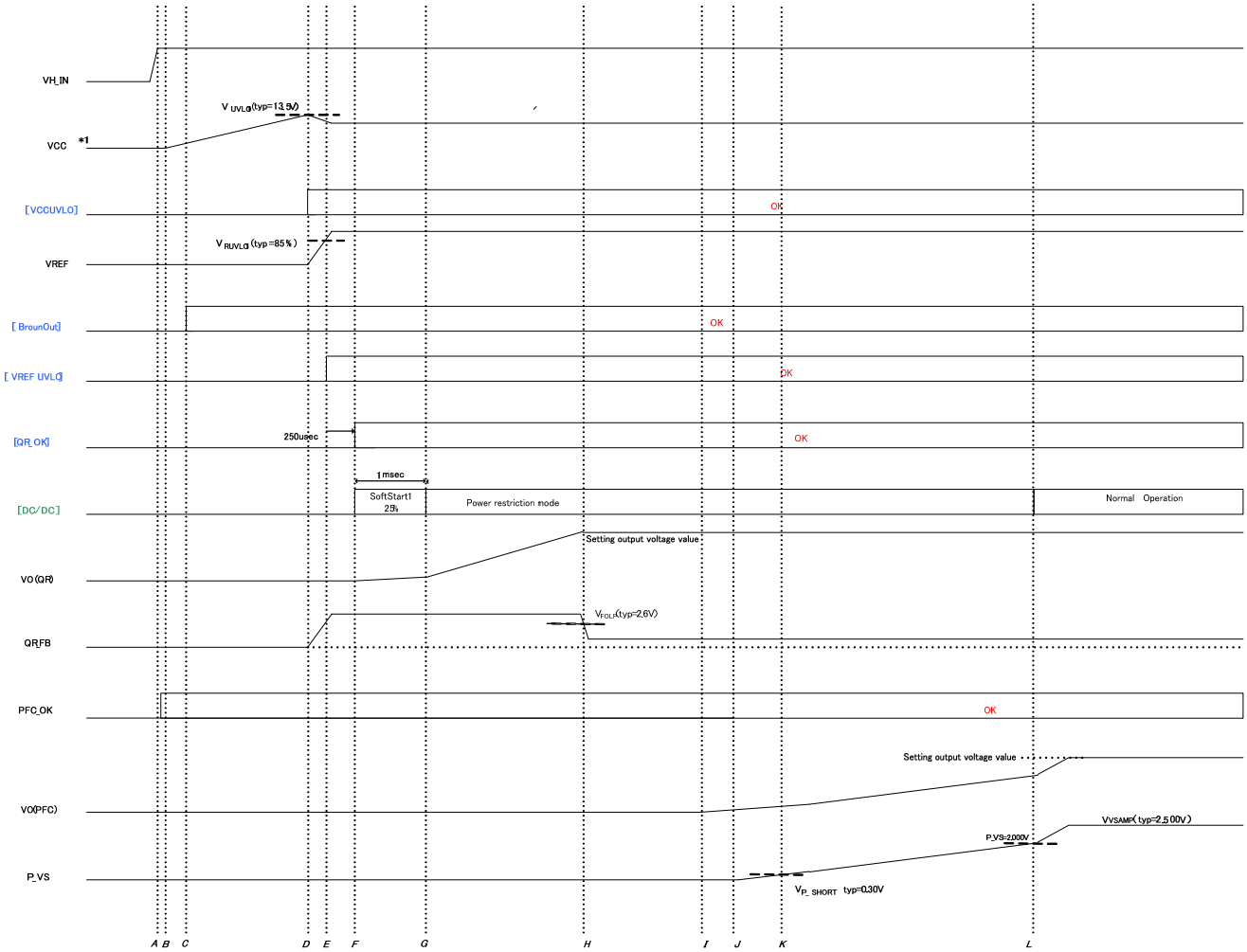

Figure 7. Start sequences Timing chart

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About figure7, condition is PFCON/OFF=L.
Start up operation is shown at figure8, 9 by the state shift figure.
Figure 8 is LATCH/AUTOR=L (auto return operation), and figure 9 is LATCH/AUTOR=H (LATCH operation)

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

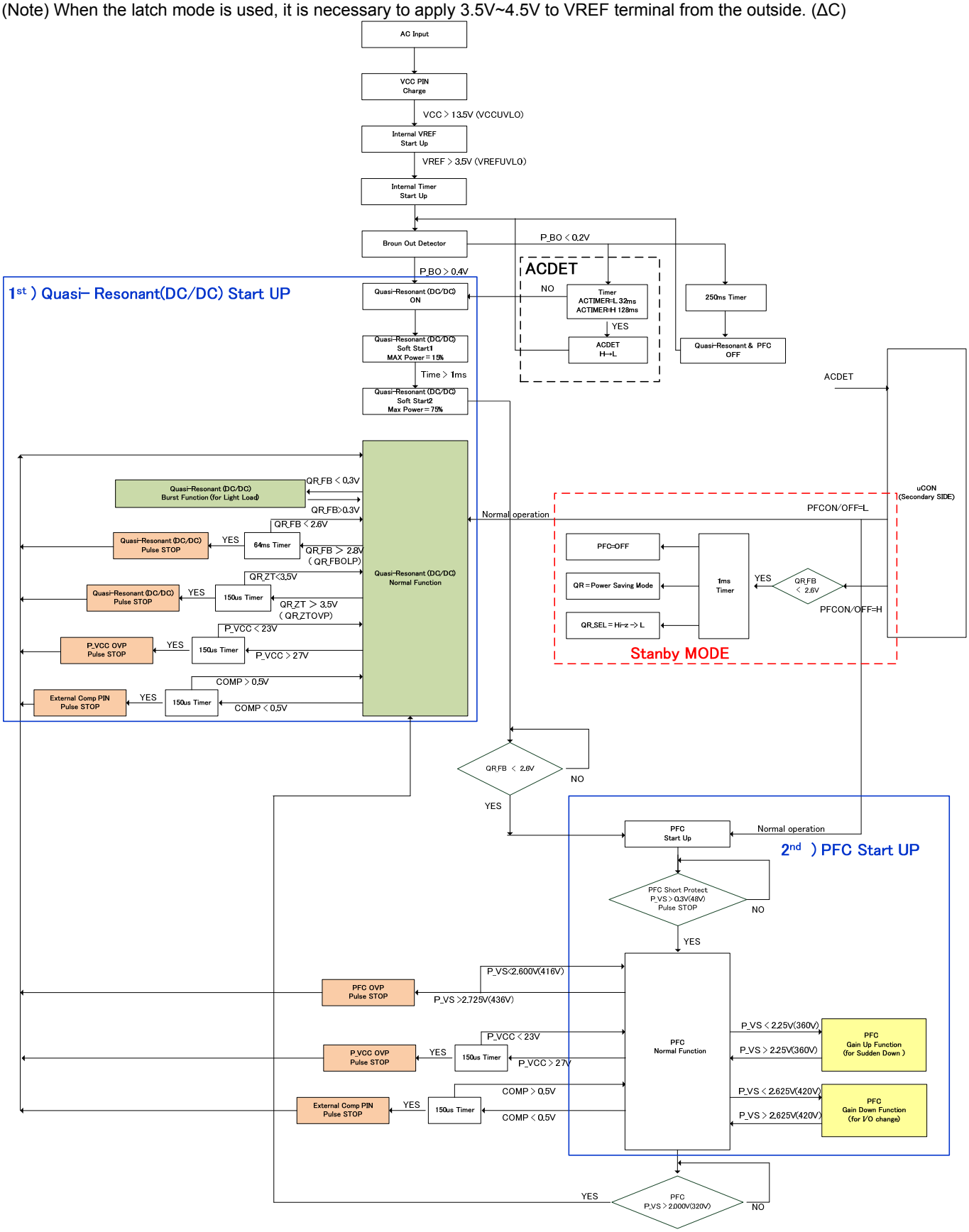

Figure 8. Diagram of state machine (LATCH/AUTOR=L)

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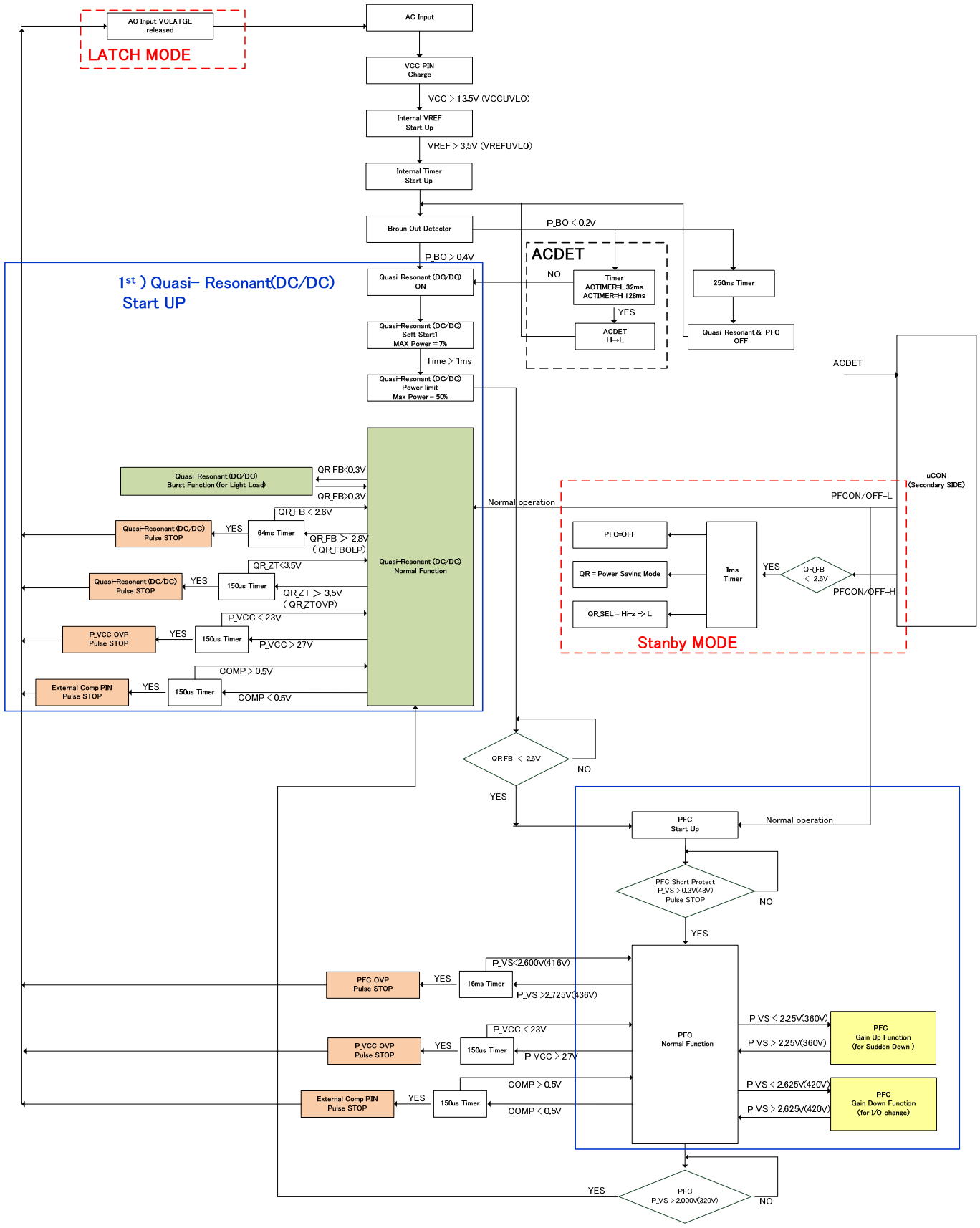

Figure 9. Diagram of state machine (LATCH/AUTOR=H)

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(3) VCC protection function and VREF pin function

(3-1) VCC pin protection function(13pin)

BM1051F built in VCC low voltage protection function of VCCUVLO (Under Voltage Lock Out) and over voltage protection function of VCC OVP (Over Voltage Protection).

This function monitors VCC pin and prevent VCC pin from destroying switching MOSFET at abnormal voltage.

VCCUVLO is auto recovery comparator that has voltage hysteresis. VCCOVP operates as latch mode comparator in the LATCH/AUTOR=H and as auto return comparator in the LATCH/AUTOR=L.

VCC<$V_{LATCHOFF}$ (typ = V_{uvlo1} - 0.5) is condition of latch release (reset) after detection of latch operation by VCCOVP.

Refer to the operation figure10.

VCCOVP built in mask time T_{COMP} (typ=150us), in case of continuing VCCOVP 150us, operates over voltage detection.

By this function, this IC masks pin generated surge etc.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

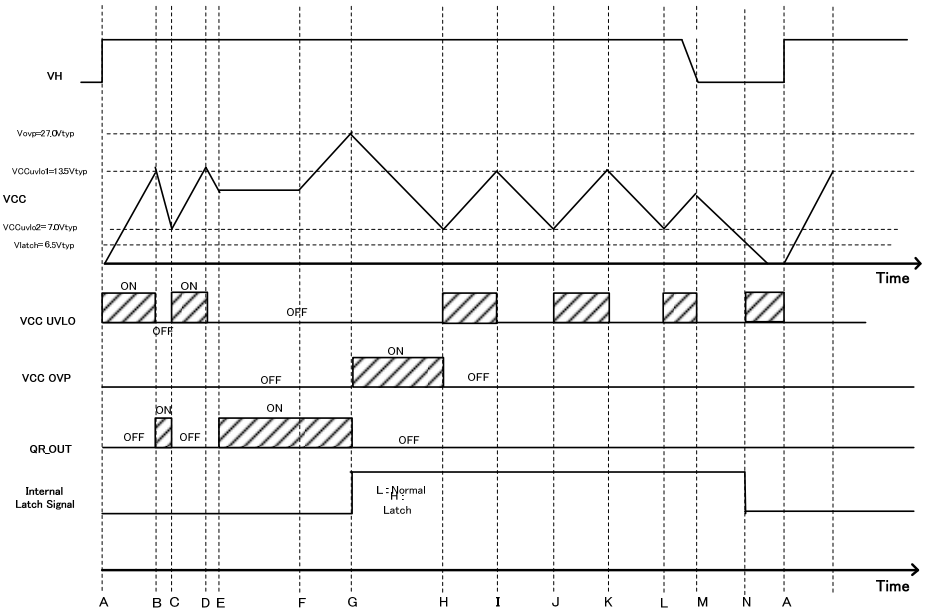

Figure10. VCC UVLO / OVP (LATCH/AUTOR=H at Latch stop)

A:VH input, VCC voltage rise

B:VCC>V_{uvlo1},DC/DC operation start

C:VCC<V_{uvlo2},DC/DC operation stop

D:VCC>V_{uvlo1},DC/DC operation start

E:VCC voltage decreases until starting DC/DC switching

F:VCC rise

F:When VCC>Vovp1,DC/DC operation is stopped. Switching is stopped by internal latch signal.

G:Then DC/DC operation is stopped, power supply is lost from auxiliary, VCC voltage downs.

H:VCC<Vuvlo2, VCC voltage rises for dropping IC's consumption current.

I:VCC>Vuvlo1, this IC dose not operate DC/DC for latch operation. VCC voltage drops because of dropping of IC's consumption current.

J:same of H

K:same of I

L:same of J

M:VH is open(the state is outlet out).VCC drops.

N:VCC <V_{COMP}, latch releases.

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(3-2) VREF pin function(21pin)

VREF pin is internal regulator output pin.
The use of VREF pin is IC's internal supply and connection of LATCH/AUTOR pin changing.
This pin needs an external capacitance, please use the capacitance following table.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

Table 2. VREF pin output capacitor capacitance

Parameter	Symbol	Specification			Unit	Conditions
		Minimum	Standard	Maximum		
VREF Output Capacitor	C_{REF}	0.68	1.00	2.20	uF	

(3-3) VREF pin protection function(21pin)

VREF pin built in low voltage protection function VREF UVLO (Under Voltage Protection).
This IC prevents from error operating at the time, VREF starts up and VREF is low, by this function.

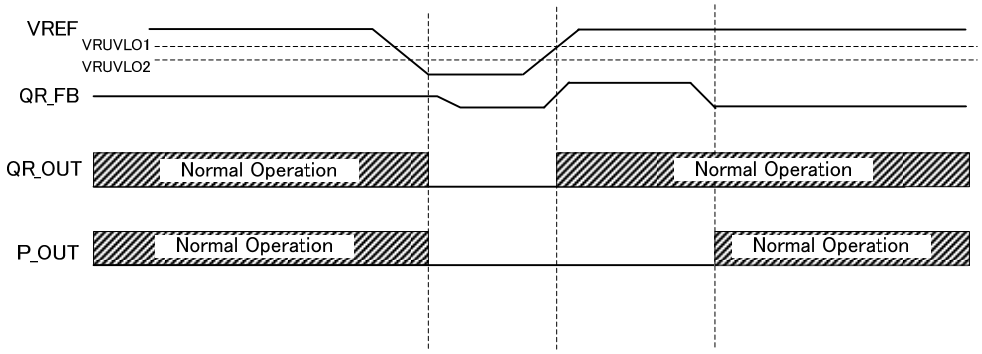

Figure11. VREF UVLO Function

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(3-4) Blown out function(1 pin)

BM1051F built in blown out function. This function is that this IC stops DCDC operating at the time when input AC voltage is low. Show the example figure12. This IC divides input voltage by the resistance, and input P_BO pin.

This IC detects from circuit normal state, and starts DC/DC operation the time when P_BO pin exceeds V_{bo1}(0.4V typ).

ACDET=L after T_{BO1}(typ.32ms) or T_{bo2}(typ.128ms) from P_BO pin drops from V_{BO2}(0.2V typ).

Moreover, if T_{BO3} (typ.250ms) passes from P_BO<V_{BO2}, DC/DC part and PFC part is stopped.

About every resistance of fugure12, because P_BO pin is used PFC operation, please set R_{bo1}=4Mohm,R_{bo2}=16kohm for operating the range of P_BO pin voltage 0~1.8V. In this case, by the following formula, P_BO=0V~0.56V at the case AC100V, P_BO=0V~1.237V at the case AC220V.

$$P\_BO = (\sqrt{2} \times V_{AC} \quad V_{F1}) \times \frac{R_{BO2}}{R_{BO1} + R_{BO2}}$$

Then

$$\sqrt{2} \times V_{AC} >> V_{F1}$$

$$P\_BO = \sqrt{2} \times V_{AC} \times \frac{R_{BO2}}{R_{BO1} + R_{BO2}}$$

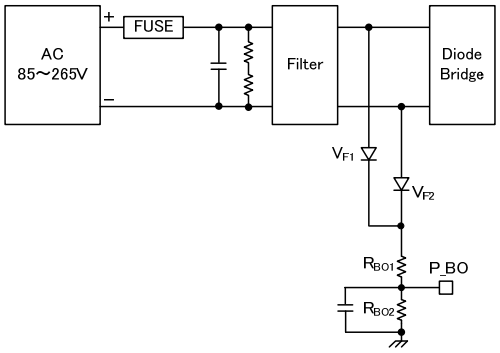

Figure12. Block Diagram of Blown out Function

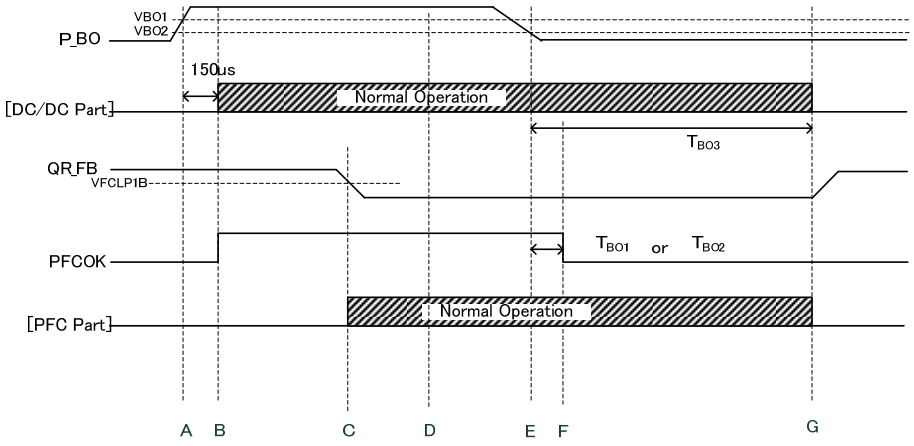

Figure13. Detection Way of Blown out Function

A : P_BO > V_{BO1}(typ.0.4V) 、ACDET=L->H

B: After 150us from A DC/DC part starts up.

C:QR_FB<V_{FCLP1B}(typ.2.6V). PFC part starts up.

D: If PFC output is larger than constant voltage, ACTIMER=L->H.

E: P_BO<V_{BO2}(typ.0.2V) Timer start operation by detection blown out protection.

F:After T_{BO1}(typ.32ms) or T_{BO2}(typ.128ms) from E, ACDET=H->L. It is possible to set T_{BO1} and T_{BO2} at ACTIMER pin

G:After T_{BO2}(typ.250ms) from E, DC/DC part and PFC part are OFF

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(4)Controller part

(4-1)ACDET pin (8pin)

ACDET pin is NMOS open drain output. It monitors AC voltage, and is used for controlling secondary micon.
Show the using example figure14, 15. Please set VIN is H voltage of micon.

ACDET=L ： Abnormal state（P_BO < 0.2V）

ACDET=H ： Normal state

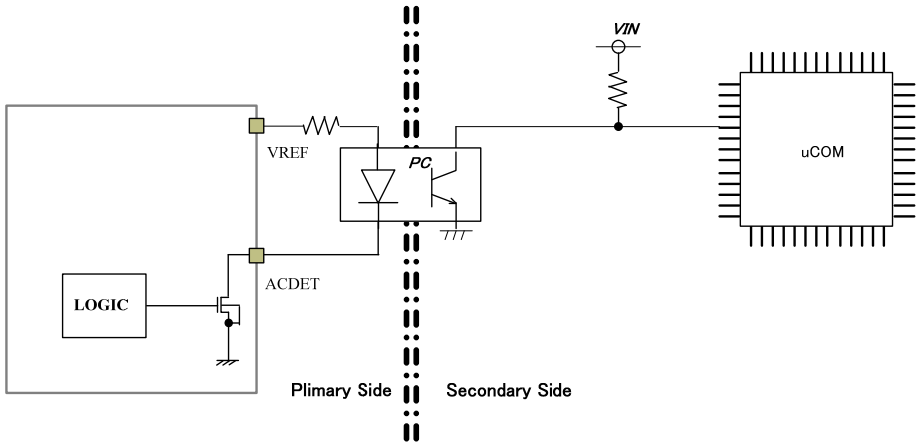

Figure14. Using Example of ACDET Pin

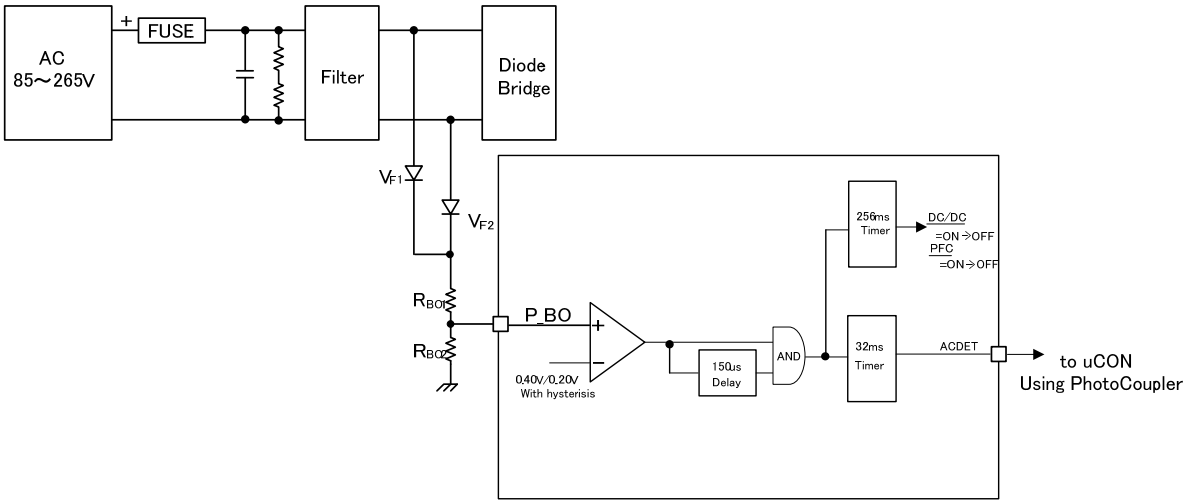

Figure15. Explanation of ACDET Pin

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Next, show an easy sequence.

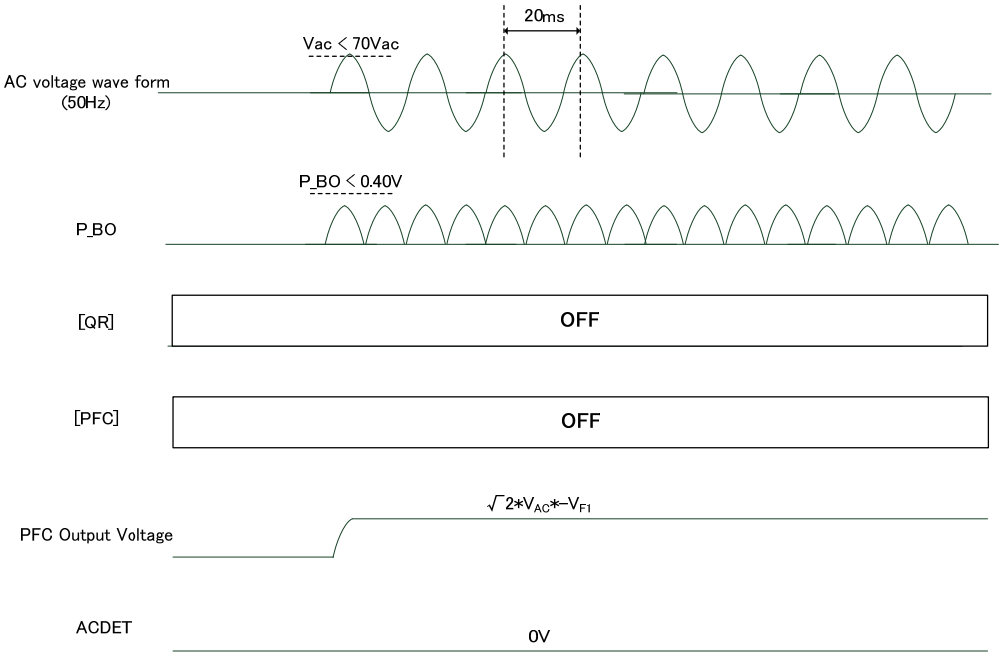

Figure16. At applied AC Input Voltage（P_BO voltage<0.4V）

Because P_BO < 0.4V, DC/DC part is OFF.
VCC voltage>13.5V

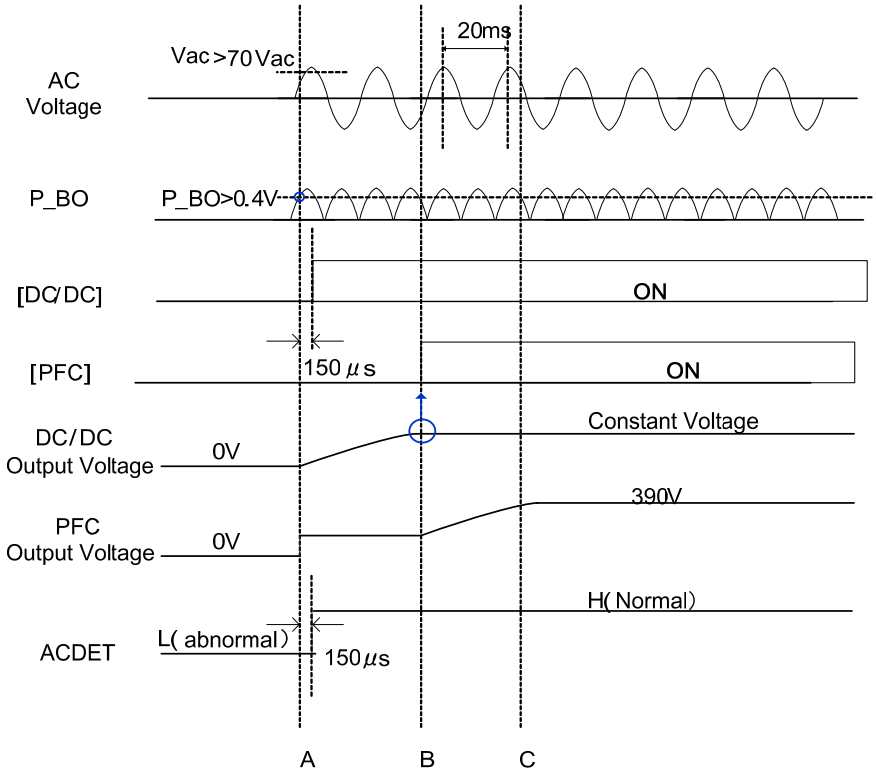

Figure17. At applied AC Input Voltage（P_BO voltage >0.4V）

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A：Detect P_BO＞0.4V, Quasi resonance starts operation After 150μs
B：PFC start up
C：PFC output stabilized
*About PFC operation, by the micon, is able to be controlled using PFCON/OFF pin.

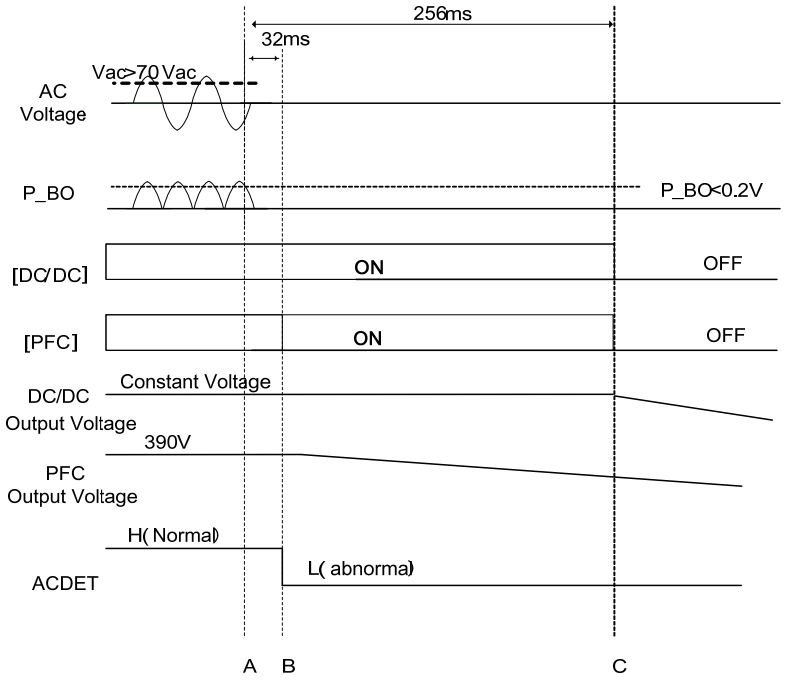

Figure18. At AC Power Supply OFF

A：Detect P_BO＜0.2V, internal ACDET timer operates. At this time, output of PWC downs.
B：After 32ms（ACTIMER=L）from the point A, ACDET pin voltage is H->L, send to the μ-controller abnormal signals.
C：After 250ms from the point of A,PFC and Quasi Resonant are stopped

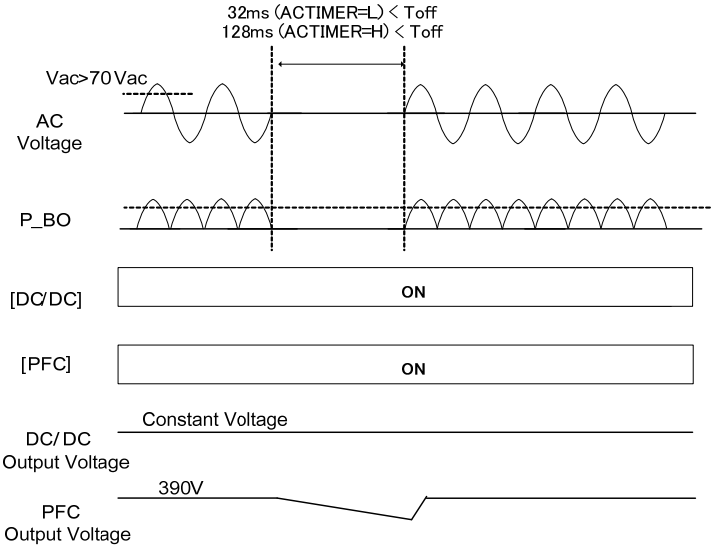

Figure19. At AC Power Supply the case of operation moment stop

The case of AC voltage is OFF suddenly, constant area is masked.
The time of constant area of masking is depends on ACTIMER pin.
The case of ACTIMER pin=L, Mask time=32ms、 the case of ACTIMER pin=H, mask time=128ms.
The moment of AC voltage momentary power interruption, because PFC output voltage is down by corresponding to load, please watch out.

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(4-3) PFCON/OFF pin

PFCON/OFF pin is NMOS gate input pin. Refer to following the functions.

An internal timer is integrated for noise protection on PFCON/OFF pin.

After $T_{PFCON/OFF}$(typ.1ms) from PFCON/OFF H→L, PFCON/OFF L operation starts. At PFCON/OFF L→H, internal timer is not integrated.

function1）PFC circuit operation is OFF control.

In order to reduce standby power, IC controls PFC part operation at PFCON/OFF pin.

function2）QR_SEL pin is Hi-z→L

Refer to example of using at figure 20.

PFCON/OFF=L ： DC/DC part＝ON、 PFC part＝ON、QR_SEL＝Hi-Z

PFCON/OFF=H ： DC/DC part＝ON、 PFC part＝OFF、QR_SEL=L

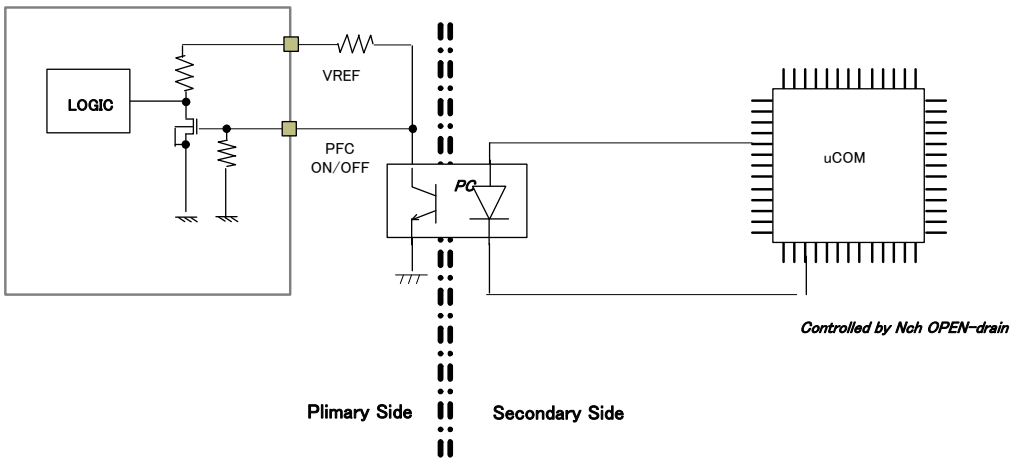

Figure20. Using example of PFCON/OFF pin

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(4-4) LATCH/AUTOR pin

LATCH/AUTOR pin is NMOS gate input pin. Refer to example of using at figure21.
Operation setting of protection function is shown at table3.

LATCH/AUTOR=L : Auto recovery
LATCH/AUTOR=H : Latch

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

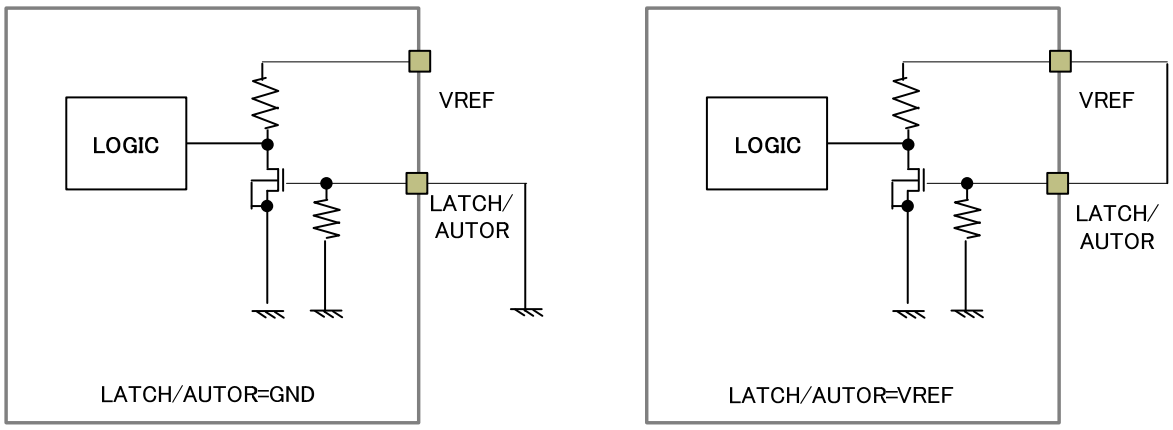

Figure21. Using example of LATCH/AUTOR pin

ITEM	Contents	LATCH/AUTOR=GND				LATCH/AUTOR			
		detection method	operation at detection	release mothod	operaetion at detection	detection method	operation at detection	release mothod	operaetion at detection
VREFUVLO	VREF PIN Low voltage protection function	VREF<2.5V (VREF falling)	PFC part, DC/DC part operation stops	VREF>3.5V (VREFrising)	PFC partDC/DC part enable to operate	same as LATCH/AUTOR=GND			
VCCUVLO	VCC PIN Low voltage protection function	VCC<7.0V (VCC falling)	PFC part, DC/DC part operation stops	VCC>13.5V (VCC rising)	PFC partDC/DC part enable to operate	same as LATCH/AUTOR=GND			
VCCOVP	VCC PIN Over voltage protection function	VCC>27V state continues between 150us(VCC rising)	PFC part, DC/DC part operation stops	VCC<23.0V (VCCfalling)	PFC partDC/DC part enable to operate	VCC>27V (VCC rising)	PFC part, DC/DC part latch operation stops	VCC<6.5V (VCC falling)	PFC part, DC/DCpart enable to operate
blown out	Input AC voltage Low voltage protection function	P_BO＜0.2V state continues between 250ms	PFC part, DC/DC part operation stops	P_BO>0.4V (P_BOrising)	PFC partDC/DC part enable to operate	same as LATCH/AUTOR=GND			
QR_FB_OLP1	QR_FB pin Over current protection function	QR_FB>2.8V state continues between 250ms(QR_FB	DC/DC part operation stops	QR_FB<2.6V (QR_FB falling)	normal operation	same as LATCH/AUTOR=GND			
QR_FB_OLP2	QR_FB pin Over current protection function	QR_FB>3.6V (QR_FB rising)	DC/DC part operation stops	QR_FB<3.4V (QR_FB falling)	normal operation	same as LATCH/AUTOR=GND			
QR_ZT OVP	QR_ZT pin Over voltage protection function	QR_ZT>3.5V state continues between 150us(QR_ZT	DC/DC part operation stops	QR_ZT<3.5V (QR_ZT falling)	normal operation	QR_ZT>3.5V state continues between 150us(QR_ZT	PFC part, DC/DC part latch operation stops	VCC<6.5V (VCC falling)	normal operation
P_VS short protection	P_VS pin Short protection function	P_VS<0.30V (P_VS falling)	PFC part operation stops	P_VS>0.30V (P_VS rising)	normal operation	same as LATCH/AUTOR=GND			
P_VS GAIN increasing	P_VS pin Low voltage gain increasing function	P_VS<2.25V (P_VS falling)	GM AMP GAIN increasing	P_VS>2.25V (P_VS rising)	normal operation	same as LATCH/AUTOR=GND			
P_VS OVP1	P_VS pin Over voltage protection function1	P_VS>2.625V (P_VS rising)	GM AMP GAIN falling	P_VS<2.625V (P_VS falling)	normal operation	same as LATCH/AUTOR=GND			
P_VS OVP2	P_VS pin Over voltage protection function2	P_VS>2.725V (P_VS rising)	PFC part stops	P_VS<2.600V (P_VS falling)	normal operation	P_VS>2.725V (P_VS rising)	PFC part, DC/DC part latch operation stops	VCC<6.5V (VCC下降時)	normal operation
COMP function	COMP pin Protection function	COMP<0.5V state continues between 150us(COMP	PFC part, DC/DC part operation stops	COMP>0.50V (COMP rising)	normal operation	COMP<0.5V state continues between 150us(COMP	PFC part, DC/DC part latch operation stops	VCC<6.5V (VCC falling)	normal operation

Table 3. List of Protection Function Operation Setting by LATCH/AUTOR pin

*Comparator level of protection function is shown by TYP value.

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(4-5) ACTIMER pin

ACTIMER pin is NMOS gate input pin. Show example of using figure 22, 23
Set the detect timer of AC voltage drop.（please refer to ACDET pin page）

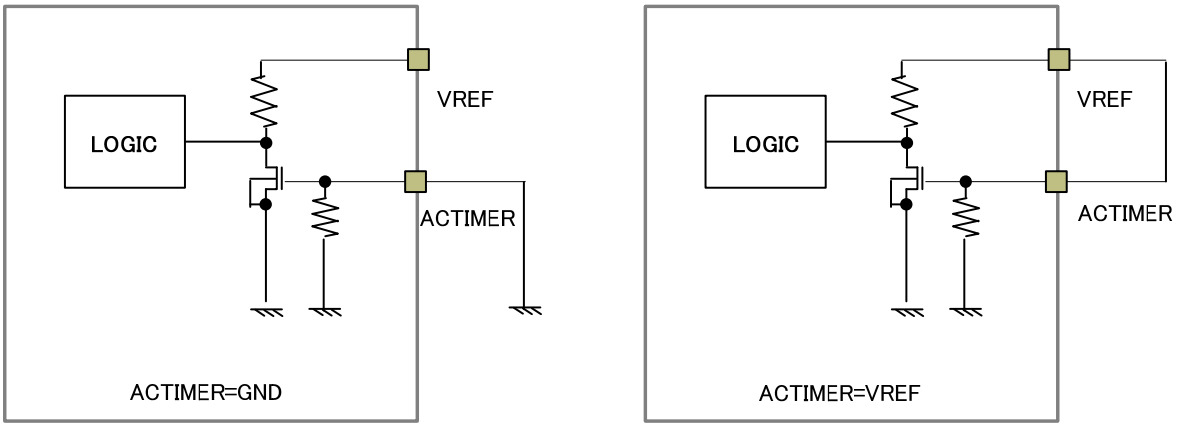

Figure22. Using example of ACTIMER pin

ACTIMER=GND : 32ms Timer
ACTIMER=VREF :128ms Timer

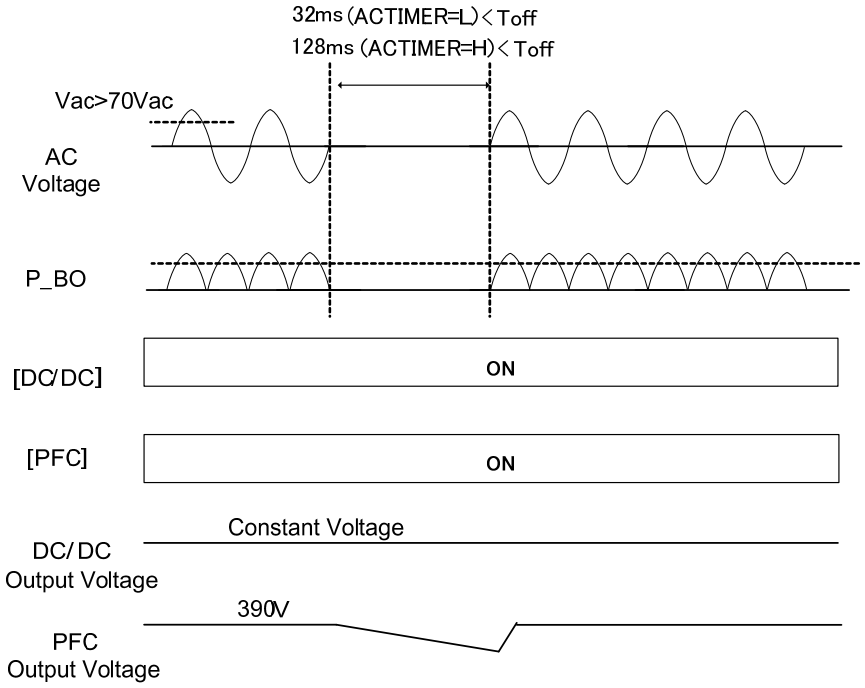

Figure23. AC power at the case momentary power interruption OFF

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(4-6) COMP pin（external stop control function）

COMP pin is stop control pin. When COMP pin voltage drops from V_{COMP} (0.5V. typ), COMP pin stops PFC and DC/DC part operation.
This IC built in T_{COMP} (150us .typ) until stopping switching, prevent from stopping by noise.
COMP pin is in pull-up resistor R_{COMP} (25.9kΩ. typ), When COMP pin is the state of pull-down with lower resistance than R_T(3.70kΩ.typ), COMP pin detects abnormal. Show application examples at the figure24, 25, and 26.

Temperature protection by NTC thermister

By putting a thermister at the COMP pin, it is possible to stop latch on temperature rising.
The case of this application, please design thermister resister is R_T(3.70kΩ.typ) on temperature detection.
（Figure24 and 25 is application circuit that latch on Ta=110℃）
(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

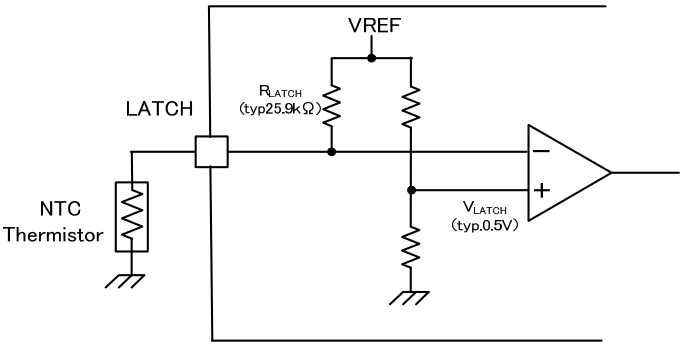

Figure 24. Temperature Protection Application

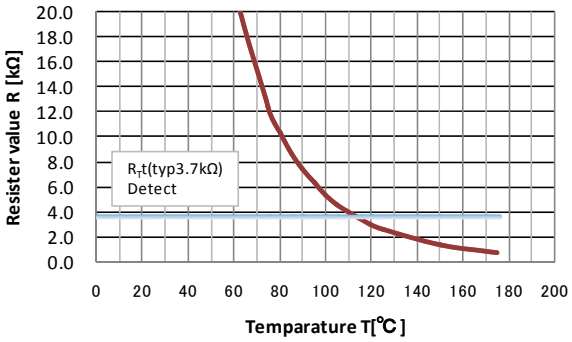

Figure 25. Temperature–Thermistor Resistor characteristic

Secondary over- voltage protection

This IC can detect secondary over-voltage by putting photo coupler to COMP pin.

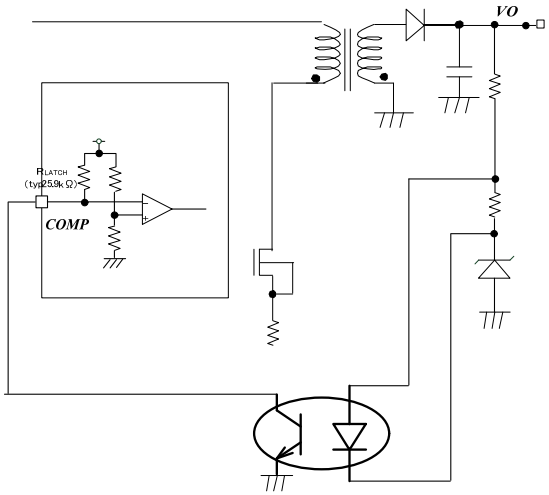

Figure26.Output Over Voltage Protection Application

Table 4. Changes of COMP function Operation by LATCH/AUTOR pin

ITEM	contents	LATCH/AUTOR=GND				LATCH/AUTOR=VREF			
		detection method	operation at detection	release mothod	operaetion at detection	detection method	operation at detection	release mothod	operaetion at detection
COMP function	COMP pin protection function	COMP<0.5V state continues between 150us(COMP falling)	PFC part, DC/DC part operation stops	COMP>0.50V (COMP rising)	normal operation	COMP<0.5V state continues between 150us(COMP falling)	PFC part, DC/DC part latch operation stops	P_VCC<6.5V (P_VCC falling)	normal operation

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