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Magnetic Sensor series

3-Axis Digital Magnetometer IC

BM1422AGMV

General Description

BM1422AGMV is a 3-axis magnetic sensor which incorporates magneto-impedance (MI) elements to detect magnetic field and a control IC in a small package.

Features

- 3-axis Magnetic Sensor using MI Elements
- I^2C Interface
- 12bit / 14bit Digital Output

Applications

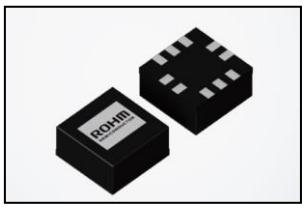
- Wristwatch
- Mobile phone, Smartphone

Key Specifications

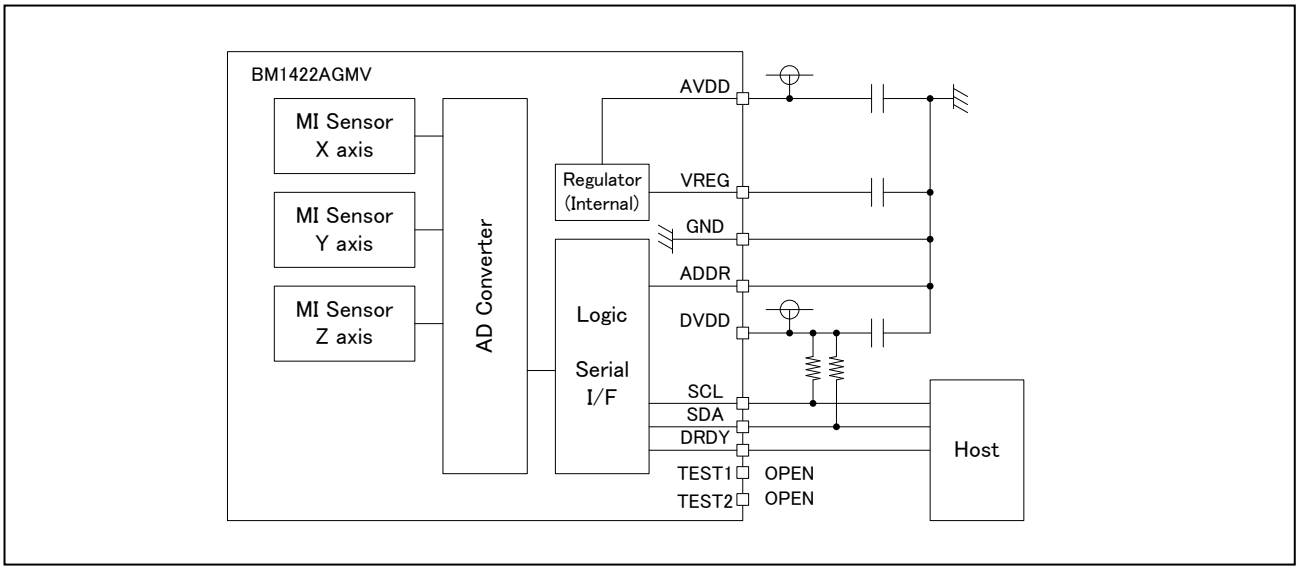
- Input Voltage Range (AVDD): 1.7V to 3.6V
- Input Voltage Range (DVDD): 1.7V to 3.6V
- Operating Current (100SPS): 0.15mA(Typ)
- Magnetic Measurable Range: ±1200μT(Typ)
- Magnetic Sensitivity: 0.042μT/LSB(Typ)
- Maximum Exposed Field: 1000mT
- Operating Temperature Range: -40°C to +85°C

Package

	W(Typ) x D(Typ) x H(Max)
MLGA010V020A	2.00mm x 2.00mm x 1.00mm



Typical Application Circuit



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Contents

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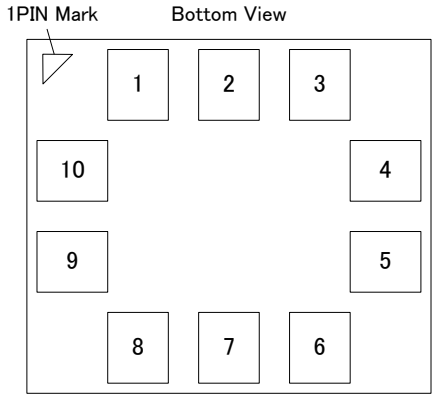
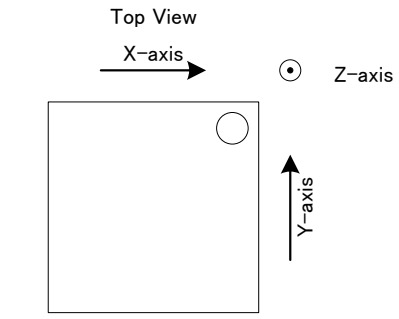
Pin Configuration





Above arrows indicate North-pole as "+".

Pin Description

Pin No.	Pin Name	Function
1	AVDD	Analog circuit power supply(Note 1)
2	GND	Ground
3	VREG	Internal regulator output(Note 2)
4	TEST1	Test pin(Note 3)
5	SDA	I^2C signal data I/O
6	TEST2	Test pin(Note 3)
7	SCL	I^2C signal clock input
8	DRDY	Data ready output pin
9	ADDR	I^2C programmable address bit(Note 4)
10	DVDD	Digital circuit power supply(Note 5)

(Note 1) Please place a bypass capacitor between AVDD and GND in the proximity of the terminals.
(Note 2) Please place a bypass capacitor between VREG and GND in the proximity of the terminals.
Please set a bypass capacitor of 1.0uF between VREG and GND
(Note 3) Use as Non-Connection (NC).
(Note 4) Please connect to DVDD or GND.
(Note 5) Please place a bypass capacitor between DVDD and GND in the proximity of the terminals.

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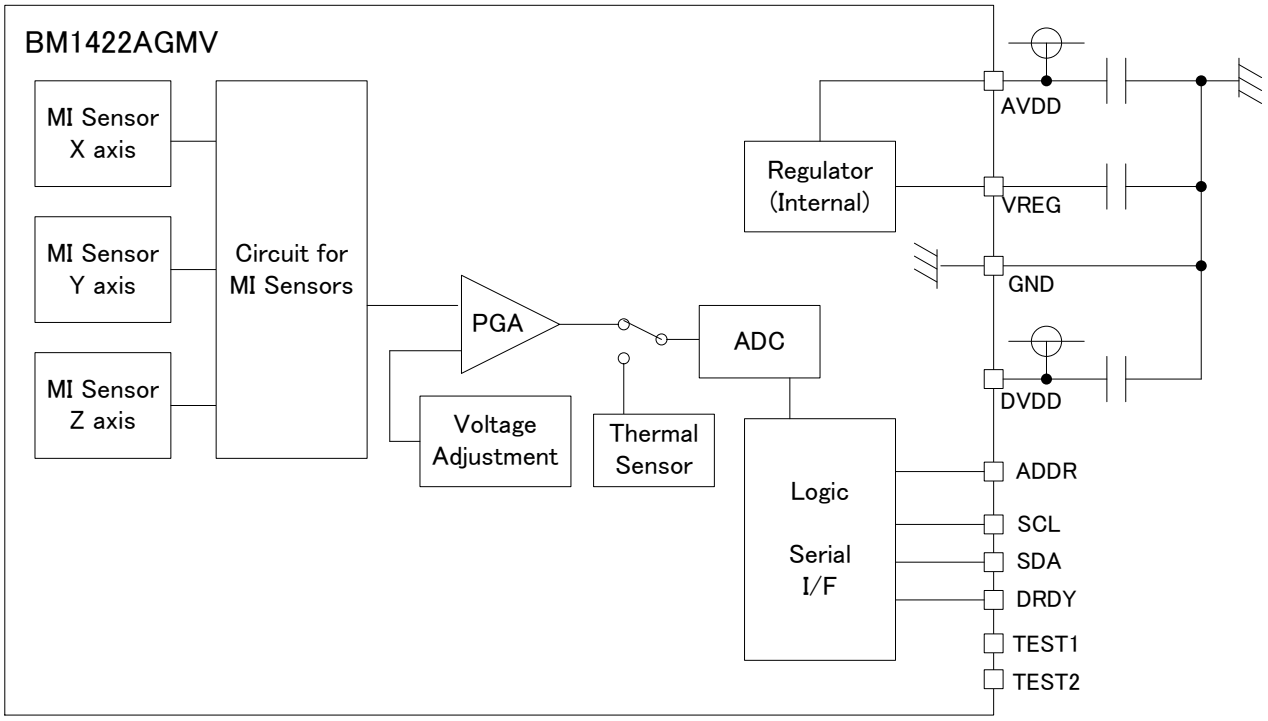
Block Diagram



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Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage (AVDD)	Vdd_a	4.5	V
Supply Voltage (DVDD)	Vdd_d	4.5	V
Input Voltage	Vin	-0.3 to +(Vdd_d+0.3)	V
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C
Maximum Exposed Field	Mef	-1000 to +1000	mT

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
MLGA010V020A				
Junction to Ambient	θ_{JA}	317.3	191.5	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	60	41	°C/W

(Note 1)Based on JESD51-2A(Still-Air)
(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4)Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Recommended Operating Conditions (Ta= -40°C to +85°C)

Parameter	Symbol	Rating	Unit
Supply Voltage (AVDD)	Vdd_a	+1.7 to +3.6	V
Supply Voltage (DVDD)	Vdd_d	+1.7 to +3.6	V
I^2C Clock Frequency	fSCL	MAX 400	kHz

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Electrical Characteristics (Unless otherwise specified AVDD=1.8V, DVDD=1.8V, GND=0.0V, Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Current Consumption						
Average Current during Measurement	Idd	-	150	300	µA	Output Data Rate = 100SPS
Stand-by-mode Current	Iss	-	1.5	5	µA	ALL Power Down
Logic						
Low-level Input Voltage	V_{IL}	GND	-	0.3 * DVDD	V	
High-level Input Voltage	V_{IH}	0.7 * DVDD	-	DVDD	V	
Low-level Input Current	I_{IL}	-10	-	0	µA	V_{IL} = GND
High-level Input Current	I_{IH}	0	-	10	µA	V_{IH} = DVDD
Low-level Output Voltage	V_{OL}	GND	-	0.2 * DVDD	V	IL = -0.3mA
High-level Output Voltage	V_{OH}	0.8 * DVDD	-	DVDD	V	IL = 0.3mA
Serial Communication						
Low-level Input Current	I_{IL2}	-10	-	0	µA	V_{IL} = GND
High-level Input Current	I_{IH2}	0	-	10	µA	At HiZ, V_{IH} = DVDD
Low-level Output Voltage	V_{OL2}	GND	-	0.2 * DVDD	V	IL = -3mA
Magnetic Sensor						
Moving Range	Rm	-	±300	-	µT	
Measurable Range(Note 1)	Ra	-	±1200	-	µT	
X,Y-axis Linearity(Note 2)	Lin1	-	0.5	2	%FS	Rm = ±200µT
Z-axis Linearity(Note 2)	Lin2	-	1.0	2.8	%FS	Rm = ±200µT
Output Offset	Vofs	-	0	-	LSB	Magnetic Field = 0µT
Magnetic Sensitivity	DeltaV	-	0.042	-	µT/ LSB	
Measurement Time	Tms	-	0.5	-	msec	Average 4times

(Note1) Measurable Range: Overall measurable range within which preset operating range can be fit by adjusting appropriate offsets.
(Note2) Linearity [%FS] = Output Error / Rm = (output – ideal output) / Rm

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Typical Performance Curves

(Unless otherwise specified, Ta=25°C, AVDD=1.8V, DVDD=1.8V, GND=0.0V)

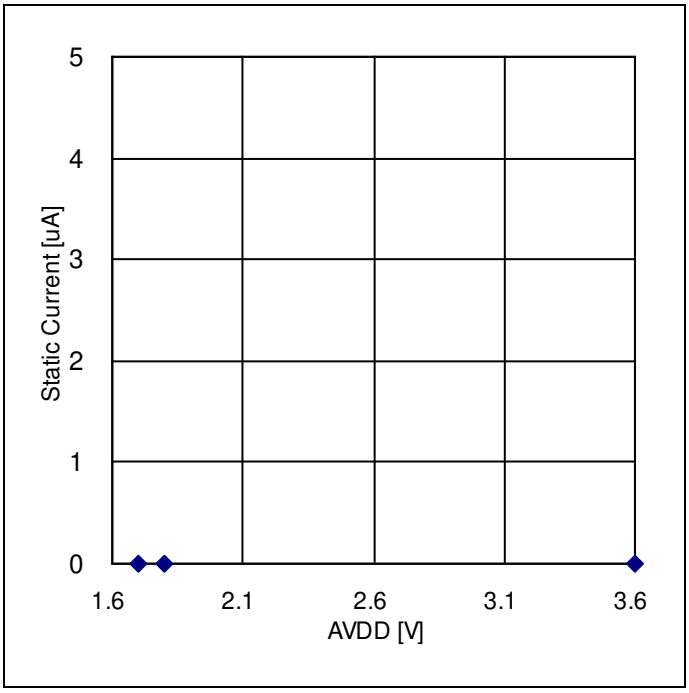

Figure 1. AVDD PowerDown Current Voltage Dependency

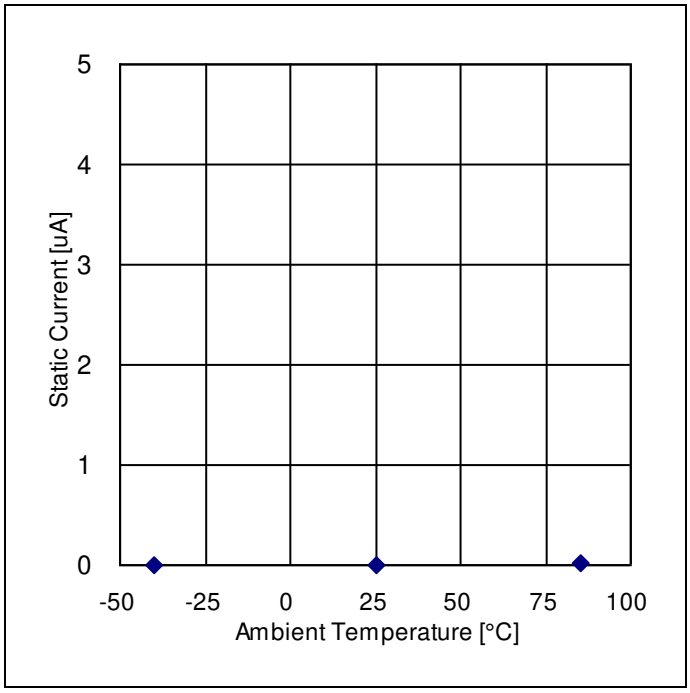

Figure 2. AVDD PowerDown Current Temperature Dependency

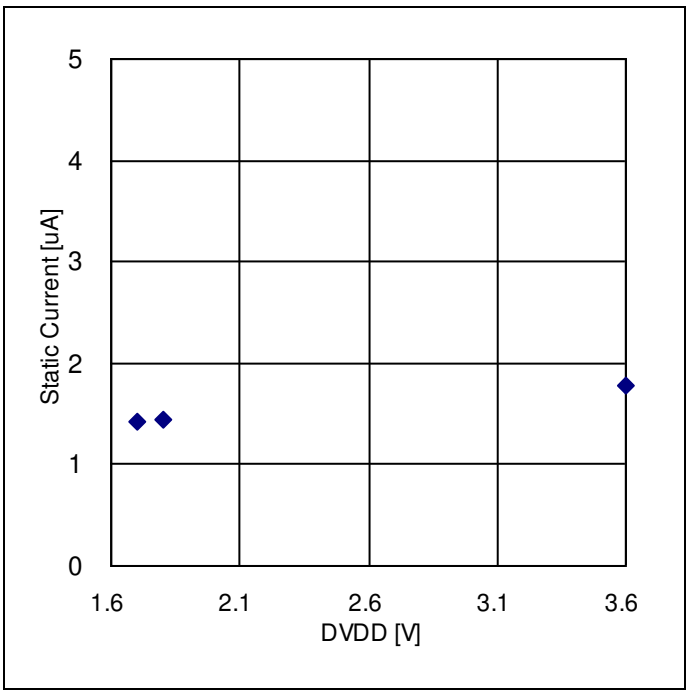

Figure 3. DVDD PowerDown Current Voltage Dependency

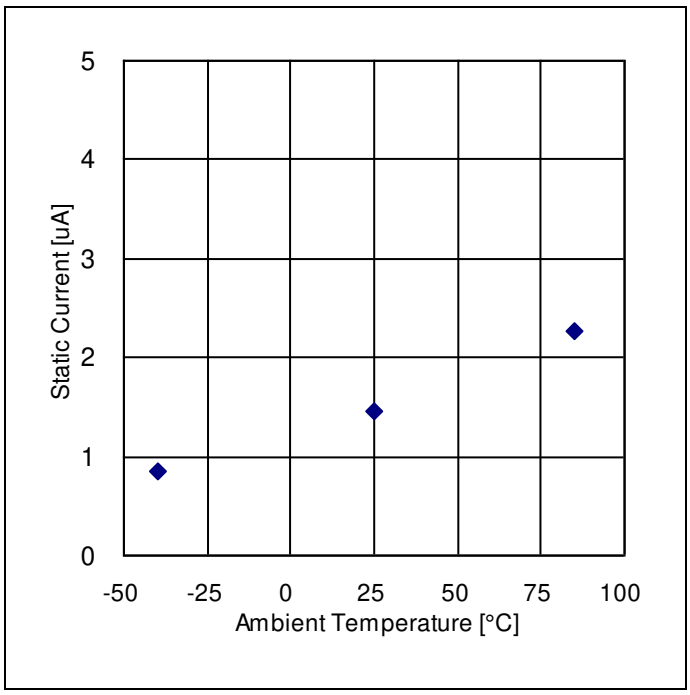

Figure 4. DVDD PowerDown Current Temperature Dependency

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Typical Performance Curves - continued

(Unless otherwise specified, Ta=25°C, AVDD=1.8V, DVDD=1.8V, GND=0.0V)

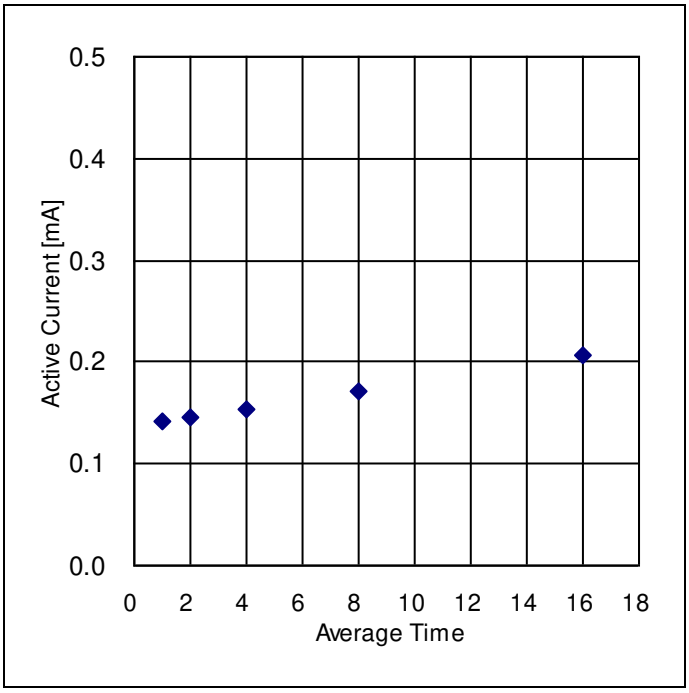

Figure 5. Average Current during Measurement Averaging Dependency (100SPS)

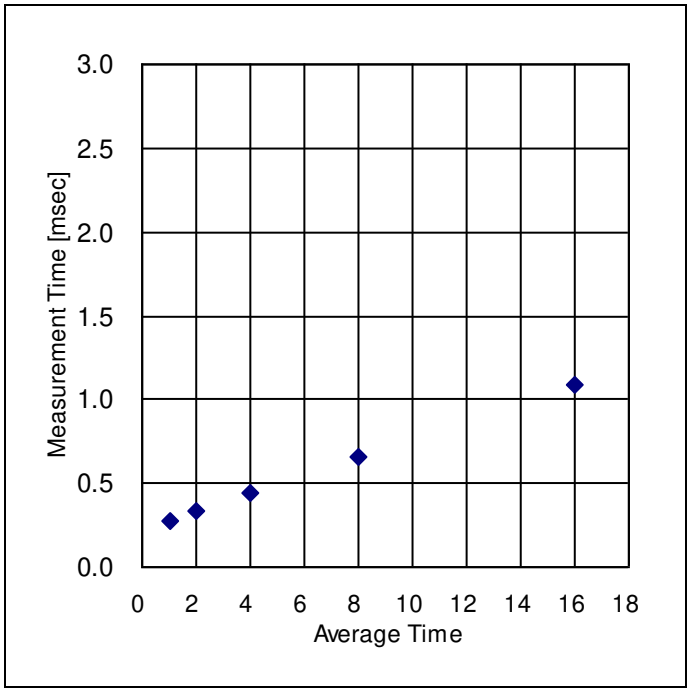

Figure 6. Measurement Time Averaging Dependency

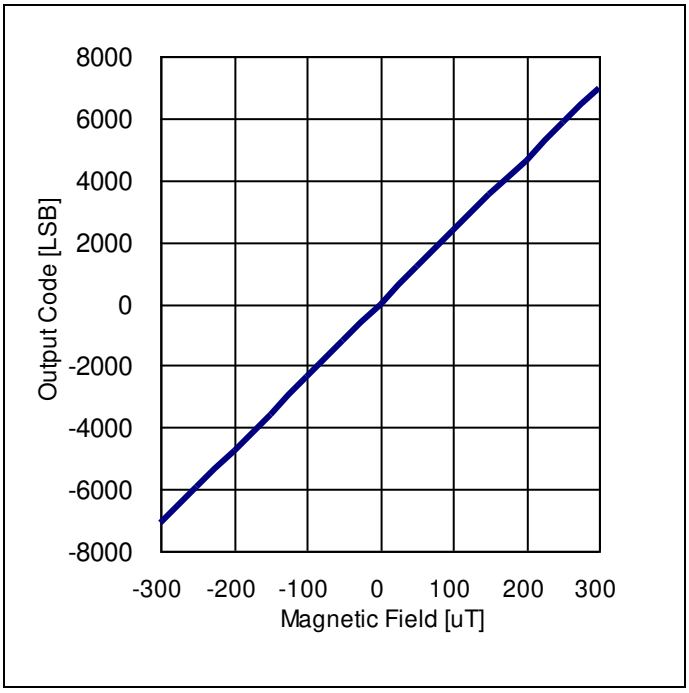

Figure 7. Output Characteristic

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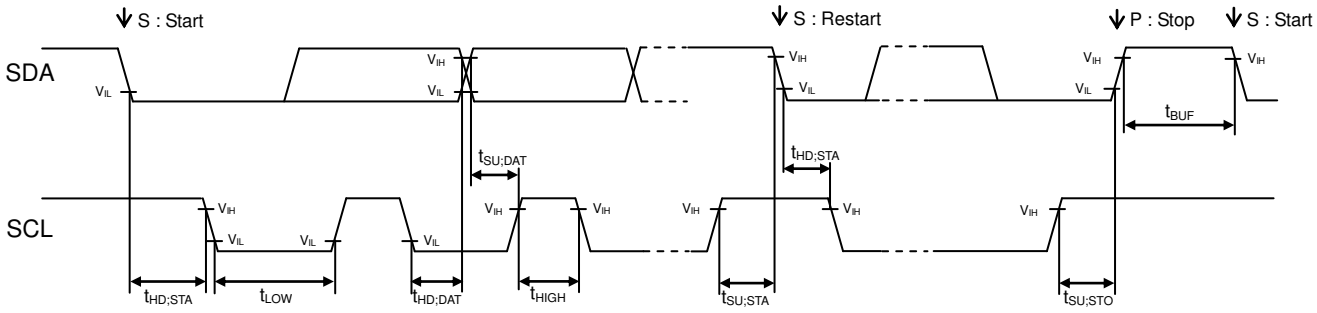
I²C bus Timing Characteristics (Unless otherwise specified DVDD =1.8V, Ta = 25°C)



Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
I²C SCL Clock frequency	f_{SCL}	0	-	400	kHz	
I²C 'L' Period of the SCL Clock	t_{LOW}	1.3	-	-	µs	
I²C 'H' Period of the SCL Clock	t_{HIGH}	0.6	-	-	µs	
I²C Setup Time for Repeated START Condition	$t_{SU;STA}$	0.6	-	-	µs	
I²C Hold Time (Repeated) START Condition	$t_{HD;STA}$	0.6	-	-	µs	
I²C Data Setup Time	$t_{SU;DAT}$	100	-	-	ns	
I²C Data Hold Time	$t_{HD;DAT}$	0	-	-	µs	
I²C Setup Time for STOP Condition	$t_{SU;STO}$	0.6	-	-	µs	
I²C Bus Free Time between a STOP and START Condition	t_{BUF}	1.3	-	-	µs	

I²C bus Communication

1. Main write format

(1) Indicate register address

S	Slave Address	W 0	ACK	Indicate register address	ACK	P

(2) Write to data register after indicating register address

S	Slave Address	W 0	ACK	Indicate register address	ACK

Data specified at register address field	ACK	· · ·	ACK	Data specified at register address field + N	ACK	P

2. Main read format

(1) Read data after indicate register address (Master issues restart condition)

S	Slave Address	W 0	ACK	Indicate register address	ACK

S	Slave Address	R 1	ACK	Data specified at register address field	ACK

Data specified at register address field + 1	ACK	· · ·	ACK	Data specified at register address field + N	NACK	P

(2) Case of read data

S	Slave Address	R 1	ACK	Data specified at register address field	ACK

Data specified at register address field + 1	ACK	· · ·	ACK	Data specified at register address field + N	NACK	P

from master to slave from slave to master

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I²C bus Slave address

Selectable I²C Slave Address
(ADDR=L: 0001110, ADDR=H: 0001111)

Register Map(Note 1)

Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x0D	INFO	R	INFO [7:0]							
0x0E		R	INFO [15:8]							
0x0F	WIA	R	WIA [7:0]							
0x10	DATAX	R	DATAX [7:0]							
0x11		R	DATAX [15:8]							
0x12	DATAY	R	DATAY [7:0]							
0x13		R	DATAY [15:8]							
0x14	DATAZ	R	DATAZ [7:0]							
0x15		R	DATAZ [15:8]							
0x18	STA1	R	0	RD_DRDY	0	0	0	0	0	0
0x1B	CNTL1	RW	PC1	OUT_BIT	RST_LV	ODR [1:0]		0	FS1	0
0x1C	CNTL2	RW	0	0	0	0	DREN	DRP	0	0
0x1D	CNTL3	RW	0	FORCE	0	0	0	0	0	0
0x40	AVE_A	RW	0	0	0	AVE_A [2:0]			0	0
0x5C	CNTL4	W	RSTB_LV [7:0]							
0x5D		W	RSTB_LV [15:8]							
0x60	TEMP	R	TEMP [7:0]							
0x61		R	TEMP [15:8]							
0x6C	OFF_X	RW	OFF_X [7:0]							
0x6D		RW	OFF_X [15:8]							
0x72	OFF_Y	RW	OFF_Y [7:0]							
0x73		RW	OFF_Y [15:8]							
0x78	OFF_Z	RW	OFF_Z [7:0]							
0x79		RW	OFF_Z [15:8]							
0x90	FINEOUTPUTX	R	FINEOUTPUTX [7:0]							
0x91		R	FINEOUTPUTX [15:8]							
0x92	FINEOUTPUTY	R	FINEOUTPUTY [7:0]							
0x93		R	FINEOUTPUTY [15:8]							
0x94	FINEOUTPUTZ	R	FINEOUTPUTZ [7:0]							
0x95		R	FINEOUTPUTZ [15:8]							
0x9C	GAIN_PARA_X	R	GAIN_PARA_X [7:0]							
0x9D		R	GAIN_PARA_X [15:8]							
0x9E	GAIN_PARA_Y	R	GAIN_PARA_Y [7:0]							
0x9F		R	GAIN_PARA_Y [15:8]							

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0xA0	GAIN_PARA_Z	R	GAIN_PARA_Z [7:0]
0xA1		R	GAIN_PARA_Z [15:8]

(Note 1) Do not write any commands to other addresses except above. Do not write '1' to the fields in which value is '0' in above table.

It is the following conditions to be able to access each register.

Condition	Accessible Register
Supply Power	CNTL1 CNTL4 INFO WIA OFF_X,Y,Z
Supply Power (CNTL1) PC1=1 (CNTL1) RST_LV=0 (CNTL4) RSTB_LV=1	STA1 CNTL2 CNTL3 AVE_A OFF_X,Y,Z
Supply Power (CNTL1) PC1=1 (CNTL1) RST_LV=0 (CNTL4) RSTB_LV=1 (CNTL3) FORCE=1 after first access	DATAX,Y,Z TEMP FINEOUTPUTX,Y,Z
Supply Power (CNTL1) PC1=1, FS1=1 (CNTL1) RST_LV=0 (CNTL4) RSTB_LV=1 (CNTL3) FORCE=1 after first access	DATAX,Y,Z TEMP FINEOUTPUTX,Y,Z GAIN_PARA_X,Y,Z

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(0x0D/0x0E) Information Register

Fields	Function
INFO [7:0]	Information LSB : 0x01
INFO [15:0]	Information MSB : 0x01

(0x0F) WIA Register

Fields	Function
WIA [7:0]	Who I am : 0x41

(0x10/0x11, 0x12/0x13, 0x14/0x15) Output Data Register

Fields	Function
DATAX [7:0]	Xch Output value LSB
DATAX [15:0]	Xch Output value MSB
DATAY [7:0]	Ych Output value LSB
DATAY [15:0]	Ych Output value MSB
DATAZ [7:0]	Zch Output value LSB
DATAZ [15:0]	Zch Output value MSB

default value 0xXXXX

signed 16bit -2048d(0xF800) to +2047d(0x07FF) [Register OUT_BIT=0]
-8192d(0xE000) to +8191d(0x1FFF) [Register OUT_BIT=1]

(0x18) Status Register

Fields	Function
RD_DRDY	This bit is output to the DRDY to inform the preparation status of the measured data 0 : Not ready NG 1 : Ready OK

default value 0x00

(0x1B) Control setting1 Register

Fields	Function
PC1	Power Control 0 : PowerDown 1 : Active
OUT_BIT	Output Data bit setting 0 : 12bit Output , 1 : 14bit Output
RST_LV	Logic reset control 0 : Reset release 1 : Reset Reset release at RST_LV(CNTL1)=0 & RSTB_LV(CNTL4)=1
ODR [1:0]	Measurement output data rates 00 : 10Hz , 10 : 20Hz , 01 : 100Hz , 11 : 1kHz
FS1	Measurement mode setting 0 : Continuous mode , 1 : Single mode

default value 0x22

(0x1C) Control setting2 Register

Fields	Function
DREN	DRDY terminal enable setting 0 : Disable , 1 : Enable
DRP	DRDY terminal active setting 0 : Low active , 1 : High active

default value 0x04

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(0x1D) Control setting3 Register

Fields	Function
FORCE	AD start measurement trigger at continuous mode (FS1=0) and single mode (FS1=1) 1: Start measurement ※Register is automatic clear “0” after write data “1” ※Write data “0” is invalid ※If write data “1” on measurement way, restart measurement

default value 0x00

(0x40) Average time Register

Fields	Function
AVE_A	Average Time 000:4times, 001:1times, 010:2times, 011:8times, 100:16times

default value 0x00

(0x5C/0x5D) Control setting4 Register

Fields	Function
RSTB_LV [7:0]	Reserved (ignore write data)
RSTB_LV [15:8]	RSTB_LV=1 by write access (ignore write data) Reset release at RST_LV(CNTL1)=0 & RSTB_LV(CNTL4)=1 RSTB_LV=0 by write PC1(CNTL1)=0

default value 0x04

(0x60/0x61) Temperature value Register

Fields	Function
TEMP [7:0]	Temperature value LSB
TEMP [15:8]	Temperature value MSB

default value 0xXXXX

unsigned 16bit 0d(0x0000) to +4095d(0x0FFF) [Register OUT_BIT=0]
0d(0x0000) to +16383d(0x3FFF) [Register OUT_BIT=1]

(0x6C/0x6D, 0x72/0x73, 0x78/0x79) Output Data Register

Fields	Function
OFF_X [7:0]	Xch Offset value
OFF_X [15:8]	Reserved Write ”00000000”
OFF_Y [7:0]	Ych Offset value
OFF_Y [15:8]	Reserved Write ”00000000”
OFF_Z [7:0]	Zch Offset value
OFF_Z [15:8]	Reserved Write ”00000000”

default value 0x30

unsigned 8bit 1d(0x01) to +95d(0x5F)

(0x90/0x91, 0x92/0x93, 0x94/0x95) Fine output Register

Fields	Function
FINEOUTPUTX [7:0]	DATAX value per OFF_X LSB
FINEOUTPUTX [15:0]	DATAX value per OFF_X MSB
FINEOUTPUTY [7:0]	DATAY value per OFF_Y LSB
FINEOUTPUTY [15:0]	DATAY value per OFF_Y MSB
FINEOUTPUTZ [7:0]	DATAZ value per OFF_Z LSB
FINEOUTPUTZ [15:0]	DATAZ value per OFF_Z MSB

default value 0xXXXX

unsigned 16bit 0d(0x0000) to +16383d(0x3FFF)

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(0x9C/0x9D, 0x9E/0x9F, 0xA0/0xA1) Axis interference Register

Fields	Function
GAIN_PARA_X [7:0]	Axis interference Xch to Zch
GAIN_PARA_X [15:0]	Axis interference Xch to Ych
GAIN_PARA_Y [7:0]	Axis interference Ych to Zch
GAIN_PARA_Y [15:0]	Axis interference Ych to Xch
GAIN_PARA_Z [7:0]	Axis interference Zch to Ych
GAIN_PARA_Z [15:0]	Axis interference Zch to Xch

default value 0xXX

unsigned 8bit 0d(0x00) to +255d(0xFF)

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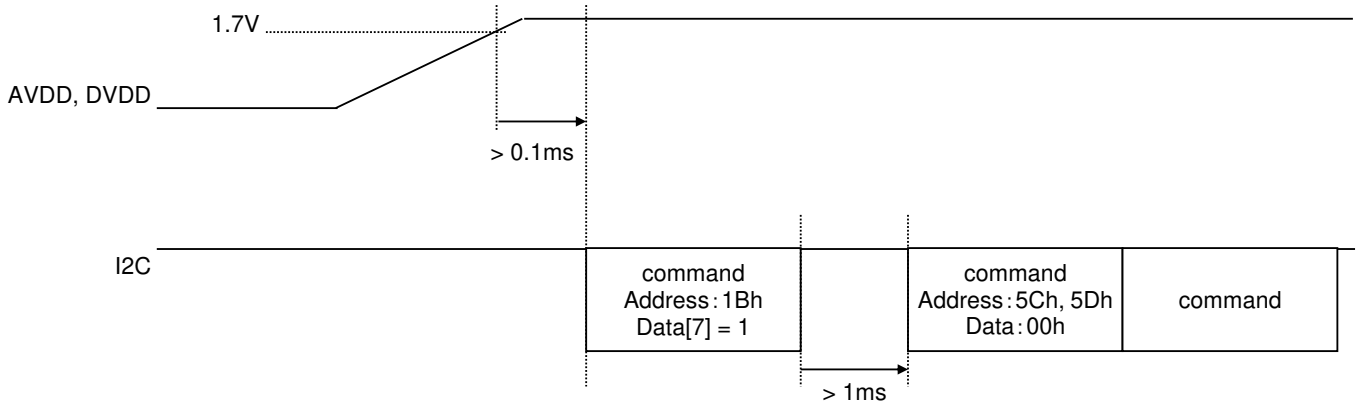
Control Sequence

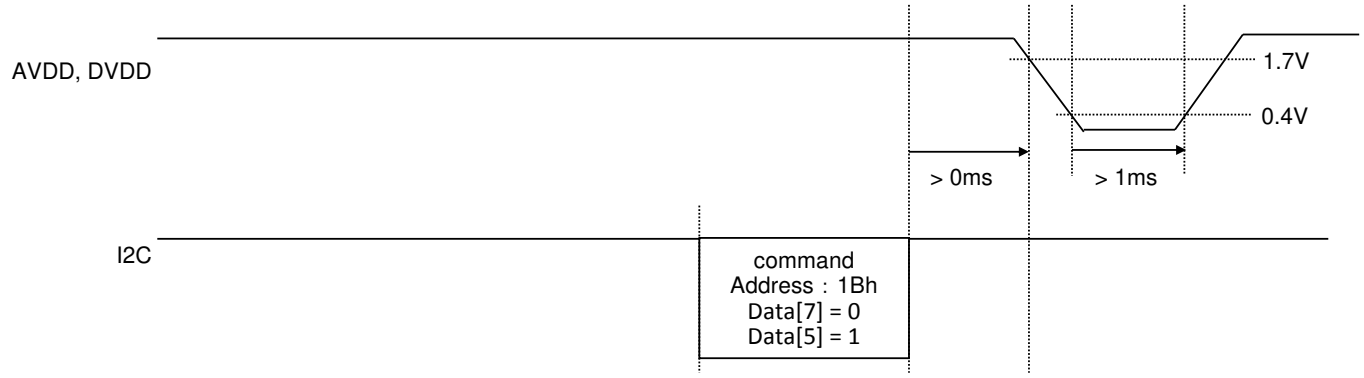
1. Control Sequence

1.1 Power supply start-up sequence

The order of starting up the power supplies of AVDD and DVDD is arbitrary, when they are supplied from different sources. Please do the command control by I^2C after all powers are supplied.



1.2 Power supply end sequence



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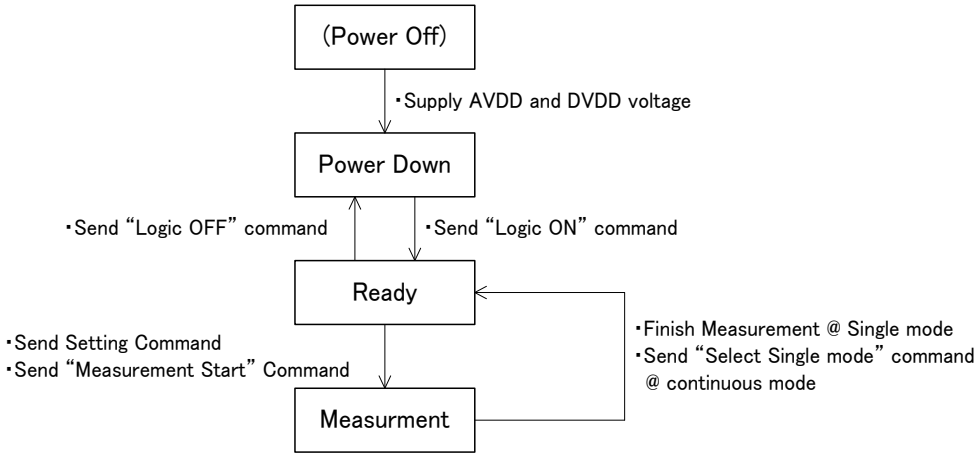
2. Measurement sequence

There are the following two kinds of measurement modes

Continuous Mode	BM1422AGMV is measured at specified cycle (ODR=10,20,100,1kHz) at the cycle.
Single Mode	BM1422AGMV is measured by the measurement request from the host.



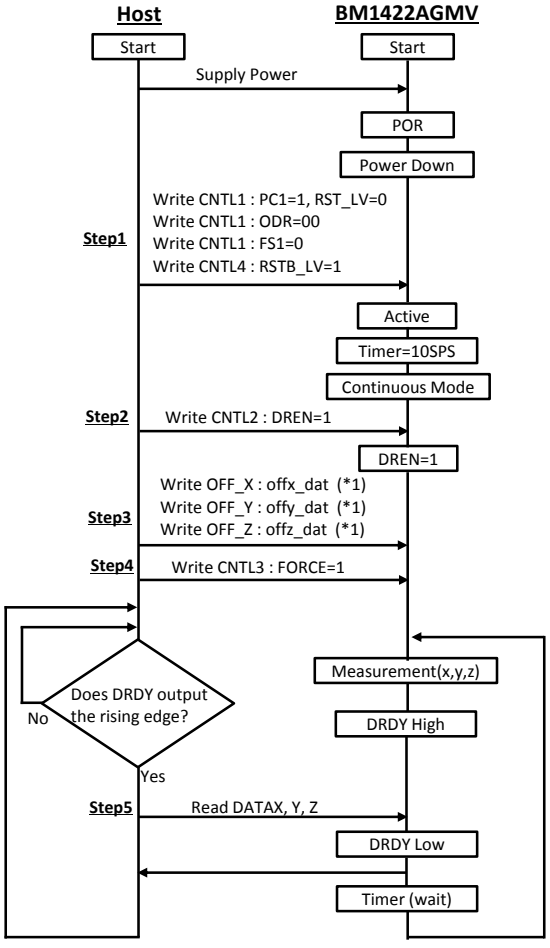
2.1 Continuous Mode

(Send command example) Case of 12bit Output Data

	Register Name	Address	Data
Step1	CNTL1	0x1B	0x80
	CNTL4	0x5C	0x00
		0x5D	0x00
Step2	CNTL2	0x1C	0x0C
Step3	OFF_X	0x6C	offx_dat
	OFF_Y	0x72	offy_dat
	OFF_Z	0x78	offz_dat
Step4	CNTL3	0x1D	0x40
Step5	DATAX	0x10	Read
		0x11	
	DATAY	0x12	Read
		0x13	
	DATAZ	0x14	Read
		0x15	

(Send command example) Case of 14bit Output Data

	Register Name	Address	Data
Step1	CNTL1	0x1B	0xC0
	CNTL4	0x5C	0x00
		0x5D	0x00
Step2	CNTL2	0x1C	0x0C
Step3	OFF_X	0x6C	offx_dat
	OFF_Y	0x72	offy_dat
	OFF_Z	0x78	offz_dat
Step4	CNTL3	0x1D	0x40
Step5	DATAX	0x10	Read
		0x11	
	DATAY	0x12	Read
		0x13	
	DATAZ	0x14	Read
		0x15	



(*1) The value is obtained at offset adjustment.
If not obtained yet, then skip.

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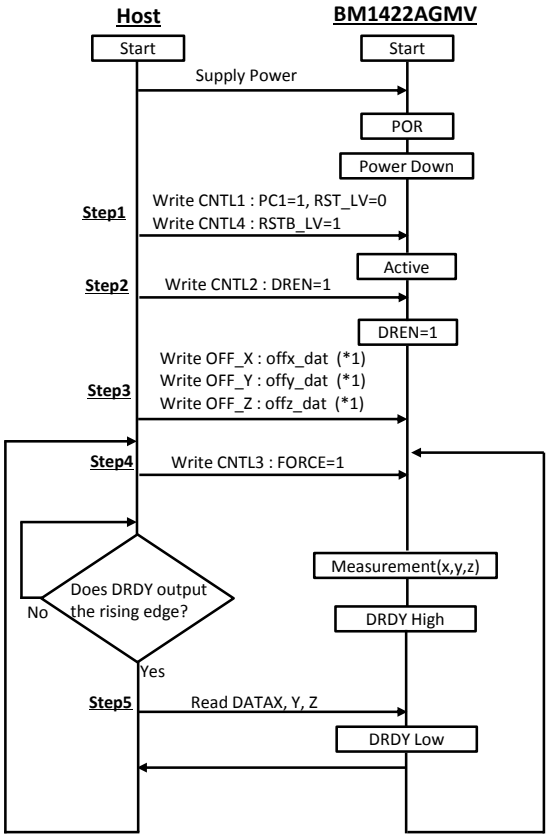
2.2 Single Mode

(Send command example) Case of 12bit Output Data

	Register Name	Address	Data
Step1	CNTL1	0x1B	0x82
	CNTL4	0x5C	0x00
		0x5D	0x00
Step2	CNTL2	0x1C	0x0C
Step3	OFF_X	0x6C	offx_dat
	OFF_Y	0x72	offy_dat
	OFF_Z	0x78	offz_dat
Step4	CNTL3	0x1D	0x40
Step5	DATAX	0x10	Read
		0x11	
	DATAY	0x12	Read
		0x13	
	DATAZ	0x14	Read
		0x15	

(Send command example) Case of 14bit Output Data

	Register Name	Address	Data
Step1	CNTL1	0x1B	0xC2
	CNTL4	0x5C	0x00
		0x5D	0x00
Step2	CNTL2	0x1C	0x0C
Step3	OFF_X	0x6C	offx_dat
	OFF_Y	0x72	offy_dat
	OFF_Z	0x78	offz_dat
Step4	CNTL3	0x1D	0x40
Step5	DATAX	0x10	Read
		0x11	
	DATAY	0x12	Read
		0x13	
	DATAZ	0x14	Read
		0x15	



(*1) The value is obtained at offset adjustment.
If not obtained yet, then skip.

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3. Offset Adjustment

Offset adjustment sequence make the output value around zero under the normal magnetic environment. After measuring the following parameter, HOST should save it in memory, and it needs to be set after applying power supply to BM1422AGMV.

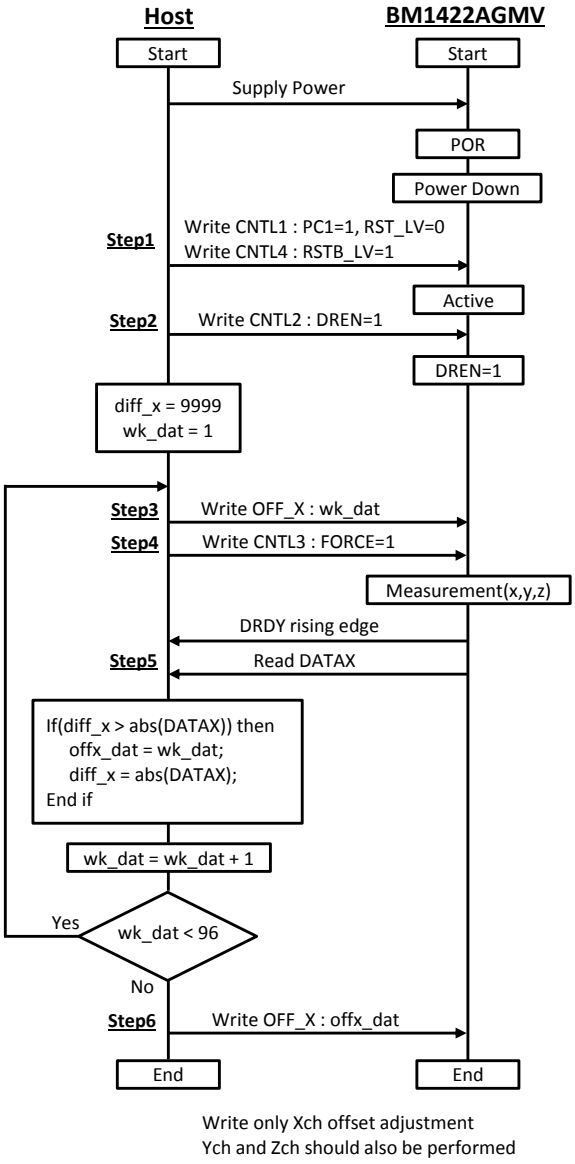
Parameter	Description
offx_dat	Adjusted value of Xch offset
offy_dat	Adjusted value of Ych offset
offz_dat	Adjusted value of Zch offset

(Send command example) Case of 12bit Output Data

	Register Name	Address	Data
Step1	CNTL1	0x1B	0x82
	CNTL4	0x5C	0x00
		0x5D	0x00
Step2	CNTL2	0x1C	0x0C
Step3	OFF_X	0x6C	wk_dat
Step4	CNTL3	0x1D	0x40
Step5	DATAX	0x10	Read
		0x11	
Step6	OFF_X	0x6C	offx_dat

(Send command example) Case of 14bit Output Data

	Register Name	Address	Data
Step1	CNTL1	0x1B	0xC2
	CNTL4	0x5C	0x00
		0x5D	0x00
Step2	CNTL2	0x1C	0x0C
Step3	OFF_X	0x6C	wk_dat
Step4	CNTL3	0x1D	0x40
Step5	DATAX	0x10	Read
		0x11	
Step6	OFF_X	0x6C	offx_dat



Write only Xch offset adjustment
Ych and Zch should also be performed

When OFF_X, OFF_Y, OFF_Z are changed in the same magnetic field environment, the change directions of the output are as follows

	OFF_X,Y,Z +	OFF_X,Y,Z −
X axis	−	+
Y axis	−	+
Z axis	−	+

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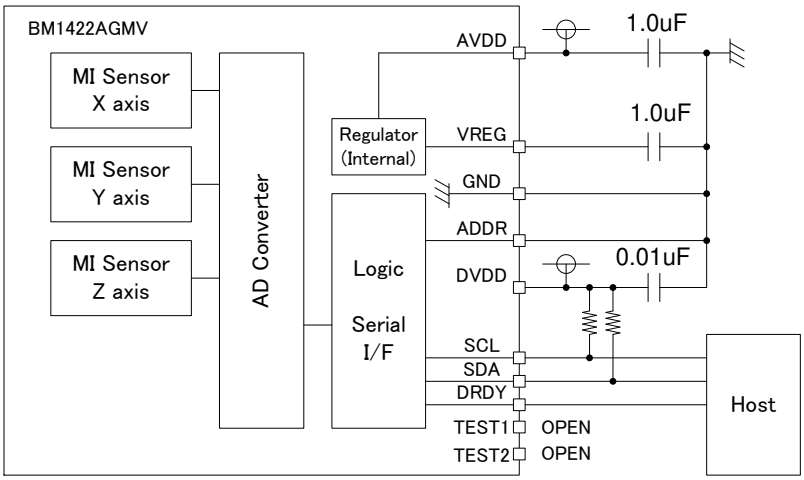
Application Example



(Note) Sensor property may change due to around magnetic parts. We recommend calibrating the sensitivity and origin point of magnetic sensors after mounting.

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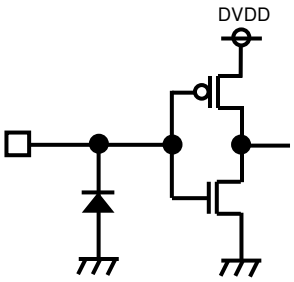
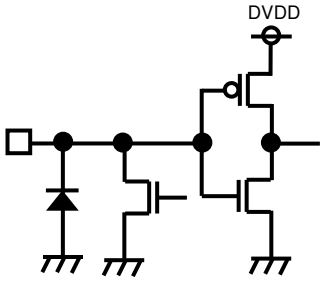
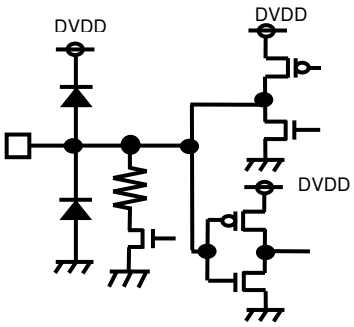
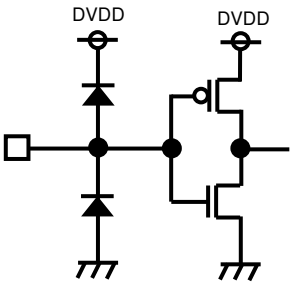
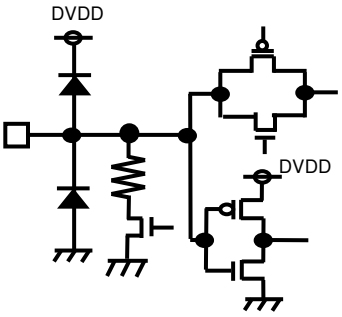
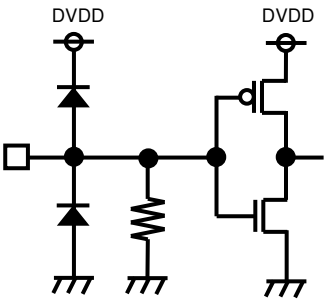
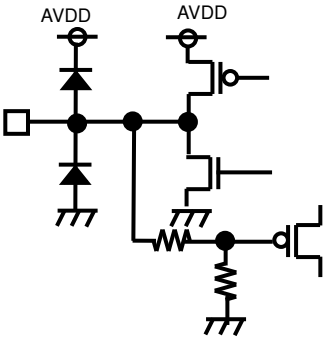
I/O equivalent circuit

Pin name	Equivalent Circuit Diagram	Pin name	Equivalent Circuit Diagram
SCL		SDA	
DRDY		ADDR	
TEST1		TEST2	
VREG			

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

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Operational Notes – continued

10. Inter-pin Short and Mounting Errors
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Ceramic Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Absolute Maximum Ratings
Operate the IC such that the output voltage, output current, and power dissipation are all within the Absolute Maximum Ratings.

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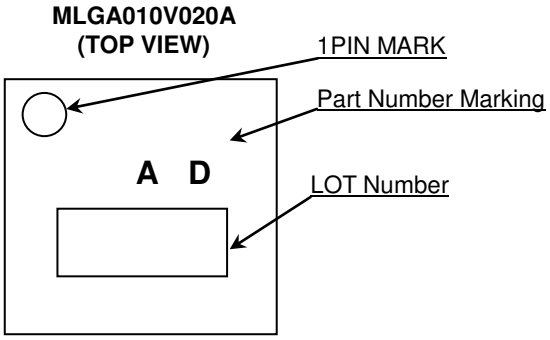
Ordering Information

B M 1 4 2 2 A G M V	-	Z E2
Part Number	Package GMV:MLGA010V020A	Packaging and forming specification E2: Embossed tape and reel

Marking Diagrams



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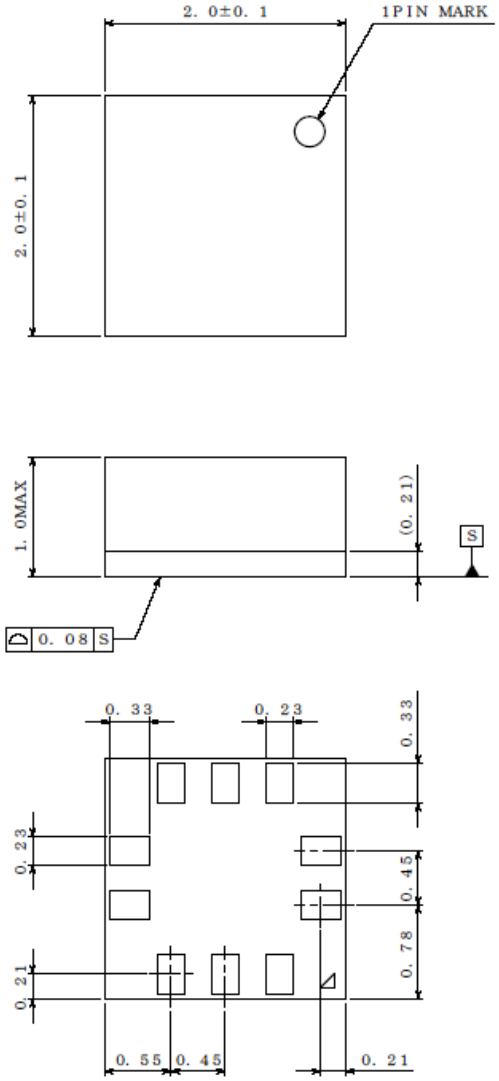
Physical Dimension, Tape and Reel Information

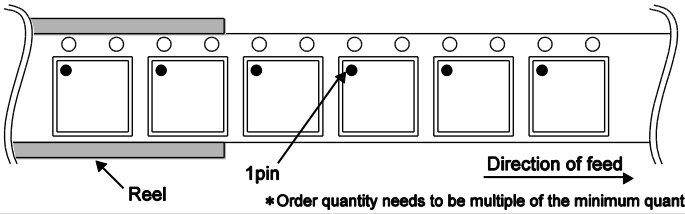
Package Name	MLGA010V020A



(UNIT : mm)

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
17.Oct.2016	001	New Release

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