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AC/DC Drivers

Power Factor Correction and Quasi-Resonant DC/DC converter IC

BM1C102F

General Description

The compounded LSI of the Power Factor Correction (PFC) converter and Quasi-Resonant (QR) controller type DC/DC converter IC provides an optimum system for all products that include an electrical outlet. BM1C102F has a built in High Voltage starter circuit that tolerates 650V and X-Cap discharge function, and contributes to low power consumption and high speed start.

The PFC part operates by Boundary Conduction Mode (BCM). It reduces the switching loss and the switching noise. Because of zero current detection (ZCD) by a resistance, this solution achieves no auxiliary winding and reduces external parts and the bias current.

The DC/DC part operates by Quasi-Resonant Mode. This method enables soft switching and helps to keep the EMI low. With putting MOSFET for switching and current detection resistors as external devices, a higher freedom design is possible.

This IC has double over voltage protection for the PFC output terminal. IC makes the standby power consumption low by the PFC ON/OFF control function. The IC includes various protect functions such as VCC over voltage protection, external latch protection, brown out protection, soft start function, per-cycle current limiter and over load protection.

Features

- PFC+QR Combo IC
- Built-in 650V tolerance start circuit
- VCC pin: under and over voltage protection
- Brown out function
- External latch terminal function
- PFC boundary conduction mode (voltage control)
- PFC Zero Cross Detection
- PFC variable max frequency
- PFC Dynamic & Static OVP function
- PFC ON/OFF setting
- QR low power when load is light (Burst operation) and frequency decrease function
- QR maximum frequency control (120kHz)
- QR_CS pin open protection and OCP function
- QR Soft Start function
- QR secondary side protection circuit of over-current
- QR_ZT pin 2 step timeout function and OVP function

Applications

AC adapters, TV, Lighting, Household appliances (Vacuum cleaners, Air cleaners, Air conditioners, IH cooking heaters, Rice cookers, etc.).

Key Specifications

Operating Power Supply Voltage Range:	VCC	8.9V to 26.0V
	VH_IN	80V to 500V
Operating Current:	Normal	1.2mA (Typ)
	Burst	0.6mA (Typ)
Max frequency:	PFC	External setting
	QR	120kHz (Typ)
The range of temperature:		-40°C to 105°C

Package W(Typ) x D(Typ) x H(Max)
SOP18 11.20mm × 7.80mm × 2.01mm pitch 1.27mm

SOP18

Typical Application Circuit

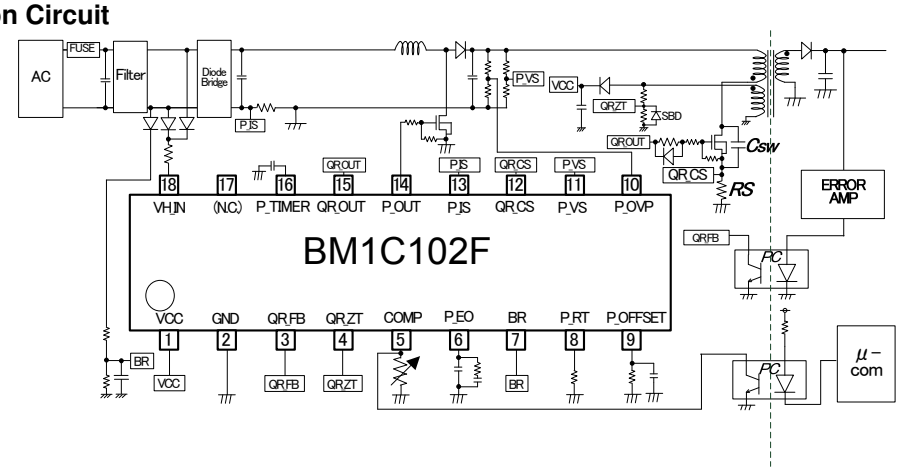


Figure 1. Application circuit

Pin Configuration

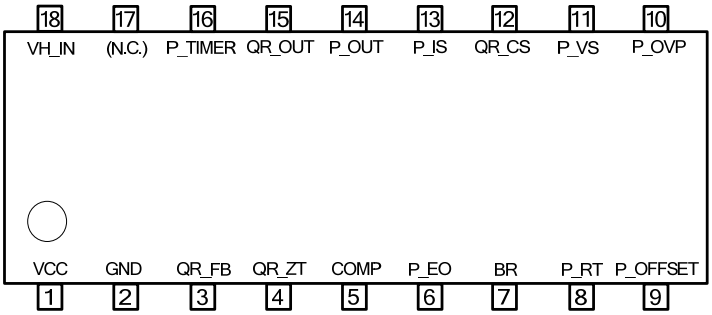


Figure 2. Pin Layout (Top View)

Pin Description

Table 1. I/O Pin Functions

Pin Name	I/O	Pin No.	Function	ESD Diode	
				VCC	GND
VCC	I/O	1	[General] Power supply pin	-	○
GND	I/O	2	[General] GND pin	○	-
QR_FB	I	3	[QR] Feedback detection pin	−	○
QR_ZT	I	4	[QR] Zero cross detection pin	-	○
COMP	I	5	[General] External latch input pin	−	○
P_EO	O	6	[PFC] Error amplifier output pin	−	○
BR	I	7	[General] Input AC voltage monitor pin	−	○
P_RT	I	8	[PFC] Max frequency setting pin	−	○
P_OFFSET	I	9	[PFC] ON/OFF setting voltage	−	○
P_OVP	I	10	[PFC] Over voltage detection pin	−	○
P_VS	I	11	[PFC] Feedback signal input pin	−	○
QR_CS	I	12	[QR] MOSFET current detection pin	−	○
P_IS	I	13	[PFC] Zero cross detection pin	−	○
P_OUT	O	14	[PFC] External MOS drive pin	○	○
QR_OUT	O	15	[QR] External MOS drive pin	○	○
P_TIMER	I	16	[PFC] OFF time setting pin	−	○
N.C.	-	17	-	-	-
VH_IN	I	18	[General] Starter circuit pin	-	○

Block Diagram

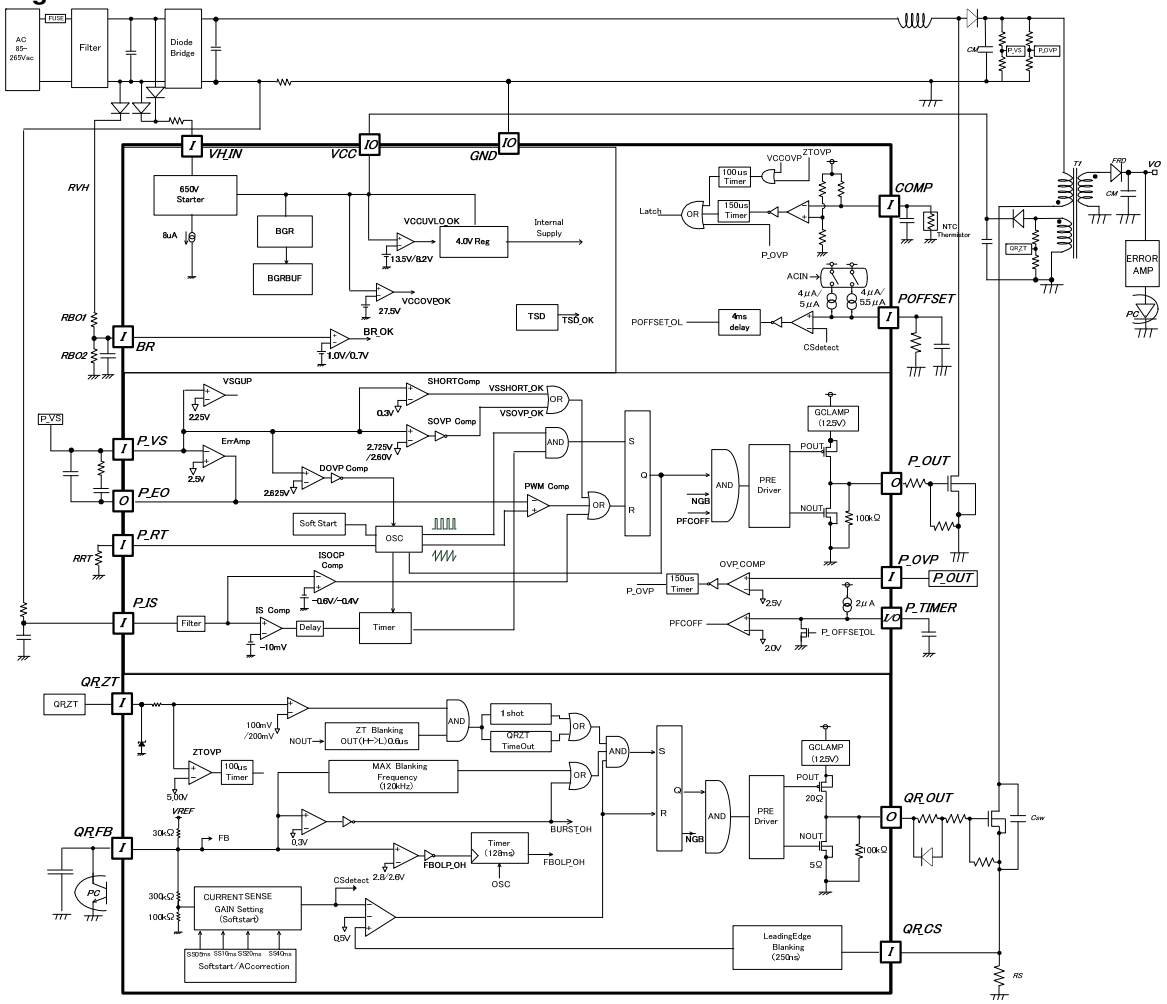


Figure 3. Block Diagram

Description of Blocks

(1) Starter Block (VH_IN Pin)

The IC builds in starter circuit which tolerates 650V. It is shown in Figure 4. For that it enables low standby mode current consumption and high speed starting.
After starting, current consumption is idle I_{START3} (typ=8uA) only. (Shown in Figure 5)
To supply electric power from AC supply to VH_IN pin, diode rectification connection is needed from both AC input.
It is shown in Figure 4.

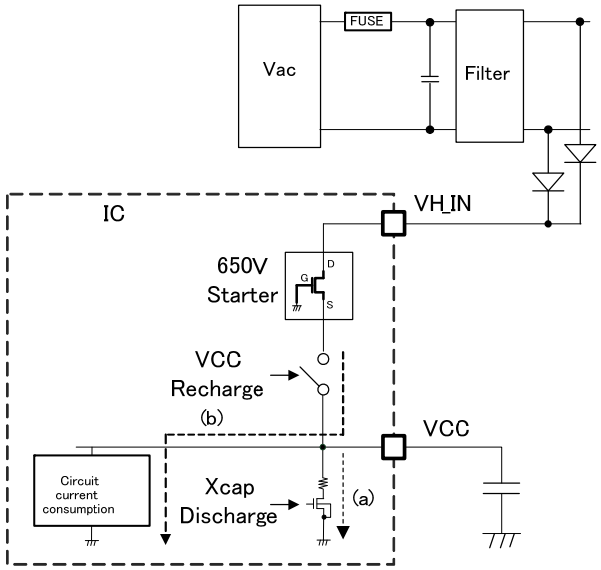


Figure 4. Starter Circuit Block Diagram

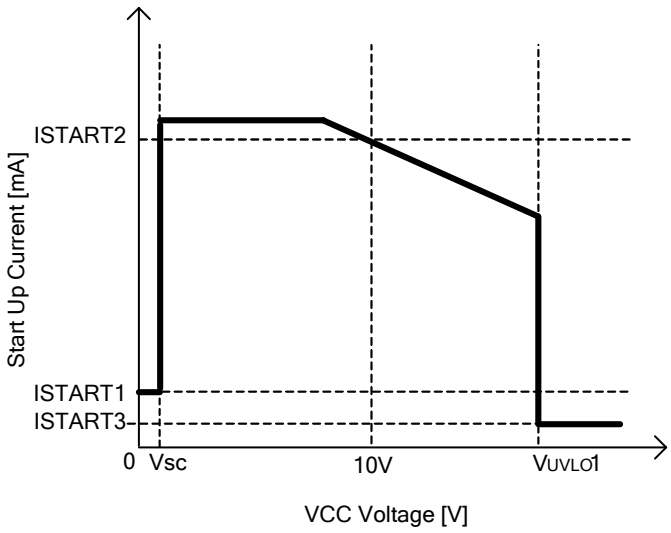


Figure 5. Start-up Current vs VCC Voltage

In addition, VH_IN pin has an X-cap discharge function. If the input voltage peak of BR pin goes below 1.0V, discharge function starts after passing 256ms. X-cap discharge is the function that once VH_IN charge moves from VH_IN to VCC pin by VCC recharge function, IC discharges VCC charge by X-cap discharge node (Figure 4(a)).
In the case there is no power supply from the auxiliary winding such as a light load, the OLP state of the secondary side output, the IC operates VCC recharge function. VCC recharge function charges VCC pin from VH_IN pin, VCC pin voltage rises. As the result, X-cap is discharged. When VCC recharge function operates, the current path is Figure 4 (b). After it past 256ms timer from pulling out the outlet, X-cap function discharges the charge of X-cap by the current path of Figure 4(a).

(2) Start-Up Sequence(Soft Start Operation)

This IC has a built-in AC voltage detection function and this switches the over current detection voltage of PFC and POFFSET current (PFC OFF state only). When BR pin peak voltage > V_{ACIN1}(typ=2.5V), IC judges ACIN=H. When V_{BR1} < BR pin peak voltage <V_{ACIN1}, IC judges ACIN=L.

The over current detection voltage of PFC: The over current detection voltage of PFC is changed.
ACIN=H: -0.4V, ACIN=L: -0.6V
The POFFSET current at PFC OFF: POFFSET current at PFC=OFF is changed
ACIN=H: 5.0uA, ACIN=L: 5.5uA
*POFFSET current at PFC ON is fixed to 4.0uA regardless of ACIN setting.

At starting, IC initial condition is ACIN=L.

When the VCCUVLO is released and the brown out function is released, then IC starts. At starting, QR starts to operate in soft start first. After the soft start finishes, PFC starts to operate. After QR output is stable, in the case of POFFSET voltage > CS detect voltage PFC stops. The PFC off time is set at P_TIMER pin. In the case of POFFSET voltage < CS detect voltage for more than 4ms, PFC switches from OFF to ON. The waveform of start-up is shown in Figure 6.
However, if P_EO voltage isn't charge, PFC operates according to the charge of P_EO voltage.
・Operation explanation of Figure 6.

A: Input voltage is applied. Then the input voltage $\times\sqrt{2}$ is PFC output.
B: Charge current flows from VH_IN pin to the VCC pin capacitor through the start circuit. Then VCC pin voltage rises.
C: When V_{UVLO1} (typ=13.5V) < VCC pin, VCC UVLO is released and the internal regulator rises.
D: BR pin monitors AC voltage. It is confirmed by brown out protection function (BR pin>1.0V) that the condition is normal or not.
E: After the internal regulator rises, QR DC/DC part starts to operate. When the switching operation starts, PFC and the secondary output voltage VOUT rise. Please design that the secondary output voltage becomes a prescribed voltage within T_{FOLP} (typ=128ms) after starting QR DC/DC.

[QR Start-Up Operation]
E: IC adjusts the over-current limiter of QR DC/DC part during the operation of soft start 1 against over voltage and current rising. IC operates in the soft start1 state for T_{ss1} (typ=0.5ms). Then maximum current of QR is limited to 12%.
F: IC adjusts the over-current limiter of QR DC/DC part during the operation of soft start 2 against over voltage and current rising. IC operates in the soft start2 state for T_{ss2} (typ=1.0ms). Then maximum current of QR is limited to 25%.
G: IC adjusts the over-current limiter of QR DC/DC part during the operation of soft start 3 against over voltage and current rising. IC operates in the soft start3 state for T_{ss3} (typ=2.0ms). Then maximum current of QR is limited to 50%.
H: IC adjusts the over-current limiter of QR DC/DC part during the operation of soft start 4 against over voltage and current rising. IC operates in the soft start4 state for T_{ss4} (typ=4.0ms). Then maximum current of QR is limited to 75%.
I: When T_{SS4} (typ=4ms) passes from start-up, soft start function finishes.
J: When secondary output voltage is stable, the QR_FB voltage is stable by constant value corresponding to load current through photo coupler. At normal state, QR_FB voltage is QR_FB<V_{FOLP1B} (typ=2.60V).

[PFC Start-Up Operation]
I: When P_VS pin voltage is more than V_{P_SHORTH} (typ=0.3V), the IC judges that the PFC output is normal condition.After the soft start of QR finishes, PFC starts to operate. The ON width of P_OUT pin increases as P_EO voltage increases. IC makes the rising speed of error amp increase during P_VS<V_{PGUPH} (typ=2.25V).
K: If the output voltage become stability P_VS pin voltage stabilizes to the voltage of V_{P_SAMP} (typ=2.5V).
L: AC voltage is detected seven consecutive waveforms by BR pin. The operation is started by ACIN setting controlled by AC voltage.

The IC PFC OCP detect voltage is switched from -0.6V to -0.4V because ACIN=H is detected in Figure 6.

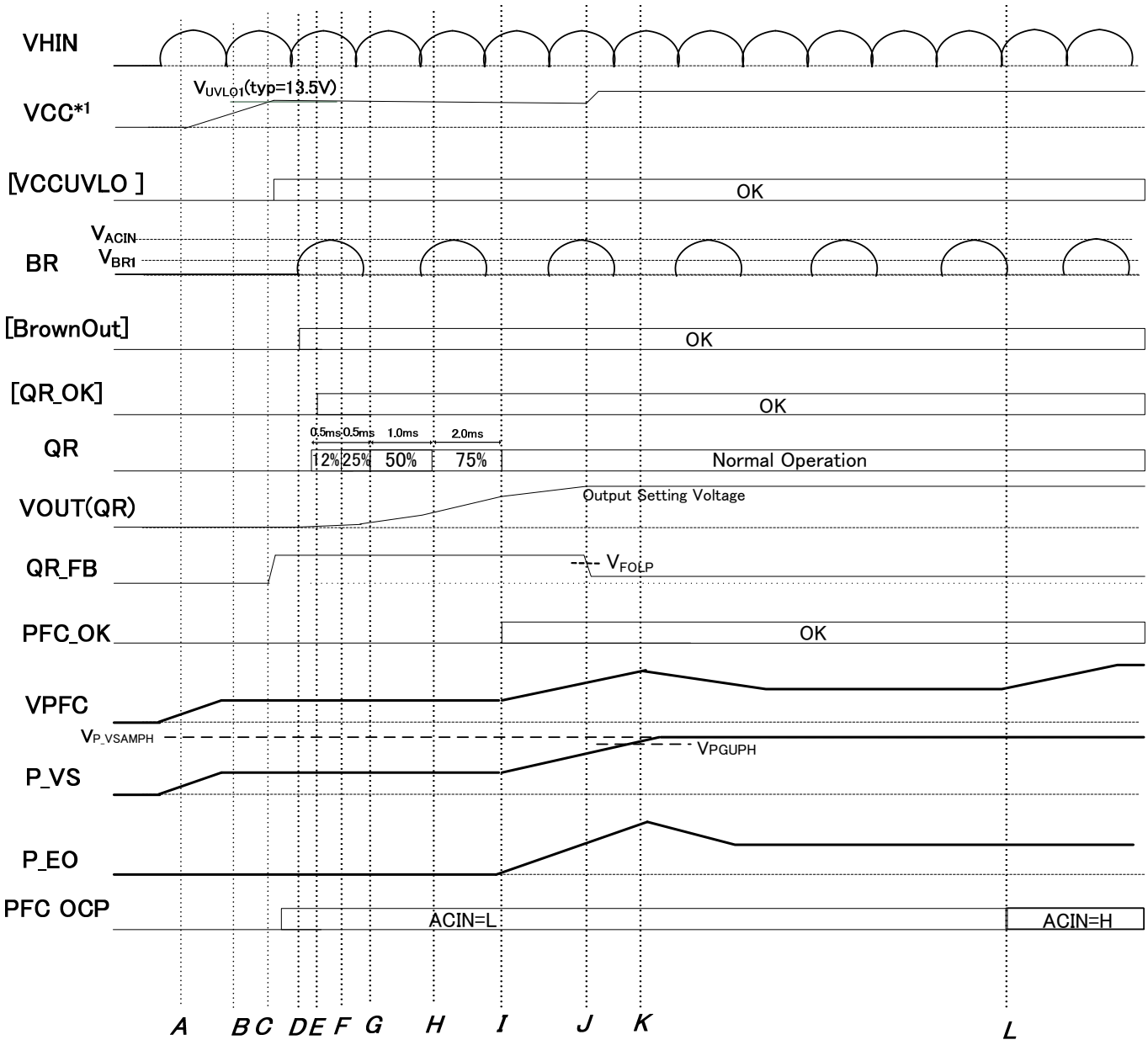


Figure 6. Start-up Sequence Timing Chart

(3) VCC Pin Protection Function

The IC builds in VCC low voltage protection function, "VCC UVLO (Under Voltage Lock Out)", VCC over voltage protection function, "VCC OVP (Over Voltage Protection)", and VCC charge function that operates in case the VCC voltage drops. VCC UVLO and VCC OVP are for stopping switching to prevent the switching MOSFET from destroying at abnormal voltage. VCC charge function stabilizes the secondary output voltage by stabilizing VCC voltage to charge the power from the high voltage line to VCC pin through the starter circuit when the VCC voltage drops.
And VCC pin releases latch protection when VCC voltage is low.

(3-1) VCC UVLO／VCC OVP Function

VCC UVLO is an auto recovery protection that has voltage hysteresis. VCC OVP is latch protection. VCCOVP has mask time to prevent a false detection by surge etc. When the situation of VCC pin voltage > V_{OVP} (typ=27.5) continues for T_{LATCH} (typ=100us), OVP protection is operated.

(3-2) VCC Charge Function

After the VCC pin voltage >V_{UVLO1}, once VCC < V_{CHG1} VCC charge function operates. Then VCC pin is charged from VH_IN pin through starter circuit. The function prevents VCC starting failure. In charging VCC, PFC switching operation is stopped to stable VCC pin charge. When the VCC pin voltage rises to VCC >V_{CHG2}, VCC charging is stopped, and PFC starts to work. The operations are shown in Figure 7. However, as VH_IN voltage is AC input, VCC is not charged in the range of low voltage. During this time, VCC charging function operates but VCC pin is not charged. Even If the AC voltage is low, adjust the value of VCC capacitor in order for VCC pin not to become lower than UVLO and more than 22uF is recommended as the value of VCC capacitor. And to prevent thermal runaway, this function also stops when the overheating of the IC operates.

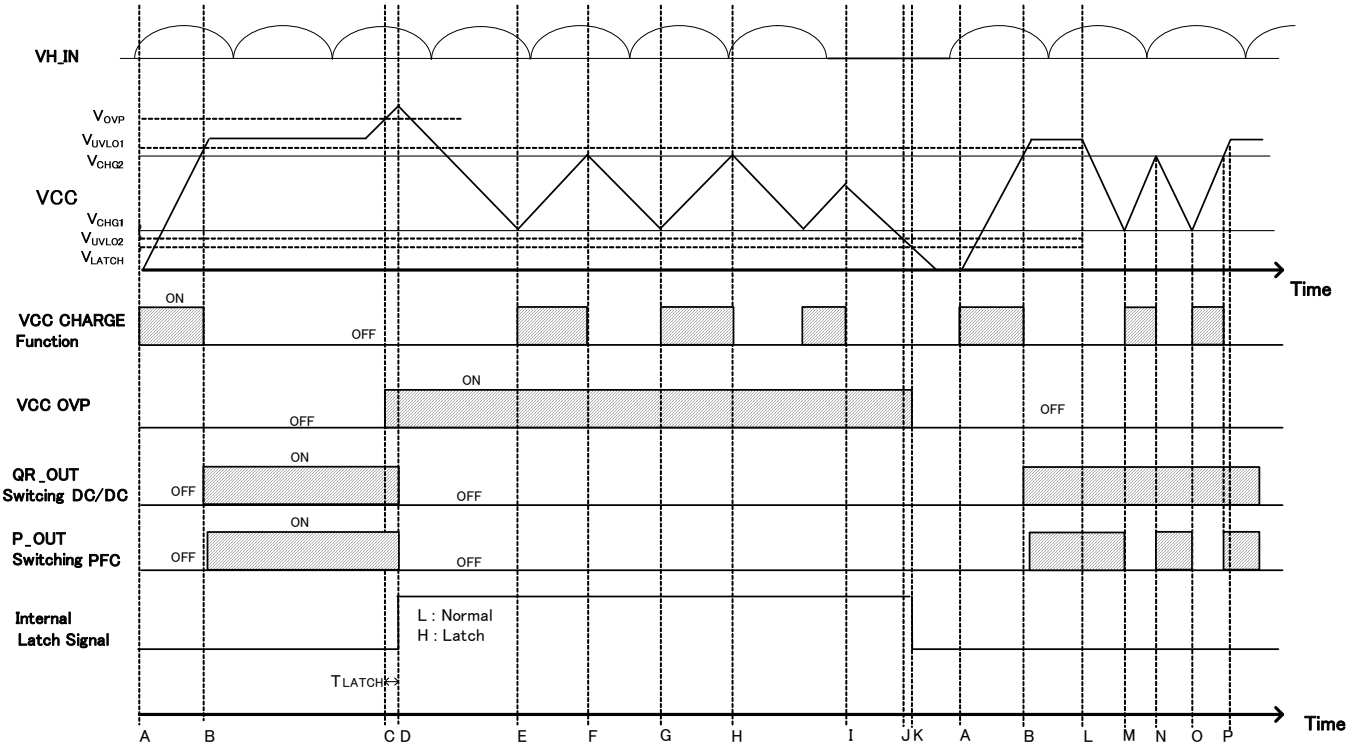


Figure 7. VCC UVLO / VCC OVP / VCC Charge Function Timing Chart

A: VH _IN pin voltage is applied, VCC pin voltage starts rising.
B: VCC > V_{UVLO1}, VCC UVLO is released, QR DC/DC operates. After that, PFC operation starts at QR soft-start finished.
C: VCC > V_{OVP}, VCC OVP detects the overvoltage in the IC.
D: If the state of VCC > V_{OVP} continues for T_{LATCH} (typ=100us) time, switching stops by the OVP function. (Latch mode).
E: Because of latch protection, PFC and QR don't operate switching. Then, VCC voltage decreases because there is supply from an auxiliary winding. If VCC pin voltage<V_{CHG1}, VCC pin voltage rises by operating VCC recharging function.
F: VCC pin voltage > V_{CHG2}, VCC recharge function stops. Because of latch protection, PFC and QR don't operate switching. By the operation of E and F, latch is not released since VCC voltage is stabilized. For that, latch protection is not released.
G: (The same as E.)
H: (The same as F.)
I: The voltage of VH_IN is stopped to supply. Then the brown out is detected and X-cap electrical discharge is started.
J: Because VH_IN is lost, VCC charging function operates but VCC is not charged. So VCC voltage decreases. If VCC pin voltage < V_{UVLO2}, VCC UVLO function operates.
K: VCC<V_{LATCH}, Latch is released.
L: When the secondary output has no load, QR DCDC works burst operation. VCC pin voltage drops because power does not supply from auxiliary winding
M: VCC<V_{CHG1}, VCC recharging function operates.
N: VCC> V_{CHG2}, VCC recharge function stops.
O: (The same as M.)
P: To increase a load, the power supply of the auxiliary winding starts.

However when the VCC recharge function operates, the standby power is increased because the loss of (VHIN voltage – VCC voltage) × VH current occurs. So design the application which supplies electricity from the auxiliary winding to VCC during no load. And operate VCC recharge function in time of a start-up assist, an over load protection, and a latch protection.

(4) COMP Pin (Outside forced stop function)

The COMP pin is used for forced stop function. When the COMP voltage is lower than V_{COMP} (typ=0.5V), PFC part and QR DC/DC part stop. A detection timer T_{COMP} (typ=150us) is built in to prevent detection errors caused by noise. The stop mode is latched.

The COMP pin is pulled up by R_{COMP} (typ=25.9kΩ), When the COMP pin is pulled down by a lower resistance value than R_T(typ=3.70kΩ), IC detects the abnormality and IC operates latch off. The application examples are shown in Figure 8, 9, 10.

Overheating Protection by NTC Thermistor

When a thermistor is attached to the COMP pin, latch stop can operate when overheating occurs.
In the case of this application, it should be designed so that the thermistor resistance becomes R_T (typ=3.70kΩ) when overheating is detected.
(Figure 8, 9 is application circuit examples in which latching occurs when Ta = 110°C.)
Please set the capacitor value less than 0.01uF to stabilize COMP pin voltage if COMP pin is attached capacitor to GND.

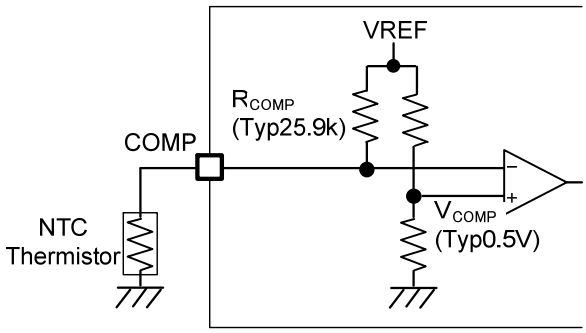


Figure 8. COMP Pin Overheating Protection Application

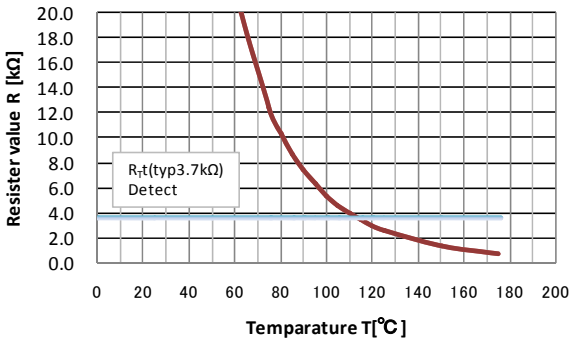


Figure 9. Temperature-Thermistor Resistance Value Characteristics

Secondary Output Voltage Overvoltage Protection

A photo-coupler is attached to the COMP pin to perform detection of secondary output overvoltage.

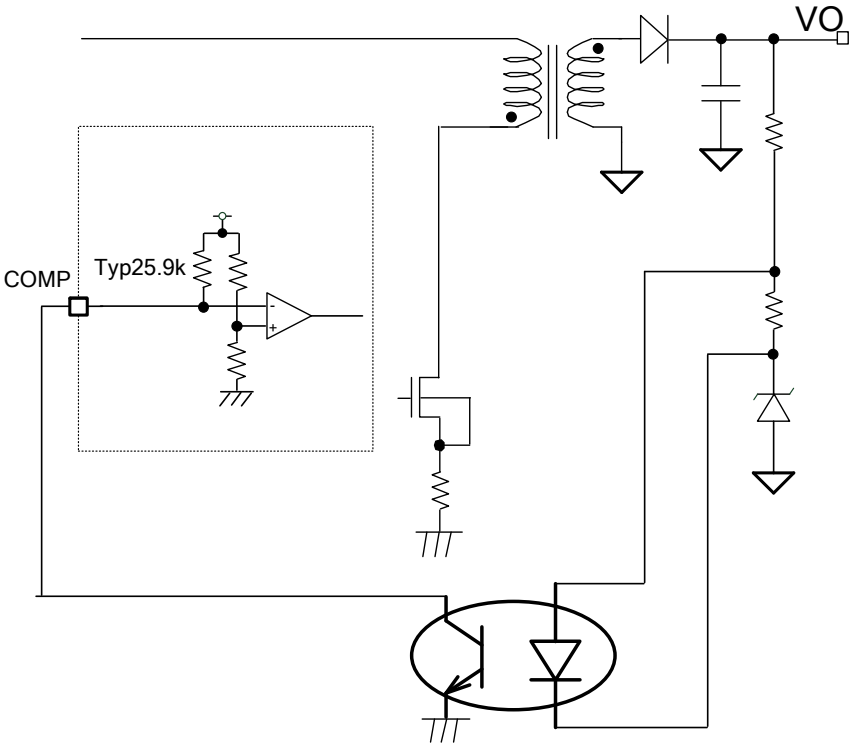


Figure 10. Output Overvoltage Protection Application

(5) BR Pin

The BR Pin has built-in three functions below. Usage example is shown in Figure 11.

1: Low AC voltage protection. (Blown IN/OUT) If BR pin voltage peak is lower than V_{BR1} (typ=1.0V), the operation is stopped.
2: When the condition is detected that BR pin voltage peak is lower than V_{BR1} (typ1.0V), x-cap discharging function is operated from VH_IN pin.
3: AC input voltage judges whether 240V or 100V, and the voltage level of the PFC over-current detection and POFFSET current are switched. When the peak of BR pin voltage is higher than V_{ACIN}(typ=2.5V),IC judges ACIN=H. And when it is lower, it judges AC100V.

The Input voltage to the BR pin is the full-wave / half-wave rectified AC waveform of 50Hz/60Hz voltage divided by resistance. In addition, in order to stabilize the input waveform, the capacitor (0.1nF to 10nF) must be connected close to the BR pin.

(5-1) Low AC Voltage Protection (Blown IN/OUT)

When AC voltage is low, blown out function can stop the PFC block and QR block operation. The AC input voltage is connected to the BR pin through two divider resistors. When the peak voltage of the BR pin is higher than V_{BR1} (typ=1.0V), the IC judges normal state and QR and PFC start to operate.

If the AC outlet is plugged out after the IC operates, QR and PFC stop after T_{BR} (typ=256ms) after the IC detects that BR pin exceeds V_{BR} (typ=1.0V) finally. Moreover, X capacitor discharge function is operated.

(5-2) X Capacitor Discharge Function

After it passes T_{BR} (typ=256ms) from AC voltage dropping, X-capacitor discharge function is operated.
X-cap discharge function operates to be linked VCC recharge function after VCC is discharged.

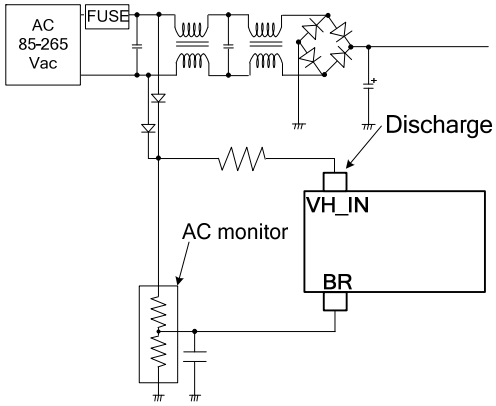
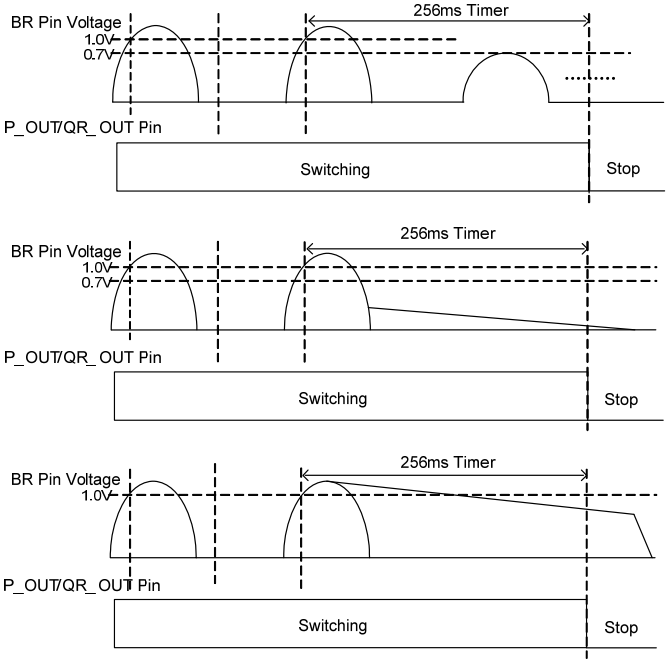


Figure 11. Blown IN/OUT Application Circuits



(1) When AC input voltage drops BR < V_{BR1} (typ=1.0V) for more than 256ms, QR /PFC operation stops.
In this case, X-Cap discharge function starts to operate.

(2) When the AC outlet is pulled out, BR pin voltage < V_{BR1} (typ=1.0V), QR DC/DC output stops after 256ms from the time which the BR terminal voltage drops to 1.0V or less.
In this case, Xcap discharge function operates.

(3) If the AC outlet is pulled out or BR pin voltage is higher than V_{BR1} (typ=1.0V), QR DC/DC does not stop.
After T_{BR} (typ=256ms) from the time which the BR pin peak voltage drops to V_{BR1}(typ=1.0V), QR / PFC stops and X-cap discharge function operates.

Figure 12. BR Pin Timing Chart

(6) The Quasi-Resonant DC/DC Driver

QR part of the IC operates with PFM (Pulse Frequency Modulation) mode method. By monitoring the QR_FB pin, QR_ZT pin, and QR_CS pin, it supplies an optimum system for QR DC/DC operation. it controls ON width (Turn Off) of external MOSFET by QR_FB pin and QR_CS pin. And it controls OFF width (Turn ON) of external MOSFET by QR_ZT pin. The details are shown below. (Refer to Figure 13)

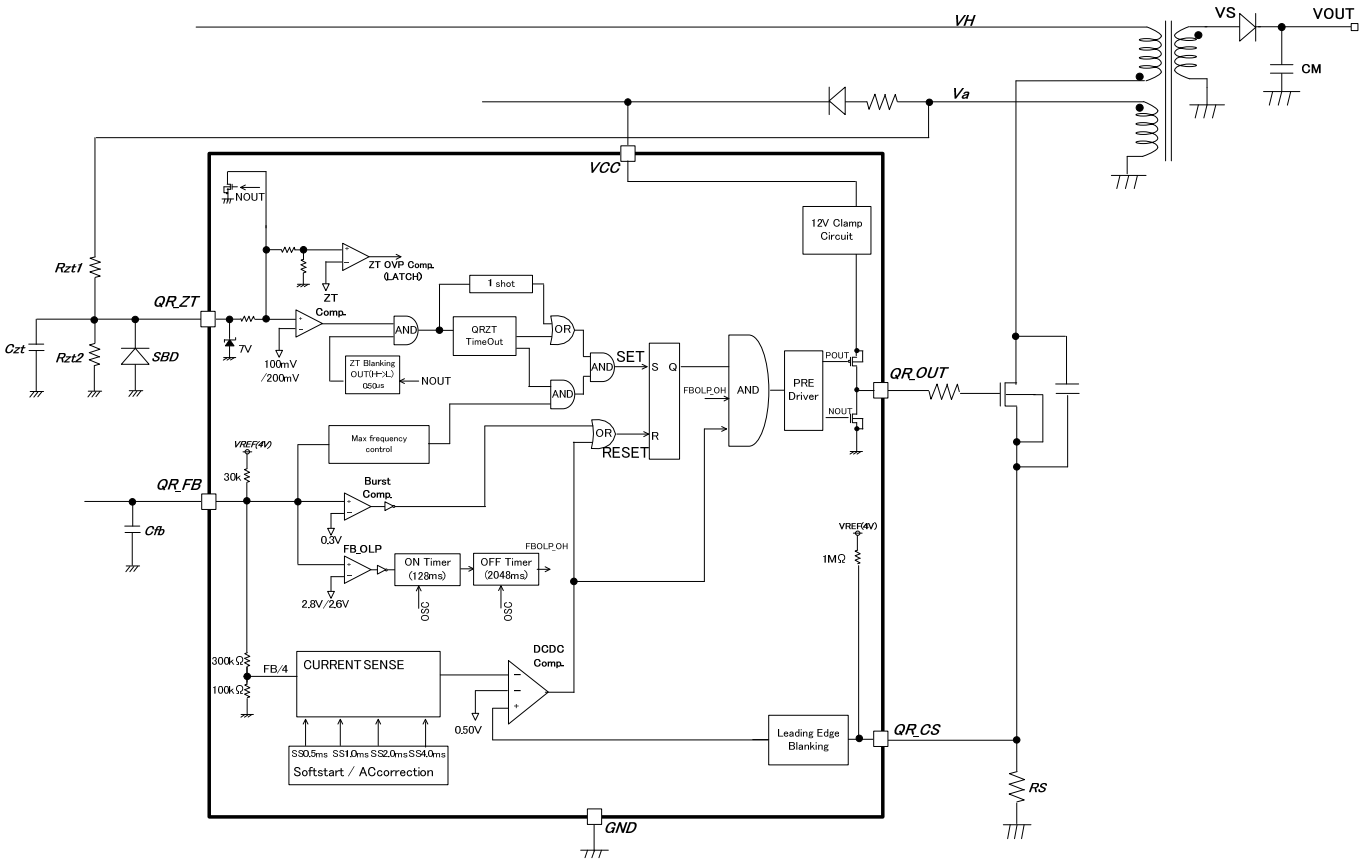


Figure 13. DC/DC Block Diagram

(6-1) Determination of ON width (Turn OFF)

ON width is controlled by QR_FB and QR_CS. The IC decides ON width by comparison between the value which QR_FB pin divided voltage by AV_{CS1} (typ=4) and QR_CS pin voltage. CS Limiter has changed comparator level lineally by QR_FB voltage shown in Figure 14. QR_CS voltage is also used over current limiter per pulse.
By changing over current limiter level and maximum blanking frequency by QR_FB voltage, IC regulates output.

mode1: Burst operation
mode2: Frequency reduction operation (reduce max frequency)
mode3: Max frequency operation (limited by max frequency)
mode4: Over load operation (To detect over load state, IC stops switching)

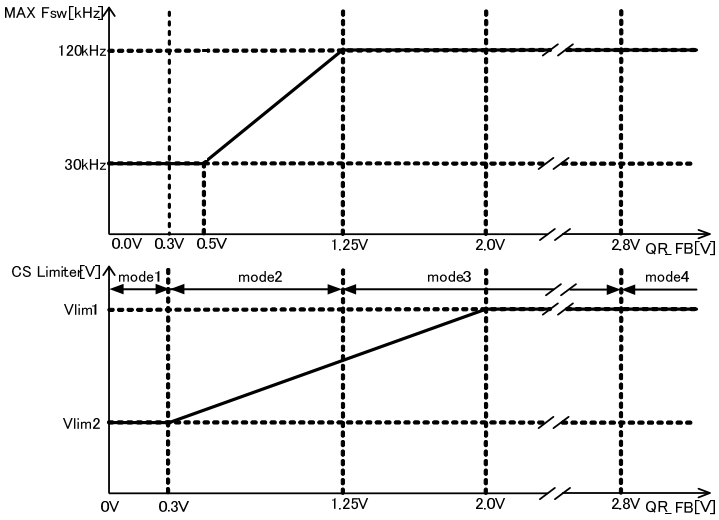


Figure 14. QR_FB Pin Voltage – Over-Current Limiter, Max Frequency Characteristics

To adjust over-current limiter level, CS Over-Current Protection voltage is switched in soft-start, AC voltage. Vlim1 and Vlim2 are changed below.

Table 2. Over-Current Protection Voltage Detail

Soft Start	CS current detection voltage	
	Vlim1	Vlim2
Start to 0.5ms	0.063V (12%)	0.009V (1.8%)
0.5ms to 1ms	0.125V (25%)	0.019V (3.8%)
1ms to 2ms	0.250V (50%)	0.038V (7.6%)
2ms to 4ms	0.375V (75%)	0.056V (11.2%)
4ms ≤	0.500V (100%)	0.075V (15%)

* The values inside ( ) shows comparative value with Vlim1(typ =0.5V)in normal operation.

(6-2) LEB (Leading Edge Blanking) Function

When a MOSFET for switching is turned ON, surge current occurs because of capacitance or rush current. Therefore, when QR_CS voltage rises temporarily, the over-current limiter circuit may result to miss detections. To prevent miss detections, the IC has a built-in blanking function which masks for T_{LEB} (typ=250ns) from switching QR_OUT pin from L to H. This blanking function enables to reduce noise filter of QR_CS pin.

(6-3) Determination of OFF Width (Turn on)

OFF width is controlled at the QR_ZT pin. When QR_OUT is Low, the power stored in the coil is supplied to the secondary-side output capacitor. When this power supply ends as there is no more current flowing to the secondary side, the drain pin voltage of switching MOSFET drops. Consequently, the voltage on the auxiliary winding also drops. A voltage that was resistance-divided by Rzt1 and Rzt2 is applied to QR_ZT pin. When this voltage level drops to V_{ZT1} (typ=100mV) or below, MOSFET is turned ON by the ZT comparator. Since zero current status is detected at the QR_ZT pin, time constants are generated using Czt, Rzt1, and Rzt2. Additionally, a ZT trigger mask function (described in section 6-4) and a ZT timeout function (described in section 6-5) are built in IC.

In addition, the voltage on auxiliary winding becomes negative value while the switching is turned ON, when the surge voltage negative is input to the QR_ZT pin, IC may be mal-functioned. For this reason, preventing QR_ZT voltage is lower than -0.3V, please connect a Schottky diode between the pin and GND. (Refer to Figure 13) And, when the diode flows large leak current, ZT voltage is changed, ZTOVP level has changed. For the reason, it needs to select low leakage current diode in high degree. The Schottky diode is recommended RB751CM-40, RB530VM-30, RB751VM-40(made by Rohm) .

(6-4) ZT Trigger Mask Function (Figure 15)

When MOSFET is switched from ON to OFF, surge noise may occur at the QR_ZT pin.
Then, the ZT comparator and ZTOVP comparator are masked for the T_{ZTMASK} time to prevent ZT comparator operation errors. (Figure 15)

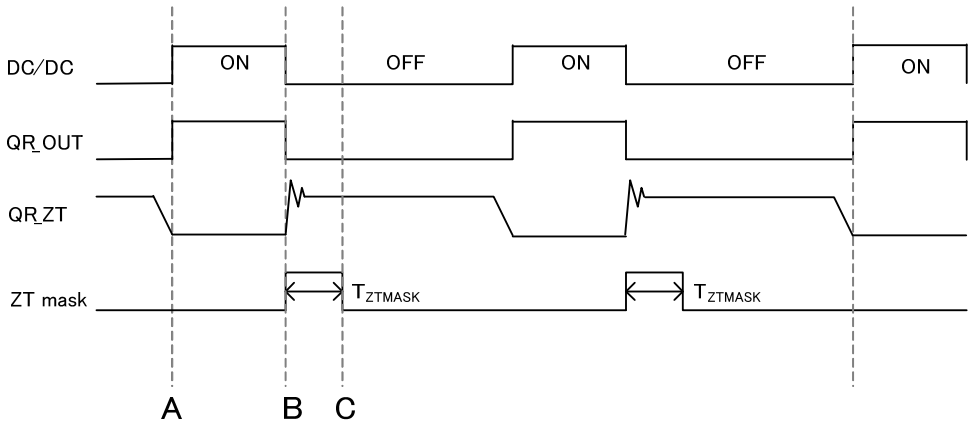


Figure 15. QR_ZT Trigger Mask function

A: DC/DC OFF => ON
B: DC/DC ON => OFF
C: Since a noise occurs to QR_ZT pin at B, the detection is masked ZT comparator and ZTOVP comparator detection for T_{ZTMASK} time.

(6-5) ZT Timeout Function (Figure 16)

(6-5-1) ZT Timeout Function 1

When QR_ZT pin voltage is not higher than V_{ZT2}(typ=200mV) for T_{ZTOUT1} such as start or low output voltage, or QR_ ZT pin shorts to GND, IC turns on MOSFET by force. (Figure 16)

(6-5-2) ZT Timeout Function 2

After ZT comparator detects V_{ZT1} low voltage level, when IC does not detect a following V_{ZT1} low voltage level within T_{ZTOUT2}, IC turns on MOSFET by force. After ZT comparator detects one bottom per one pulse, the function operates. For that, it does not operate at start or at low output voltage. When IC turns on more than 2nd bottom number, IC cannot detect QR_ZT low voltage level by decreasing auxiliary winding voltage. Then, the function is operated.

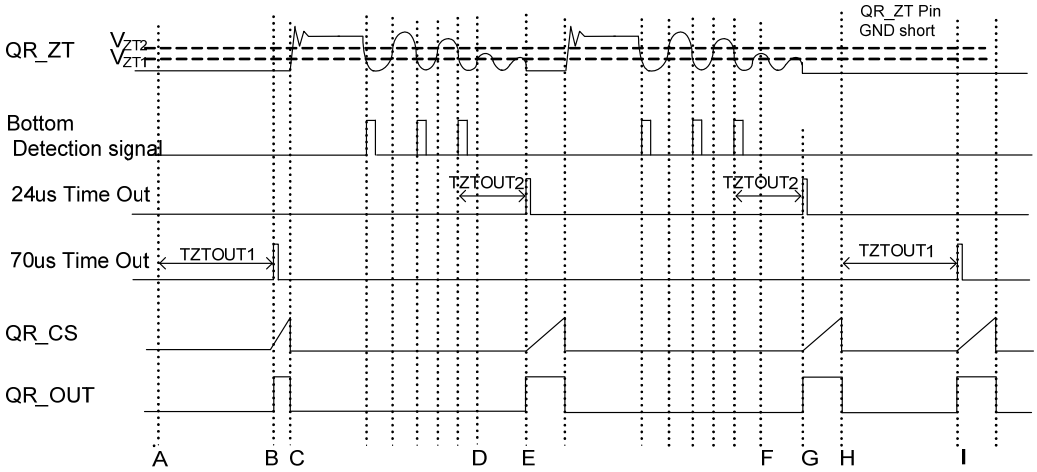


Figure 16. The Function of ZT Time Out.

A: At the starting, IC starts to operate by ZT timeout function1 for QR_ZT=0V.
B: MOSFET turns ON
C: MOSFET turns OFF
D: QR_ZT voltage decreases but the IC is not turned on by the maximum frequency function. During this function operated, QR_ZT peak voltage is lower than V_{ZT2} (typ=200mV) because of a reduction of QR_ZT pin vibration. After this, the maximum frequency function is released.
E: MOSFET turns ON by ZT timeout fucntion2 after T_{ZTOUT2} (typ=24us) from D point.
F: QR_ZT voltage decreases but the IC is not turned on by the maximum frequency function. During this function operated, QR_ZT peak voltage is lower than V_{ZTOUT2} (typ=200mV) because of a reduction of QR_ZT pin vibration.
G: MOSFET turns ON by ZT timeout fucntion2 after T_{ZTOUT2} (typ=24us) from F point.
H: QR_ZT pin is short to GND.
I: MOSFET turns ON by ZT timeout function1 after T_{ZTOUT1} (typ=70us).

(6-6) Soft Start operation

Normally, when AC voltage is applied, a large current flows, then secondary the output voltage and current overshoot. To prevent it, the IC has a built-in soft-start function. When VCC pin voltage is lower than V_{UVLO2}(typ=8.2V), IC is reset. After that, when AC voltage is applied, the IC operates soft-start. The soft start function is shown below:

start to 0.5ms	=>	Set QR_CS limiter to 12.5% of normal operation.
0.5ms to 1ms	=>	Set QR_CS limiter to 25% of normal operation.
1ms to 2ms	=>	Set QR_CS limiter to 50% of normal operation.
2ms to 4ms	=>	Set QR_CS limiter to 75% of normal operation.
More than 4ms	=>	normal operation

(6-7) QR_ZT OVP (Over Voltage Protection)

The built-in OVP function to QR_ZT pin of the IC has a protection type that is latch mode. ZTOVP corresponds to DC voltage detection and pulse detection for QR_ZT pin.

For DC detection, when the QR_ZT pin voltage is over V_{ZTL}(typ=5.0V) for T_{LATCH}(typ=100us), IC starts to detect ZTOVP function. For pulse detection, IC detects high voltage pulse of 3 count and T_{LATCH}(typ=100us) timer.

ZT OVP function operates in all states (normal state and over load state and burst state) after T_{ZTMASK}(typ=0.5us) to prevent ZT OVP from miss-detecting by surge noise,.

For pulse detection, ZT OVP operation starts detection after T_{ZTMASK} delay time from QR_OUT: H->L

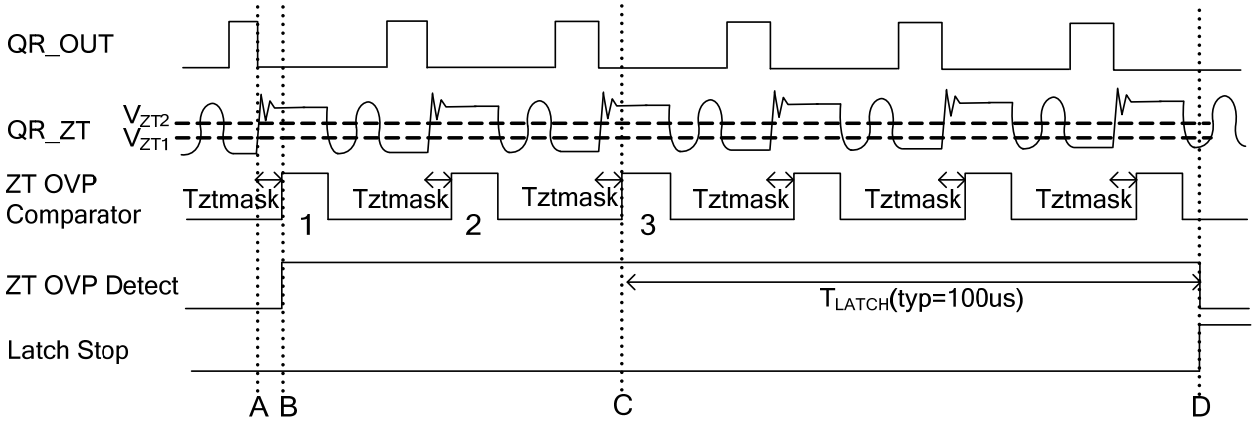


Figure 17. The Function of Latch Mask and ZT OVP (pulse detection)

A: When QR_OUT voltage is changed from H to L, the surge occurs at QR_ZT pin. However, QR_ZT pin OVP is not detected by T_{ZTMASK} (typ=0.5us).

B: After it passes T_{ZTMASK} time (typ=0.5us) from A point, the IC detects QR_ZT pin OVP by ZT OVP comparator when QR_ZT voltage > V_{ZTL} (typ=5.0V).

C: When ZTOVP comparator counts 3 pulse, T_{LATCH} timer (typ=100us) operates.

D: When the situation of pulse or DC of QR_ZT pin voltage > VZTL (typ=5.0V) continues for T_{LATCH} timer (typ=100us) from C point, IC operates latch protection by QR_ZT OVP function.

(6-9) QR_CS Open Protection

When QR_CS pin is OPEN, to prevent a malfunction of QR_OUT pin by a noise, the IC has built-in QR-CS pin open protection circuit. When QR_CS is open, QR_OUT switching is stopped by the function. (Auto recovery protection.)

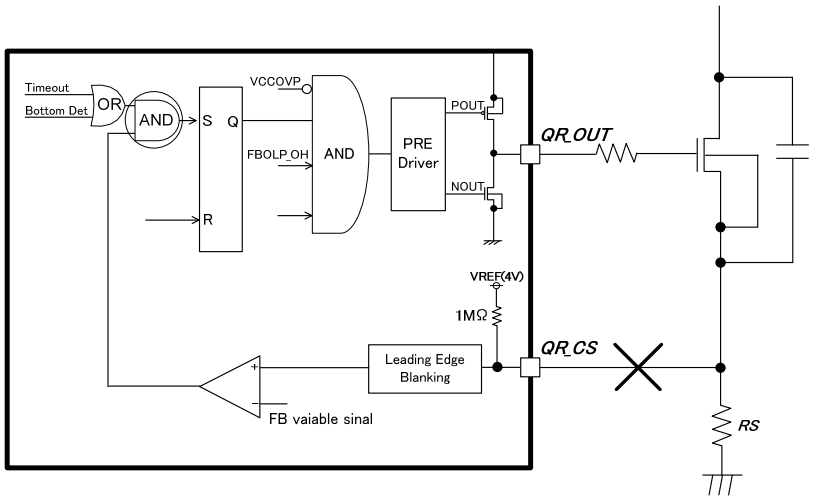


Figure 18. QR_CS Open Protection Circuit.

(6-10) OUTPUT Over Load Protection (FB OLP Comparator)

Over load protection is the function that monitors the load state of secondary output by QR_FB pin, and fixes QR_OUT pin on L. In over load status, photo-coupler has no current flow and QR_FB pin rise, over load protection is detected. If the condition continues for T_{FOLP} (typ=128ms), IC judges it is over load state, and QR_OUT pin and P_OUT pin is fixed to L. After QR_FB voltage is over V_{FOLP1A} (typ=2.8V), if QR_FB voltage is lower than V_{FOLP1B} (typ=2.6V) within T_{FOLP} (typ=128ms), over load protection timer is reset.

Because QR_FB is pull-up by a resistor to internal voltage , QR_FB voltage starts to operate in the state which is more than V_{FOLP1A} (typ=2.8V) in starting. For that, please set the stable time of secondary output voltage within T_{FOLP} (typ=128ms) from the starting. After detecting over load, IC is stopped for T_{OLPST} (typ =2048ms), and it is on auto-recovery operation. At this moment, the IC operates a soft start. In stopping switching, though VCC voltage decreases, the IC keeps the condition VCC pin voltage > V_{UVLO2} because VCC recharging function charges VCC voltage from the starting circuit.

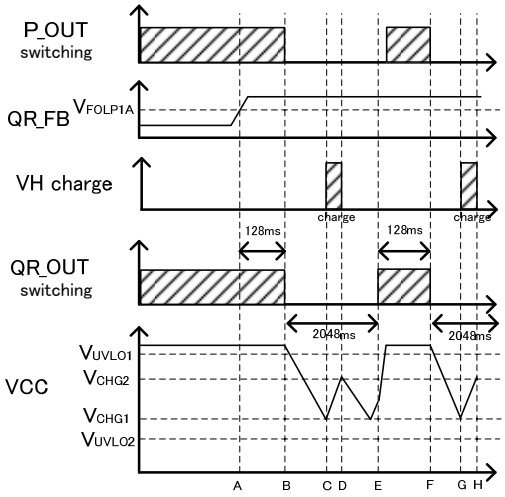


Figure 19. Auto Restart Operation by Over Load Protection.

A: Because of QR_FB > V_{FOLP1A}, FBOLP comparator detects over load.
B: When the state of A continues for T_{FOLP} (typ=128ms), the IC stops switching by over load protection.
C: During stopping switching by over load protection, VCC voltage drops. When VCC voltage is lower than V_{CHG1}, VCC re-charge function operates, and VCC voltage rises.
D: When VCC voltage is higher than V_{CHG2} by re-charge function, VCC recharge function is stopped.
E: It takes for T_{OLPST} (typ=2048ms) from B point until IC starts switching with soft-start.
F: While over load state continues, QR_FB voltage is over V_{FOLP1A}. When it passes for T_{FOLP} (typ=128ms) from E,IC stops switching.
G: During stopping switching, VCC voltage drops. When VCC voltage is lower than V_{CHG1}, VCC re-charge function operates and VCC voltage rises.
H: When VCC voltage is higher than V_{CHG2} by re-charge function, VCC recharge function is stopped.

(6-10) QR_OUT Pin Voltage Clamp Function

For the purpose of protecting the external MOSFET, H level of QR_OUT is clamped to V_{OUTH} (typ=12.5V)
It prevents gate destruction of MOSFET by rising VCC voltage. (refer to Figure 20) QR_OUT is pull-down R_{PDOUT} (typ=100kΩ).

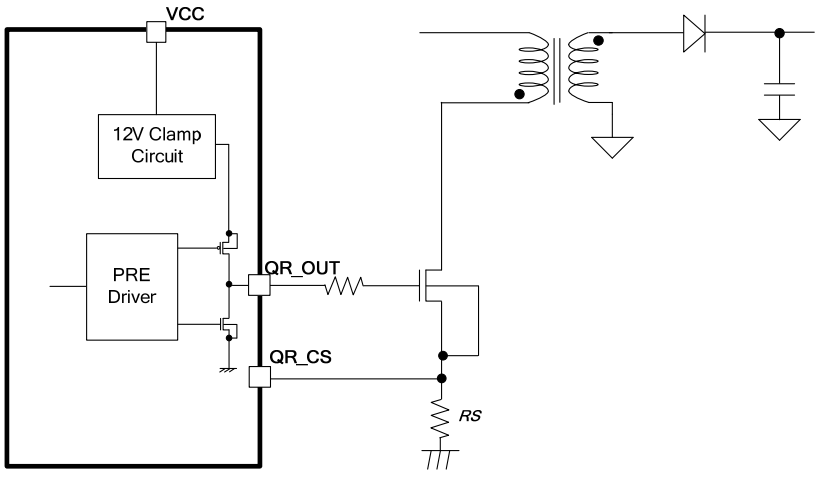


Figure 20. The Simple Circuit of QR_OUT Pin.

(7) Power Factor Correction (PFC: Power Factor Correction) Part

The Power Factor Correction Circuit is a voltage control method with the PFM boundary conduction mode. Because of this mode, ON width is fixed for a load. The operation circuit is shown in Figure 21 and switching operation is shown in Figure 22.

Switching Operation

(1) Inductor current (I_L) increases after MOSFET changes to ON.
(2) When Vramp voltage becomes higher by comparing with the slope set by P_RT pin, MOSFET turns OFF.
(3) MOSFET is set to be ON after P_IS pin detects at the zero point of IL.

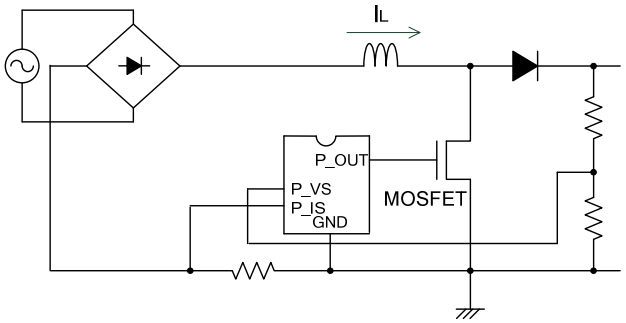


Figure 21. The Operation Circuit of PFC.

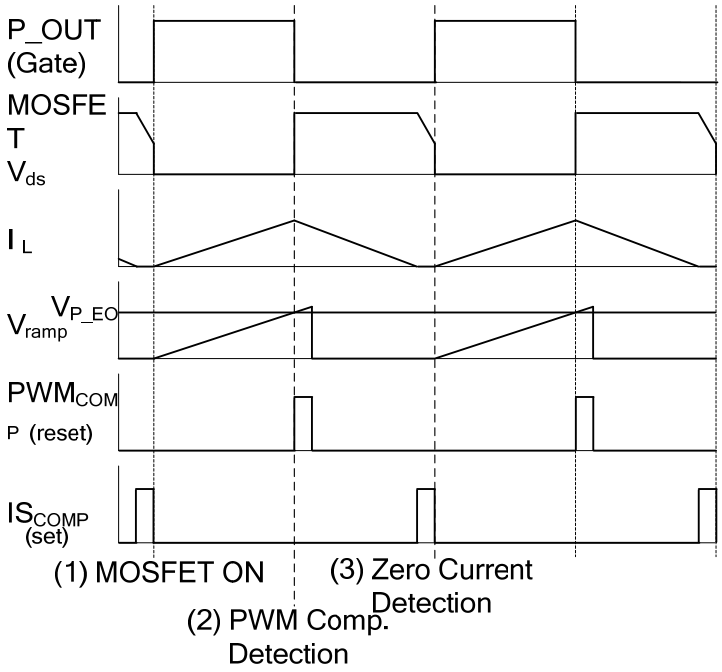


Figure 22. The Switching Timing Chart.

ON width is determined by Vramp voltage and V_{P_EO} pin voltage which controlled by loads. Vramp waveform is generated in the inside of the IC. Using this ON width fixing operation, peak current is decided by the below formula.

IL = Vac × Ton/L1 (IL: coil current, Vac: input voltage, ton: ON width, L1: PFC inductance)

In case of constant loads, IL is determined according to the value of Vac because Ton and L1 are a fixing value. As a result, there is no phase difference between AC current and AC voltage, and a higher harmonic wave becomes smaller. Zero current detection operates with a negative voltage detection at P_IS pin. The current flowing in sense resistor is detected by voltage.

If currents except for PFC loop flow to this resistor by the pattern of application board, the operation becomes an unstable condition because it can't detect current accurately. For that, please pay attention to the pattern of boards making application boards.

(7-1) gm amplifier

P_VS pin monitors a voltage divided resistors of PFC output voltage. P_VS voltage has the piled up ripple voltage of AC frequency (50Hz/60Hz).
The gm amplifier filters this ripple voltage and controls the voltage level of P_EO, by responding to error of P_VS pin voltage and internal reference voltage V_{P_VSAMP} (typ=2.5V).
Please remove the ripple of AC frequency by a error amp which is configured by P_EO pin shown in figure 23.
Gm constant is designed 44uA / V.

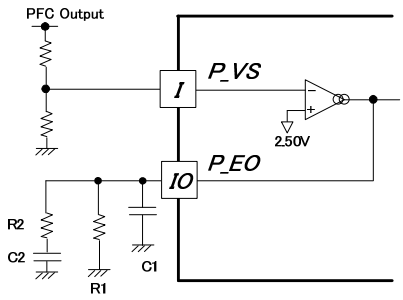


Figure 23. The Block Diagram of gm amplifier.

PFC works switching operation within the P_EO voltage range from about 0.8V to 3.0V. As P_EO pin voltage rises, the ON width of P_OUT pin becomes longer. And when it becomes lower than about 0.8V, the switching operation is stopped. For that, as P_EO pin is shorted to GND forcibly by the exterior, it enables to stop the PFC operation.
The transfer function of an error amp is shown below.

$$G = \frac{Vout}{Vin} = gm \times Z = gm \times \frac{1}{\frac{1}{Rout} + \frac{1}{R1} + \frac{1}{R2 + \frac{1}{j\omega C2}} + j\omega C1}$$

(In this formula, Rout means an output impedance of an amplifier.)
In the case of attaching R1, P_EO voltage is clamped by the voltage which is multiplied by gm amplifier current and R1
If R1 is attached, R1 should be higher than 1MΩ. Basically, it is recommended that R1 is not attached.
Figure 24 shows this specific characteristic.

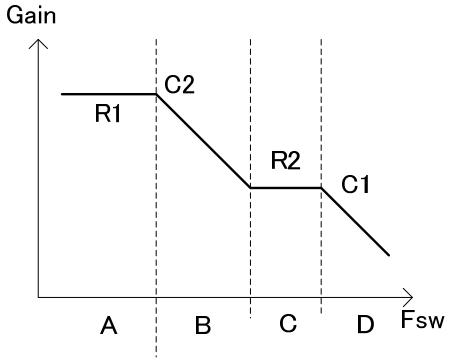


Figure 24. gm amplifier specific characteristic of frequency

According to the transfer function and Figure 24,
If you want the gain of A area to rise, please rise R1.
If you want pole between A to B to lower, please rise C2
If you want the gain of C area to rise, please rise R2.
If you want pole between C to D to lower, please rise C1

The whole of the transfer function as PFC determined by not only error amp but also IC peculiar gain, LC resonance, and the voltage dividing resistor of PFC output. Please set the invariable of the error amp and regulate the AC frequency in order it not to appear at P_EO pin. And it is necessary to check in real applications.

(7-2) P_VS Short Protection

The PFC built-in short protection function at P_VS works by stopping switching at P_OUT when P_VS voltage < V_{P_SHORT} (typ=0.3V: -88% voltage of PFC output). The operation is shown is Figure 25.

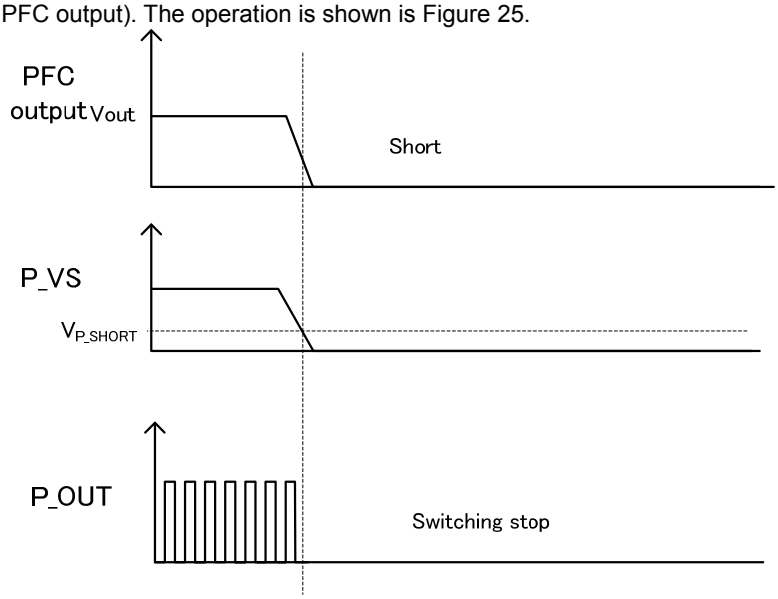


Figure 25. The Short Protection of P_VS Terminal..

(7-3) Gain Boost Function in P_VS low Voltage

When the output voltage lowers by occurring sudden load changes, the tarn of a lowing output voltage becomes longer because of the slow voltage control loop. Therefore, when P_VS pin voltage lowers to V_{PGUPH} (typ=2.25V), it is suitable for -10% of the output voltage, the IC speeds up the voltage control loop. In the operation, ON width at P_OUT pin increases, and PFC prevents the output voltage from dropping for a long time. This operation is stopped when P_VS pin voltage is higher than V_{PGUPH} (typ=2.25V).

(7-4) Gain Decrease Function in P_VS over Voltage (Dynamic OVP)

In case the output voltage rises by starting up or sudden output load changes, as PFC voltage response is slow, output voltage is high for a long time. Therefore, the IC speeds up voltage control loop gain by P_VS first voltage protection function when P_VS pin voltage is higher than V_{P_OVP1H} (typ=2.625V), it is suitable for +5% of the output voltage. In this operation, ON width at P_OUT pin decreases, the IC prevents output voltage from rising for a long time. This operation is stopped when P_VS pin voltage is lower than V_{P_OVP1H} (typ=2.625V).

(7-5) P_VS over Voltage Protection Function (Static OVP)

The IC has a second over voltage protection, for the case that P_VS voltage exceeds over the first over voltage protection voltage V_{P_OVP1H} (typ=2.625V). P_VS pin voltage is exceeded V_{P_OVP2H} (typ=2.725V), PFC switching is stopped instantly. When P_VS pin voltage decrease lower than V_{P_OVP3H} (typ=2.603V), switching operation is re-start. Refer to Figure 26.

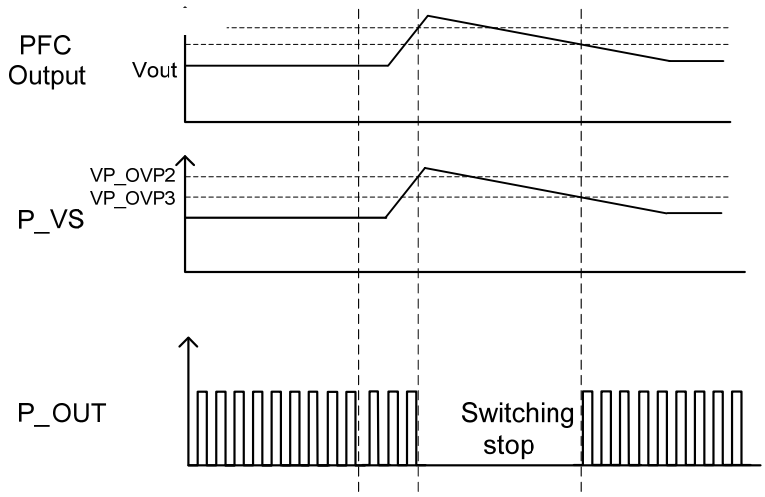


Figure 26. P_VS Over Voltage Protection (Auto Restart Mode).

(7-6) P_OVP pin Over Voltage Protection Function

P_OVP pin is an over voltage protection function which is available in the case that the output of PFC rises more than P_VS over voltage protection function V_{P_OVP2} under an abnormal condition made latch. (Refer to Figure 27) This function makes it possible to protect PFC by double putting together with P_VS over voltage protection function.
The IC stops switching operation (latch mode) after timer (typ=200us), if P_OVP increases more than V_{POVP4} (typ=2.5V). By the internal timer, the IC avoids detection error. The operation is shown is Figure 28.

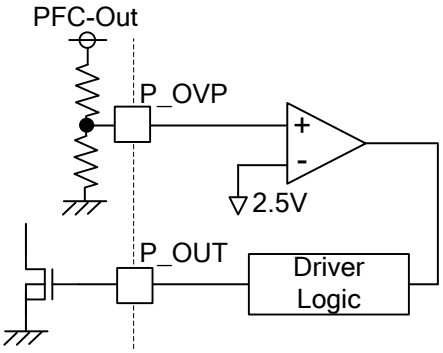


Figure 27. The Protection of P_POVP (Latch mode).

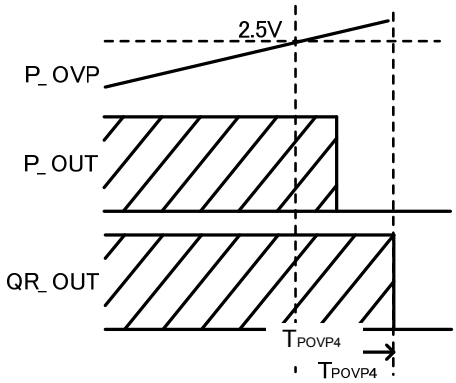


Figure 28. Timing Chart

(7-7) P_IS Pin: Zero Current Detection and Over-Current Detection Function

Zero current detection circuit is the function that detects zero cross of PFC inductor current (IL). (Shown in Figure30) The voltage of P_IS pin becomes more than the voltage of zero current detection and P_OUT output turn ON after it is passes for Delay time.

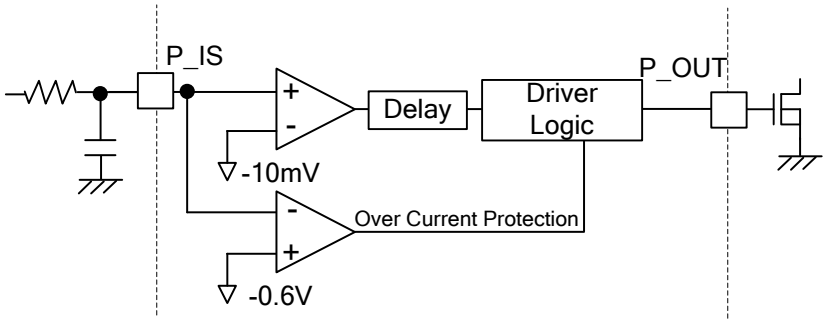


Figure 29. Current Detection Circuit of P_IS Terminal

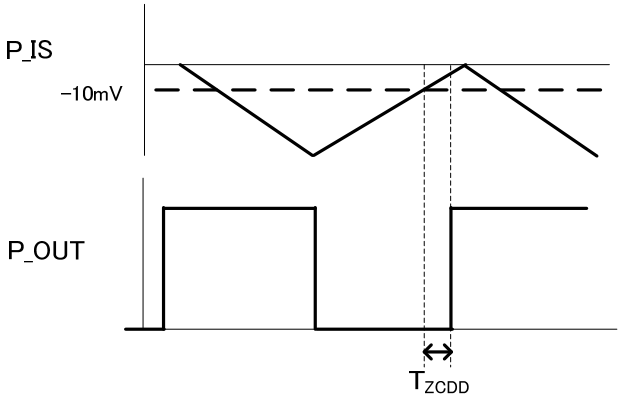


Figure 30. P_IS Zero Current Detection Delay Time

(7-8) P_IS pin over current detection protection function

In normal operation, turn OFF of PFC is controlled by the ON width determined by P_EO pin voltage. However, it turns OFF with pulse- by-pulse by operating over current protection when P_IS pin voltage is lower than the VISOCP voltage (IS over current detection voltage). VIS_OCP (ACIN=L: typ=-0.6V/ACIN=H : typ=-0.4V) This protection prevents the IC from flowing over current to MOSFET.

This function controls the ON width, so PFC voltage falls if the function operates. Please decide the sense resistor of PFC within the range of AC voltage specification in order the function not to operate in normal operation.
The level of over current detection protection switches by detecting AC voltage.

(7-9) P_RT pin setting

This pin sets the maximum frequency by external resistor which generated in the interior of the IC.
By P_RT resistor value, maximum frequency, maximum ON width, and P_IS delay time are set. They are shown in Figure 31-33. The maximum ON width for minimum AC voltage is calculated by the following expression on application.
The maximum ON width set by P_RT resistance is shown in Figure 31.

$$T_{MAXON}\,[s] = \frac{2 \times L \times P_O}{V_{ACMin}{}^2 \times \eta}$$

V_{ACMin}: Minimum Input power 、Inductor: L、Po : Max output power (W)、Efficiency : η [%]

The maximum ON width which set in Figure 31 needs to set more than TMAX ON width which shows above.
In order to improve the efficiency in a light load, the frequency rising in a light load is limited to set value at P_RT pin, by the maximum frequency of Figure 32.
Furthermore, Delay time from the comparator for zero cross detection VZCD (typ=-10mV) can be set in P_RT pin. (Refer to Figure 33)
The IC can't operate in more 500kHz than maximum frequency because it has a peculiar delay time, external MOSFET delay and delay time of drive circuit even if P_RT resistor is attached less than 39kΩ..

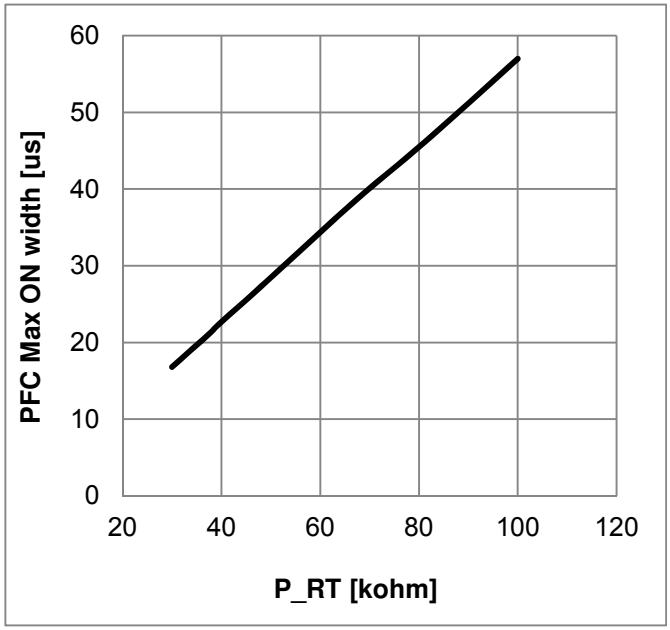


Figure 31. The Relationship of RT and Operation Frequency*

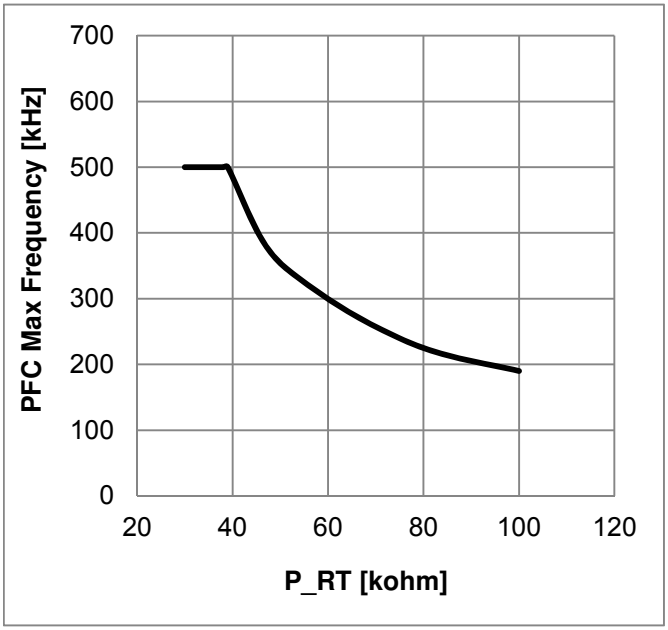


Figure 32. The Relationship of RT and ON Width*

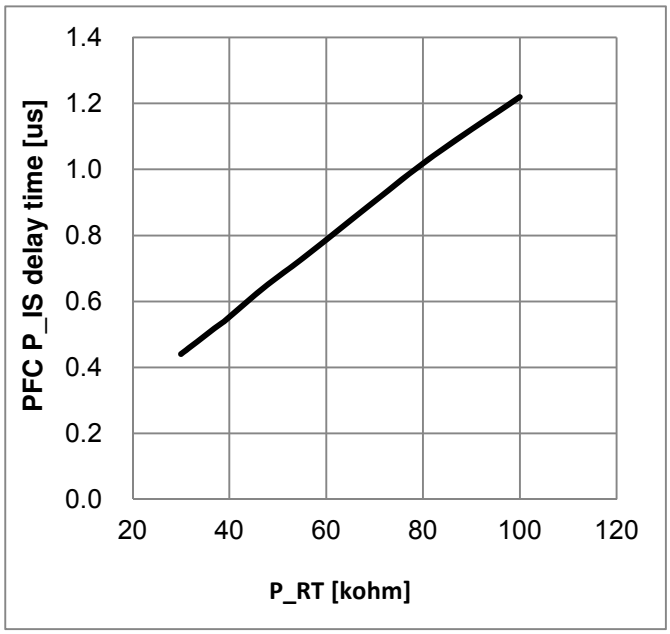


Figure 33. The Relationship of RT and PFC Zero Current Detection Delay*

*The above chart is for reference only. After confirmation of the actual device, please set the constant.

(7-10) PFC ON/OFF setting function

This is a function that stops PFC switching operation in a light load, and improve the efficiency of the whole of systems. PFC ON/OFF power is detected by a current limiter level of QR_CS pin (CS detection voltage). (It is CS detect shown in Figure 36.)

CS detect = QR_FB voltage / AV_{CS1}

In application design, QR_FB voltage is needed to set to the power which hopes PFC ON/OFF. The P_OFFSET voltage is calculated by QR_FB voltage /4. It is set by P_OFFSET resistor that P_OFFSET voltage corresponds to the value.

With comparing the current limiter voltage with the voltage set P_OFFSET pin, PFC ON/OFF electric power is set. The relation of CS detection voltage and QR_FB is shown in below. To set P_OFFSET voltage within the range of this CS detection voltage enables the IC to operate PFC ON/OFF.

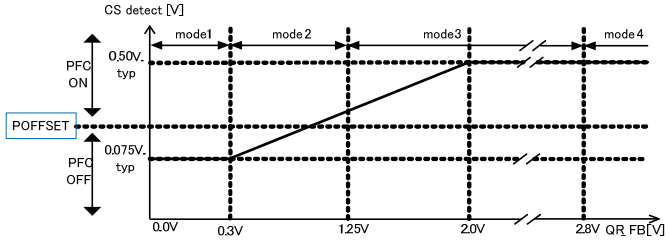


Figure 34. relation of CS detection(POFFSET) - QRFB voltage

The relation of CS detect signal and output voltage is shown in below.

Output power: $Po=1/2 \times Lp \times Ip^2 \times Fsw \times \eta=1/2 \times Lp \times (Vcs/Rs)^2 \times Fsw \times \eta$

(L: QR primary side inductance, V_{CS}: QR_CS detection voltage, Rs: sense resistor, Fsw: Switching frequency, η: efficiency)

V_{CS} = CS detection + Vpfc × Tondelay Lp*Rs (Vpfc: input voltage of QR)

The CS detection voltage is detected PFC ON/OFF.
According to this formula the graph of the relation is shown in Figure 35.

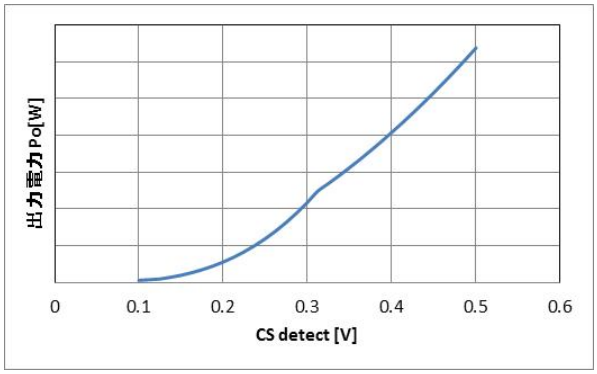


Figure 35. Relation of output power - CS detect voltage

IC operates PFC ON/OFF comparing CS detection voltage with POFFSET pin voltage. As a load increases in PFC OFF state, CS detection voltage increases. CS detection voltage increases than fixed P_OFFSET voltage for T_{PFCON} (typ=4ms), PFC turns from OFF to ON. While, as a load decreases in PFC ON state, CS detection voltage decreases. PFC turns OFF when the CS detection voltage lowers than the fixed POFFSET voltage.

It is expressed in electric specification that the P_OFFSET voltage turns PFC from ON to OFF in QR_CS = 0.15V (DC). It is regulated in P_OFFSET current in order to reduce the power varying of PFC ON/OFF (V_{OFSON}, V_{OFSOFF}) by decreasing the difference between CS detection voltage and P_OFFSET voltage. So that, there is a large varying in P_OFFSET current, but it is designed that the varying of CS detection voltage and P_OFFFSET become to be small.

P_OFFSET pin current is determined below.

PFC OFF :ACIN=L => PFC current is $I_{OFFSET3}$ (typ=5.5uA)
:ACIN=H => PFC current is $I_{OFFSET2}$ (typ=5.0uA)
PFC ON :Regardless of ACIN, PFC current is $I_{OFFSET1}$ (typ=4.0uA)

For the current, PFC ON/OFF is needed to adjust P_OFFSET pin resistor.
To compensate PFC ON/OFF power variation by AC voltage, PFC OFF current is changed in ACIN=H/L.
An operation circuit diagrams shown in Figure 36, a resources operation circuit diagram is shown in Figure37, and a switching operation is shown in Figure 38.

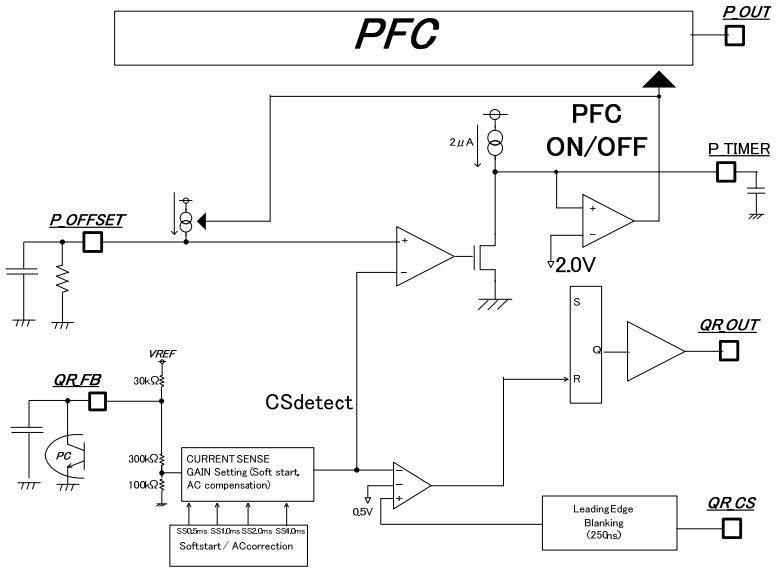


Figure 36. PFC ON/OFF operation circuit diagrams

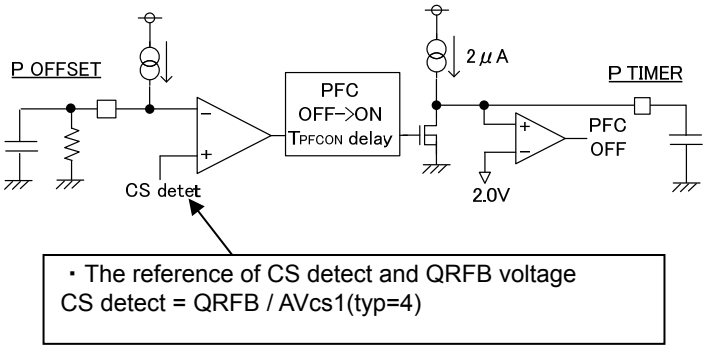


Figure 37. Resources Operation Circuit

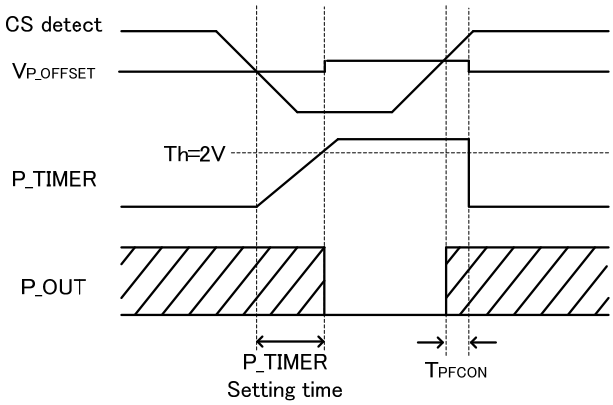


Figure 38. Timing Chart

Because CS detection voltage shown in Figure 37 is generated by QR_FB voltage. When QR_FB voltage ripple is large, PFC ON/OFF may not be at target point because CS detection voltage is also piled up ripple. In this case, please regulate output capacitors or capacitors of QR_FB pin and so on.

P_TIMER pin is setting time pin which sets the time of detecting output electric power decline (CS limit voltage decline) to stopping PFC (PFC: ON to OFF). In order not to switch PFC by changing loads in such a case of pulse loads, please coordinate the time by this pin.

If the QR loads become to be light, peak current of QR is lower. Thus, if the voltage of CS limit lowers than DC voltage setting at P_OFFSET pin, the IC starts to charge to external capacity of P_TIMER pin. P_TIMER pin voltage rises, and PFC is stopped at the moment of exceeding the P_TIMER detection voltage (typ=2.0V).

To stabilize the P_OFFSET voltage, a capacitor 0.1uF is recommended at P_OFFSET pin.

When it wants to decrease PFC OFF power setting, it needs to decrease P_OFFSET resistor. Then, IC may be burst operation. When IC operates in burst operation, it needs to fit P_TIMER capacitor value because PFC ON/OFF is decided by burst frequency and P_TIMER setting time. And, please confirm operation in an actual application when setting.

And if you want PFC to continue operation without PFC=OFF function, please connect P_OFFSET pin and P_TIMER pin to GND. And if PFC is operated in a light load condition, there is a possibility that a current supply from an auxiliary winding fails. In that case, please pay attention to VCC decreasing, and PFC and QR are stopping.

Furthermore, when it is set PFC ON/OFF by using external photo-coupler without using PFC ON/OFF function, set in below circuit.

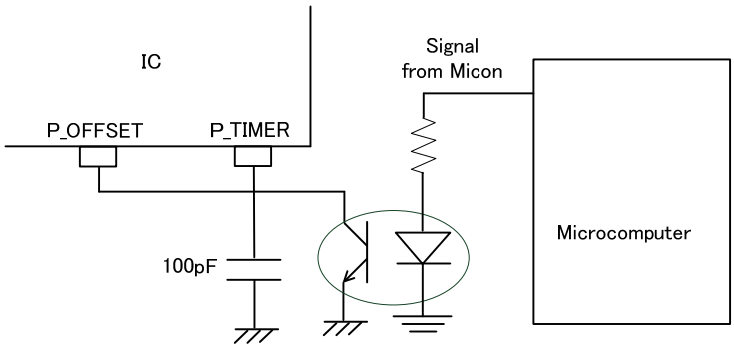


Figure 39. PFC ON/OFF circuit to use photo-coupler

Operation Mode of Protection Circuit

Operation mode of protection functions are shown in Table 3.

Table 3. Operation Mode of Protection Circuit.

Item	Comments	Operation Mode			
		Detection Method	Operation At Detection	Release Method	Operation At Release
VCCUVLO	VCC Pin Low Voltage Protection	VCC<8.2V （VCC Falling）	PFC Part, DC/DC Part STOP	VCC>13.5V （VCC Rising）	PFC Part, DC/DC Part Start Up Operation
VCCOVP	VCC Pin Over Voltage Protection	VCC>27.5V During 100us （VCC Rising）	PFC Part, DC/DC Part Latch STOP	VCC<6.2V （VCC Falling）	PFC Part, DC/DC Part Latch released
Brown Out	Input AC Voltage Low Voltage Protection	BR＜1.0V During 256ms （BR Falling）	PFC Par, DC/DC stop, X-Cap Discharging	BR>1.0V （BR Rising）	Normal Operation
COMP	COMP Pin Protection	COMP<0.5V During 150us （COMP Falling）	PFC Part, DC/DC Part Latch Stop	VCC<6.2V （VCC Falling）	PFC Part, DC/DC Part Latch released
QR_FB_OLP	QR_FB Pin Over-Current Protection	QR_FB>2.8V During 128ms （QR_FB Rising）	DC/DC ,PFC Parts STOP	QR_FB<2.6V During 2048ms （QR_FB Falling）	Normal Operation
QR_ZT OVP	QR_ZT Pin Over Voltage Protection	QR_ZT>5.0V During 100us （QR_QR_ZT Rising）	DC/DC, PFC Parts Latch STOP	VCC<6.2V （VCC Falling）	Latch released
P_IS_OCP	P_IS pin Short Protection	P_IS<-0.60V (P_IS Falling)	PFC Parts Output STOP	Pulse by Pulse	Normal Operation
P_VS Short Protection 1(2)	P_VS Pin Short Protection	P_VS<0.300V （P_VS Falling）	PFC Part Operation STOP	P_VS>0.300V （P_VS Rising）	Normal Operation
P_VS Gain rise voltage1(2)	P_VS Pin Low Voltage Gain Boost Function	P_VS<2.250V （P_VS Falling）	Gm-Amp. GAIN Boost	P_VS>2.250V （P_VS Rising）	Normal Operation
P_VS Gain fall voltage1(2)	P_VS Pin Dynamic Over Voltage Protection1	P_VS>2.625V （P_VS Rising）	Gm-Amp. GAIN Down	P_VS<2.625V （P_VS Falling）	Normal Operation
P_VS over voltage protection1(2)	P_VS Pin Static Over Voltage Protection2	P_VS>2.725V （P_VS Rising）	PFC Part STOP	P_VS<2.603V （P_VS Falling）	Normal Operation
P_OVP Over voltage protect	P_OVP Pin Over Voltage Protection3	P_OVP>2.5V During 200us （P_VS Rising）	PFC Part, DC/DC Part Latch Stop	VCC<6.2 V （VCC Falling）	PFC Part, DC/DC Part Latch released

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	V_{max1}	-0.3 to +30.0	V	VCC
Maximum Applied Voltage 2	V_{max2}	-0.3 to +650	V	VH_IN
Maximum Applied Voltage 3	V_{max3}	-0.3 to +15.0	V	P_OUT, QR_OUT
Maximum Applied Voltage 4	V_{max4}	-0.3 to +6.5	V	QR_FB, COMP, P_EO, BR, P_RT,P_OFFSET,P_OVP, P_VS, QR_CS, P_TIMER
Maximum Applied Voltage 5	V_{max5}	-0.3 to +7.0	V	QR_ZT
Maximum Applied Voltage 6	V_{max6}	-6.5 to +0.3	V	P_IS
P_OUT Pin Output Peak Current 1	I_{P_OUT1}	-0.5	A	
P_OUT Pin Output Peak Current 2	I_{P_OUT2}	+1.0	A	
QR_OUT Pin Output Peak Current 1	I_{QR_OUT1}	-0.5	A	
QR_OUT Pin Output Peak Current 2	I_{QR_OUT2}	+1.0	A	
Allowable Dissipation	P_d	0.68 (Note1)	W	mounted
Operating Temperature Range	T_{opr}	-40 to +105	°C	
Storage Temperature Range	T_{str}	-55 to +150	°C	

(Note1) Derate by 5.5 mW/°C when operating above Ta = 25°C when mounted (on 70 mm × 70 mm, 1.6 mm thick, glass epoxy on single-layer substrate).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Power supply voltage range 1	V_{CC}	8.9 to 26.0	V	VCC Pin Voltage
Power supply voltage range 2	V_H	80 to 500	V	VH_IN Pin Voltage

Recommended External Parts (Ta = 25°C)

Parameter	Symbol	Rating	Unit
VCC Pin Capacitor	C_{VCC}	22.0～	μF
BR Pin Capacitor	C_{BR}	0.1 to 10	nF
P_OFFSET Pin Capacitor	C_{P_OFFSET}	0.1～	uF
COMP Pin Capacitor	C_{COMP}	to 0.01	uF
QR_ZT pin diode	D_{ZTD}	Schottkey diode	-