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Datasheet

Middle Power Class-D Speaker Amplifier series

20W+20W Full Digital Speaker Amplifier with built-in DSP

BM28720MUV

General Description

BM28720MUV is a Full Digital Speaker Amplifier with built-in DSP (Digital Sound Processor) designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 20W+20W. This IC employs Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency. In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

Key Specifications

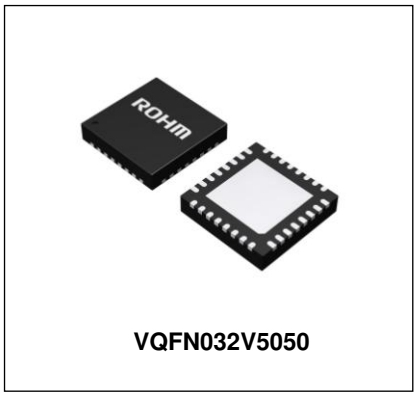
- Supply voltage (VCC) 10V to 24V
- Speaker output power (VCC=18.5V, R_L=8Ω) 20W+20W (Typ.)
- THD+N 0.07 [%] (Typ.)

Applications

- Flat Panel TVs (LCD, OEL)
- Home Audio
- Desktop PC
- Amusement equipments
- Electronic Music equipments, etc.

Package

	W(Typ) x D(Typ) x H(Max)
VQFN032V5050	5.00mm x 5.00mm x 1.00mm



VQFN032V5050

Features

- This IC includes the DSP (digital sound processor) for Audio signal processing for Flat TVs.
  12 Band/ch BQ, 3 Band DRC, Pre-Scaler, Channel Mixer, Fine Master Volume, Hard Clipper, Level Meter etc.
- This IC has one input systems of digital audio interface. (No needs of Master Clock)
  - I^2S / LJ / RJ format
  - LRCLK: 32k/44.1k/48KHz
  - BCLK: 32fs / 48fs / 64fs
  - SDATA: 16 / 20 / 24bit
- This IC has one output systems of digital audio interface.
  - I^2S format
  - SDATA: 16 / 20 / 24bit
- With wide range of power supply voltage.
- The monaural output that can reduce the number of external parts can be used.
- With high efficiency and low heat dissipation contributing to miniaturization, slim design, and also power saving of the system.
- Eliminates pop-noise generated during the power supply on/off. High quality muting performance is realized by using the soft-muting technology.
- This IC is built-in with various protection functions for highly reliability design.
  - High temperature protection
  - Under voltage protection
  - Output short protection
  - DC voltage protection
  - Clock stop protection
- Small package

Typical Application Circuit

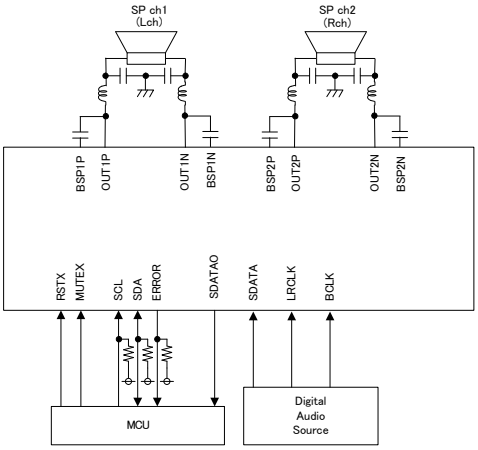


Figure 1. Typical application circuits

Pin configuration and Block diagram

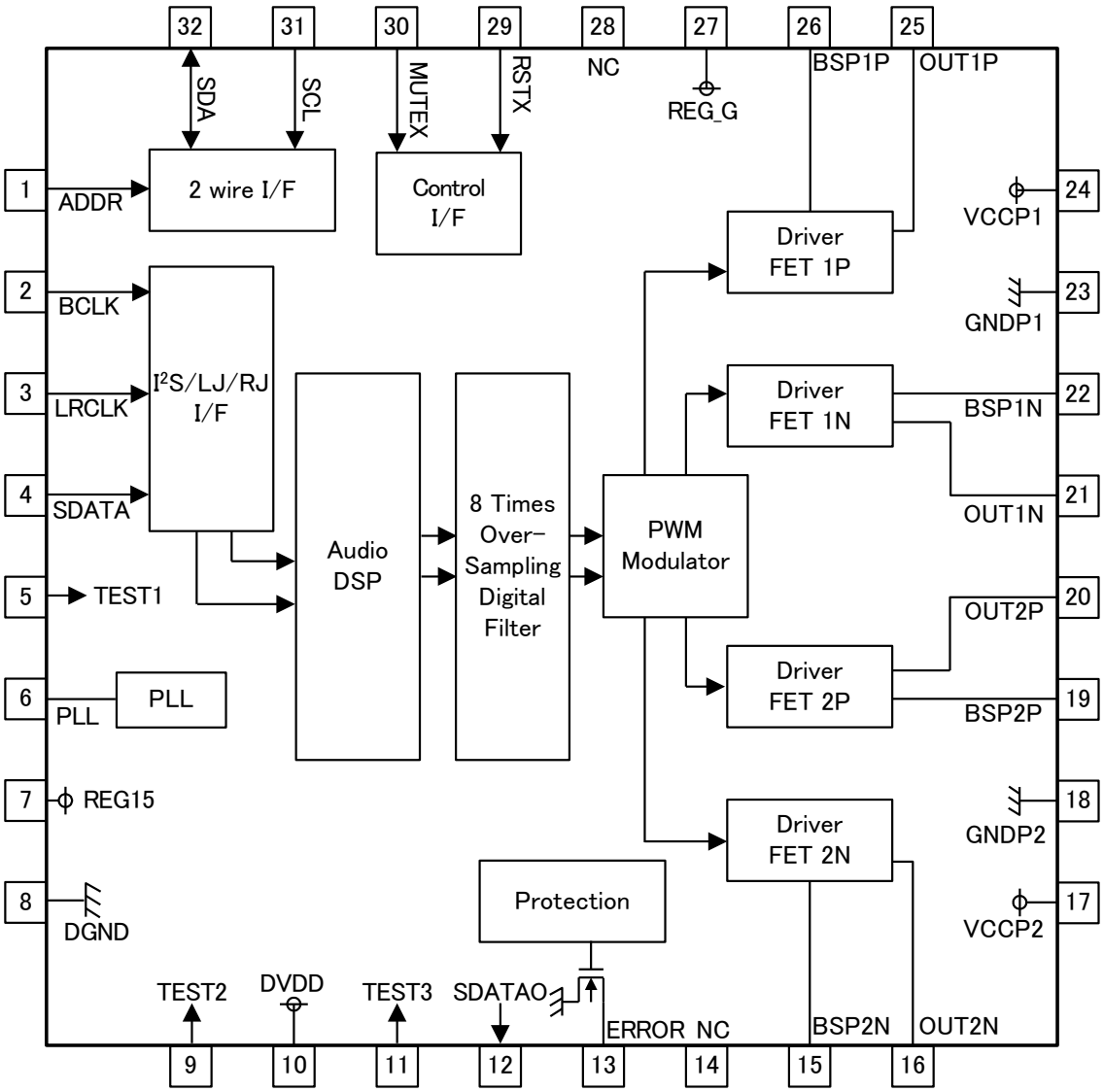


Figure 2. Pin configurations and Block diagram (Top View)

Pin Description

No.	Name	I/O	No.	Name	I/O	No.	Name	I/O	No.	Name	I/O
1	ADDR	I	9	TEST2	I	17	VCCP2	-	25	OUT1P	O
2	BCLK	I	10	DVDD	-	18	GNDP2	-	26	BSP1P	I
3	LRCK	I	11	TEST3	I	19	BSP2P	I	27	REG_G	O
4	SDATA	I	12	SDATAO	O	20	OUT2P	O	28	NC	-
5	TEST1	I	13	ERROR	O	21	OUT1N	O	29	RSTX	I
6	PLL	-	14	NC	-	22	BSP1N	I	30	MUTEX	I
7	REG15	O	15	BSP2N	I	23	GNDP1	-	31	SCL	I
8	DGND	-	16	OUT2N	O	24	VCCP1	-	32	SDA	I/O

I = input; O = output; - = others

Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	VCC	-0.3 to 34	V	Pin 17, 24 (Note 1) (Note 2)
	DVDD	-0.3 to 4.5	V	Pin 10 (Note 1)
Power dissipation	Pd	3.26	W	(Note 3)
		4.56	W	(Note 4)
Input voltage 1	VIN1	-0.3 to DVDD+0.3	V	Pin 1 - 5, 9, 11, 12, 13, 29 -32 (Note 1)
Terminal voltage 1	VPIN1	-0.3 to 7.0	V	Pin 27 (Note 1)
Terminal voltage 2	VPIN2	-0.3 to 29	V	Pin 16, 20, 21, 25 (Note 1)(Note 5)
Terminal voltage 3	VPIN3	OUTxx+6.0	V	Pin 15, 19, 22, 26 (Note 1)
Operating temperature range	Topr	-25 to +85	℃	
Storage temperature range	Tstg	-55 to +150	℃	
Maximum junction temperature	Tjmax	+150	℃	

(Note 1) The voltage that can be applied reference to GND (Pin 8, 18, 23).
(Note 2) Do not exceed Pd and Tjmax=150℃.
(Note 3) 74.2mm × 74.2mm × 1.6mm, FR4, 4-layer glass epoxy board
(Top and bottom layer back copper foil size: 20.2mm^2, 2nd and 3rd layer back copper foil size: 5505mm^2)
Derating in done at 26.1 mW/℃ for operating above Ta＝25℃. There are thermal via on the board.
(Note 4) 74.2mm × 74.2mm × 1.6mm, FR4, 4-layer glass epoxy board (Copper area 5505mm^2)
Derating in done at 36.5 mW/℃ for operating above Ta＝25℃. There are thermal via on the board.

(Note 5) It should use it below this ratings limit including the AC peak waveform (overshoot) for all conditions.
At only undershoot, it is admitted using at ≦10ns and ≦29V by the VCC reference. (Please refer following figure.)

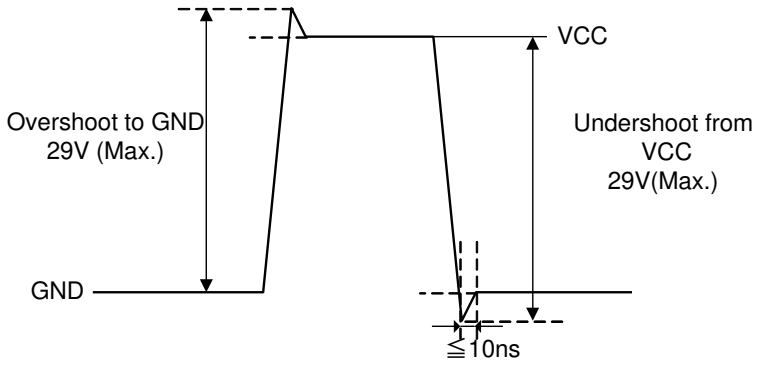


Figure 3.

Recommended Operating Ratings (Ta=25℃)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	VCC	10 to 24	V	Pin 17, 24 (Note 1) (Note 2)
	DVDD	3 to 3.6	V	Pin 10 (Note 1)
Minimum load impedance	R_L	5.4	Ω	Pin 16, 20, 21, 25 VCC = 18V to 24V (Note 6)
		3.6	Ω	Pin 16, 20, 21, 25 VCC < 18V (Note 6)

(Note 6) Do not exceed Pd.

Electrical Characteristics

(Unless otherwise specified Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz, R_L=8Ω, DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Total circuit						
Circuit current 1 (Normal mode)	I_{CC1}	-	45	90	mA	Pin 17, 24, No load
	I_{DD1}	-	9	19	mA	Pin 10, -infinity dBFS input, No load
Circuit current 2 (Reset mode)	I_{CC2}	-	10	40	μA	Pin 17, 24, No load RSTX=0V, MUTEX=0V
	I_{DD2}	-	2.5	7.0	mA	Pin 10, -infinity dBFS input, No load RSTX=0V, MUTEX=0V
Open-drain terminal Low level voltage	V_{ERR}	-	-	0.8	V	Pin 13, I_O=0.5mA
Regulator output voltage 1	V_{REG_G}	4.9	5.7	6.5	V	Pin 27
Regulator output voltage 2	V_{REG15}	1.3	1.5	1.7	V	Pin 7
High level input voltage	V_{IH}	2.5	-	3.3	V	Pin 1 - 5, 9, 11, 29 -32
Low level input voltage	V_{IL}	0	-	0.8	V	Pin 1 - 5, 9, 11, 29 -32
Input current (Input pull-up terminal)	I_{UP}	-150	-100	-50	μA	Pin 2 – 4 VIN = 0V
Input current (Input pull-down terminal)	I_{DN}	35	70	105	μA	Pin 1, 29, 30, VIN = 3.3V
Input current (SCL, SDA terminal)	I_{IL}	-1	0	-	μA	Pin 31, 32, VIN = 0V
Input current (SCL, SDA terminal)	I_{IH}	-	0	1	μA	Pin 31, 32, VIN = 3.3V
Speaker amplifier output						
Maximum output power 1	P_{O1}	-	10	-	W	VCC=13V,THD+N=10% (Note 7)
Maximum output power 2	P_{O2}	-	20	-	W	VCC=18.5V,THD+N=10% (Note 7)
Total harmonic distortion 1	THD1	-	0.07	-	%	P_O=1W, AES17 (Note 7)
Crosstalk 1	CT1	60	80	-	dB	VCC=13V, P_O=1W, A-weighted (Note 7)
Output noise voltage 1	V_{NO1}	-	80	-	μVrms	-infinity dBFS input, A-weighted (Note 7)
PWM sampling frequency	f_{PWM1}	-	256	-	kHz	fs=32 kHz
	f_{PWM2}	-	352.8	-	kHz	fs=44.1 kHz
	f_{PWM3}	-	384	-	kHz	fs=48 kHz

(Note 7) These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

Typical Performance Curves

Speaker output(Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=0V/3.3V, MUTEX=0V/3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

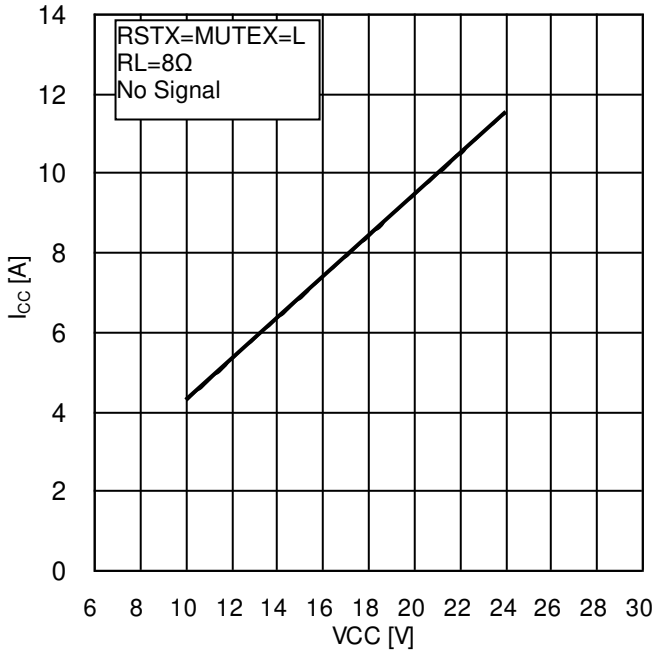


Figure 4.
Power supply voltage- Current consumption

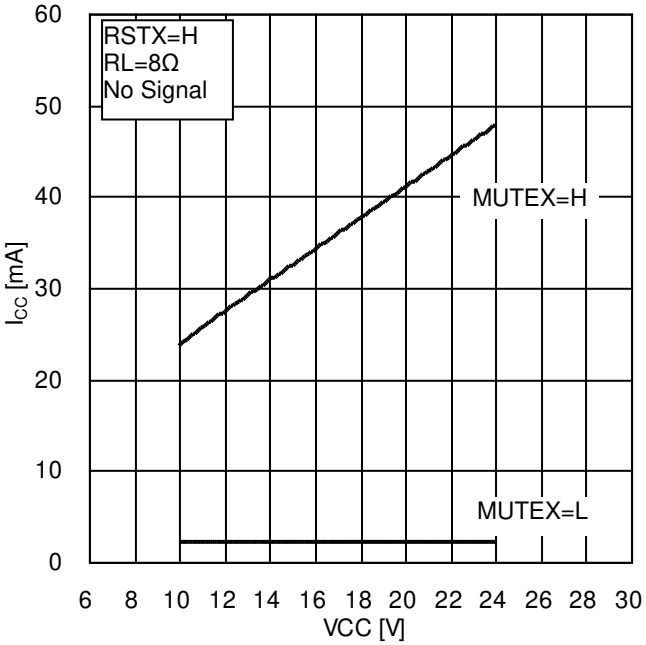


Figure 5.
Power supply voltage- Current consumption

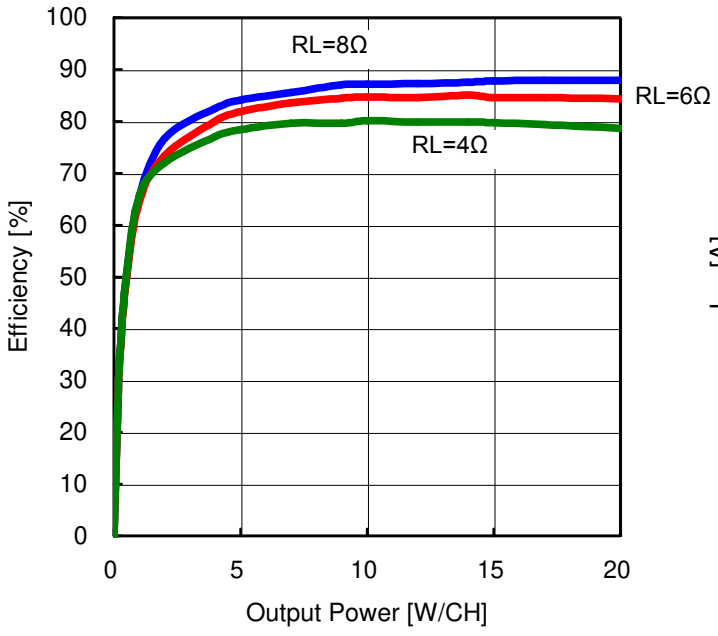


Figure 6.
Output power - Efficiency

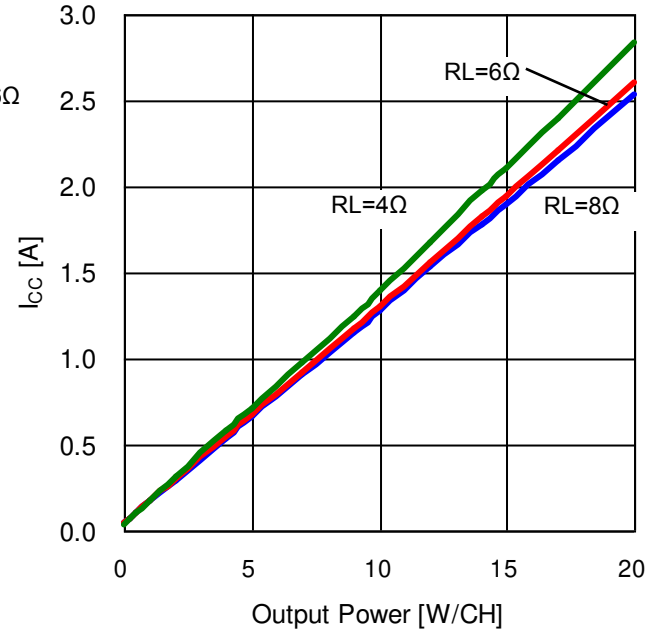


Figure 7.
Output power - Current consumption

Typical Performance Curves

Speaker output(Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

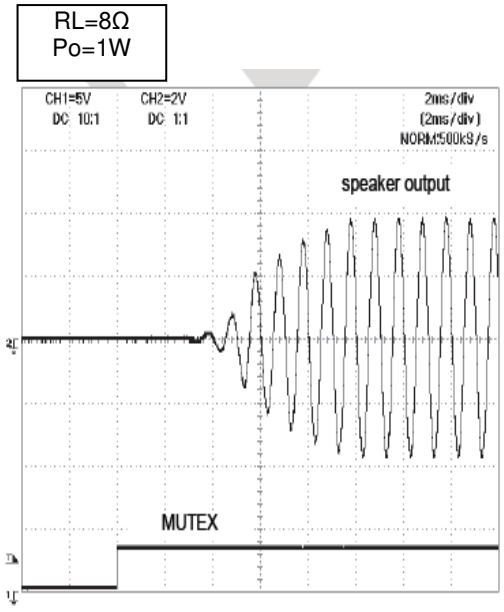


Figure 8.
Waveform at soft start

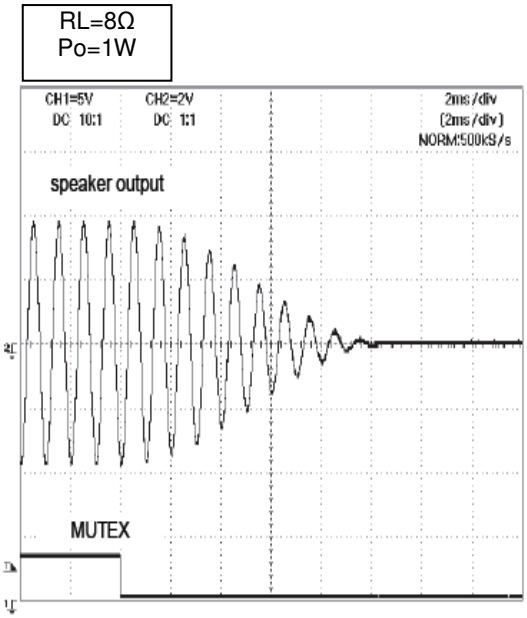


Figure 9.
Waveform at soft mute

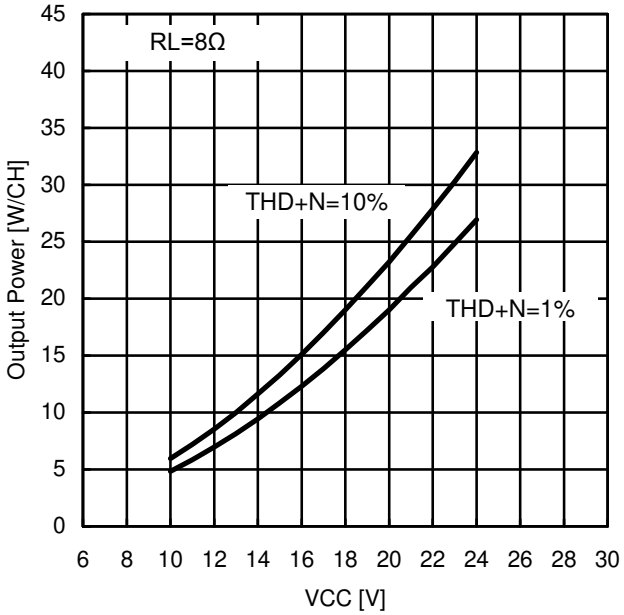


Figure 10.
Output voltage - Power voltage (R_L=8Ω)

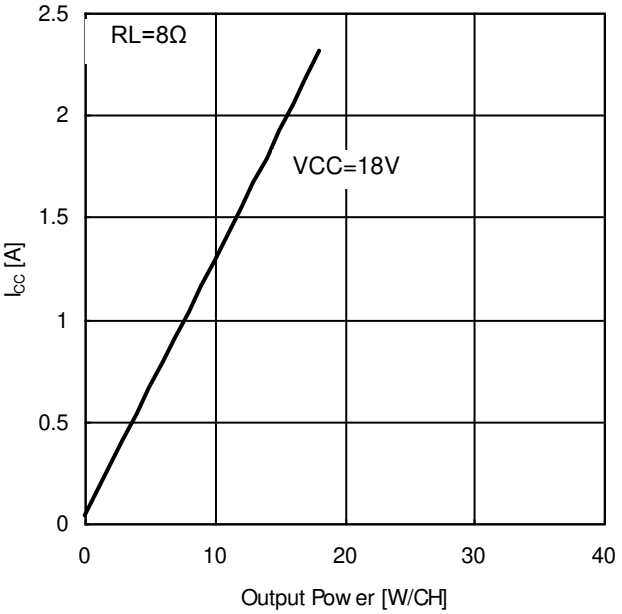


Figure 11.
Output power - Current consumption (R_L=8Ω)

※Dotted line means internal dissipation is over package power.

Typical Performance Curves

Speaker output(Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

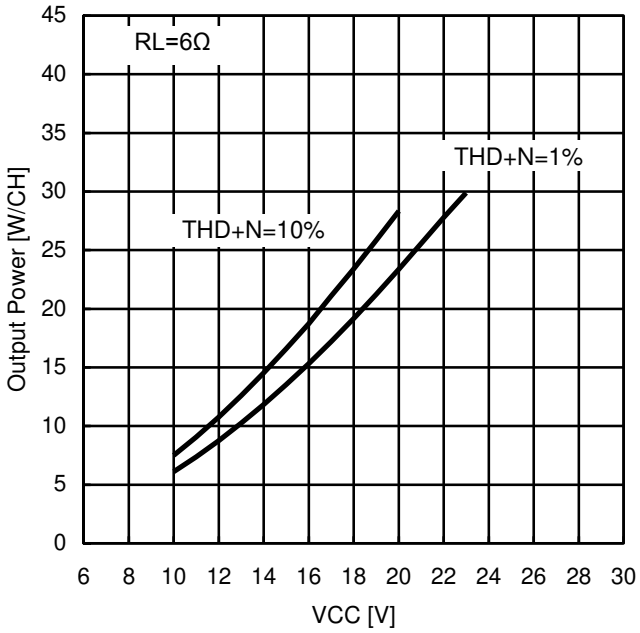


Figure 12.
Output voltage - Power voltage (R_L=6Ω)

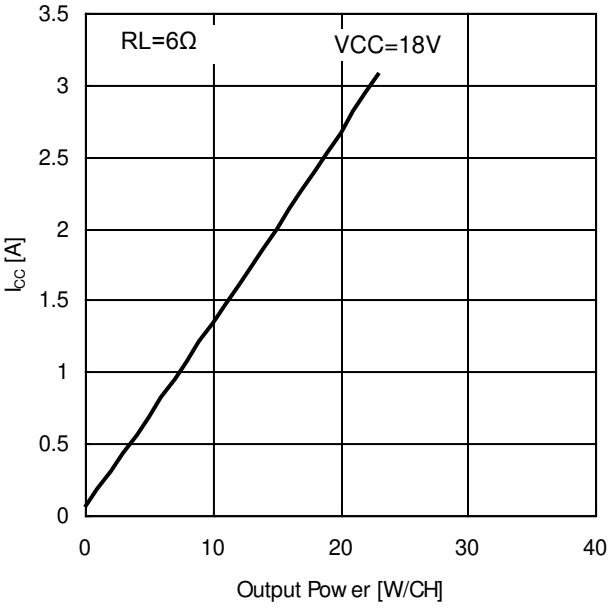


Figure 13.
Output power - Current consumption (R_L=6Ω)

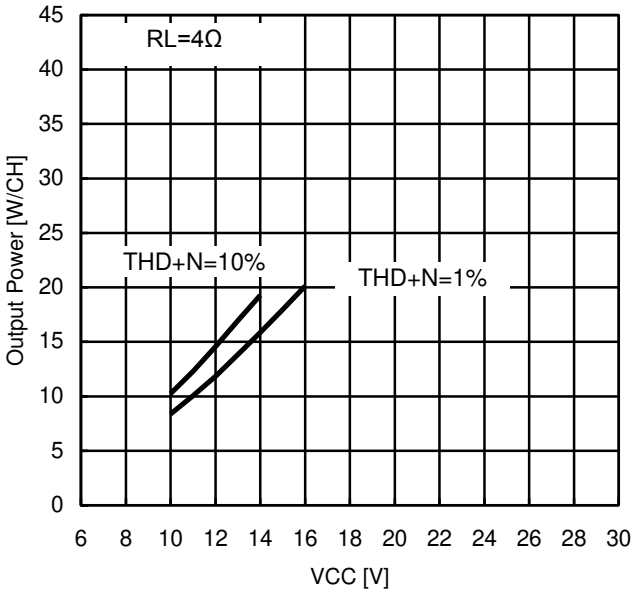


Figure 14.
Output Voltage – Power Voltage (R_L=4Ω)

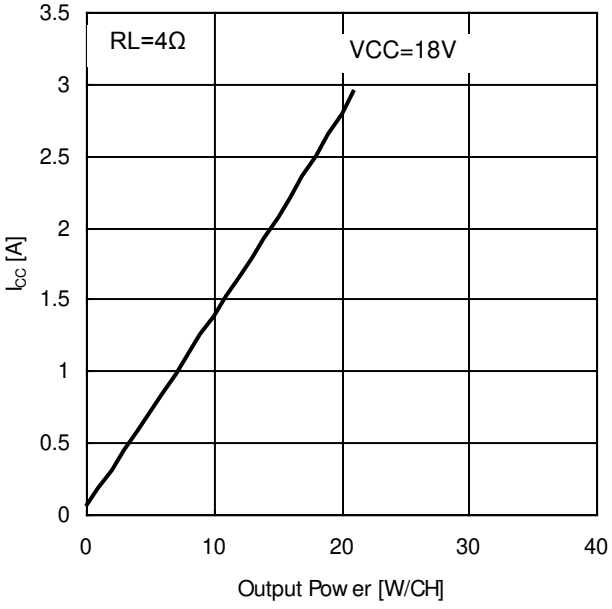


Figure 15.
Output power - Current consumption (R_L=4Ω)

※Dotted line means internal dissipation is over package power.

Typical Performance Curves

Speaker output(R_L=8Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

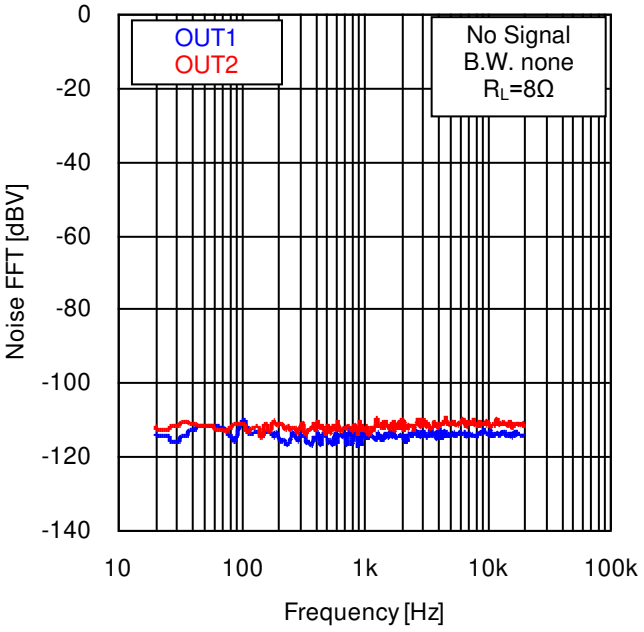


Figure 16.
FFT of output noise voltage

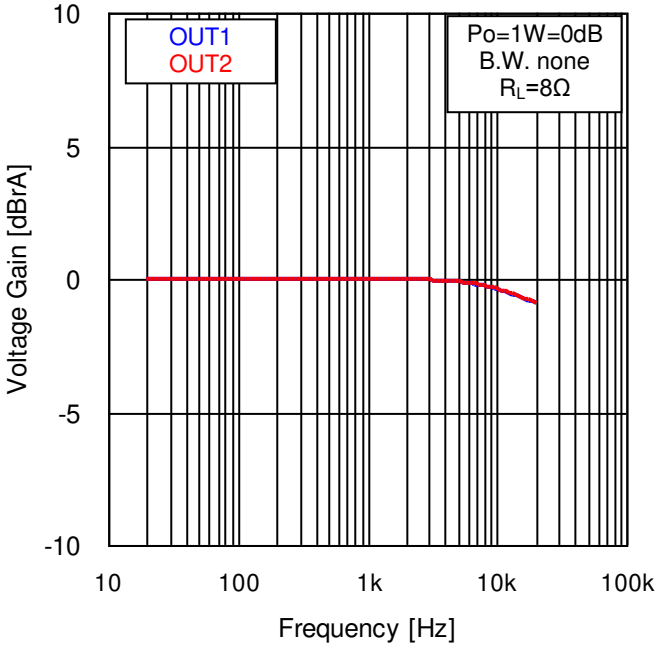


Figure 17.
Frequency – Output power

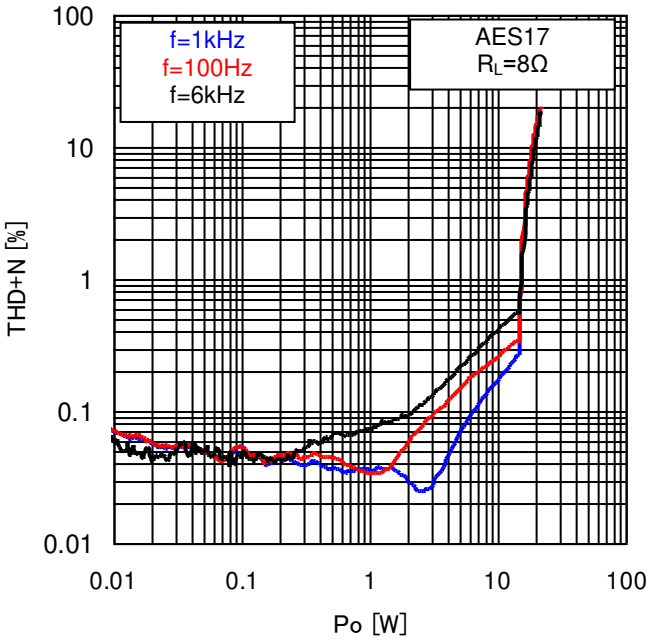


Figure 18.
Output Power - THD+N

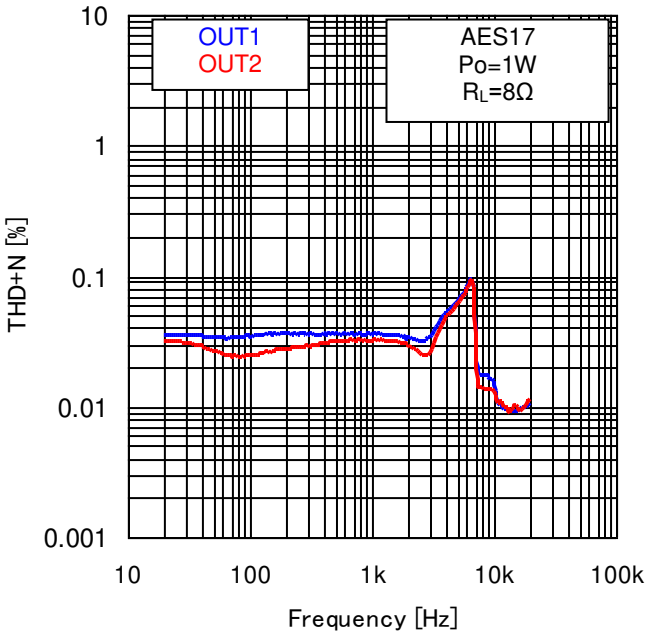


Figure 19.
Frequency - THD+N

Typical Performance Curves

Speaker output(R_L=8Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

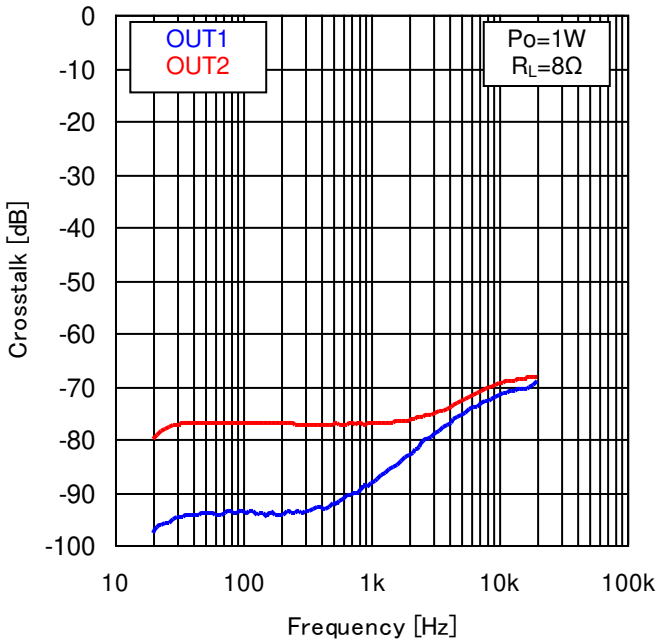


Figure 20.

Frequency - Crosstalk

Typical Performance Curves

Speaker output(R_L=6Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

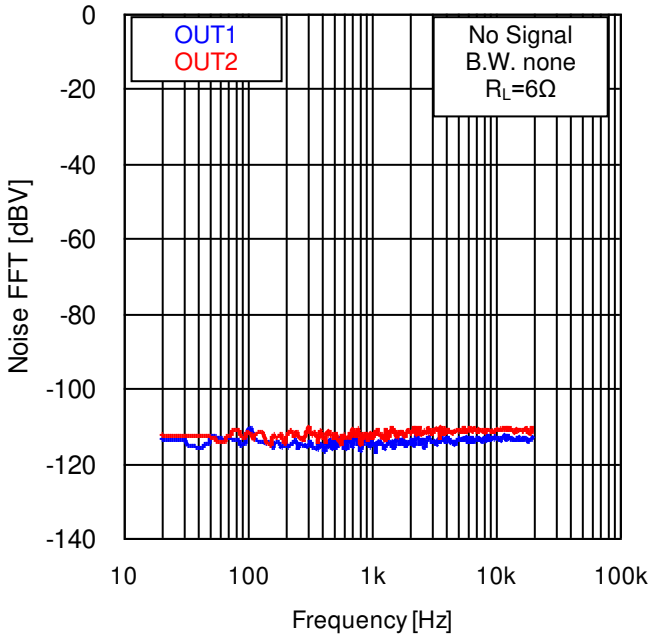


Figure 21.
FFT of output noise voltage

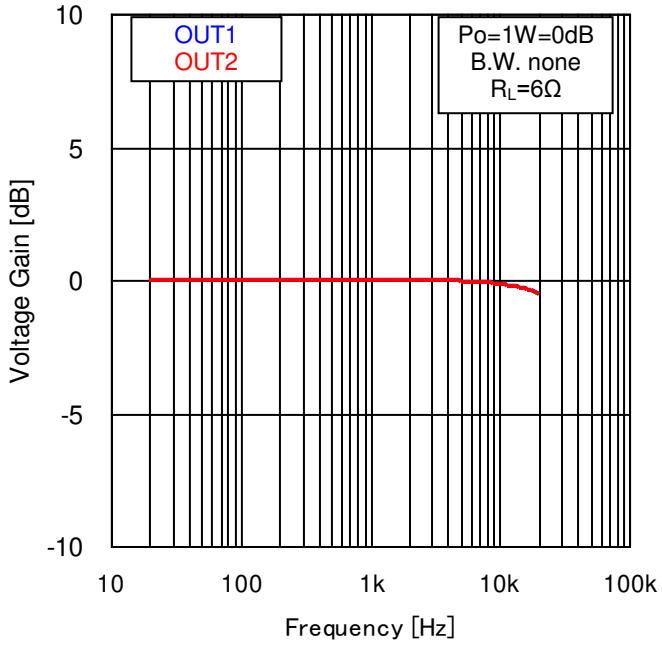


Figure 22.
Frequency – Output power

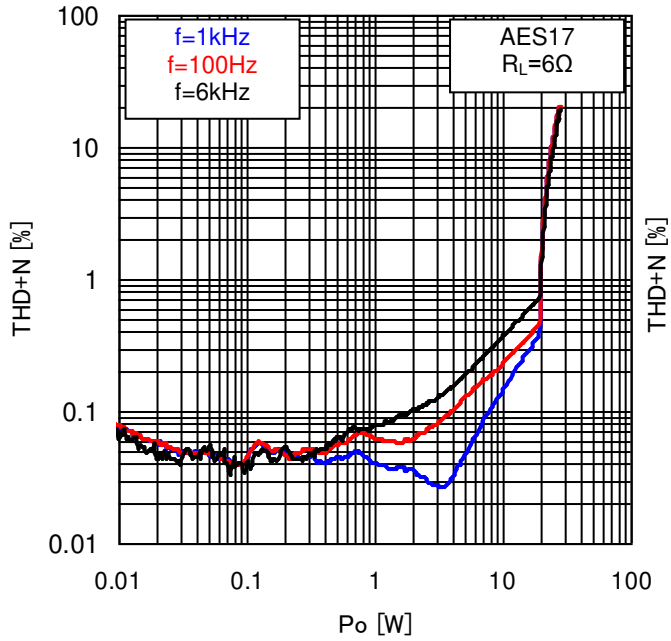


Figure 23.
Output Power - THD+N

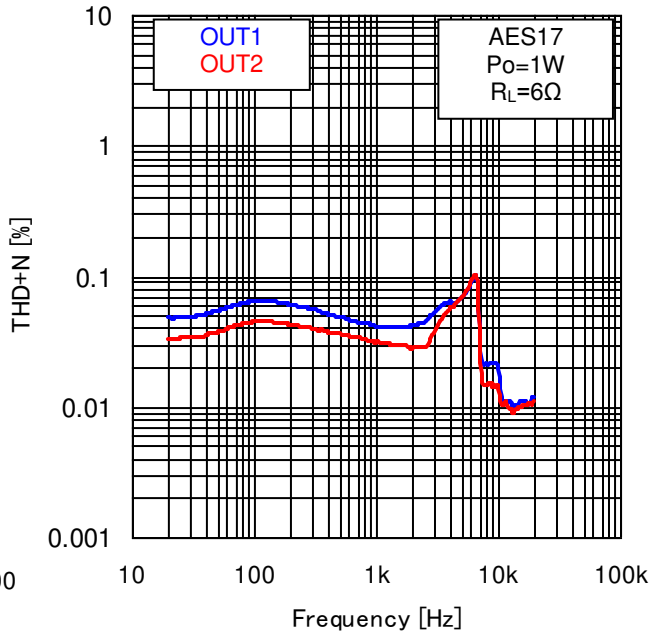


Figure 24.
Frequency - THD+N

Typical Performance Curves

Speaker output R_L=6Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

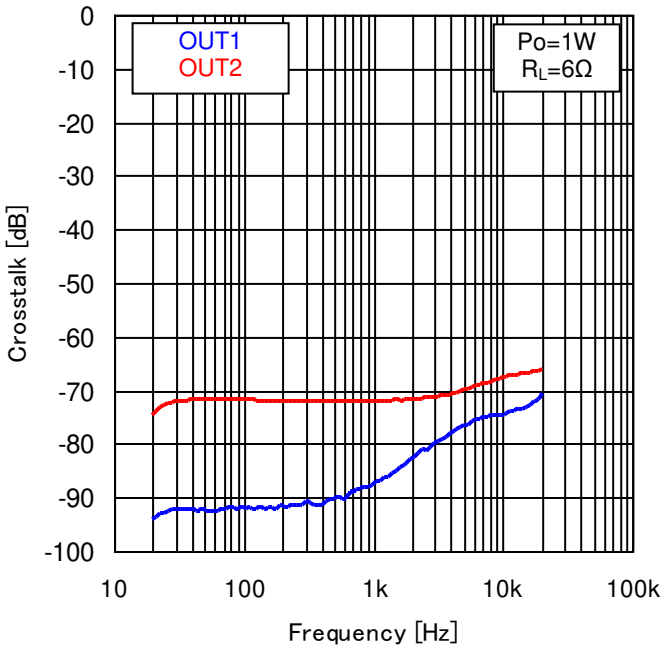


Figure 25.
Frequency - Crosstalk

Typical Performance Curves

Speaker output(R_L=4Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

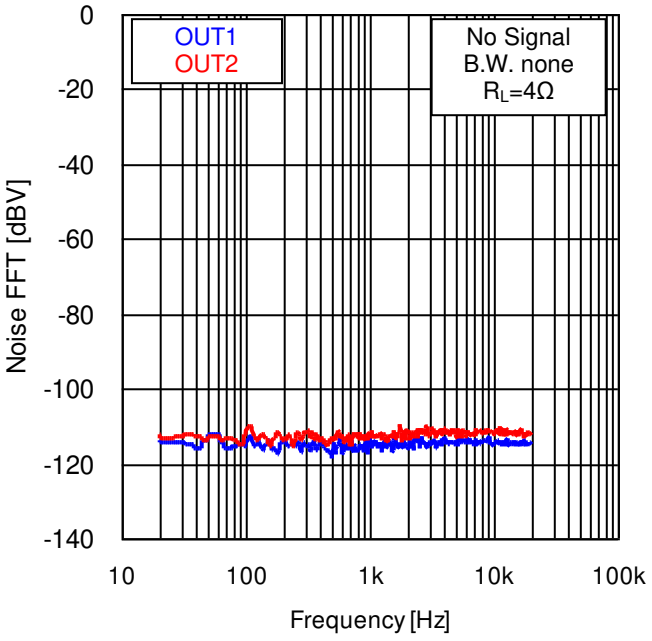


Figure 26.
FFT of output noise voltage

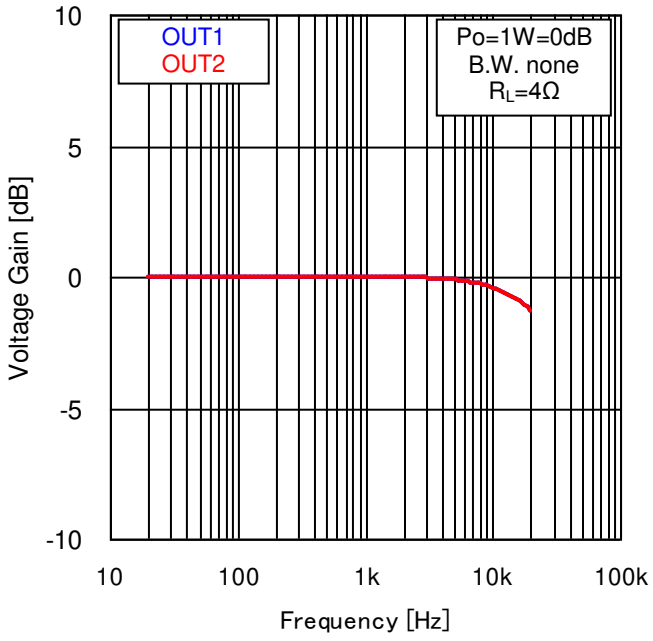


Figure 27.
Frequency – Output power

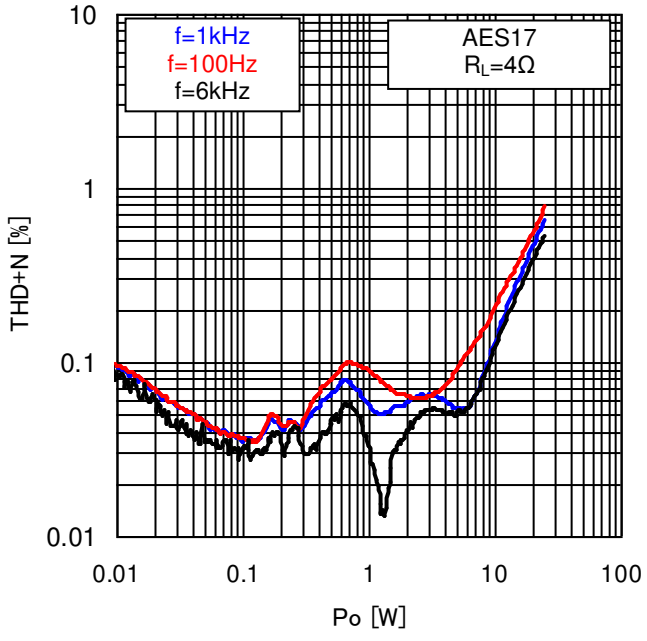


Figure 28.
Output Power - THD+N

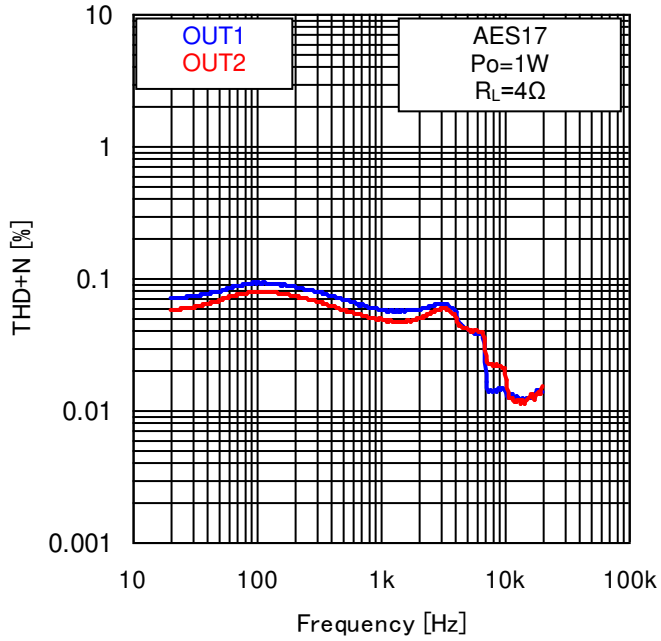


Figure 29.
Frequency - THD+N

Typical Performance Curves

Speaker output(R_L=4Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

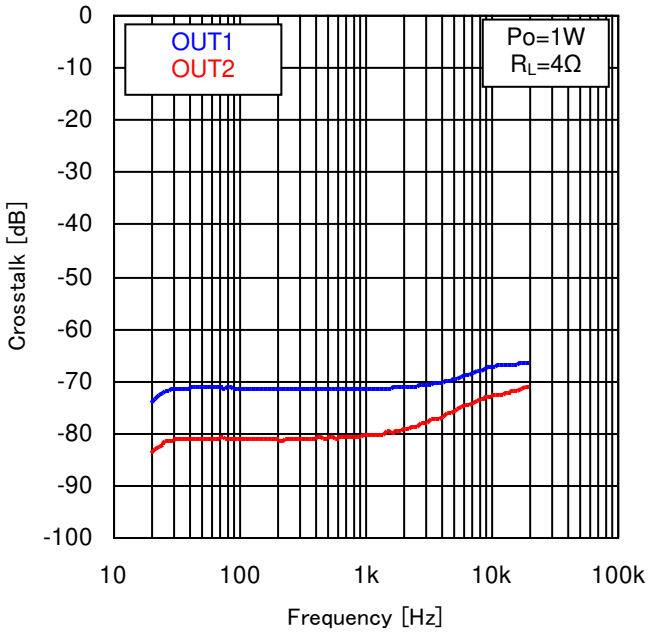


Figure 30.
Frequency - Crosstalk

Digital Block Functional Overview

No.	Function	Specification
1	Pre-Scaler	・Lch / Rch become same set point. ・+48dB to -79dB (0.5dB step),-∞dB
2	Channel Mixer	・Lch <= Mute, Lch(default), Rch, (L+R)/2, L-R ・Rch <= Mute, Lch, Rch(default), (L+R)/2, L-R ・Lch/Rch are independent phase reversal control available
3	12 Band BQ	・12 Band biquad type filter ・Only 5 coefficient is required.(b0,b1,b2,a1,a2) ・The Filter types which can be realized is Peaking/Low-shelf/High-shelf/Low-pass/High-pass/All-pass/Notch. ・Lch/Rch become same set point or independent set. There is soft transition function.
4	Fine Master Volume	・Lch / Rch become same set point or independent set. ・+24dB to -103dB (0.125dB step),-∞dB ・There is soft transition function
5	3 Band DRC	・Non clip output is achieved ・Available three band operation ・Threshold level : +12dB to -32dB (0.5dB step)
6	Post-Scaler	・Lch / Rch become same set point ・+48dB to -79dB (0.5dB step),-∞dB
7	Fine Post-Scaler	・Lch / Rch become independent set point ・+0.7dB to -0.8dB (0.1dB step)
8	DC Cut HPF	・Fc : 1Hz
9	Clipper	・Lch / Rch become same set point ・Clip level : +3dB to -22.5dB (-0.1dB step)

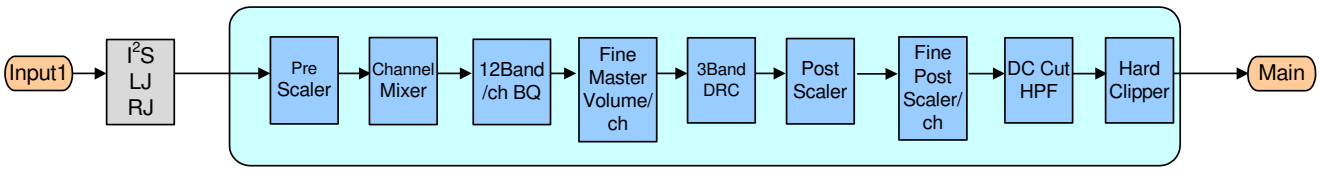


Figure 31. DSP Block diagram

RSTX pin, MUTEX pin function

RSTX (29pin)	MUTEX (30pin)	DSP block condition	Speaker output condition
Low	Low	Reset ON	HiZ_low (Low consumption)
High	Low	Normal operation (Mute ON)	HiZ_low(Note 4) (Mute ON)
High	High	Normal operation (Mute OFF)	Normal operation (Mute OFF)
Low	High	Don't use.	

(Note 1) RSTX is set to low, internal registers are initialized.
(Note 2) VCCP1, VCCP2< 2.5V, IC latched by protection circuit and ERROR terminal condition are initialized.
(Note 3) If DVDD is under 3V, RSTX is set to low once for 10ms(min), and set high again. Then DSP is needed to set parameter again.
(Note 4) Speaker output becomes HiZ-low after elapse of PWM stop time after setting MUTEX low. Please refer to PWM sampling frequency.

PWM sampling frequency

PWM sampling frequency of Speaker output and Soft-mute transition time depends on sampling frequency (fs) of the digital sound input. These transition times are changed by sending select address 0x15[1:0].

Sampling frequency (fs)	PWM frequency	0x15[1:0] value	Soft mute transition time		PWM stop time
			Mute ON	Mute OFF	
48kHz	384kHz	0x0	10.7ms	10.7ms	86ms
		0x1	21.4ms	10.7ms	106ms
		0x2	42.7ms	10.7ms	125ms
		0x3	85.4ms	10.7ms	162ms
44.1kHz	352.8kHz	0x0	11.7ms	11.7ms	93ms
		0x1	23.3ms	11.7ms	113ms
		0x2	46.5ms	11.7ms	135ms
		0x3	92.9ms	11.7ms	177ms
32 kHz	256kHz	0x0	16.1ms	16.1ms	116ms
		0x1	32.1ms	16.1ms	148ms
		0x2	64.1ms	16.1ms	178ms
		0x3	128.1ms	16.1ms	241ms

Wait time(Twait) rules from releasing RSTX to releasing MUTEX.

When the time from releasing RSTX to releasing MUTEX prescribes **Twait**, please secure **Twait** by all means more than 450ms.

2 wire Bus control signal specification

1) Electrical characteristics and Timing of Bus line and I/O stage

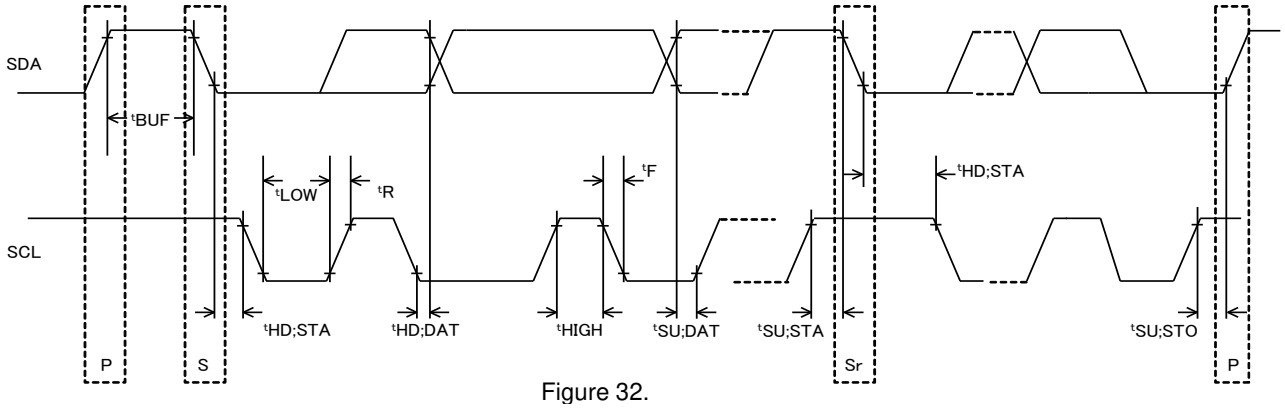


Figure 32.

SDA and SCL bus line characteristics(Unless otherwise specified Ta=25℃, VDD=3.3V)

	Parameter	Symbol	High speed mode		Unit
			Min.	Max.	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between「Stop」condition and「Start」condition	tBUF	1.3	—	μs
3	Hold-time of (sending again)「Start」condition. After this period the first clock pulse is generated.	tHD;STA	0.6	—	μs
4	SCL clock's LOW state Hold-time	tLOW	1.3	—	μs
5	SCL clock's HIGH state Hold-time	tHIGH	0.6	—	μs
6	Set-up time of sending again「Start」condition	tSU;STA	0.6	—	μs
7	Data hold time	tHD;DAT	0 (Note 1)	—	μs
8	Data set-up time	tSU;DAT	250	—	ns
9	Rise-time of SDA and SCL signal	tR	20+0.1Cb	300	ns
10	Fall-time of SDA and SCL signal	tF	20+0.1Cb	300	ns
11	Set-up time of 「Stop」condition	tSU;STO	0.6	—	μs
12	Capacitive load of each bus line	Cb	—	400	pF

The above-mentioned numerical values are all the values corresponding to VIH min and the VIL max level.

(Note 1) To exceed an undefined area on the fall-edge of SCL (VIH min of the SCL signal), the transmitting set should internally offer the holding time of 300ns or more for the SDA signal.

(Note 2) SCL and SDA pin is not corresponding to threshold tolerance of 5V.
Please use it within 4.5V of the absolute maximum rating.

2)Command interface

2 wire Bus control is used for command interface. It not only writes but also it is possible to read it excluding a part of register. In addition to "Slave Address " , set and write 1 byte of "Select Address " to read out the data. 2 wire Bus Slave mode format is illustrated below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

Figure 33.

S : Start Condition

Slave Address : The data of eight bits in total is sent putting up bit of Read mode (high) or Write mode (low) after slave address (7bit) set with the terminal ADDR. (MSB first)

A : The acknowledge bit adds to data that the acknowledge is sent and received in each byte.
When data is correctly sent and received, "low" is sent and received.
There was no acknowledgement for "high".

Select Address : The select address in one byte is used.(MSB first)

Data : Data byte is sent and received data(MSB first)

P : Stop Condition

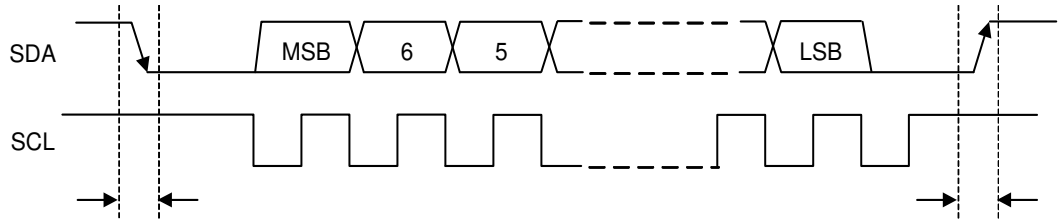


Figure 34.

3)Slave Address

・While ADDR pin is "low"

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	1/0

・While ADDR pin is "high"

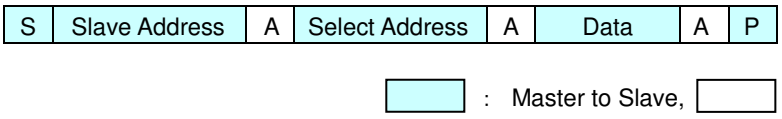
MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	1/0

Figure 35.

4) Writing of data

・Basic format



・Auto-increment format

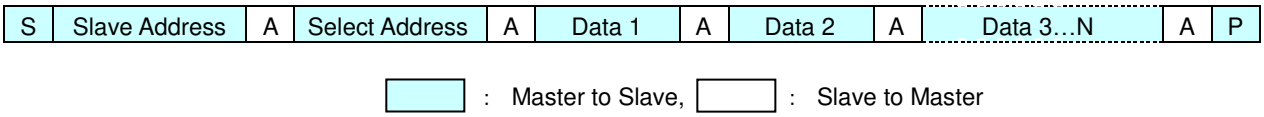


Figure 36.

5)Reading of data

First of all, the destination address (0x20 in the example) for reading is written in the register of the 0xD0 address at the time of reading. In the following stream, data is read after the slave address. Please do not return acknowledge when you end the reception.

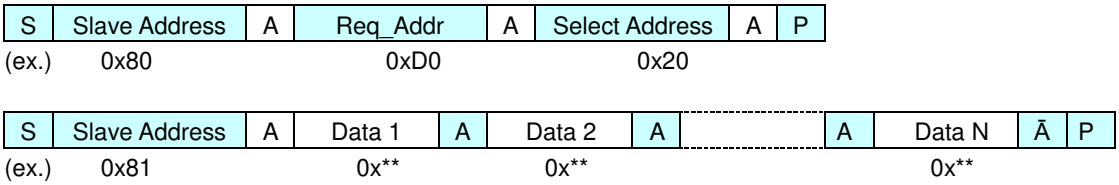


Figure 37.

Format of digital audio input

- LRCLK: It is L/R clock input signal.
  It corresponds to 32kHz/44.1kHz/48kHz and that is same as the sampling frequency (fs).
  This signal shows left or right of audio data.

- BCLK: It is Bit Clock input signal.
  It is used for the latch of data in rising edge. Frequency of BCLK is 64 times of sampling frequency (64fs) or 48 times (48fs) or 32 times (32fs). If BCLK frequency is 32fs, only 16 bit data width is available.

- SDATA: It is data input signal.
  It is amplitude data. The data length is different according to the resolution of the input digital data.
  Data width is selectable as 16 bit, 20 bit or 24 bit.

  The digital input has I2S, Left-justified and Right-justified formats.
  The figure below shows the timing chart of each transmission mode.

- SDATAO: Audio data after DSP processing.
  Data is audio data after DSP processing.
  This output is synchronous to LRCK and BCLK.
  Output supports only I2S format.

BCLK clock 64fs

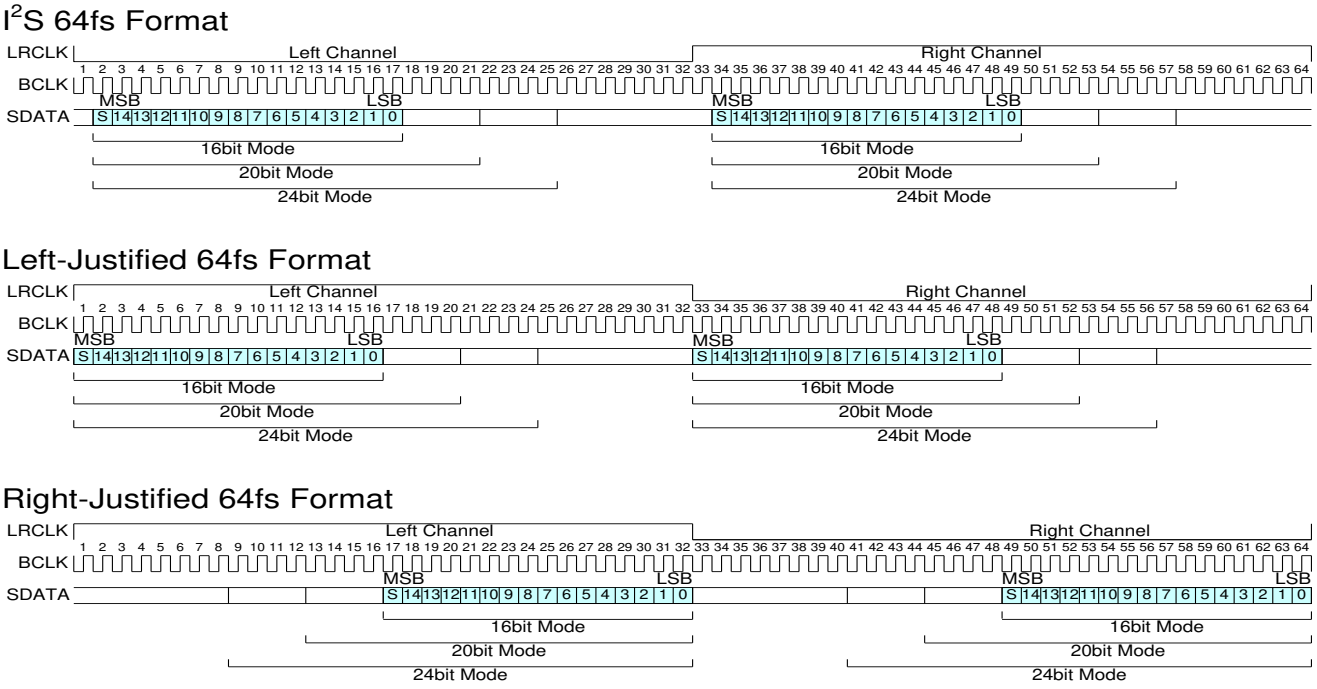
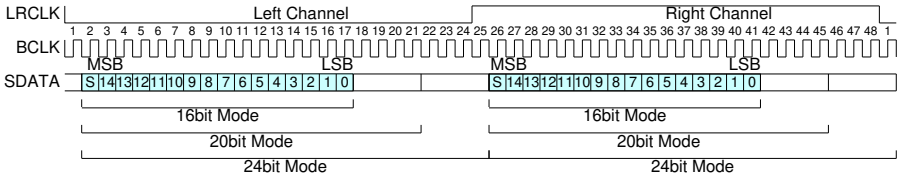


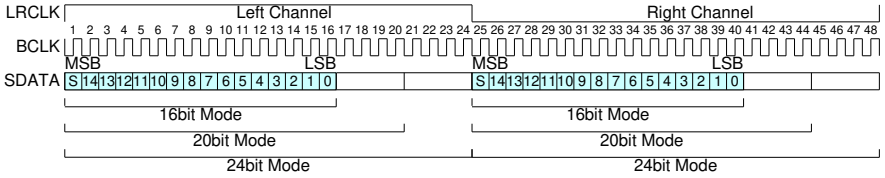
Figure 38.

BCLK clock 48fs

I²S 48fs Format



Left-Justified 48fs Format



Right-Justified 48fs Format

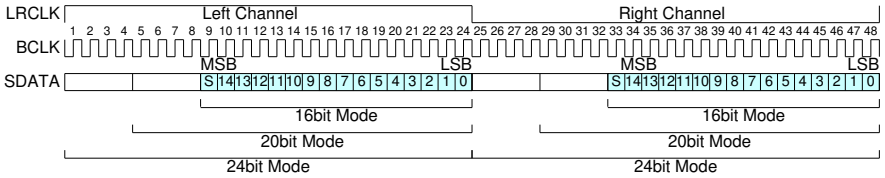
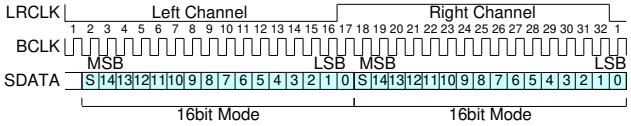


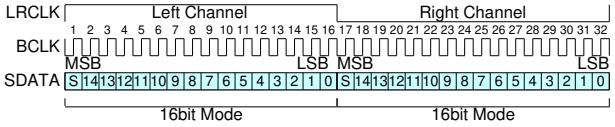
Figure 39.

BCLK clock 32fs

I²S 32fs Format



Left-Justified 32fs Format



Right-Justified 32fs Format

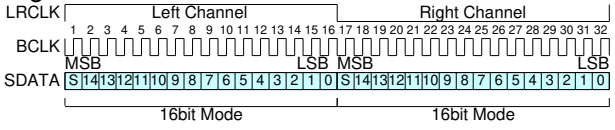


Figure 40.

Format setting for Digital Audio Interface

Please set BCLK clock fs, Data length and Format by transmitting command according to inputted Digital Serial Audio signal.

SDATAO output data bit width is able to be set independently.

Output supports only I^2S format.

BCLK clock

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x03[5:4]	0x0	64fs
	0x1	48fs
	0x2	32fs
	0x3	Don't use

Data format

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x03[3:2]	0x0	I^2S format
	0x1	Left-justified format
	0x2	Right-justified format
	0x3	Don't use

Data width

Default = 0x2 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x03[1:0]	0x0	16 bit
	0x1	20 bit
	0x2	24 bit
	0x3	Don't use

SDATAO output data width

Default = 0x2 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x78[1:0]	0x0	16 bit
	0x1	20 bit
	0x2	24 bit
	0x3	Don't use

Audio Interface format and timing

Recommended timing and operating conditions (BCLK, LRCLK, SDATA)

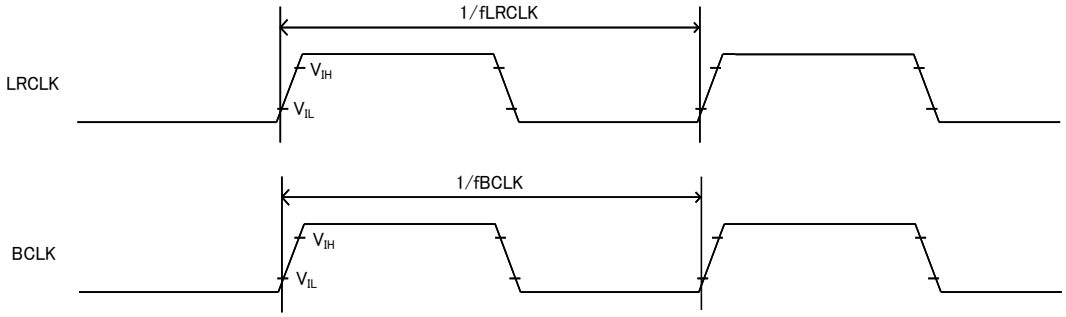


Figure 41. Clock timing

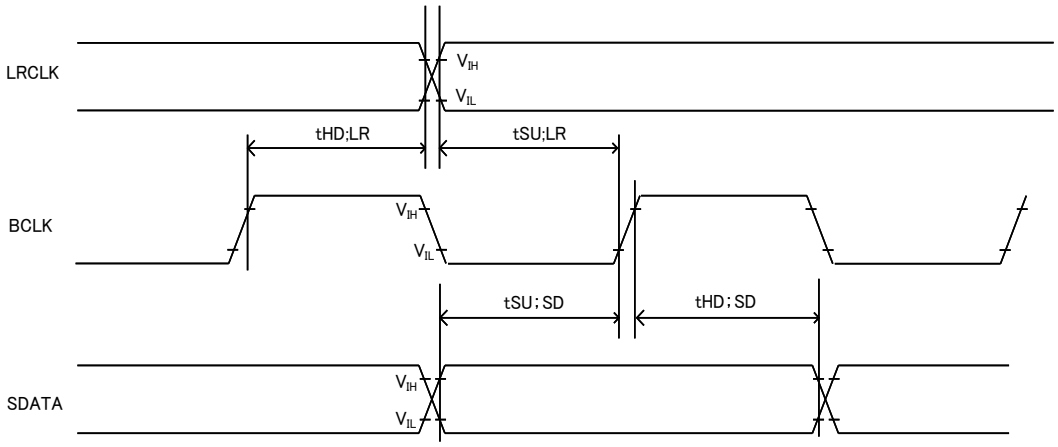
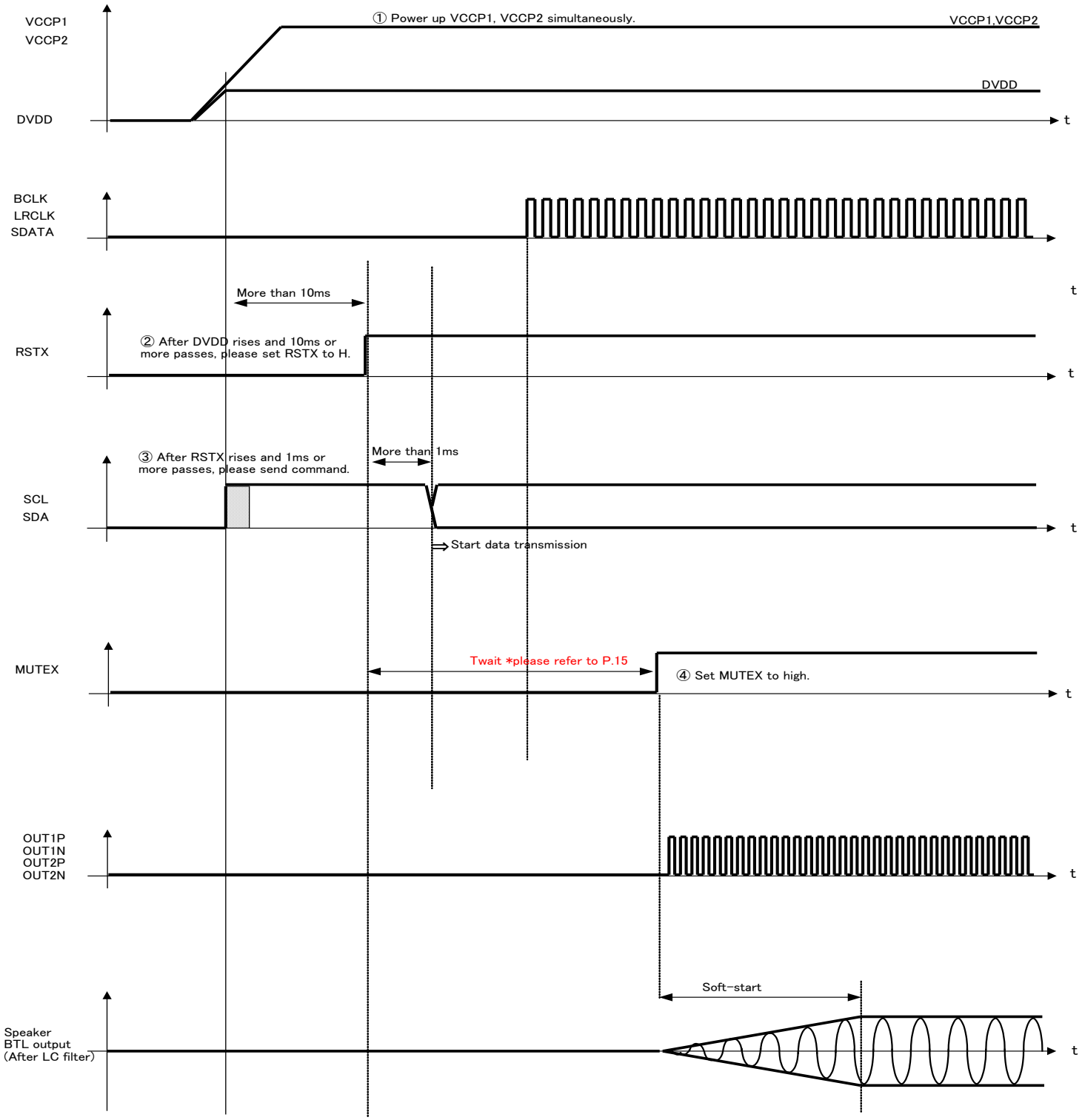


Figure 42. Audio Interface timing

No.	Parameter	Symbol	Limit		Unit
			Min.	Max.	
1	LRCLK frequency	fLRCLK	32	48	kHz
2	BCLK frequency	fBCLK	2.048	3.072	MHz
3	Setup time, LRCLK(Note 1)	tSU;LR	20	—	ns
4	Hold time, LRCLK(Note 1)	tHD;LR	20	—	ns
5	Setup time, SDATA	tSU;SD	20	—	ns
6	Hold time, SDATA	tHD;SD	20	—	ns
7	LRCLK, DUTY	dLRCLK	40	60	%
8	BCLK, DUTY	dBCLK	40	60	%

(Note 1) This regulation is to keep rising edge of LRCK and rising edge of BCLK from overlapping.

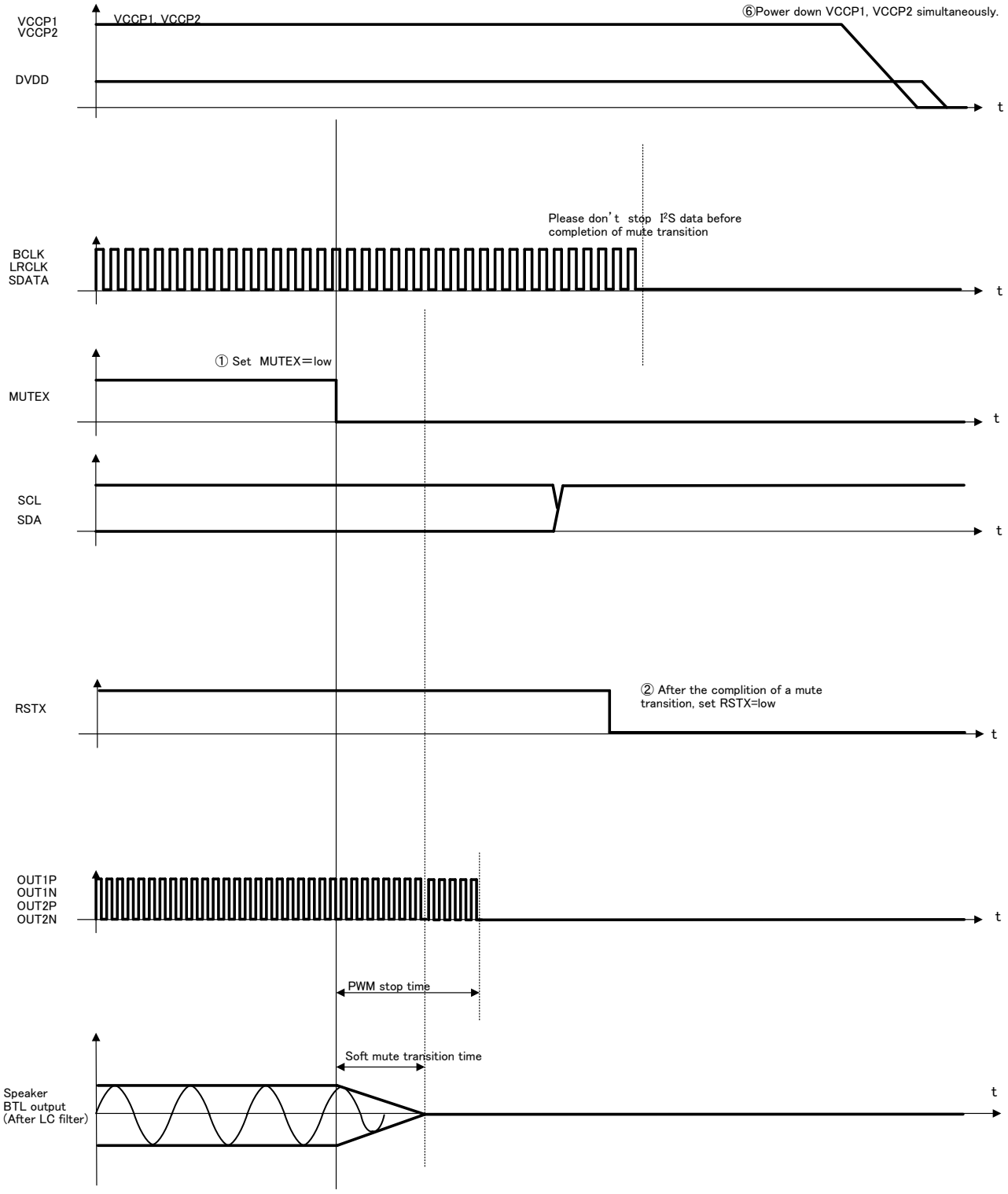
Power supply start-up sequence



*Please make sure to input low to RSTX terminal from external at the time power up DVDD.
*Please refer to [7. The wake-up Procedure of power-up].

Figure 43.

Power supply shut-down sequence



※Please make sure to input low to RSTX terminal when DVDD is powered down.

Figure 44.

About the protection function

Protection function	Detecting & Releasing condition		Speaker PWM output	ERROR(Note 1) output
Output short protection	Detecting condition	Detecting current = 7.2A (TYP.)	HiZ_low (latch) (Note 2)	Low (latch)
DC voltage protection	Detecting condition	PWM output Duty=0% or 100% for 12μs(TYP)and over	HiZ_low (latch) (Note 2)	Low (latch)
High temperature protection	Detecting condition	Chip temperature to be above 150℃ (TYP.)	HiZ_low	Low
	Releasing condition	Chip temperature to be below 120℃ (TYP.)	Normal operation	
Under voltage protection	Detecting condition	Power supply voltage to be below 7.0V (TYP.)	HiZ_low	High
	Releasing condition	Power supply voltage to be above 7.5V (TYP.)	Normal operation	
Clock stop protection	Detecting condition	BCLK signal have stopped among constant period. LRCLK signal have stopped among constant period. BCLK frequency is under constant value. BCLK frequency is over constant value. Please refer to P.55-58 about constant value.	HiZ_low	High
	Releasing condition	LRCLK signal haven't stopped among constant period and BCLK continues maximum 60ms or more of continuous appropriate frequency. Please refer to P.55-58 about constant value.	Normal operation	

(Note 1) The ERROR pin is Nch open-drain output.
(Note 2) Once an IC is latched, the circuit is not released automatically even after an abnormal status is removed.
The following procedures ① or ② is available for recovery.
①After MUTEX pin is made low once over PWM stop time, MUTEX pin is returned to high again.
②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

1) Output short protection (Short to the power supply)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTEX pin is set high and the current that flows in the PWM output pin becomes 7.2A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-low if detected, and IC does the latch.

Releasing method - ①After MUTEX pin is set low once over the PWM stop time(see page 15), MUTEX pin is returned to high again.

②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

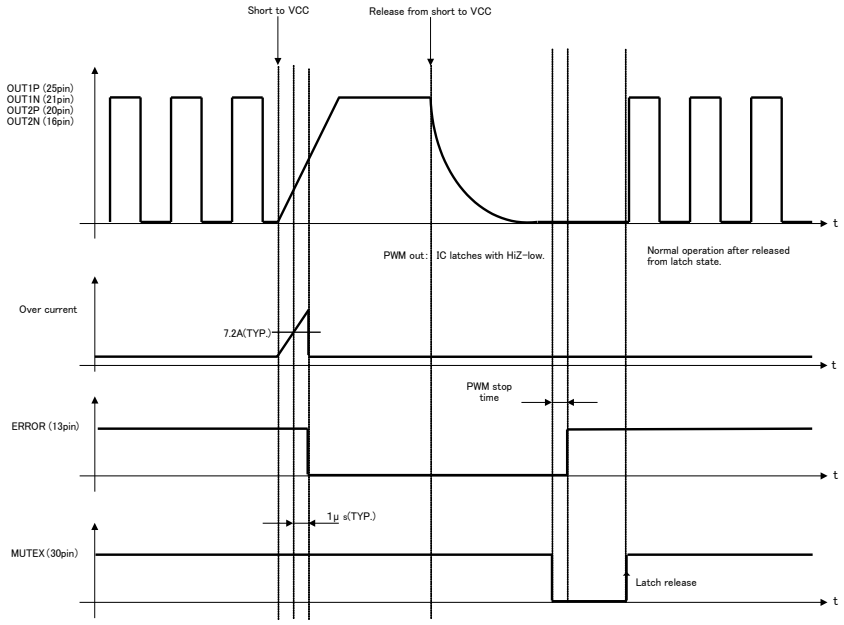


Figure 45.

2) Output short protection (Short to GND)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTEX pin is set high and the current that flows in the PWM output terminal becomes 7.2A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-low if detected, and IC does the latch.

Releasing method – ①After MUTEX pin is set low once over the PWM stop time(see page 15), MUTEX pin is returned to high again.

②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

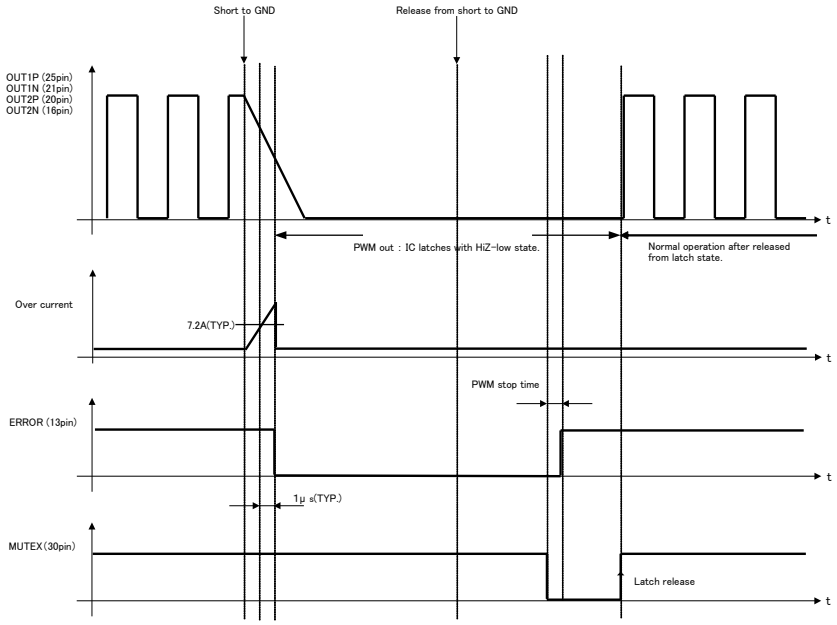


Figure 46.