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Middle Power Class-D Speaker Amplifier series

17W+17W Full Digital Speaker Amplifier with built-in DSP

BM28723MUV

General Description

BM28723MUV is a 17W+17W Class D stereo Speaker Amplifier with built-in DSP designed for TVs specifically for space-saving and low-power consumption.
BM28723MUV features BCD (Bipolar, CMOS, DMOS) process technology to achieve high efficiency. In addition, BM28723MUV is packaged in a compact back surface heatsink type power package to attain low power consumption, low heat generation without external heatsink. The package Max output power is only 17W+17W (When R_L=8Ω) as compared to 20W+20W (When R_L=8Ω) Max output power of package with external heat-sink.
The product satisfies all needs for drastic downsizing, low-profile structures and powerful high quality playback of sound systems.

Key Specifications

- Supply voltage range (V_{CCP1},V_{CCP2}): 10V to 24V
- Speaker output power (V_{CCP1},V_{CCP2}=18V, R_L=8Ω): 17W+17W (Typ)
- THD+N: 0.08 [%] (Typ)

Applications

- TVs (LCD, OLED)
- Home Audio
- Desktop PC
- Amusement equipment
- Electronic Music equipment, etc.

Typical Application Circuit

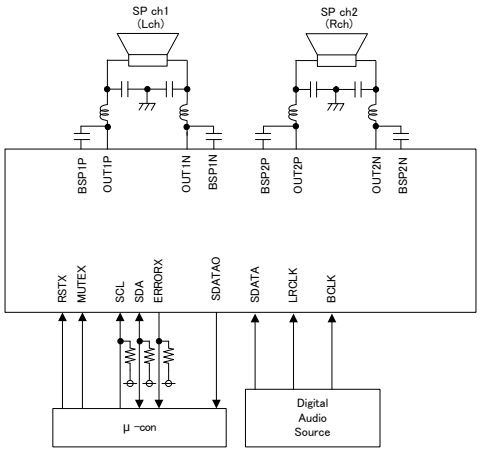

Figure 1. Typical application circuit

Features

- Built-in DSP (Digital Sound Processor) for Audio Signal Processing for TVs
  12-Band/ch BQ, 3-Band DRC, Pre-Scaler, Channel Mixer, Fine Master Volume, Hard Clipper, Level Meter, etc.
- Single Input System for Digital Audio Interface (No Master Clock Required)
  - I^2S / LJ / RJ Format
  - LRCLK: 32 / 44.1 / 48kHz
  - BCLK: 32 / 48 / 64f_S
  - SDATA: 16 / 20 / 24 bit
- Single Output System for Digital Audio Interface
  - I^2S Format
  - SDATA: 16 / 20 / 24 bit
- No Snubber Circuit Required (V_{CCP1},V_{CCP2}≤22V) because of Slew Rate Control
- Output Feedback Circuit which prevents decrease of sound quality caused by change of power supply voltage, achieves low noise and low distortion, So no large electrolytic-capacitors for Vcc bypass is required.
- Wide Range of Power Supply Input Voltage
- The monaural output reduces the number of external parts needed.
- High Efficiency and Low Heat Dissipation allowing Miniaturization, Slim Design, and also Power Saving of the System
- Eliminates pop-noise generated during the power supply ON/OFF. High quality muting performance is achieved using the soft-muting technology.
- Built-in with Various Protection Functions for Highly Reliability Design
  - High Temperature Protection
  - Under Voltage Protection
  - Output Short Protection
  - DC Voltage Protection for speaker
  - Clock Stop Protection
- Small Package, It reduces surface mount area

Package	W(Typ) x D(Typ) x H(Max)
VQFN032V5050	5.00mm x 5.00mm x 1.00mm

VQFN032V5050

○Product structure:Silicon monolithic integrated circuit ○This product has not designed protection against radioactive rays

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Pin configuration and Block diagram

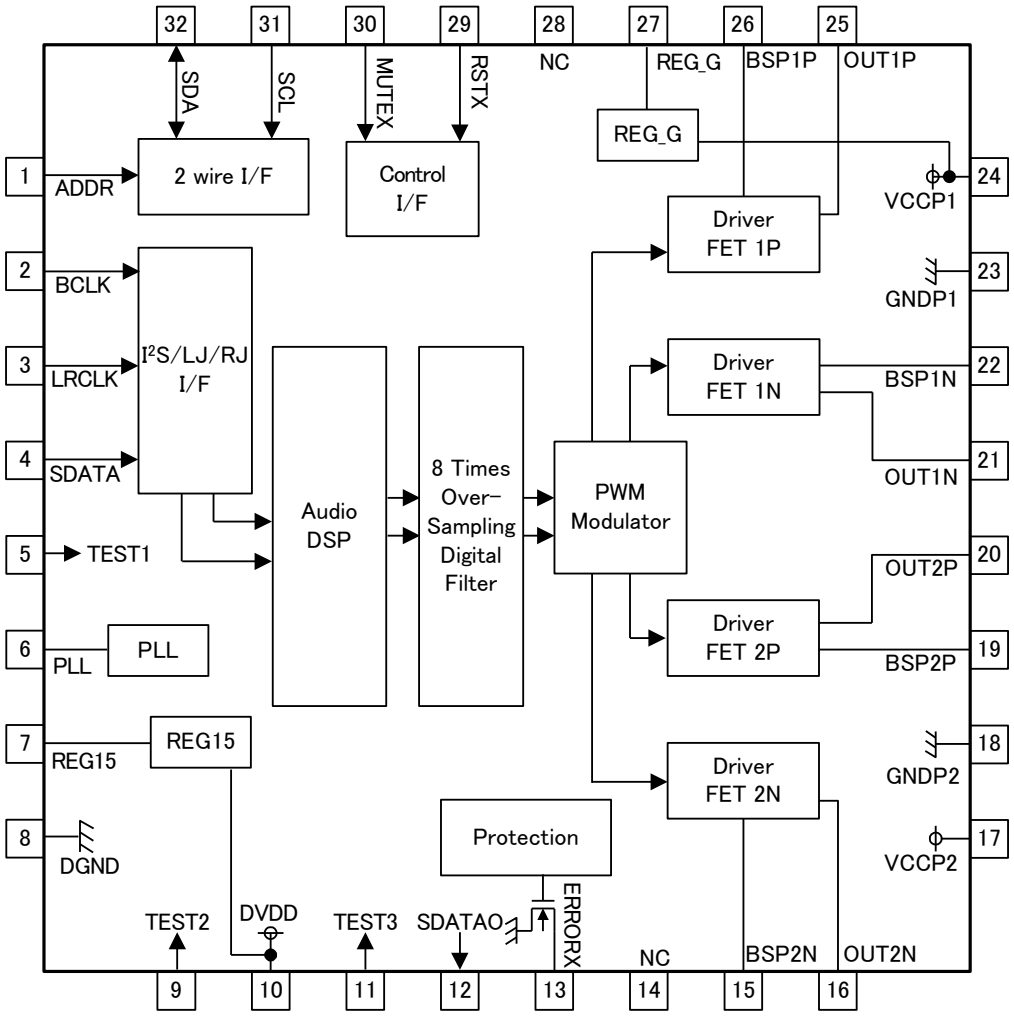

Figure 2. Pin configurations and Block diagram (Top View)

Pin Description

No.	Name	I/O	No.	Name	I/O	No.	Name	I/O	No.	Name	I/O
1	ADDR	I	9	TEST2	I	17	VCCP2	-	25	OUT1P	O
2	BCLK	I	10	DVDD	-	18	GNDP2	-	26	BSP1P	I
3	LRCLK	I	11	TEST3	I	19	BSP2P	I	27	REG_G	O
4	SDATA	I	12	SDATAO	O	20	OUT2P	O	28	NC	-
5	TEST1	I	13	ERRORX	O	21	OUT1N	O	29	RSTX	I
6	PLL	I/O	14	NC	-	22	BSP1N	I	30	MUTEX	I
7	REG15	O	15	BSP2N	I	23	GNDP1	-	31	SCL	I
8	DGND	-	16	OUT2N	O	24	VCCP1	-	32	SDA	I/O

I = input; O = output; - = others

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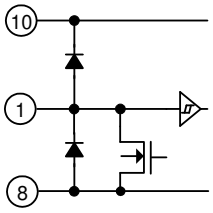
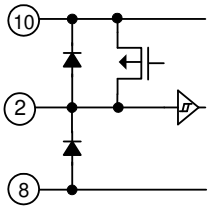
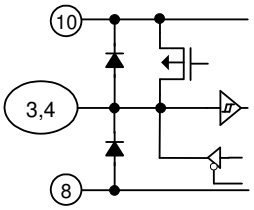
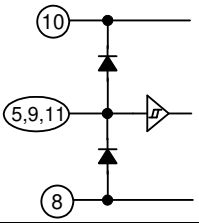
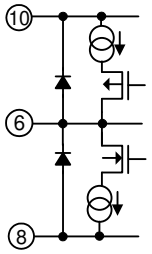
I/O equivalence circuits

Pin No.	Pin name	Pin voltage	Pin explanation	I/O equivalence circuit
1	ADDR	0V	2 wire Bus control Slave address select pin Select LSB data of slave address for 2 wire Bus control. Input High level to set LSB=1. Input Low level to set LSB=0. Select pull-down resistor after DVDD is applied.	
2	BCLK	3.3V	Digital audio signal input pin Input bit clock of digital audio signal. Select pull-up resistor after DVDD is applied.	
3 4	LRCLK SDATA	3.3V	Digital audio signal input pin Input LR clock of digital audio signal to LRCLK terminal. Input data of digital audio signal to SDATA terminal. Select pull-up resistor after DVDD is applied.	
5 9 11	TEST1 TEST2 TEST3	- - -	Test pin Connect to DGND.	
6	PLL	1V	PLL filter pin Connect filter circuit for PLL.	

The numerical value of I/O equivalence circuit is typical value, not guaranteed.

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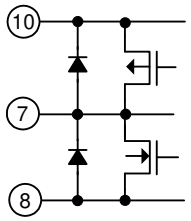
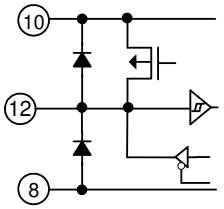
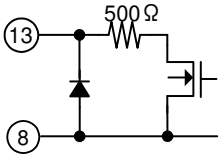
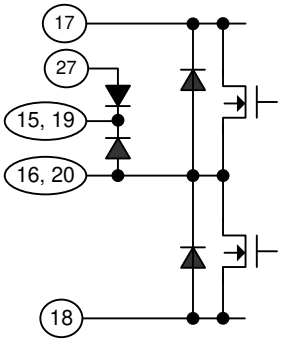
I/O equivalence circuit(s) - continued

Pin No.	Pin name	Pin voltage	Pin explanation	I/O equivalence circuit
7	REG15	1.5V	Internal power supply pin for digital circuit Connect capacitor. (Note) The REG15 terminal of BM28723MUV should not be used as an external supply and cannot support voltage load from external source. Therefore, do not connect anything except capacitor for stabilization.	
8	DGND	0V	GND pin for Digital I/O	-
10	DVDD	3.3V	Power supply pin for Digital I/O. Connect capacitor.	-
12	SDATAO	3.3V	Digital audio signal output pin Output data of digital audio signal. Select pull-up resistor after DVDD is applied.	
13	ERRORX	3.3V	Error flag pin Connect pull-up resistor. High: Normal operation Low: Error (Note) An error flag is indicated when Output Short Protection, DC Voltage Protection for speaker, and High Temperature Protection are activated. The flag shows the IC condition during operation. Don't use for the protection except this product.	
14 28	NC	-	No-Connection Pin Don't connect anything	-
15	BSP2N	-	Boot strap pin, CH2 negative Connect a capacitor from pin to OUT2N.	
16	OUT2N	V_{CCP2} to 0V	PWM output pin, CH2 negative Connect pin to output LPF. (Note) If this pin is shorted to GND, the IC may break. (Note) When Reset ON or Mute ON, all output transistors are OFF and output terminals are pulled down by 10kΩ (Typ).	
17	VCCP2	V_{CCP2}	Power supply pin for CH2	
18	GNDP2	0V	Power GND pin for CH2	
19	BSP2P	-	Boot strap pin, CH2 positive Connect a capacitor from pin to OUT2P.	
20	OUT2P	V_{CCP2} to 0V	PWM output pin, CH2 positive Connect pin to output LPF. (Note) If this pin is shorted to GND, the IC may break. (Note) When Reset ON or Mute ON, all output transistors are OFF and output terminals are pulled down by 10kΩ (Typ).	

The numerical value of I/O equivalence circuit is typical value, not guaranteed.

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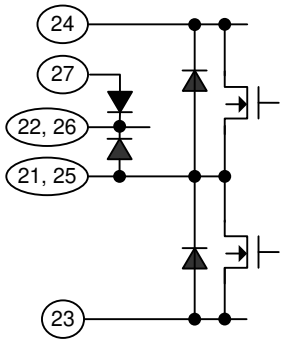
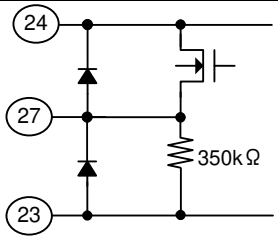
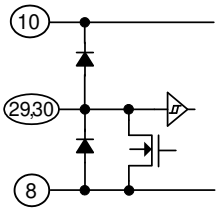
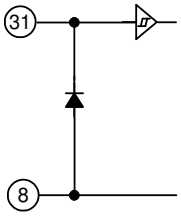
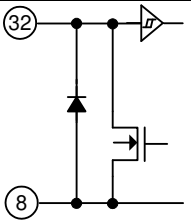
I/O equivalence circuit(s) - continued

Pin No.	Pin name	Pin voltage	Pin explanation	I/O equivalence circuit
21	OUT1N	V_{CCP1} to 0V	PWM output pin, CH1 negative Connect pin to output LPF. (Note) If this pin is shorted to GND, the IC may break. (Note) When Reset ON or Mute ON, all output transistors are OFF and output terminals are pulled down by 10kΩ (Typ).	
22	BSP1N	-	Boot strap pin, CH1 negative Connect a capacitor from pin to OUT1N.	
23	GNDP1	0V	Power GND pin for ch1	
24	VCCP1	V_{CCP1}	Power supply pin for ch1	
25	OUT1P	V_{CCP1} to 0V	PWM output pin, CH1 positive Connect to output LPF. (Note) If this pin is shorted to GND, the IC may break. (Note) When Reset ON or Mute ON, all output transistors are OFF and output terminals are pulled down by 10kΩ (Typ).	
26	BSP1P	-	Boot-strap pin of ch1 positive Connect a capacitor from pin to OUT1P.	
27	REG_G	5.7V	Internal power supply pin for gate driver Connect capacitor (Note) The REG_G terminal of BM28723MUV should not be used as an external supply and cannot support voltage load from external source. Therefore, do not connect anything except capacitor for stabilization.	
29	RSTX	0V	Reset pin for Digital circuit High: Reset OFF Low: Reset ON Select pull-down resistor after DVDD is applied.	
30	MUTEX	0V	Speaker output mute control pin High: Mute OFF Low: Mute ON Select pull-down resistor after DVDD is applied.	
31	SCL	-	2 wire Bus control transmit clock input pin Input the transmit clock to this pin for 2 wire Bus control. This pin is not corresponding to threshold tolerance of 5V. Refer to: Absolute Maximum Ratings, Input voltage 1	
32	SDA	-	2 wire Bus control data input/output pin Input the transmit data to this pin for 2 wire Bus control. This pin is not corresponding to threshold tolerance of 5V. Refer to: Absolute Maximum Ratings, Input voltage 1	

The numerical value of I/O equivalence circuit is typical value, not guaranteed.

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Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Limit	Unit	Conditions
Supply Voltage	V_{CCMAX}	30	V	Pin 17, 24 (Note 1) (Note 2)
	$V_{DVDDMAX}$	4.5	V	Pin 10 (Note 1)
Input Voltage 1	V_{IN1}	-0.3 to V_{DVDD}+0.3(Note 3)	V	Pin 1 - 5, 9, 11, 29 - 32 (Note 1)
Terminal Voltage 1	V_{PIN1}	-0.3 to +7.0	V	Pin 27 (Note 1)
Terminal Voltage 2	V_{PIN2}	-0.3 to +V_{CCMAX}	V	Pin 16, 20, 21, 25 (Note 1)(Note 4-1)
Terminal Voltage 3	V_{PIN3}	-0.3 to V_{OUT1P}+7	V	Pin 26 (Note 1)(Note 4-2)
		-0.3 to V_{OUT1N}+7		Pin 22 (Note 1)(Note 4-2)
		-0.3 to V_{OUT2P}+7		Pin 19 (Note 1)(Note 4-2)
		-0.3 to V_{OUT2N}+7		Pin 15 (Note 1)(Note 4-2)
Terminal Voltage 4	V_{PIN4}	-0.3 to +2.1	V	Pin 7 (Note 1)
Open-drain Terminal Voltage	V_{ERR}	-0.3 to +7.0	V	Pin13 (Note 1)
Operating Temperature Range	Topr	-25 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Junction Temperature Range	Tj	-40 to +150	°C	

(Note 1) The voltage that can be applied reference to GND (Pin 8, 18, 23).
(Note 2) Do not exceed Tj=150°C.
(Note 3) Refer to Recommended Operating Ratings for V_{DVDD}.
(Note 4-1) This IC should be used within AC peak limits at all conditions. Overshoot should be ≤30V with reference to GND.
Undershoot should be ≤10ns and ≤30V with reference to VCCP1 and VCCP2. (Refer to figure 3-1.)
(Note 4-2) This IC should be used in lower than this rating by all means.
Undershoot should be ≤10ns and ≤(V_{OUT1P} or V_{OUT1N} or V_{OUT2P} or V_{OUT2N})+7V. (Refer to figure 3-2.)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

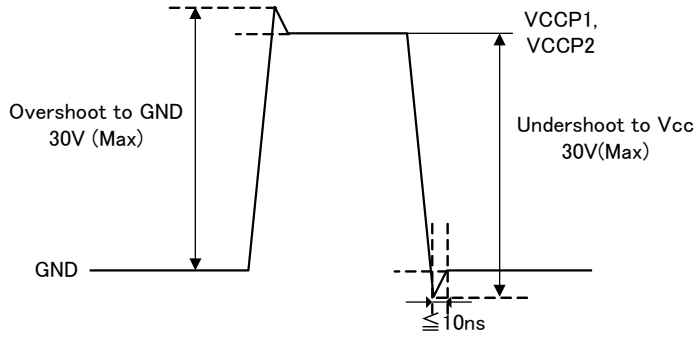

Figure 3-1

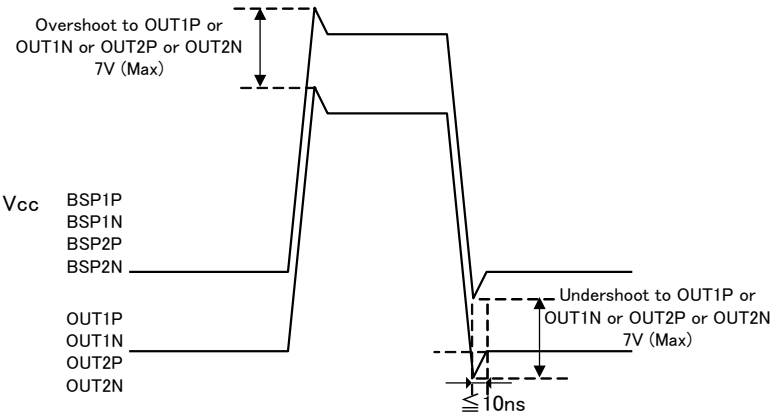

Figure 3-2

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Thermal Resistance(Note 5)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 7)	2s2p(Note 8)	
VQFN032V5050				
Junction to Ambient	θ_{JA}	138.9	39.1	°C/W
Junction to Top Characterization Parameter(Note 6)	Ψ_{JT}	11	5	°C/W

(Note 5)Based on JESD51-2A(Still-Air)
(Note 6) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 7)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 8)Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 9)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 9) This thermal via connects with the copper pattern of all layers..

Recommended Operating Ratings (Ta= -25°C to +85°C)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	V_{CCP1}	10 to 24	V	Pin 24 (Note 1) (Note 2)
	V_{CCP2}	10 to 24	V	Pin 17 (Note 1) (Note 2)
	V_{DVDD}	3.0 to 3.6	V	Pin 10 (Note 1)
Minimum load impedance	R_L	6.4	Ω	$21V<V_{CCP1},V_{CCP2}\leq 24V$ (Note 2)
		4.8	Ω	$14V<V_{CCP1},V_{CCP2}\leq 21V$ (Note 2)
		3.6	Ω	$V_{CCP1},V_{CCP2}\leq 14V$ (Note 2)

(Note 1) The voltage that can be applied reference to GND (Pin 8, 18, 23).
(Note 2) Do not exceed Tj=150°C.

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Electrical Characteristics

(Unless otherwise specified Ta=25°C, V_{CCP1},V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=8Ω, DSP: Through, Driver Gain(G_{DRV})=26dB, LC Filter: L=10μH, C_g=0.47μF, Without Snubber circuit)

Parameter	Symbol	Limit			Unit	Pin and Conditions
		Min	Typ	Max		
Total circuit						
Circuit current 1 (Normal mode)	I_{CC1}	-	45	90	mA	Pin 17, 24, -infinity dBFS input, No load
	I_{DD1}	-	9	19	mA	Pin 10, -infinity dBFS input, No load
Circuit current 2 (Reset mode)	I_{CC2}	-	110	400	μA	Pin 17, 24, -infinity dBFS input, No load, V_{RSTX}=0V, V_{MUTEX}=0V
	I_{DD2}	-	2.5	7.0	mA	Pin 10, -infinity dBFS input, No load V_{RSTX}=0V, V_{MUTEX}=0V
Open-drain terminal Low level voltage	V_{ERR}	-	-	0.8	V	Pin 13, I_{OUT}=0.5mA
High level input voltage	V_{IH}	2.5	-	3.3	V	Pin 1 - 5, 9, 11, 29 -32
Low level input voltage	V_{IL}	0	-	0.8	V	Pin 1 - 5, 9, 11, 29 -32
Input pull-up resistance	R_{UP}	22	33	-	kΩ	Pin 2 - 4, V_{IN} = 0V
Input pull-down resistance	R_{DN}	31	47	-	kΩ	Pin 1, 29, 30, V_{IN} = 3.3V
Input current (SCL, SDA terminal)	I_{IL}	-1	0	-	μA	Pin 31, 32, V_{IN} = 0V
Input current (SCL, SDA terminal)	I_{IH}	-	0	1	μA	Pin 31, 32, V_{IN} = 3.3V
Speaker amplifier output						
Maximum output power 1(Note 10)	P_{O1}	-	10	-	W	V_{CCP1},V_{CCP2}=13V,THD+N=10%
Maximum output power 2(Note 10)	P_{O2}	-	15	-	W	V_{CCP1},V_{CCP2}=16V,THD+N=10%
Total harmonic distortion(Note 10)	THD	-	0.08	-	%	V_{CCP1},V_{CCP2}=12V, P_O=1W, BW=AES17(20-22kHz) With snubber circuit
Crosstalk(Note 10)	CT	60	90	-	dB	P_O=1W, 1kHz BPF
PSRR(Note 10)	PSRR	-	60	-	dB	V_{ripple}=1V_{rms}, f=1kHz
Output noise voltage(Note 10)	V_{NO}	-	150	-	μVrms	-Infinity dBFS input, BW=A-Weight
PWM (Pulse Width Modulation) frequency	f_{PWM1}	-	256	-	kHz	f_S=32 kHz
	f_{PWM2}	-	352.8	-	kHz	f_S=44.1 kHz
	f_{PWM3}	-	384	-	kHz	f_S=48 kHz

(Note 10) These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

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Typical Performance Curves

Unless otherwise specified Ta=25°C, V_{CCP1},V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=8Ω, DSP: Through, Driver Gain(G_{DRV})=26dB
Measured by ROHM designed 4 layers board(Note 11)

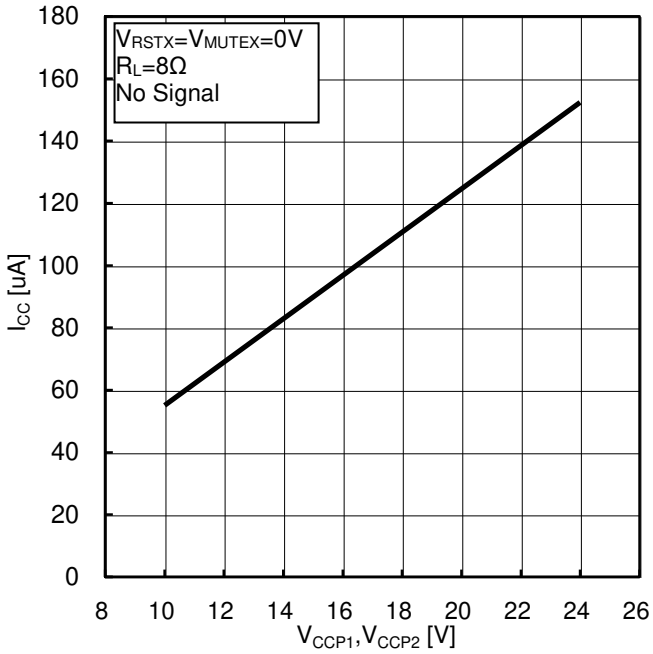

Figure 4.
Current consumption - Power supply voltage

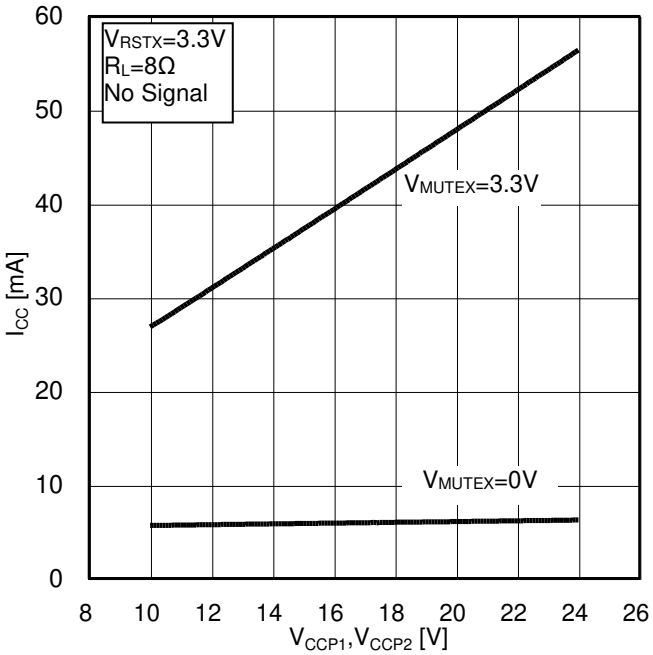

Figure 5.
Current consumption - Power supply voltage

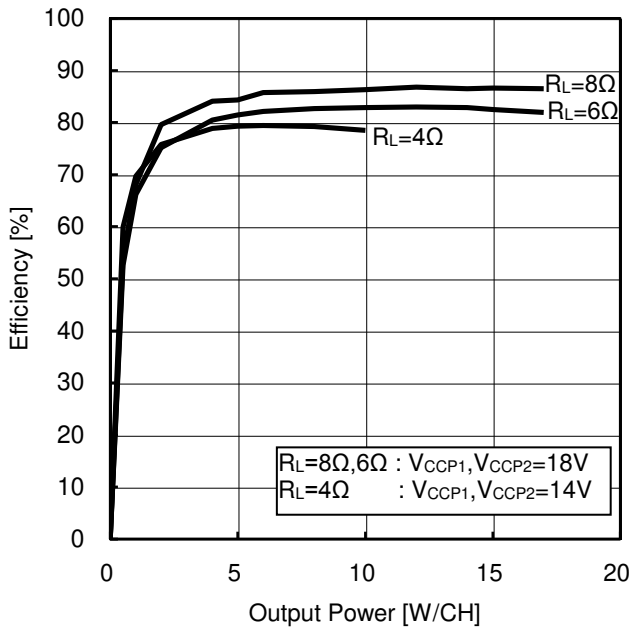

Figure 6.
Efficiency - Output Power

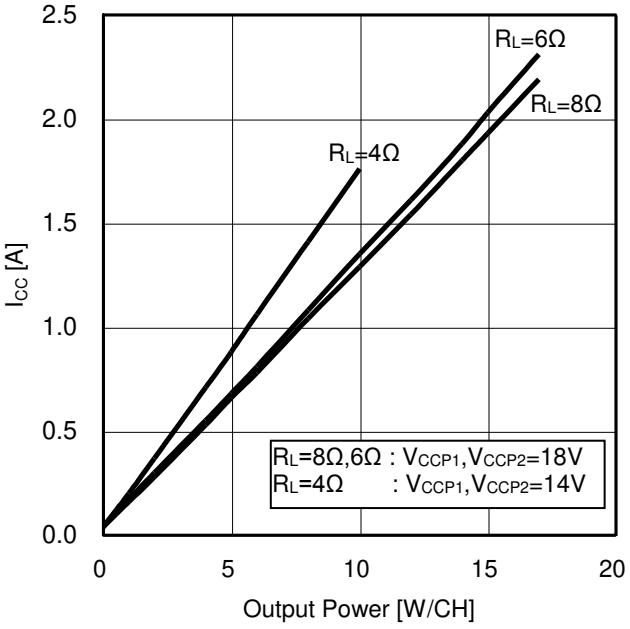

Figure 7.
Current consumption - Output power

(Note 11) 100mm×100mm×1.6mm FR4 4-layer glass epoxy board Cu Thickness 35μm/70μm/70μm/35μm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1},V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=8Ω, DSP: Through, Driver Gain(G_{DRV})=26dB
Measured by ROHM designed 4 layers board(Note 11)

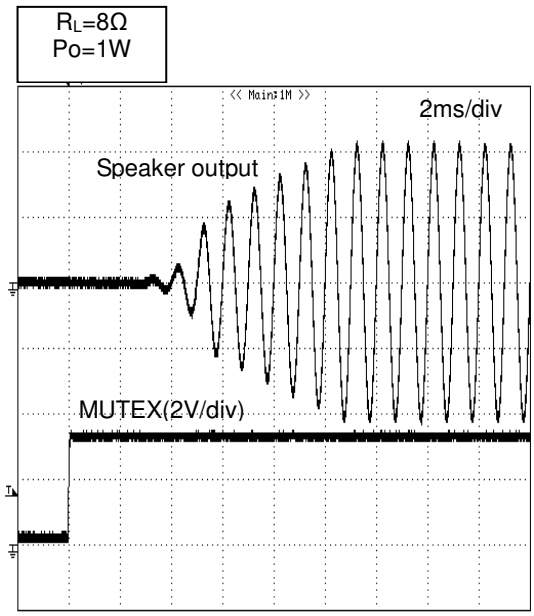

Figure 8.
Waveform at soft start

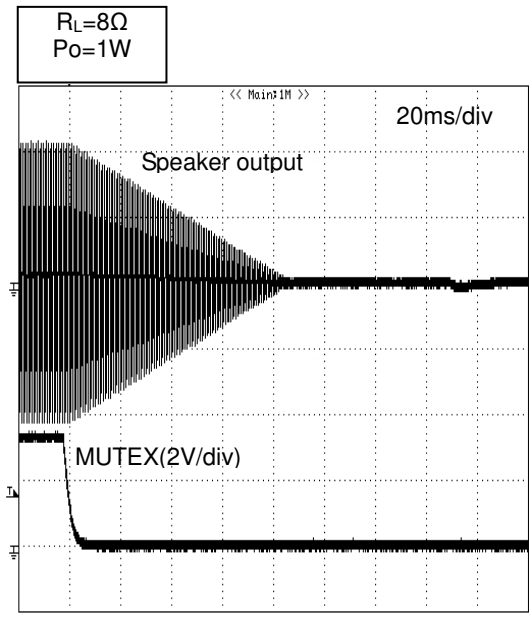

Figure 9.
Waveform at soft mute

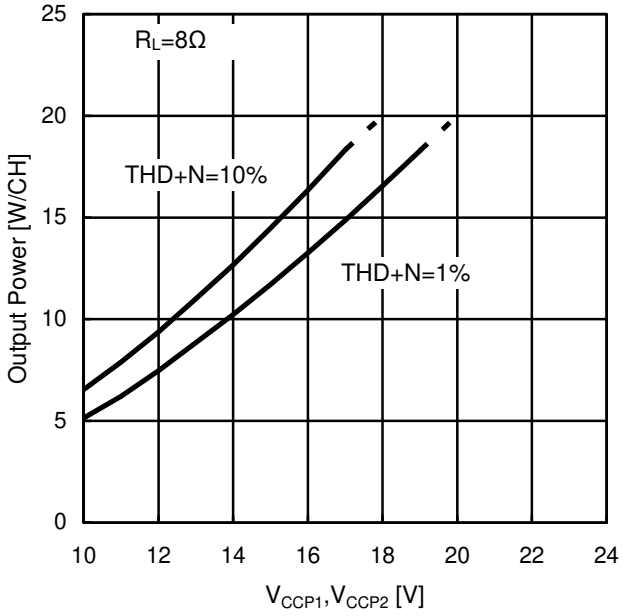

Figure 10.
Output Power - Power supply voltage (R_L=8Ω)

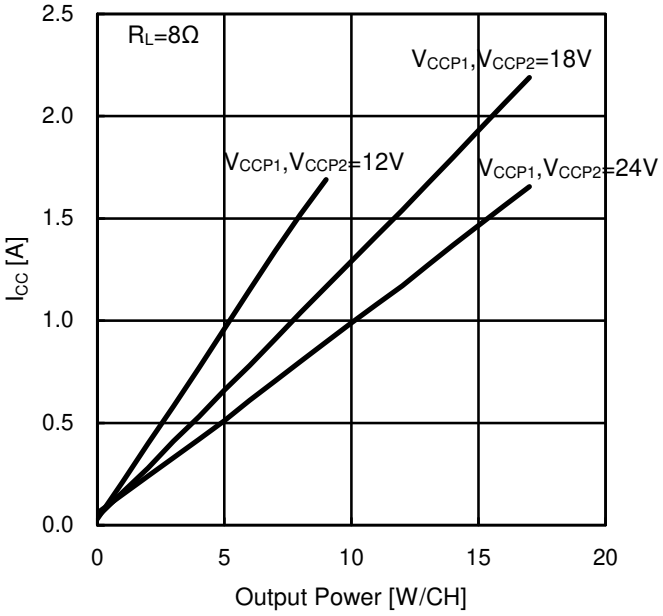

Figure 11.
Current consumption - Output Power (R_L=8Ω)

*Dotted line means exceeding maximum junction temperature.
In that case heat dissipation measures such as the heat sink are necessary separately.
* Use this IC in 20W or less output power even with heat dissipation measures.

(Note 11) 100mm×100mm×1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1},V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz,
DSP: Through, Driver Gain(G_{DRV})=26dB
Measured by ROHM designed 4 layers board(Note 11)

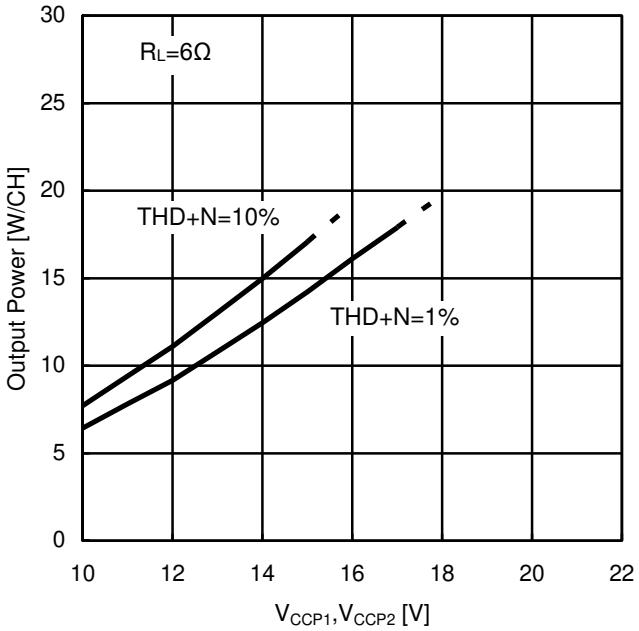

Figure 12.

Output Power - Power supply voltage (R_L=6Ω)

*Dotted line means exceeding maximum junction temperature.
In that case heat dissipation measures such as the heat sink are necessary separately.
* Use this IC in 20W or less output power even with heat dissipation measures.

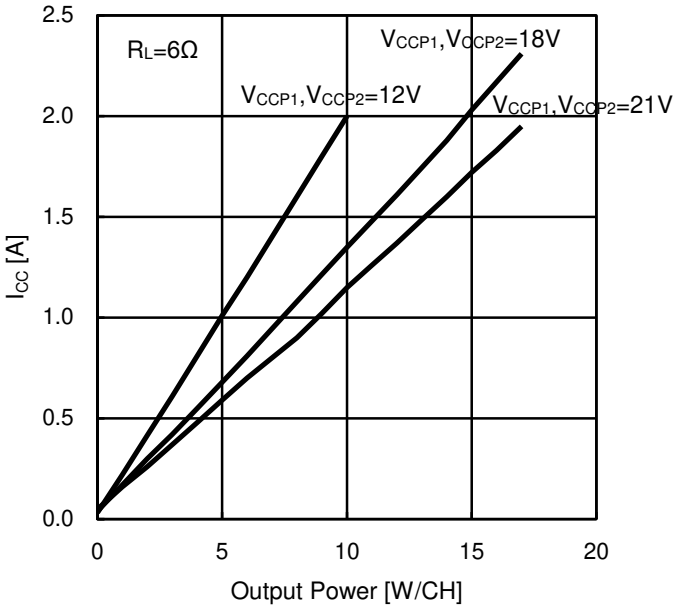

Figure 13.

Current consumption - Output Power (R_L=6Ω)

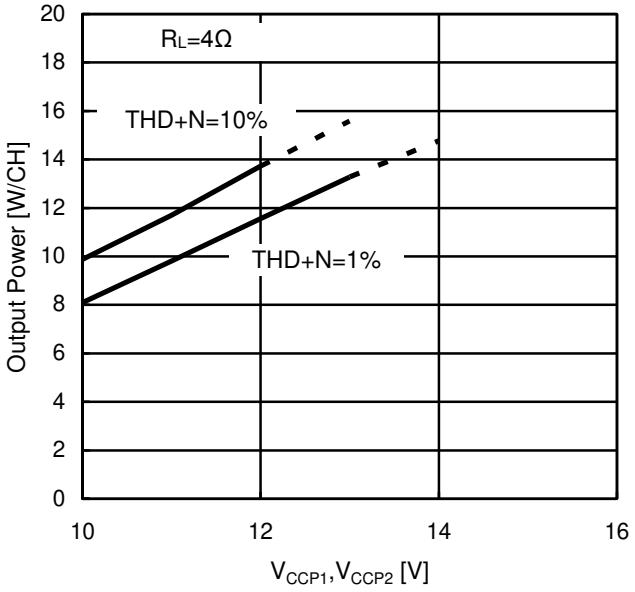

Figure 14.

Output Power - Power supply voltage (R_L=4Ω)

*Dotted line means exceeding maximum junction temperature.
In that case heat dissipation measures such as the heat sink are necessary separately.
* Use this IC in 15W or less output power even with heat dissipation measures.

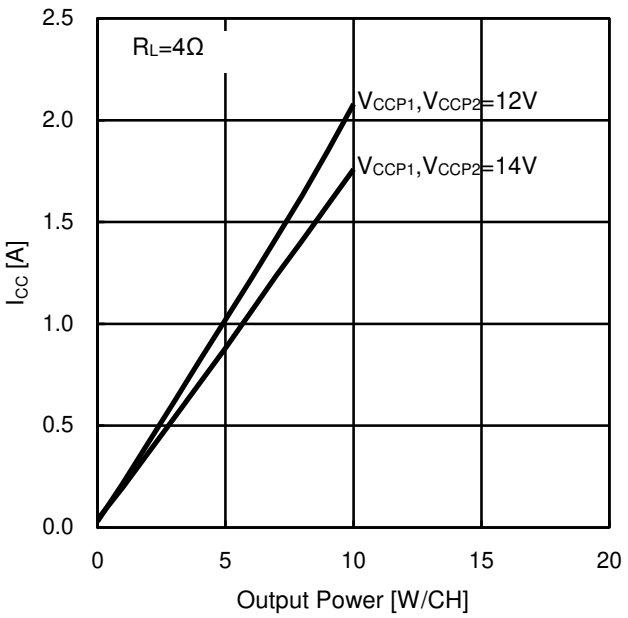

Figure 15.

Current consumption - Output Power (R_L=4Ω)

(Note 11) 100mm×100mm×1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1},V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=8Ω, DSP: Through, Driver Gain(G_{DRV})=26dB
Measured by ROHM designed 4 layers board(Note 11)

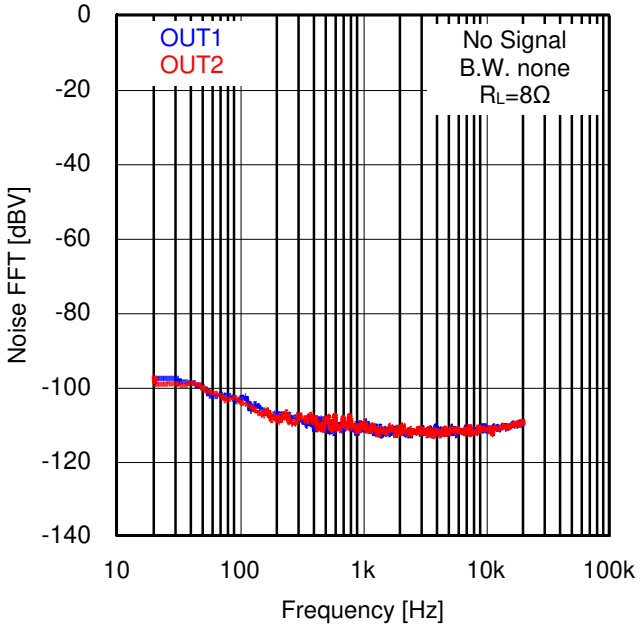

Figure 16.
FFT of output noise voltage

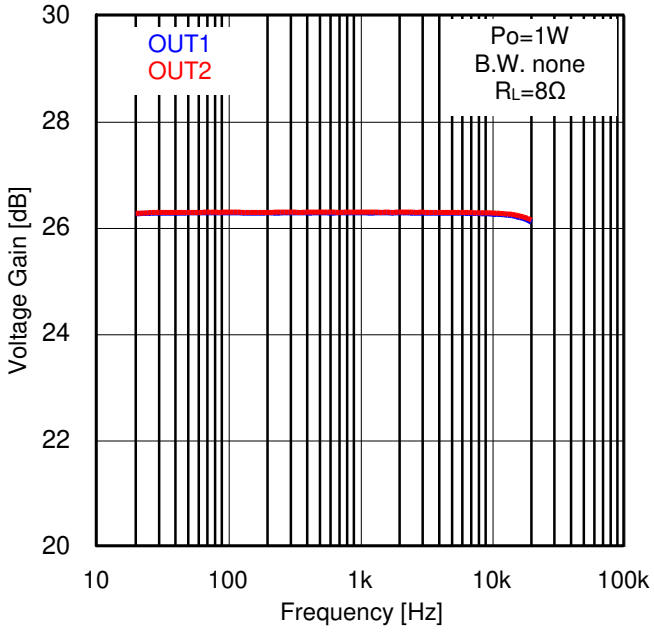

Figure 17.
Voltage Gain - Frequency

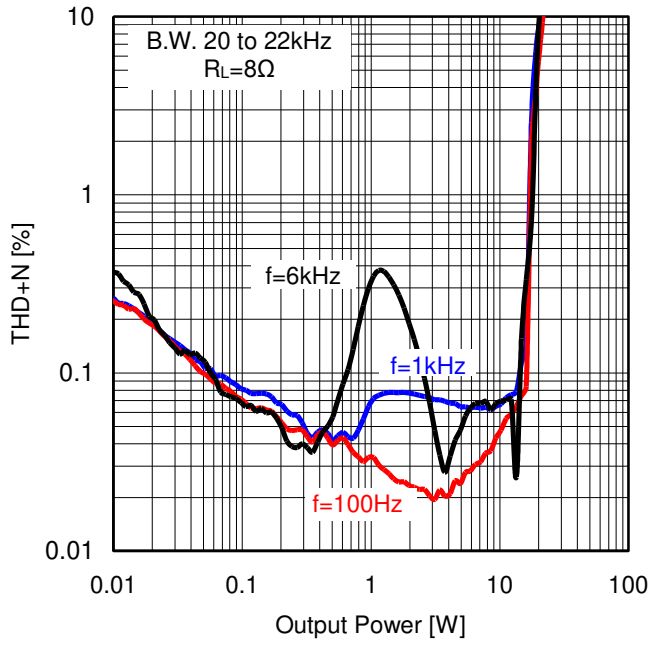

Figure 18.
THD+N - Output Power

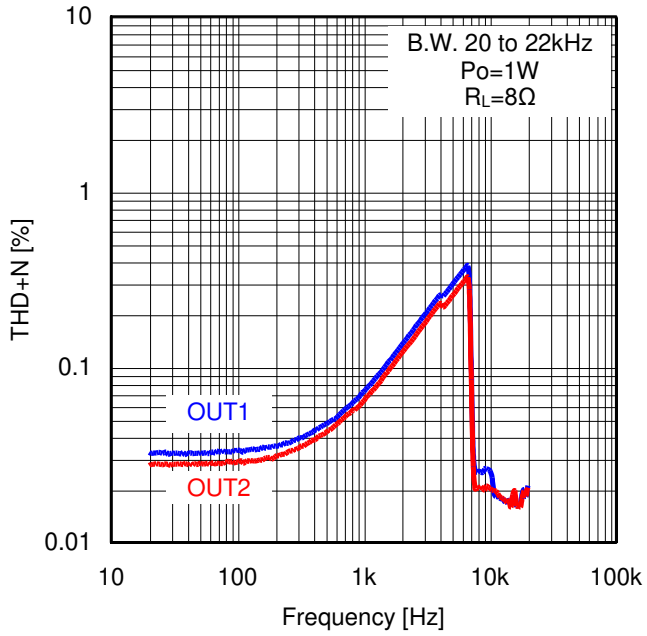

Figure 19.
THD+N - Frequency

(Note 11) 100mm×100mm×1.6mm FR4 4-layer glass epoxy board Cu Thickness 35μm/70μm/70μm/35μm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1},V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=8Ω, DSP: Through, Driver Gain(G_{DRV})=26dB
Measured by ROHM designed 4 layers board(Note 11)

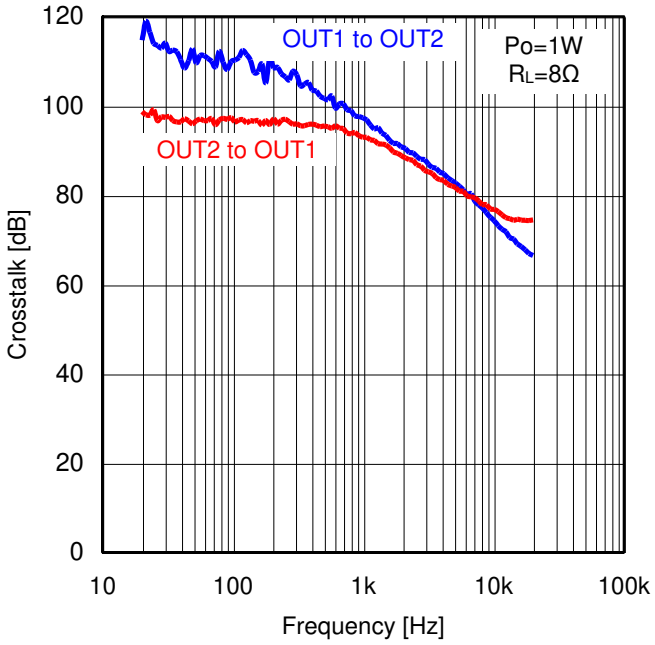

Figure 20.
Crosstalk - Frequency

(Note 11) 100mm×100mm×1.6mm FR4 4-layer glass epoxy board Cu Thickness 35μm/70μm/70μm/35μm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1},V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=6Ω, DSP: Through, Driver Gain(G_{DRV})=26dB
Measured by ROHM designed 4 layers board(Note 11)

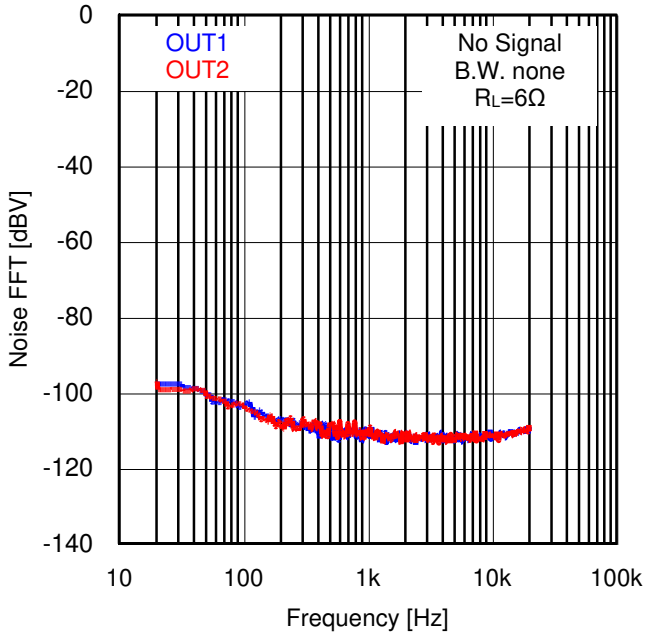

Figure 21.
FFT of output noise voltage

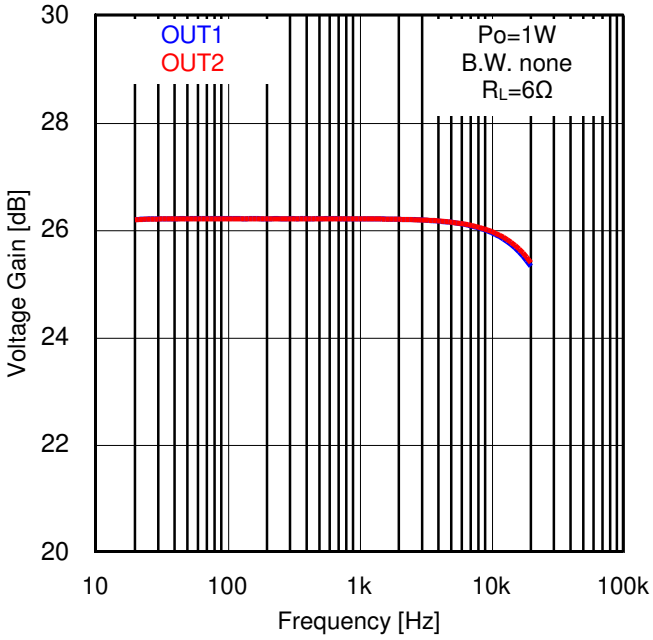

Figure 22.
Voltage Gain - Frequency

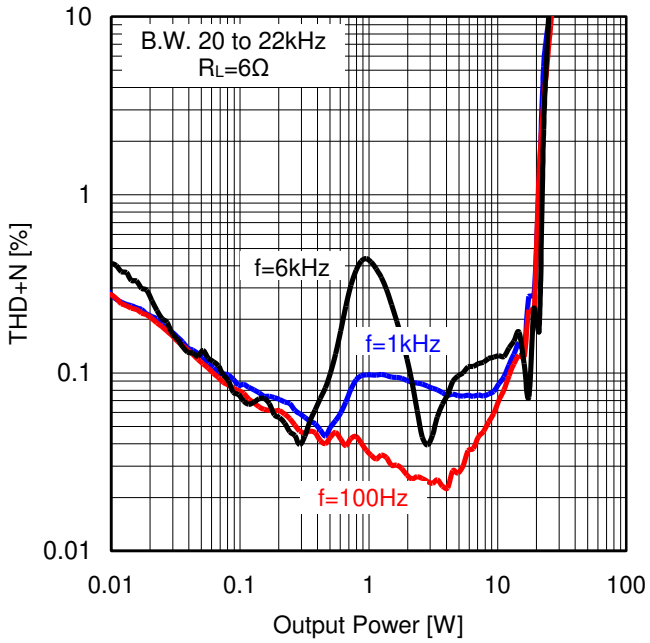

Figure 23.
THD+N - Output Power

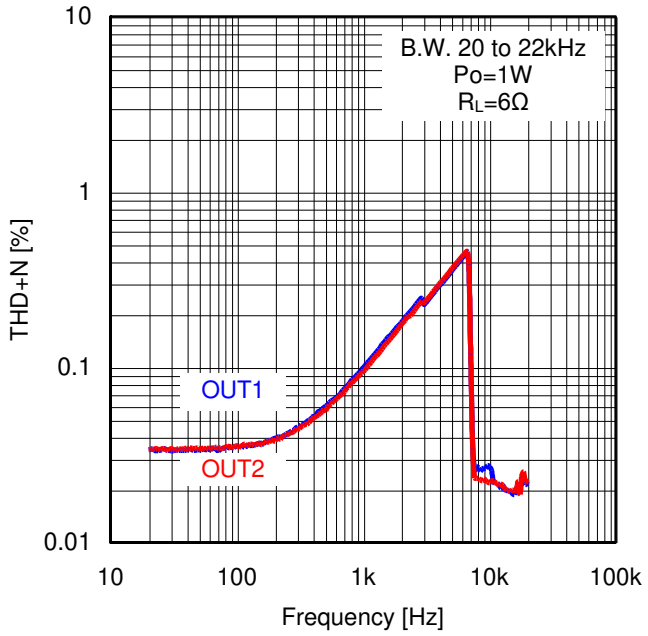

Figure 24.
THD+N - Frequency

(Note 11) 100mm×100mm×1.6mm FR4 4-layer glass epoxy board Cu Thickness 35μm/70μm/70μm/35μm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1},V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=6Ω, DSP: Through, Driver Gain(G_{DRV})=26dB
Measured by ROHM designed 4 layers board(Note 11)

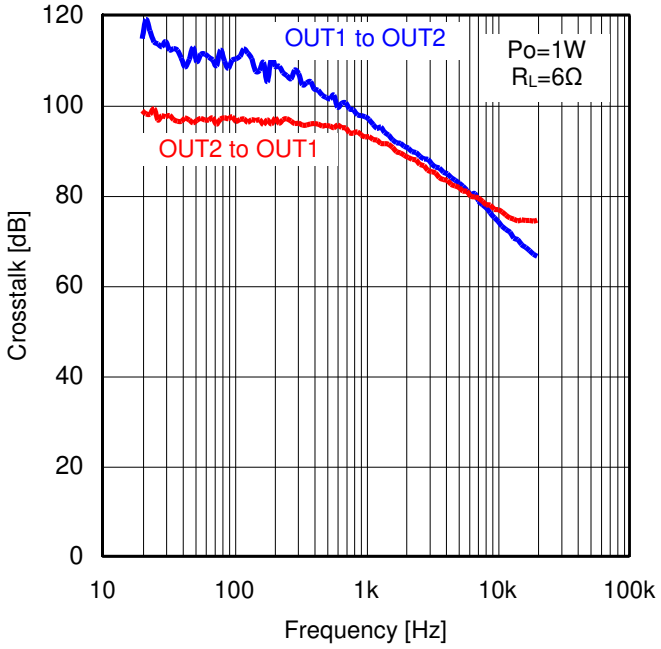

Figure 25.
Crosstalk - Frequency

(Note 11) 100mm×100mm×1.6mm FR4 4-layer glass epoxy board Cu Thickness 35μm/70μm/70μm/35μm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1},V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=4Ω, DSP: Through, Driver Gain(G_{DRV})=26dB
Measured by ROHM designed 4 layers board(Note 11)

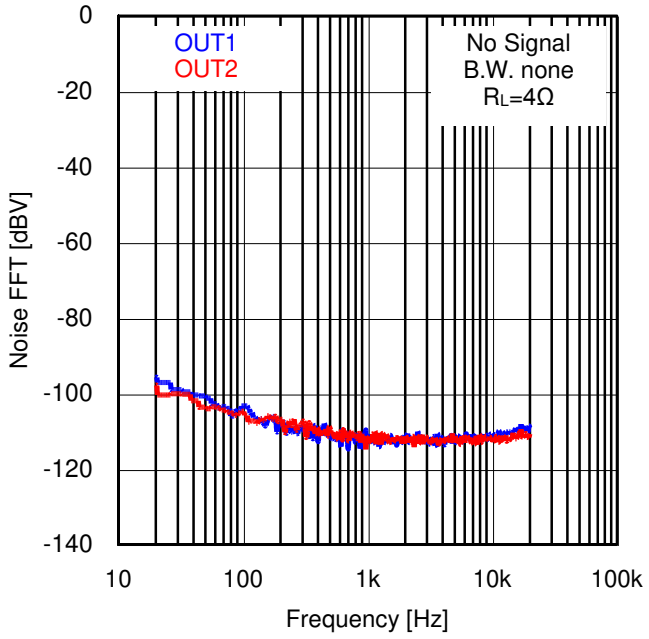

Figure 26.
FFT of output noise voltage

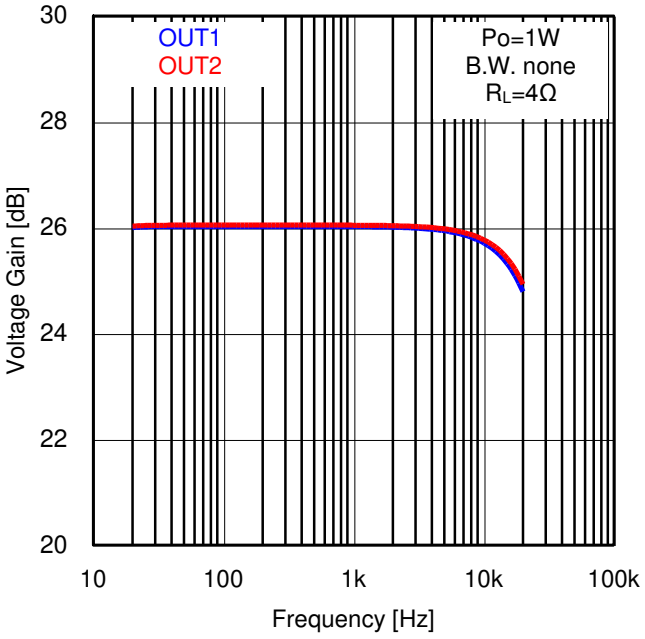

Figure 27.
Voltage Gain - Frequency

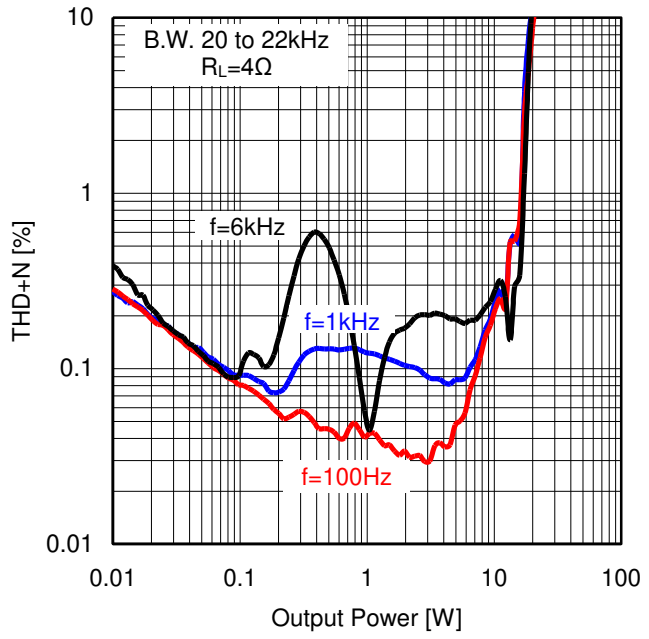

Figure 28.
THD+N - Output Power

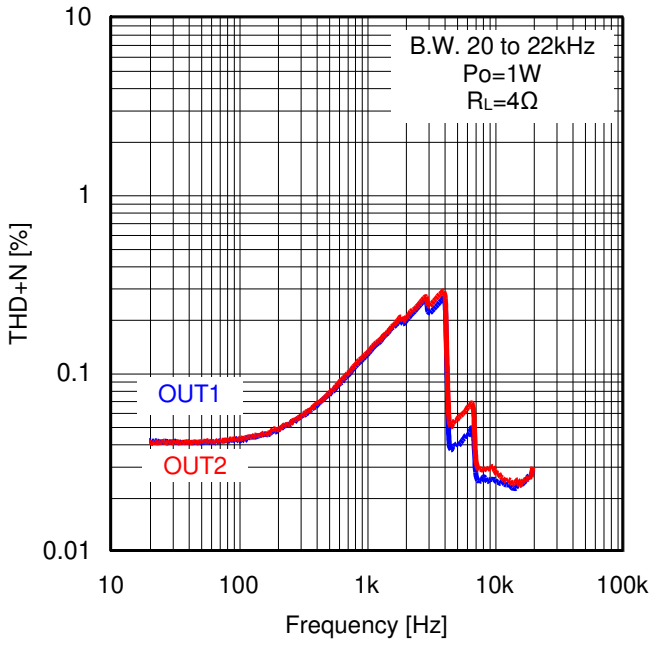

Figure 29.
THD+N - Frequency

(Note 11) 100mm×100mm×1.6mm FR4 4-layer glass epoxy board Cu Thickness 35μm/70μm/70μm/35μm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1},V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=4Ω, DSP: Through, Driver Gain(G_{DRV})=26dB
Measured by ROHM designed 4 layers board(Note 11)

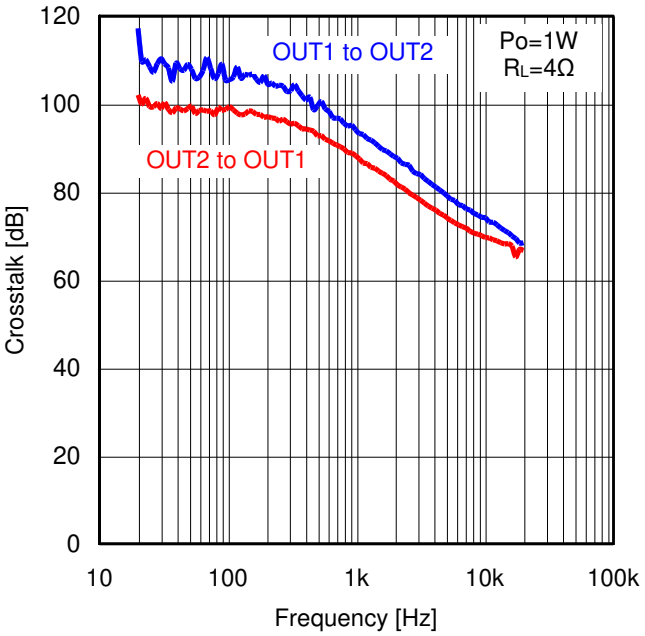

Figure 30.
Crosstalk - Frequency

(Note 11) 100mm×100mm×1.6mm FR4 4-layer glass epoxy board Cu Thickness 35μm/70μm/70μm/35μm For Application Evaluation Board

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DSP Block Functional Overview

No.	Function	Specification
1	Pre-Scaler	•Lch / Rch become same set point. •+48dB to -79dB (0.5dB step),-∞dB
2	Channel Mixer	•It is able to set mixing of Left and Right channel which are inputted digital signal to Audio DSP •Selectable in L,(L+R)/2, L-R, R, MUTE
3	12 Band BQ	•12 Band Bi-quad(BQ) type filter . •Only 5 coefficients are required.(b0,b1,b2,a1,a2) •Lch/Rch dependent or independent. •The Filter types which can be attained are Peaking/Low-shelf/High-shelf/Low-pass/High-pass/All-pass/Notch. •There is soft transition function.
4	Fine Master Volume	•Lch / Rch become same set point or independent set. •+24dB to -103dB (0.125dB step),-∞dB •There are soft transition and soft mute functions.
5	3 Band DRC	•There are 3 band DRC. •It is possible to set the slope of compression level.
6	Post-scaler	•Lch / Rch become same set point. •+48dB to -79dB (0.5dB step),-∞dB
7	Fine Post-scaler	•Lch / Rch become independent set point. •+0.7dB to -0.8dB (0.1dB step)
8	DC cut HPF	•1st order HPF •Cut off frequency fc : 1Hz
9	Hard Clipper	•Lch / Rch become same set point. •Clip level : 0dB to -22.5dB (-0.1dB step)

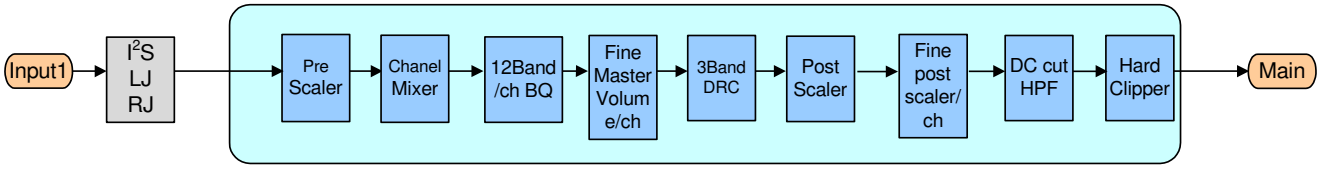

Figure 31. DSP Block diagram

RSTX Pin(Note 12) (Note 13), MUTEX Pin function

RSTX (29pin)	MUTEX (30pin)	DSP block	Speaker output (OUT1P, OUT1N, OUT2P, OUT2N)
Low	Low	Reset ON	High-Z_low(Note 14) (Low power consumption)
High	Low	Normal operation (Mute ON)	High-Z_low(Note 14) (Mute ON) (Note 15)
High	High	Normal operation (Mute OFF)	Normal operation (Mute OFF)
Low	High	Don't use.	

(Note 12) When RSTX is set to low, internal registers are initialized.
(Note 13) If V_{DVDD} is under 3V, RSTX is set to low once for 10ms(Min), and set to high again. Then DSP is needed to set parameter again.
(Note 14) This means that all output transistors are OFF and output terminals are pulled down by 10kΩ (Typ).
(Note 15) Speaker output becomes High-Z_low after elapse of PWM stop time after setting MUTEX low.
Refer to PWM Sampling Frequency in next page for PWM stop time.

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PWM Sampling Frequency

PWM sampling frequency of speaker output, Soft mute time, Soft start time and PWM stop time depend on sampling frequency (f_S) of the digital audio signal. These transition times are changed by sending the data to select address 0x15[1:0].

Default = 0x3 *Blue square means initial value.

Sampling frequency (f_S)	PWM sampling frequency	0x15[1:0] value	Soft mute time	Soft start time	PWM stop time
48kHz	384kHz	0x0	10.7ms	10.7ms	86ms
		0x1	21.4ms	10.7ms	106ms
		0x2	42.7ms	10.7ms	125ms
		0x3	85.4ms	10.7ms	162ms
44.1kHz	352.8kHz	0x0	11.7ms	11.7ms	93ms
		0x1	23.3ms	11.7ms	113ms
		0x2	46.5ms	11.7ms	135ms
		0x3	92.9ms	11.7ms	177ms
32 kHz	256kHz	0x0	16.1ms	16.1ms	116ms
		0x1	32.1ms	16.1ms	148ms
		0x2	64.1ms	16.1ms	178ms
		0x3	128.1ms	16.1ms	241ms

Setting Driver Gain (G_{DRV})

It can change the driver gain of the output FET driver part.
Set it depending on speaker used because the maximum output level changes by speaker load impedance value.

When set the driver gain, change after setting MUTEX terminal to low (>PWM stop time).
Pop noise may be occur if the driver gain is set while MUTEX=high.

Default = 0x03 *Blue square means initial value.

Select Address	Value	Driver Gain G_{DRV} (BTL)
0xF3[7:0]	0x03	26dB(Typ)
0xF3[7:0]	0x0B	32dB(Typ)

Regarding 0xF3 address,
Prohibit to set except data "0x03" and "0x0B" to address 0xF3.
The setting value is fixed by transmitting 0xF8=0x01. If the setting value of address 0xF3 is changed, certainly set 0xF8=0x01 again. In addition, Wait time more than 10ms is necessary after 0xF8=0x01 setting.

Setting of When Monaural output

When monaural output setting is applied as shown in Application Circuit Example3, set 0xF2 register during start-up (Refer to P.62 "7. The wake-up Procedure of power-up").
Setting 0xF2 = 0x0A, DC voltage protection function at the speaker of OUT2 side can be disabled, therefore it is possible to use Application Circuit Example3.

Default = 0x02 *Blue square means initial value.

Select Address	Value	PWM Output Signal
0xF2[7:0]	0x02	Stereo
0xF2[7:0]	0x0A	Monaural

Regarding 0xF2 address,
Prohibit to set except data "0x02" and "0x0A" to address 0xF2.
The setting value is fixed by transmitting 0xF8=0x01. If the setting value of address 0xF2 is changed, certainly set 0xF8=0x01 again. In addition, Wait time more than 10ms is necessary after 0xF8=0x01 setting.

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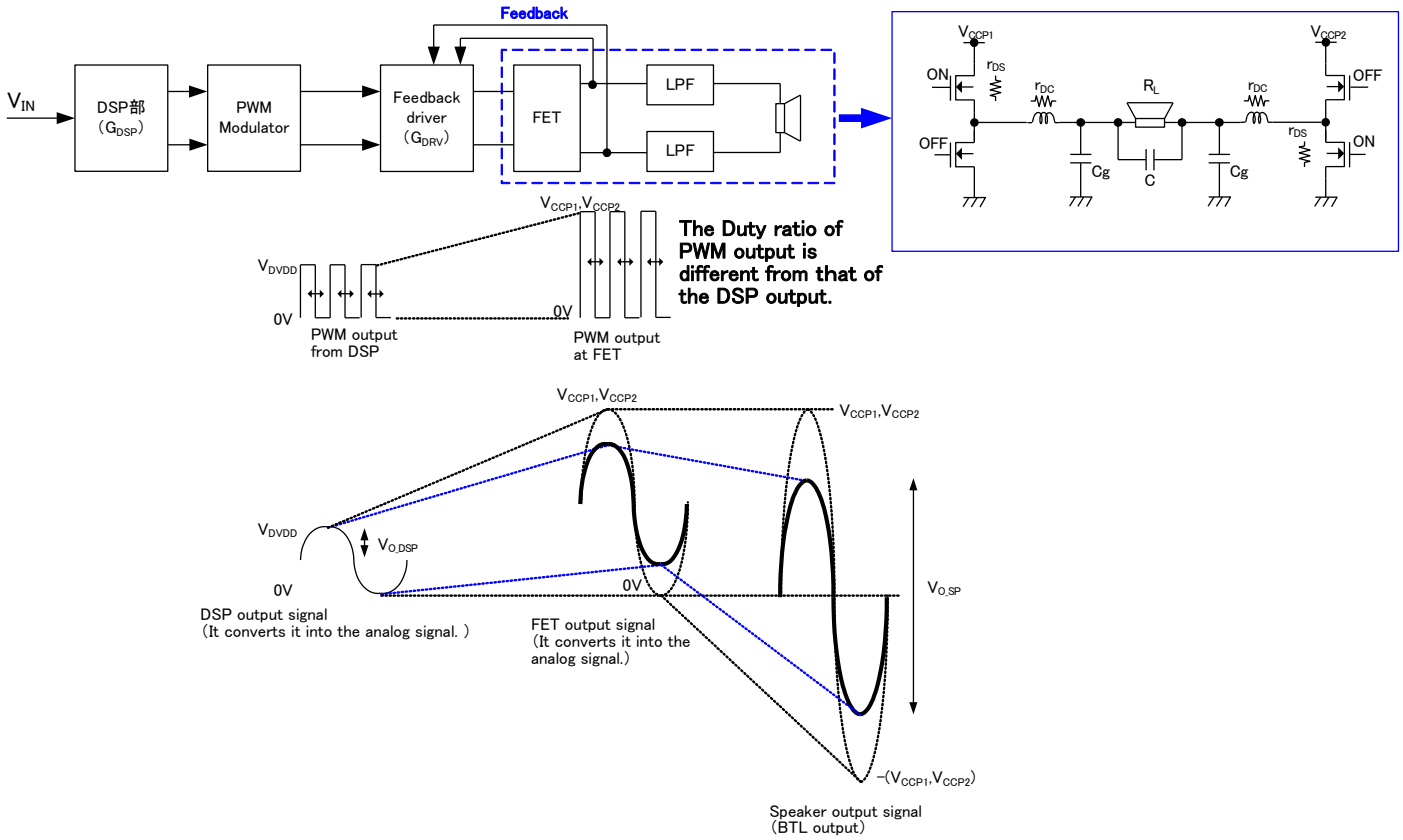
Level Diagram

$$(1)DSP\ Gain = 10^{\left(\frac{V_{IN}+G_{DSP}}{20}\right)}$$

$$(2)Driver\ Gain(BTL) = 10^{\left(\frac{G_{DRV}}{20}\right)}$$

$$(3)Loss = \frac{R_L}{2(r_{DS}+r_{DC})+R_L}$$



$$V_{O\_DSP} = 10^{\left(\frac{V_{IN}+G_{DSP}}{20}\right)} \text{ [Vrms]}$$

$$V_{O\_SP} = V_{O\_DSP} \times 10^{\left(\frac{G_{DRV}}{20}\right)} \times \frac{R_L}{2(r_{DS}+r_{DC})+R_L} \text{ [Vrms]}$$

$$P_{O(THD=1\%)} = \frac{\left[10^{\left(\frac{V_{IN}+G_{DSP}}{20}\right)} \times 10^{\left(\frac{G_{DRV}}{20}\right)} \times \frac{R_L}{2(r_{DS}+r_{DC})+R_L}\right]^2}{R_L} \text{ [W]}$$

$$P_{O(THD=10\%)} = P_{O(THD=1\%)} \times 1.25 \text{ [W]}$$

V_{IN}	: I²S input level [dBFS]
G_{DSP}	: DSP gain [dB]
G_{DRV}	: Feedback driver gain [dB]
V_{CCP1},V_{CCP2}	: Power supply voltage for power amp [V]
V_{DVDD}	: Power supply voltage for DSP [V]
R_L	: Speaker load resistance [Ω]
r_{DS}	: Output FET on resistance[Ω] (Typ = 0.23Ω)
r_{DC}	: Direct current resistance of coil [Ω]

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2 Wire Bus Control Signal Specification

1) Electrical Characteristics and Timing of Bus Line and I/O Stage

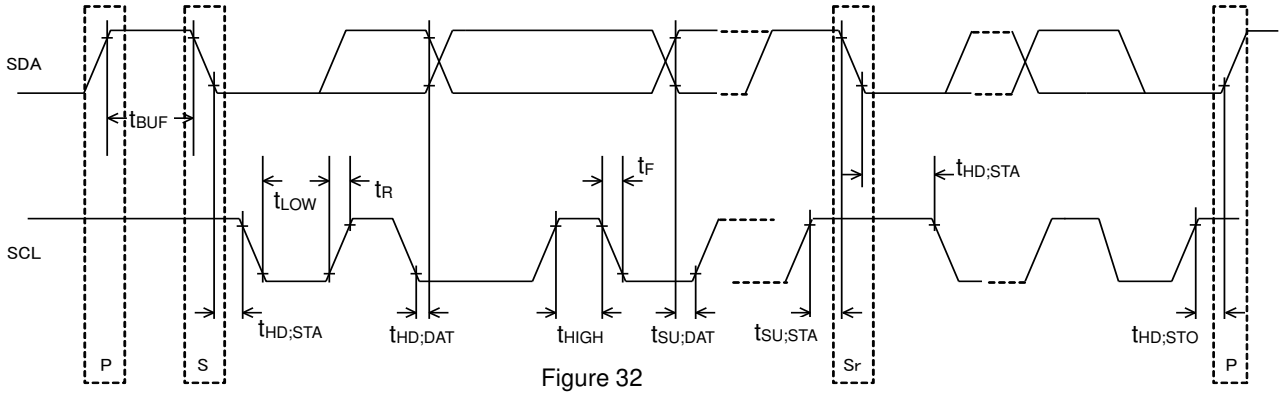

Figure 32

SDA and SCL bus line characteristics(Note 17) (Unless otherwise specified Ta=25°C, V_{DVDD}=3.3V)

Parameter		Symbol	High Speed Mode		Unit
			Min	Max	
1	SCL clock frequency	f_{SCL}	0	400	kHz
2	Bus free time between a STOP and START condition	t_{BUF}	1.3	-	µs
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	0.6	-	µs
4	Low period of the SCL clock	t_{LOW}	1.3	-	µs
5	High period of the SCL clock	t_{HIGH}	0.6	-	µs
6	Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	µs
7	Data hold time	$t_{HD;DAT}$	0 (Note 16)	-	µs
8	Data set-up time	$t_{SU;DAT}$	250	-	ns
9	Rise time of both SDA and SCL signals	t_R	20+0.1Cb	300	ns
10	Fall time of both SDA and SCL signals	t_F	20+0.1Cb	300	ns
11	Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	µs
12	Capacitive load for each bus line	Cb	-	400	pF

The above-mentioned numerical values are all the values corresponding to V_{IHmin} and the V_{ILmax} level.

(Note 16) To exceed an undefined area on the fall-edge of SCL (Refer to V_{IH} min of the SCL signal), the transmitting set like SoC should internally offer the holding time of 300ns or more for the SDA signal.

(Note 17) SCL and SDA pin is not corresponding to threshold tolerance of 5V. Use it within Input voltage 1 of the absolute maximum rating.

2) Command Interface

2 wire Bus Control is used for command interface between host CPU. It not only writes but also it is possible to read it excluding a part of register. In addition to “Slave Address“ , set and write 1 byte of “Select Address“ to read out the data. 2 wire bus Slave mode format is illustrated below.

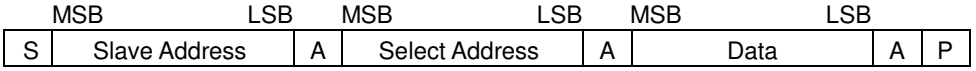

Figure 33

S : Start Condition

Slave Address : Data of 8bit in total is sent with a bit of Read mode (high) or Write mode (low) after slave address (7bit) set by ADDR terminal. (MSB first)

A : Acknowledge-bit will be added byte per byte in the data that acknowledge is sent and received. “low” will be sent and received when the data is correctly sent and received. There was no acknowledgement for “high”.

Select Address : Use 1byte of select address. (MSB first)

Data : Sent and received data-byte data. (MSB first)

P : Stop Condition

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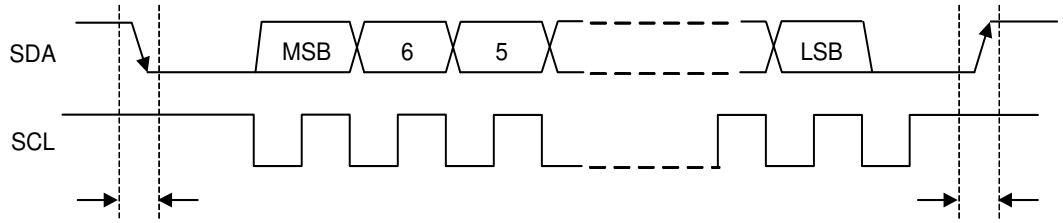

Figure 34

3) Slave Address

•While ADDR Pin is "low"

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	1/0

•While ADDR Pin is "high"

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	1/0

Figure 35

4) Writing of Data

•Basic format

S	Slave Address	A	Select Address	A	Data	A	P

: Master to Slave, Slave to Master

•Auto-increment format

S	Slave Address	A	Select Address	A	Data 1	A	Data 2	A	Data 3…N	A	P

: Master to Slave, Slave to Master

Figure 36

5) Reading of Data

First of all, the address (0x20 in the example) for reading is written in the register of the 0xD0 address at the time of reading. In the following stream, data is read after the slave address. Do not return the acknowledge when ending the reception.

S	Slave Address	A	Req_Addr	A	Select Address	A	P
(ex.)	0x80		0xD0		0x20		

S	Slave Address	A	Data 1	A	Data 2	A		A	Data N	Ā	P
(ex.)	0x81		0x**		0x**				0x**		

: Master to Slave, : Slave to Master,A:With Acknowledge,Ā:Without Acknowledge

Figure 37

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Format of Digital Audio Interface

- LRCLK: It is L/R Clock Input Signal
  It is available of 32kHz/44.1kHz/48kHz with those clocks (f_S) that are same to the sampling frequency (f_S).
  The data of the left channel and the right channel for one sample is input to this section.

- BCLK: It is Bit Clock Input Signal
  It is used for the latch of data in every one bit by sampling frequency's 32 times frequency ($32f_S$) or 48 times frequency ($48f_S$) or 64 times sampling frequency ($64f_S$). However if the $32f_S$ is selected, the data length is held static of 16bit.

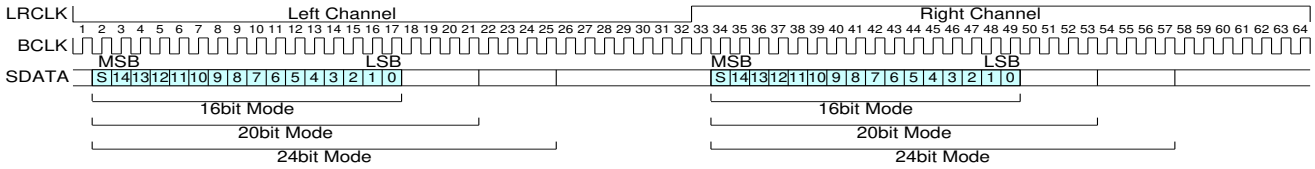
- SDATA: It is Data Input Signal
  It is amplitude data. Word length is different according to the resolution of the input digital audio signal.
  It is available of 16/ 20/ 24 bit.

  The digital input format is available of I^2S, Left-justified and Right-justified formats.
  The figure below shows the timing chart of each transmission mode.

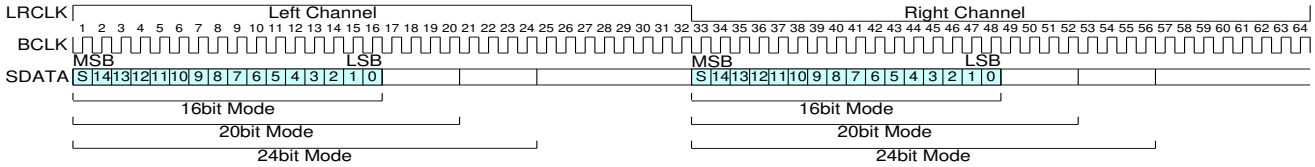
- SDATAO: Audio Data Output After DSP Processing
  This output syncs with inputted LRCLK and BCLK.
  Output format is available of I^2S format only.

BCLK Clock $64f_S$

I^2S 64fs Format



Left-Justified 64fs Format



Right-Justified 64fs Format

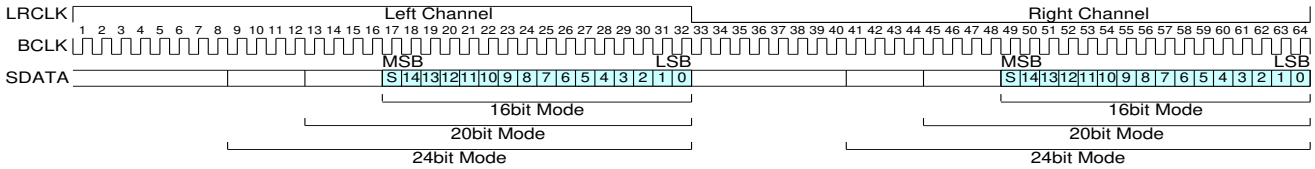


Figure 38

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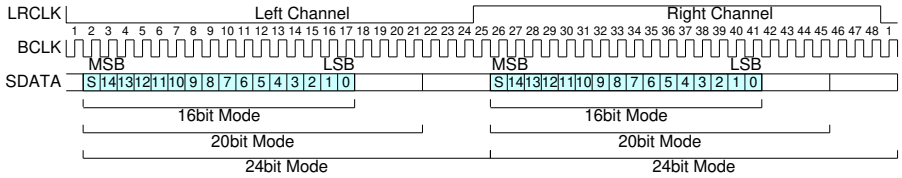
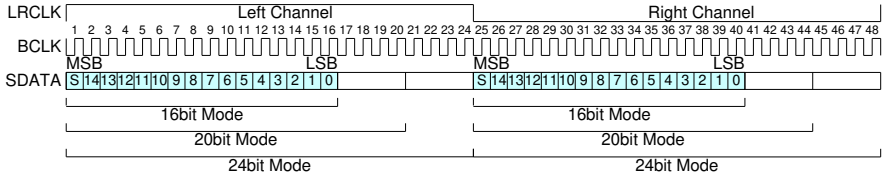
BCLK Clock 48fS

I2S 48fs Format



Left-Justified 48fs Format



Right-Justified 48fs Format

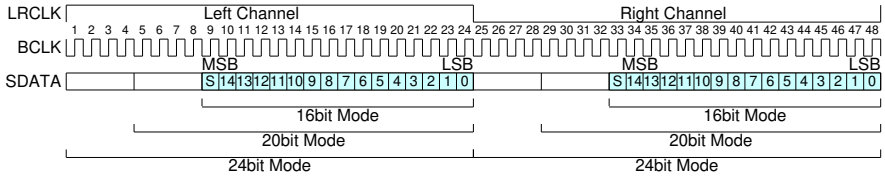
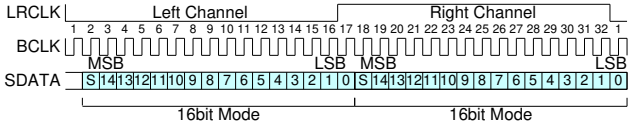


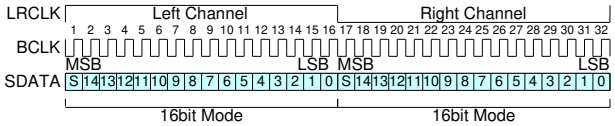
Figure 39

BCLK Clock 32fS

I2S 32fs Format



Left-Justified 32fs Format



Right-Justified 32fs Format

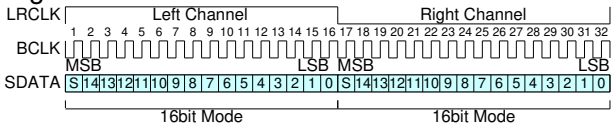


Figure 40

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Format Setting for Digital Audio Interface

Set BCLK clock f_S, word length and data format by transmitting command according to the inputted digital audio signal.
SDATAO output word length is able to be set independently of input word length.
It is available of I^2S format only.

BCLK Clock

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of Operation
0x03[5:4]	0x0	64f_S
	0x1	48f_S
	0x2	32f_S
	0x3	Don't use

Data Format

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of Operation
0x03[3:2]	0x0	I^2S format
	0x1	Left-justified format
	0x2	Right-justified format
	0x3	Don't use

Word Length

Default = 0x2 *Blue square means initial value.

Select Address	Value	Explanation of Operation
0x03[1:0]	0x0	16 bit
	0x1	20 bit
	0x2	24 bit
	0x3	Don't use

SDATAO Output Word Length

Default = 0x2 *Blue square means initial value.

Select Address	Value	Explanation of Operation
0x78[1:0]	0x0	16 bit
	0x1	20 bit
	0x2	24 bit
	0x3	Don't use

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