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Middle Power Class-D Speaker Amplifiers

Class-D Speaker Amplifier for Digital Input with Built-in DSP

BM5446EFV

No.10075EBT13

●Description

BM5446EFV is a Class D Speaker Amplifier with built-in DSP (Digital Sound Processor) designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 20W+20W. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency of 86% (10W+10W output with 8Ω load). In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

●Features

1) This IC includes the DSP (digital sound processor) for Audio signal processing for Flat TVs.
2) This IC has two input systems of digital audio interface.
   (I^2S/LJ/RJ format, LRCLK: 32 kHz/ 44.1kHz / 48kHz, SYS_CLK: 256fs / 512fs,
   BCLK: 48fs / 64fs, SDATA: 16 / 20 / 24bit)
3) With wide range of power supply voltage, it is possible to operate with single power supply. (Vcc = 10~26V)
4) With high efficiency and low heat dissipation contributing to miniaturization, slim design, and also power saving of the system.
5) S/N of the system can be optimized by adjusting the gain selection in 16 steps. (20~35dB,1dB/step)
6) With built-in feedback circuitry at the output, prevents the decrease in sound quality due to change in power supply voltage. In addition, low noise and low distortion are achieved.
7) With a built-in DAC provides best stereo-output for headphone function. As a result, the selection of output of the digital input in two systems is possible.
8) It has additional S/PDIF output for the LINE output usage.
9) Eliminates pop-noise generated during the power supply on/off. High quality muting performance is realized by using the soft-muting technology.
10) This IC is built-in with various protection functions for highly reliability design.
    (High temperature protection, Under voltage protection, Output short protection, Output DC-Voltage protection and Clock stop protection).

●Applications

Flat Panel TVs (LCD, Plasma), Home Audio, Desktop PC, Amusement equipments, Electronic Music equipments, etc.

●**Absolute maximum ratings** (Ta=25℃)

Parameter	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	30	V	Pin 27, 30, 31, 51, 52 *1*2
Power dissipation	Pd	2.0	W	*3
		4.5	W	*4
		6.2	W	*5
Input voltage	V_{IN}	-0.3 ~ 4.5	V	Pin 5 ~ 14, 22 *1
Open-drain terminal voltage	V_{ERR}	-0.3 ~ 30	V	Pin 26 *1
Operating temperature range	Topr	-25 ~ +85	℃	
Storage temperature range	Tstg	-55 ~ +150	℃	
Maximum junction temperature	Tjmax	+150	℃	

*1 The voltage that can be applied reference to GND (Pin 4, 36, 37, 45, 46) and VSS (Pin 15, 20).
*2 Do not, however exceed Pd and Tjmax=150℃.
*3 70mm×70mm×1.6mm, FR4, 1-layer glass epoxy board (Copper on bottom layer 0%)
Derating in done at 16mW/℃ for operating above Ta=25℃.
*4 70mm×70mm×1.6mm, FR4, 2-layer glass epoxy board (Copper on bottom layer 100%)
Derating in done at 36mW/℃ for operating above Ta=25℃. There are thermal via on the board.
*5 70mm×70mm×1.6mm, FR4, 4-layer glass epoxy board (Copper on bottom layer 100%)
Derating in done at 49.6mW/℃ for operating above Ta=25℃. There are thermal via on the board.

●**Operating conditions** (Ta=25℃)

Parameter	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	10 ~ 26	V	Pin 27, 30, 31, 51, 52 *1 *2
Minimum load impedance (Speaker Output)	R_{L_SP}	5.4	Ω	*6
Minimum load impedance (DAC Output)	R_{L_DA}	20	kΩ	Pin 24, 25

*6 Do not, however exceed Pd.
* No radiation-proof design.

●Electrical characteristics

(Unless otherwise specified Ta=25℃,Vcc=13V,f=1kHz,R_{L_SP}=8Ω,R_{L_DA}=20kΩ,RESETX=3.3V,MUTEX=3.3V,PDX=3.3V, Gain=20dB, DSP: Through, fs =48kHz)

Parameter	Symbol	Limits			Unit	Conditions	
		Min.	Typ.	Max.			
Total circuit							
Circuit current	I_{CC1}	-	60	120	mA	Pin 27, 30, 31, 51, 52,No load	
Circuit current (Power down mode)	I_{CC2}	-	2.5	5	mA	Pin 27, 30, 31, 51, 52,No load RESETX=0V, MUTEX=0V,PDX=0V	
Open-drain terminal Low level voltage	V_{ERR}	-	-	0.8	V	Pin 26,I_O=0.5mA	
Regulator output voltage 1	V_{REG_G}	5.0	5.5	6.0	V	Pin 28, 54	
Regulator output voltage 2	V_{REG_3}	3.0	3.3	3.6	V	Pin 3	
Regulator output voltage 3	V_{REG_15}	1.3	1.5	1.7	V	Pin 16	
High level input voltage	V_{IH}	2.5	-	3.3	V	Pin 5 ~ 14, 22	
Low level input voltage	V_{IL}	0	-	0.8	V	Pin 5 ~ 14, 22	
Input current (Input pull-up terminal)	I_{IL}	50	100	150	µA	Pin 5 ~ 9,VIN = 0V	
Input current (Input pull-down terminal)	I_{IH}	30	70	105	µA	Pin 10 ~ 12, 22,VIN = 3.3V	
Input current (SCL, SDA terminal)	I_I	-	0	1	µA	Pin 13, 14,VIN = 3.3V	
Output current (SCL, SDA terminal)	I_O	-1	0	-	µA	Pin 13, 14,VIN = 0V	
High level output voltage (S/PDIF output terminal)	V_{OH}	2.75	3.3	-	V	Pin 23,I_O=-0.6mA	
Low level output voltage (S/PDIF output terminal)	V_{OL}	-	0	0.55	V	Pin 23,I_O= 0.6mA	
Speaker Output							
Maximum momentary output power 1	P_{O1}	-	10	-	W	THD+n=10%,Gain=26dB	*7
Maximum momentary output power 2	P_{O2}	-	20	-	W	Vcc=18V,THD+n=10%,Gain=26dB	*7
Total harmonic distortion	THD_{SP}	-	0.07	-	%	P_O=1W,BW=20～20kHz	*7
Crosstalk	CT_{SP}	65	80	-	dB	P_O=1W,BW=IHF-A	*7
Output noise voltage (Sampling mode)	V_{NO_SP}	-	140	280	µVrms	-∞dBFS,BW=IHF-A	*7
Residual noise voltage (Mute mode)	V_{NOR_SP}	-	5	10	µVrms	MUTEX=0V,-∞dBFS,BW=IHF-A	*7
PWM sampling frequency	f_{PWM1}	-	512	-	kHz	fs=32kHz	*7
	f_{PWM2}	-	705.6	-	kHz	fs=44.1kHz	*7
	f_{PWM3}	-	768	-	kHz	fs=48kHz	*7
DAC Output							
Maximum output voltage	V_{OMAX}	0.85	1.0	-	Vrms	0dBFS,THD+n=1%	
Channel Balance	CB	-1	0	1	dB	0dBFS	
Total harmonic distortion	THD_{DA}	-	0.05	0.5	%	-20dBFS,BW=20～20kHz	
Crosstalk	CT_{DA}	65	80	-	dB	0dBFS,BW=IHF-A	
Output noise voltage	V_{NO_DA}	-	10	20	µVrms	-∞dBFS,BW=IHF-A	
Residual noise voltage	V_{NOR_DA}	-	3	10	µVrms	MUTEX=0V,PDX=0V, -∞dBFS,BW=IHF-A	

*7 These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

●DSP Block Functional Overview

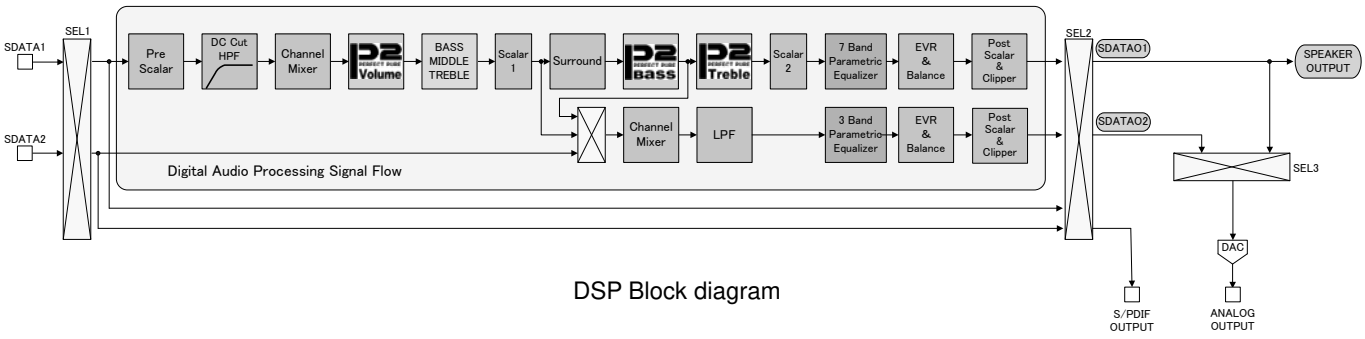
1) Main Signal line function

No.	Function	Specification	
1	Pre-scalar	・Lch / Rch synchronous control ・+24 ~ -103dB (0.5dB step),-∞dB	
2	DC cut HPF	・FC : 1Hz	
3	Channel Mixer	・Mixing of the sound of the left and right channel of the input digital signal to DSP is set up.	
4	P^2Volume (Perfect Pure Volume)	・There are some scenes when sound becomes large suddenly, like the explosion-scene in TV commercial or in an action movie. The “P2Volume” function controls volume automatically and adjusts the output level. ・It makes easy to hear small whisper voice, and is adjusted. ・Attack time : 1ms ~ 40ms (8steps) ・Recovery time : 0.25s ~ 10s (16 steps)	
5	BASS	・Peaking filter is used. ・Lch / Rch Concurrent control ・Soft transition function ・Fc Select : Same as 7 Band Parametric Equalizer ・Gain Select : ±18dB (0.5dB step) ・Q (Quality Factor) : Same as 7 Band Parametric Equalizer	・Low shelf filter is used. ・Lch / Rch Concurrent control ・Soft transition function ・Fc Select : Same as 7 Band Parametric Equalizer ・Gain Select : ±18dB (0.5dB step) ・Q (Quality Factor) : Same as 7 Band Parametric Equalizer
6	MIDDLE	・Peaking filter is used. ・Lch / Rch Concurrent control ・Soft transition function ・Fc Select : Same as 7 Band Parametric Equalizer ・Gain Select : ±18dB (0.5dB step) ・Q (Quality Factor) : Same as 7 Band Parametric Equalizer	
7	TREBLE	・Peaking filter is used. ・Lch / Rch Concurrent control ・Soft transition function ・Fc Select : Same as 7 Band Parametric Equalizer ・Gain Select : ±18dB (0.5dB step) ・Q (Quality Factor) : Same as 7 Band Parametric Equalizer	・High shelf filter is used. ・Lch / Rch Concurrent control ・Soft transition function ・Fc Select : Same as 7 Band Parametric Equalizer ・Gain Select : ±18dB (0.5dB step) ・Q (Quality Factor) : Same as 7 Band Parametric Equalizer
8	Scalar 1	・Lch / Rch Concurrent control ・ +24 ~ -103dB (0.5dB step), -∞dB	
9	Pseudo Stereo	・A stereo-feel sound is reproduced for a monophonic sound by signal processing. ・3 steps : Pseudo Stereo OFF / Pseudo Stereo ON (Weak) / Pseudo Stereo ON (Strong)	
10	Matrix Surround 3D	・Matrix Surround 3D of a wider sweet spot, and it also with little prolonged viewing and listening with a feeling of fatigue. ・The acoustic field which does not spoil a vocal feeling of the normal position is played back. ・Surround : ON / OFF function ・Loop : ON / OFF function ・Surround gain select : 16 steps	
11	P^2Bass (Perfect Pure Bass)	・Clear deep Bass with low distortion. ・Lch / Rch Concurrent control ・Soft transition function ・Frequency select : 4 steps ・Gain select : 0 ~ 15dB (1dB step)	
12	P^2Treble (Perfect Pure Treble)	・Real, pure and crystal clear sound. ・Lch / Rch Concurrent control ・Soft transition function ・Gain select : 0 ~ 15dB (1dB step)	
13	Scalar 2	・Lch / Rch Concurrent control ・+24 ~ -103dB (0.5dB step), - ∞dB	

No.	Function	Specification
14	7-Band Parametric Equalizer	・Peaking filter is used. (Possible to set the 5 coefficients directly for b0,b1,b2,a1,a2) ・Lch / Rch Concurrent control ・Fc select : Setup of 61 divisions (20Hz ~ 20kHz) is possible. ・Gain select : ±18dB (0.5dB step) ・Q(Quality Factor) : 0.33, 0.43, 0.56, 0.75, 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2
15	Volume	・+24 ~ -103dB (0.5dB step), -∞dB ・Soft transition and soft mute function ・Lch / Rch Concurrent control, Sub-Woofer ch Independent control
16	Balance	・It decreases by 1dB step from a volume setting value. (Lch/Rch : 0dB/-∞dB, 0dB/-126dB, 0dB/-125dB, ・・・・・, 0dB/0dB, ・・・・・, -125dB/0dB, -126dB/0dB, -∞dB/0dB)
17	Post-scaler	・Lch / Rch Concurrent control, Sub-Woofer ch Independent control ・+24 ~ -103dB (0.5dB step), -∞dB
18	Output Clipper	・A clip with an arbitrary output amplitude is possible. ・Lch / Rch Concurrent control, Sub-Woofer ch Independent control

2) Sub Signal line function

No.	Function	Specification
19	Channel Mixer	・Mixing of the sound of the left and right channel of the input digital signal to DSP is set up. ・Lch (Lch is input, (Lch+Rch)/2 is input, Rch is input), Rch (Rch is input, (Lch+Rch)/2 is input, Lch is input)
20	LPF	・LPF for Sub-Woofer ・Fc= 60Hz, 80Hz, 100Hz, 120Hz, 160Hz, 200Hz, 240Hz, 280Hz
21	3-Band Parametric Equalizer	・Peaking or low shelf or high shelf filter is used. ・Lch / Rch Concurrent control
22	Volume	・+24 ~ -103dB (0.5dB step), -∞dB ・Soft transition and soft mute function ・ Lch / Rch Concurrent control, Sub-Woofer ch Independent control
23	Balance	・It decreases by 1dB step from a volume setting value. (Lch/Rch : 0dB/-∞dB, 0dB/-126dB, 0dB/-125dB, ・・・・・, 0dB/0dB, ・・・・・, -125dB/0dB, -126dB/0dB, -∞dB/0dB)
24	Post-scaler	・Lch / Rch Concurrent control, Sub-Woofer ch Independent control. ・+24 ~ -103dB (0.5dB step), -∞dB
25	Output Clipper	・A clip with an arbitrary output amplitude is possible. ・Lch / Rch Concurrent control, Sub-Woofer ch Independent control.



DSP Block diagram

●**Electrical characteristic curves**(V_{CC}=13V,R_{L_SP}=8Ω,R_{L_DA}=20kΩ,Gain=20dB,fin=1kHz,fs=48kHz,by passing DSP)
Measured by ROHM designed 4 layer board.

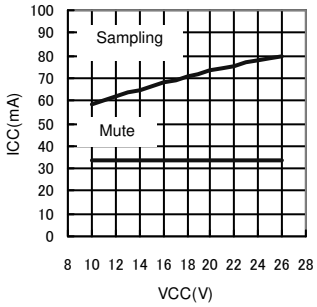


Fig.1
Current consumption
- Power supply voltage

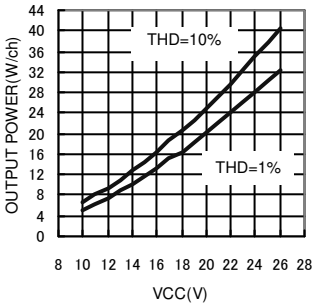


Fig.2
Output power
- Power supply voltage

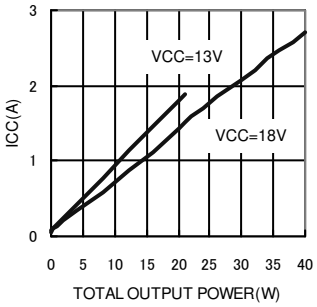


Fig.3
Current consumption
- Output power

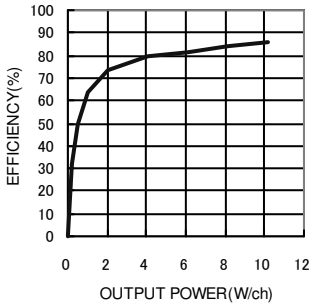


Fig.4
Efficiency - Output power

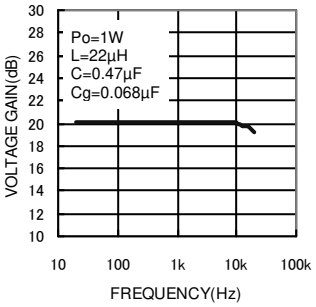


Fig.5
Voltage gain - Frequency

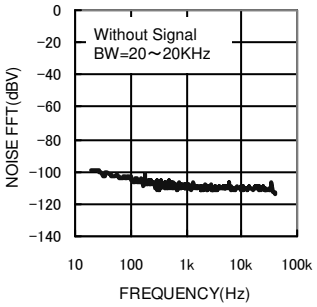


Fig.6
FFT of Output noise voltage

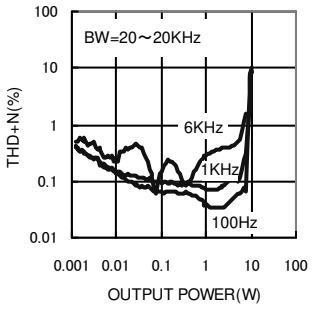


Fig.7
THD+N - Output power

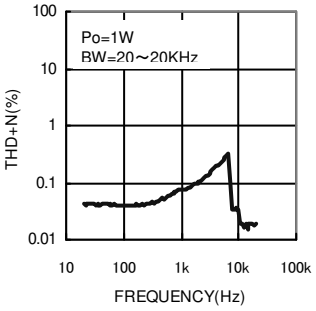


Fig.8
THD+N - Frequency

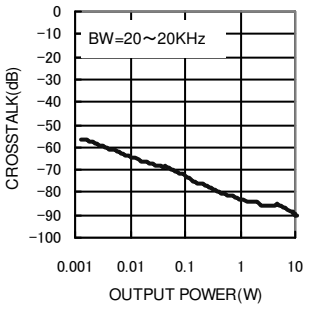


Fig.9
Crosstalk - Output power

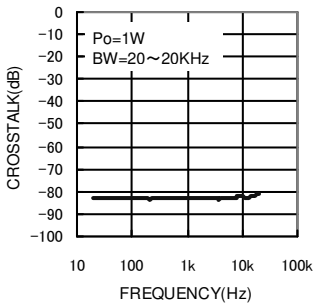


Fig.10
Crosstalk - Frequency

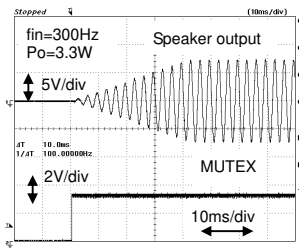


Fig.11
Wave form when
Releasing Soft-start

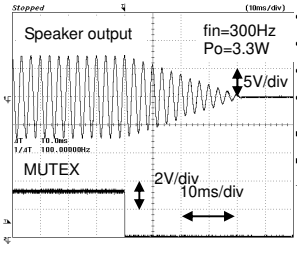


Fig.12
Wave form when
Activating Soft-mute

●**Electrical characteristic curves**(V_{CC}=18V,R_{L_SP}=8Ω,R_{L_DA}=20kΩ,Gain=20dB,fin=1kHz,fs=48kHz,by passing DSP)
Measured by ROHM designed 4 layer board.

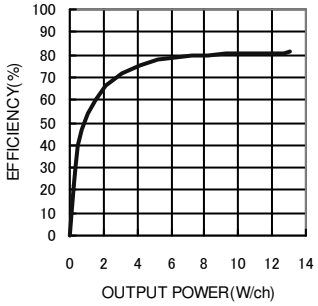


Fig.13
Efficiency – Output power

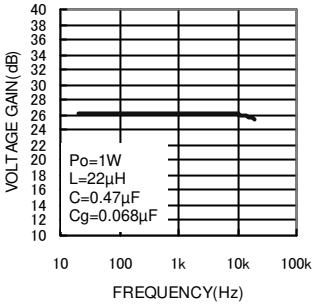


Fig.14
Voltage gain - Frequency

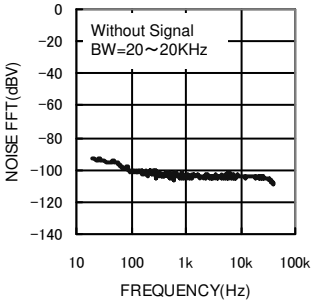


Fig.15
FFT of output noise voltage

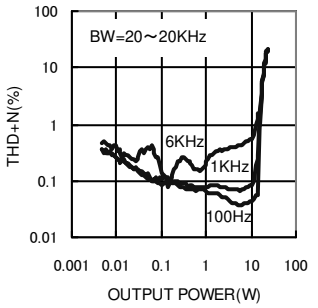


Fig.16
THD+N - Output power

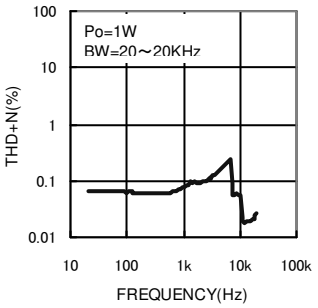


Fig.17
THD+N - Frequency

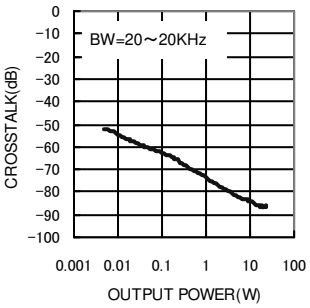


Fig.18
Crosstalk – Output power

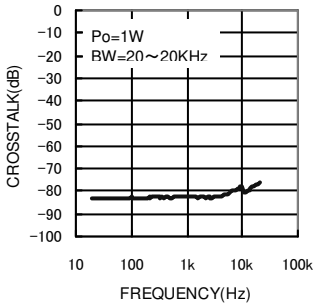
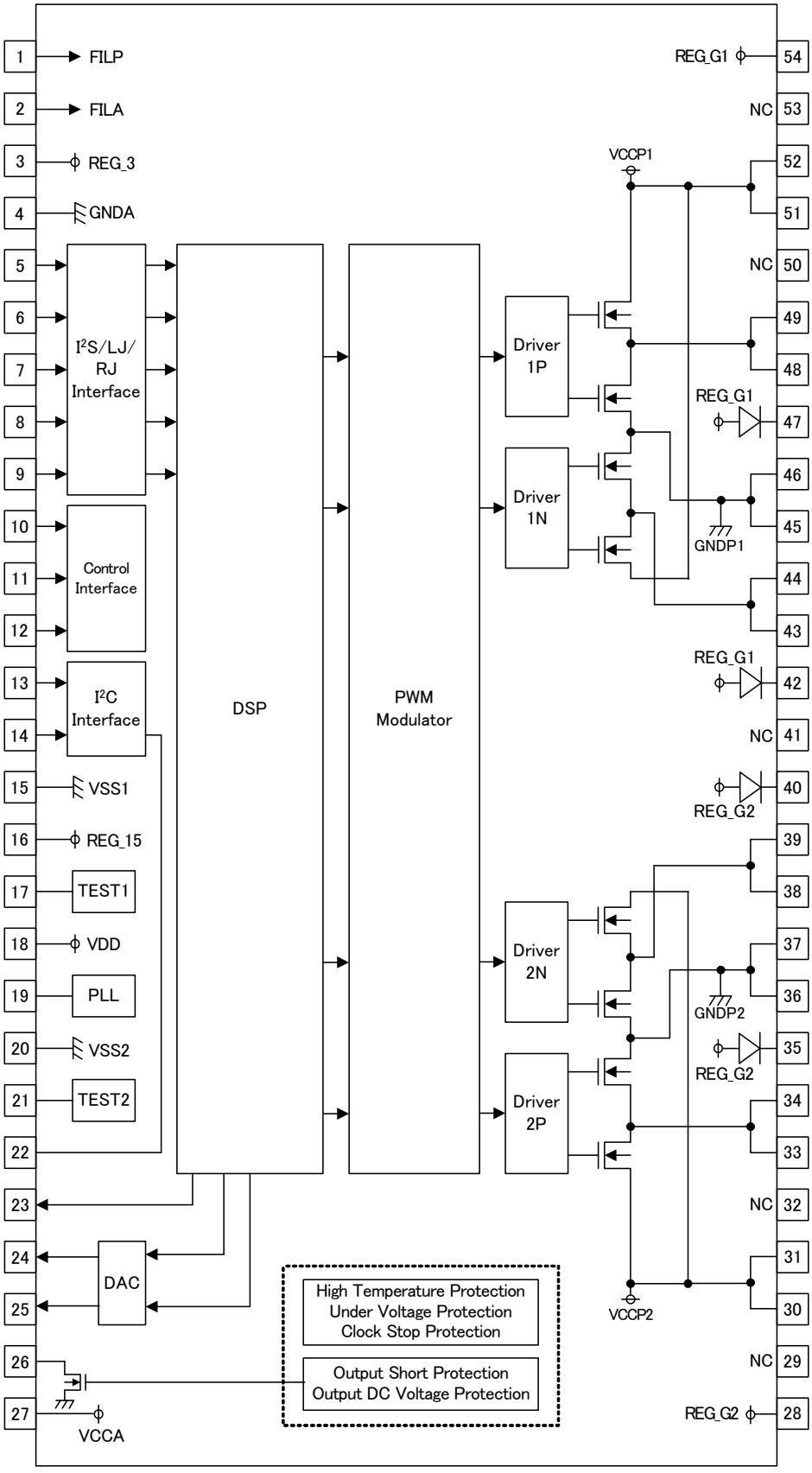
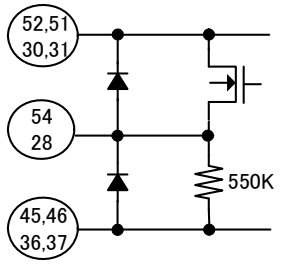
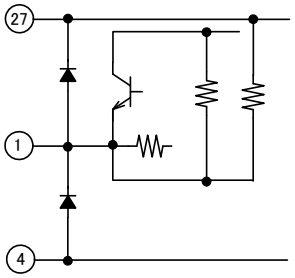
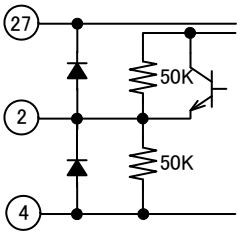
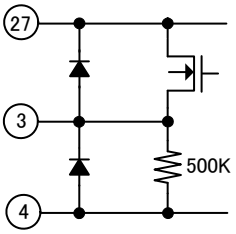
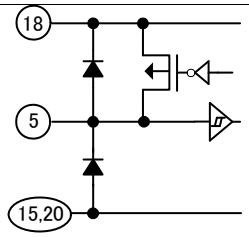
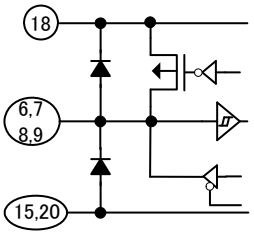
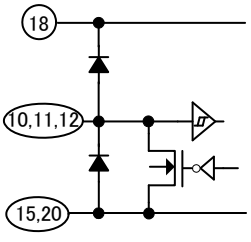


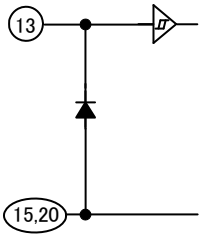
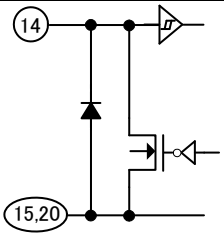
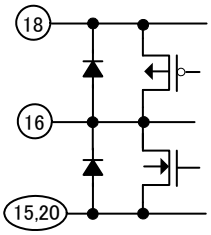
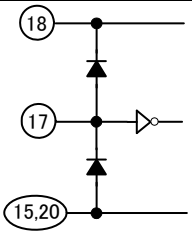
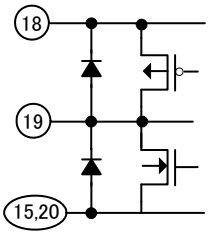
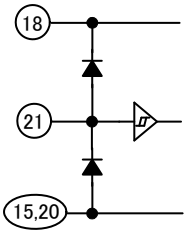
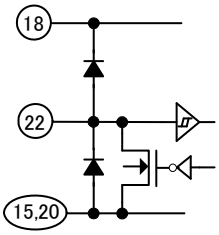
Fig.19
Crosstalk - Frequency

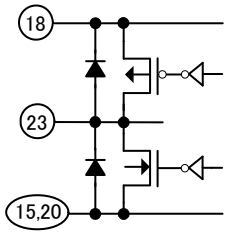
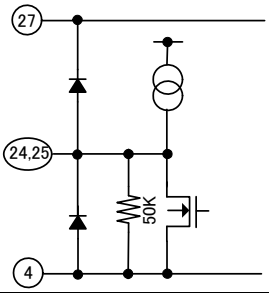
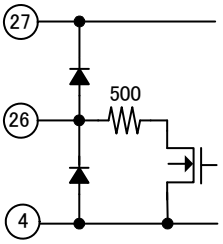
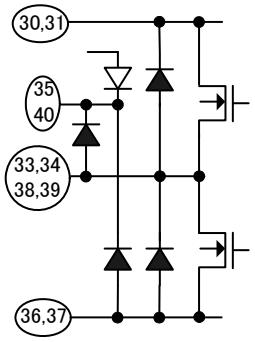
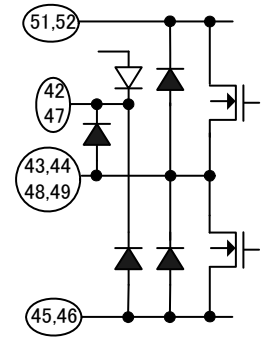
●Pin configuration and Block diagram



●**Pin function explanation (Provided pin voltages are typ. Values)**

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
54 28	REG_G1 REG_G2	5.5V	Internal power supply pin for ch1 Gate driver Internal power supply pin for ch2 Gate driver Please connect the capacitor.	
1	FILP	1.75～2.55V	Bias pin for PWM signal Please connect the capacitor.	
2	FILA	2.5V	Bias pin for Analog signal Please connect the capacitor.	
3	REG3	3.3V	Internal power supply pin for Digital circuit Please connect the capacitor.	
4	GNDA	0V	GND pin for Analog signal	—
5	SYS_CLK	3.3V	System-Clock input pin	
6 7 8 9	BCLK LRCLK SDATA1 SDATA2	3.3V	Digital audio signal input pin	
10	RESETX	0V	Reset pin for Digital circuit H: Reset OFF L: Reset ON	
11	MUTEX		Speaker output mute control pin H: Mute OFF L: Mute ON	
12	PDX		Power down control pin H: Power down OFF L: Power down ON	

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
13	SCL	—	I^2C transmit clock input pin	
14	SDA	—	I^2C data input/output pin	
15 20	VSS1 VSS2	0V	GND pin for Digital I/O	—
16	REG_15	1.5V	Internal power supply pin for Digital circuit	
17	TEST1	—	Test pin Please connect to VSS.	
18	VDD	3.3V	Power supply pin for Digital I/O	—
19	PLL	1V	PLL's filter pin	
21	TEST2	0V	Test pin Please connect to VSS.	
22	ADDR	0V	I^2C Slave address select pin	

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
23	OUT_SPDIF	—	S/PDIF output pin	
24 25	OUT_DAC2 OUT_DAC1	2.5V	ch2 DAC output pin ch1 DAC output pin Please connect it with the latter part circuit through the capacitor.	
26	ERROR	3.3V	Error flag pin Please connect pull-up resistor. H: While Normal L: While Error	
27	VCCA	Vcc	Power supply pin for Analog signal	—
30 31	VCCP2	Vcc	Power supply pin for ch2 PWM signal	
33 34	OUT2P	Vcc～0V	Output pin of ch2 positive PWM signal Please connect to Output LPF.	
35	BSP2P	—	Boot-strap pin of ch2 positive Please connect the capacitor.	
36 37	GNDP2	0V	GND pin for ch2 PWM signal	
38 39	OUT2N	Vcc～0V	Output pin of ch2 negative PWM signal Please connect to Output LPF.	
40	BSP2N	—	Boot-strap pin of ch2 negative Please connect the capacitor.	
42	BSP1N	—	Boot-strap pin of ch1 negative Please connect the capacitor.	
43 44	OUT1N	Vcc～0V	Output pin of ch1 negative PWM signal Please connect to Output LPF.	
45 46	GNDP1	0V	GND pin for ch1 PWM signal	
47	BSP1P	—	Boot-strap pin of ch1 positive Please connect the capacitor.	
48 49	OUT1P	Vcc～0V	Output pin of ch1 positive PWM signal Please connect to Output LPF.	
51 52	VCCP1	—	Power supply pin for ch1 PWM signal	
29 32 41 50 53	N.C.	—	Non connection pin	—

●RESETX pin function

RESETX (10pin)	State of Digital block
L	Reset ON
H	Reset OFF

●PDX pin,MUTEX pin function

PDX (12pin)	MUTEX (11pin)	Power Down	DAC output (24,25pin)	PWM output (33,34,38,39,43,44,48pin)
L	L or H	ON	HiZ_Low	HiZ_Low
H	L	OFF	Normal operation	
H	H			Normal operation

●Input digital audio sampling frequency (fs) explanation

PWM sampling frequency, Soft-start, Soft-mute time, and the detection time of the DC voltage protection in the speaker depends on sampling frequency (fs) of the digital audio input.

Sampling frequency of the Digital audio input (fs)	PWM sampling frequency (fpwm)	Soft-start / Soft-mute time	DC voltage protection in the speaker detection time
32kHz	512kHz	64msec.	64msec.
44.1kHz	705.6kHz	46msec.	46msec.
48kHz	768kHz	43msec.	43msec.

●For voltage gain (Gain setting)

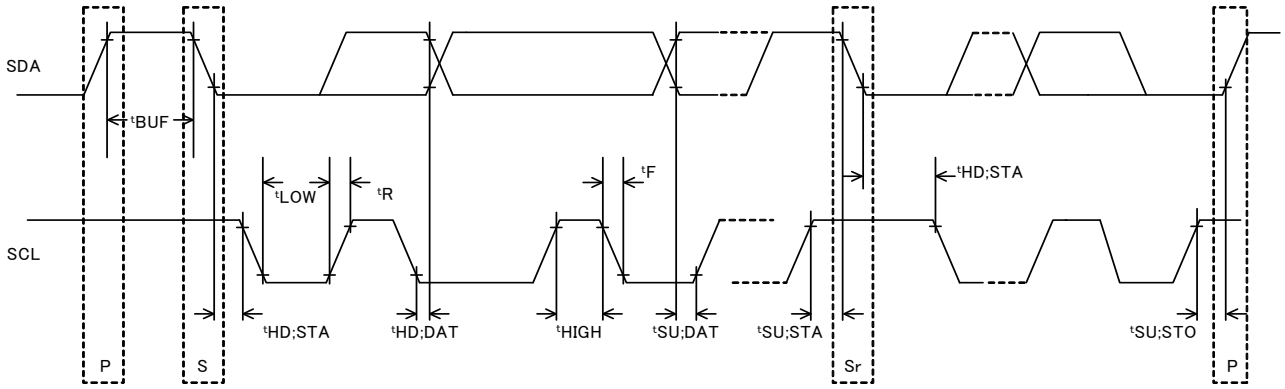
BM5446EFV prescribe voltage gain at speaker output (BTL output) under the definition 0dBV (1Vrms) as full scale input of the digital audio input signal. For example, digital audio input signal = Full scale input, Gain setting = 20dB, Load resistance R_{L_SP}= 8Ω will give speaker output (BTL output) amplitude as 10Vrms. (Output power Po = Vo^2/R_{L_SP}=12.5W)

●Speaker output

DSP output signal SDATAO1 will be output to the speaker. (SDATAO2 will not be output to the speaker. DAC output can be selected either from DSP output signal SDATAO1 or SDATAO2.)

●I²C Bus control signal specification

1) Electrical characteristics and Timing of Bus line and I/O stage



SDA and SCL bus line characteristics(Unless otherwise specified Ta=25℃, V_{CC}=13V)

	Parameter	Symbol	High speed mode		Unit
			Min.	Max.	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between ”Stop” condition and ”Start” condition	tBUF	1.3	-	µs
3	Hold-time of (sending again)”Start” condition. After this period the first clock pulse is generated.	tHD;STA	0.6	-	µs
4	SCL clock’s LOW state Hold-time	tLOW	1.3	-	µs
5	SCL clock’s HIGH state Hold-time	tHIGH	0.6	-	µs
6	Set-up time of sending again ”Start” condition	tSU;STA	0.6	-	µs
7	Data hold time	tHD;DAT	0 *1	-	µs
8	Data set-up time *2	tSU;DAT	500/250/150	-	ns
9	Rise-time of SDA and SCL signal	tR	20+Cb	300	ns
10	Fall-time of SDA and SCL signal	tF	20+Cb	300	ns
11	Set-up time of ”Stop” condition	tSU;STO	0.6	-	µs
12	Capacitive load of each bus line	Cb	-	400	pF

The above-mentioned numerical values are all the values corresponding to VIH min and the VIL max level.

*1 To exceed an undefined area on the fall-edge of SCL (VIH min of the SCL signal), the transmitting set should internally offer the holding time of 300ns or more for the SDA signal.

*2 The data set-up time is different according to the setting of SYS_CLK.
When SYS_CLK=128fs it is 500ns, for SYS_CLK=256fs it is 250ns, for SYS_CLK=512fs it will be 150ns.

*3 SCL and SDA pin is not corresponding to threshold tolerance of 5V.
Please use it within 4.5V of the absolute maximum rating.

2) Command interface

I²C Bus control is used for command interface between host CPU. It not only writes but also it is possible to read it excluding a part of register. In addition to “Slave Address “ , set and write 1 byte of “Select Address “ to read out the data. I²C bus Slave mode format is illustrated below.

MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

S : Start Condition

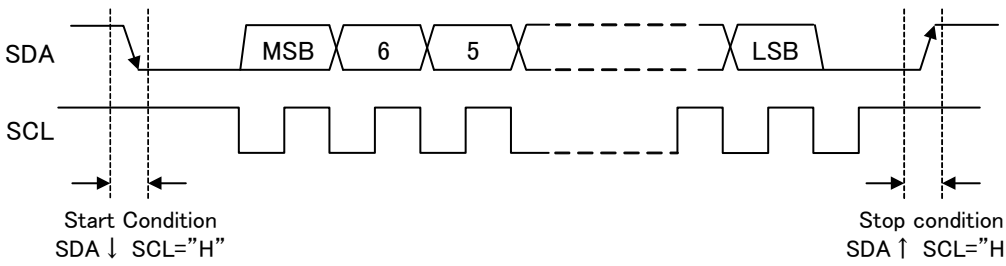
Slave Address : The data of eight bits in total is sent putting up bit of Read mode (H) or Write mode (L) after slave address (7bit) set with the terminal ADDR. (MSB first)

A : The acknowledge bit adds to data that the acknowledge is sent and received in each byte.
When data is correctly sent and received,“L”is sent and received.
There was no acknowledgement for “H”.

Select Address : The select address in one byte is used.(MSB first)

Data : Data byte is sent and received data(MSB first)

P : Stop Condition



3) Slave Address

・While ADDR pin (22pin) is“L”

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	1/0

・While ADDR pin (22pin) is“H”

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	1/0

4) Writing of data

・Basic format

S	Slave Address	A	Select Address	A	Data	A	P

: Master to Slave, : Slave to Master

・Auto-increment format

S	Slave Address	A	Select Address	A	Data 1	A	Data 2	A	Data 3…N	A	P

: Master to Slave, : Slave to Master

5)Reading of data

First of all, the address (20h in the example) for reading is written in the register of the D0h address at the time of reading. In the following stream, data is read after the slave address. Please do not return the acknowledge when you end the reception.

S	Slave Address	A	Req_Addr	A	Select Address	A	P
(ex.)	80h		D0h		20h		

S	Slave Address	A	Data 1	A	Data 2	A		A	Data N	Ā	P
(ex.)	81h		**h		**h				**h		

: Master to Slave, : Slave to Master, A : With Acknowledge, Ā : Without Acknowledge

6) Instruction Code Chart (Select Address)

MSB \ LSB		0	1	2	3	4	5	6	7
0	I/O Setting CLK Setting		RAM Clear		Input SEL S-P2,S-P1	Output SEL P-S2,P-S1	SPDIFO Output SEL		
1	SPDIF	MUTE Setting	SPDIF OUT Setting1	SPDIF OUT Setting2	SPDIF OUT				
2	DSP Volume	PRE Scaler Setting	DC Cut HPF	CH Mixer1 DSP	CH Mixer2 DF2, DF1	Scaler1 Setting	Scaler2 Setting	Main Volume Setting	Main Balance Setting
3	Sub Clipper P^2Volume	Sub Clipper ON/OFF	Sub Clipper Setting1	Sub Clipper Setting2	P^2V Setting1	P^2V_MIN	P^2V_MAX	P^2V_K	P^2V_OFS
4	DSP TONE	BASS Control	BASS Frequency	BASS Quality factor	BASS Gain	MIDDLE Control	MIDDLE Frequency	MIDDLE Quality factor	MIDDLE Gain
5	DSP 7BandP-EQ	7Band1 Control	7Band1 Frequency	7Band1 Quality factor	7Band1 Gain	7Band2 Control	7Band2 Frequency	7Band2 Quality factor	7Band2 Gain
6	DSP 7BandP-EQ	7Band5 Control	7Band5 Frequency	7Band5 Quality factor	7Band5 Gain	7Band6 Control	7Band6 Frequency	7Band6 Quality factor	7Band6 Gain
7	DSP Sound Effect	Surround Setting	Pseudo Stereo	P^2Bass Setting1	P^2Bass Setting2	P^2Bass Setting3	P^2Treble Setting1	P^2Treble Setting2	P^2Bass Soft_T Start
8	DSP 3BandP-EQ	3Band1 Control	3Band1 Frequency	3Band1 Quality factor	3Band1 Gain	3Band2 Control	3Band2 Frequency	3Band2 Quality factor	3Band2 Gain
9									
A	PLLA	PLLA Setting1						Sync Detect1	Sync Detect2
B	Power Stage	Power Stage Gain	Power Stage Test1	Power Stage Test2	Power Stage Test3	Power Stage Test4	Power Stage Test5	Power Stage Test6	Power Stage Test7
C									
D	Read Base Address	Read Base Address							
E									
F	TEST Mode	PU Setting	Initial Setting TEST Mode1	TEST Mode2	MCLK DIV Setting	PLLA Initial Setting1	PLLA Initial Setting2	PLLA Initial Setting3	PLLA Initial Setting4

MSB \ LSB		8	9	A	B	C	D	E	F
0	I/O Setting CLK Setting	SYSCLK SEL1 DSP			I^2S Format1 S-P1	I^2S Format2 S-P2	I^2S Format3 P-S1	I^2S Format4 P-S2	
1	SPDIF								
2	DSP Volume	Main Post Scalar Setting	Main Clipper ON/OFF	Main Clipper Setting1	Main Clipper Setting2	Sub Volume Setting	Sub Balance Setting	Sub Post Scalar Setting	Sub Input Selector
3	P^2Volume	A_RATE R_RATE	A_TIME R_TIME	A_RATE_Low R_RATE_Low	AR_TIME_ Low	Pulse Sound Setting1			
4	DSP TONE	TREBLE Control	TREBLE Frequency	TREBLE Quality factor	TREBLE Gain	TONE Control Soft_T Start			
5	DSP 7Band P-EQ	7Band3 Control	7Band3 Frequency	7Band3 Quality factor	7Band3 Gain	7Band4 Control	7Band4 Frequency	7Band4 Quality factor	7Band4 Gain
6	DSP 7Band P-EQ	7Band7 Control	7Band7 Frequency	7Band7 Quality factor	7Band7 Gain		CRAM Auto Over Write	CRAM Auto Setting1	CRAM Auto Setting2
7	DSP Sound Effect	P^2Treble Soft_T Start		Sub Woofer LPF Setting					
8	DSP 3BandP-EQ	3Band3 Control	3Band3 Frequency	3Band3 Quality factor	3Band3 Gain	P-EQ Setting1	P-EQ Setting2	P-EQ Setting3	P-EQ Setting4
9									
A	PLLA	Sync Detect3	Sync Detect4						
B	Power Stage	C2D speed	Refresh	Test8					
C									
D	Read Base Address								
E									
F	TEST Mode	RAM Test Setting1	RAM Test Setting2	RAM Test Setting3	RAM Test Setting4	RAM Test Setting5	DSP Mute Set		

●Format of digital audio input

・SYS_CLK: It is System Clock input signal.
It will input LRCLK, BCLK, SDATA1 (SDATA2) that synchronizes with this clock that are 128 times of sampling frequency (128fs), 256 times of sampling frequency (256fs), or 512 times frequency (512fs) of sampling frequency (fs).

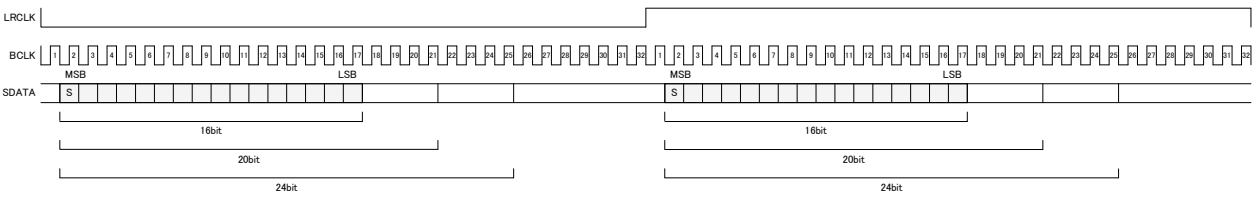
・LRCLK: It is L/R clock input signal.
It corresponds to 32kHz/44.1kHz/48kHz with those clock (fs) that are same to the sampling frequency (fs) .
The audio data of a left channel and a right channel for one sample is input to this section.

・BCLK: It is Bit Clock input signal.
It is used for the latch of data in every one bit by sampling frequency's 48 times frequency (48fs) or 64 times sampling frequency (64fs). However if the 48fs being selected, the input will be Right-justified data format and held static.

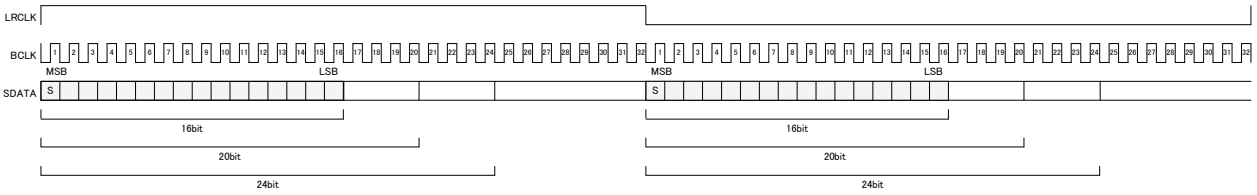
・SDATA1 & SDATA2: It is Data input signal.
It is amplitude data. The data length is different according to the resolution of the input digital data.
It corresponds to 16/ 20/ 24 bit.

The digital input has I2S, Left-justified and Right-justified formats.
The figure below shows the timing chart of each transmission mode.

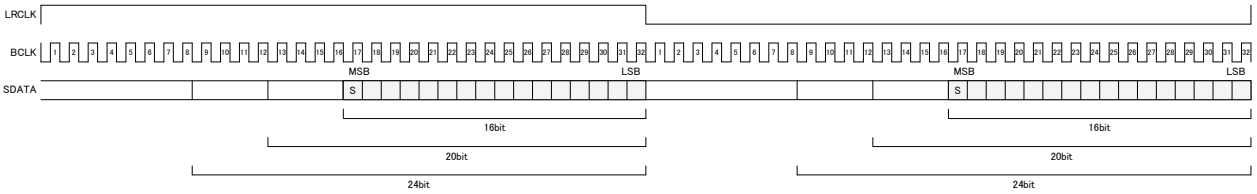
I²S data format



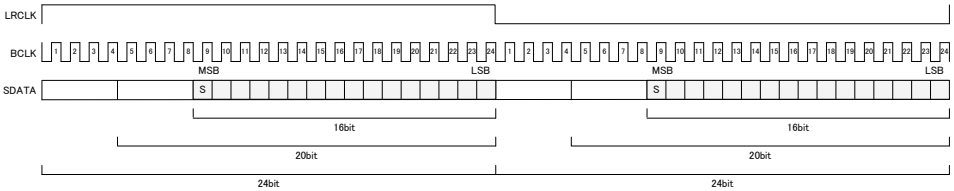
Left-justified data format



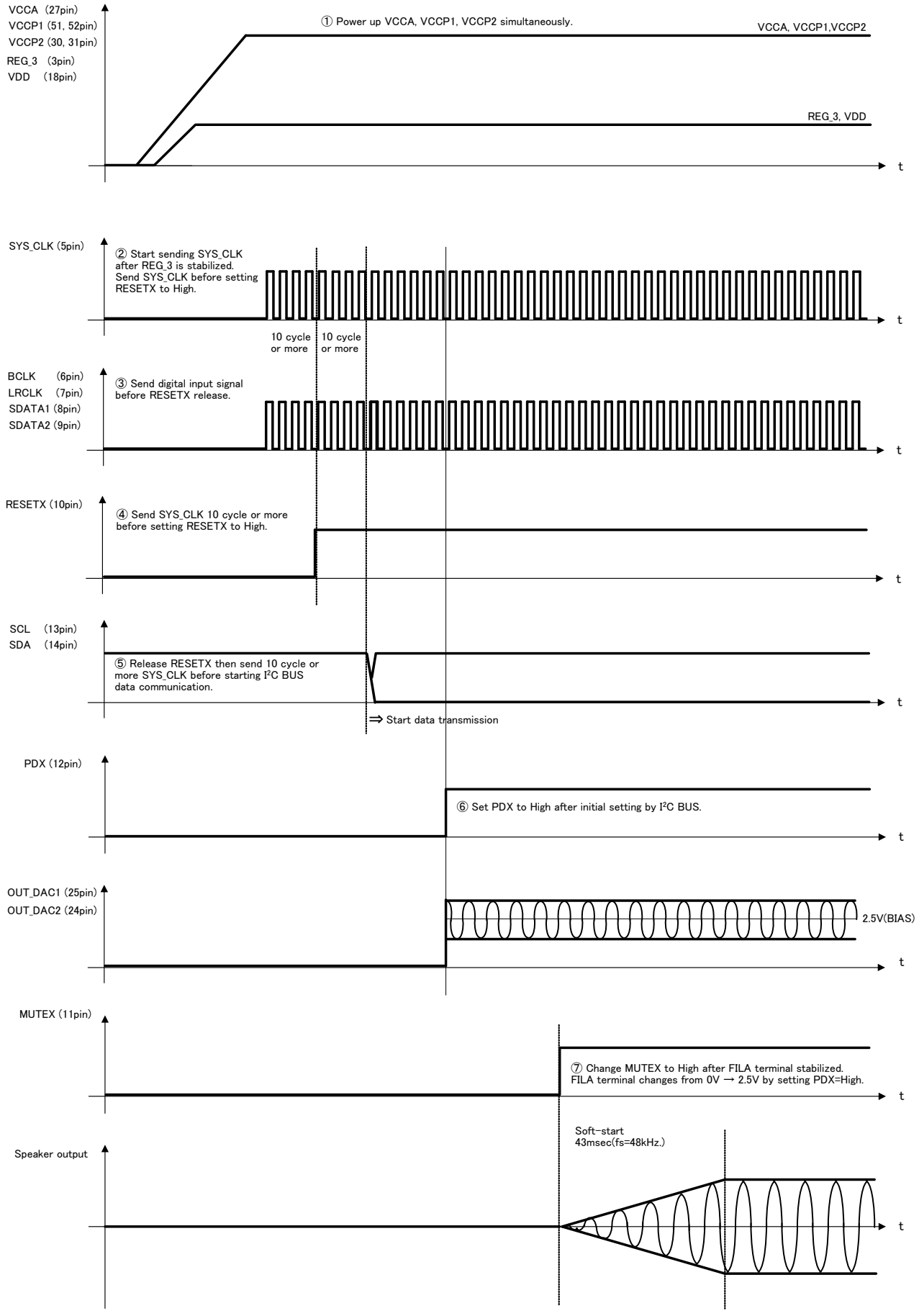
Right-justified data format



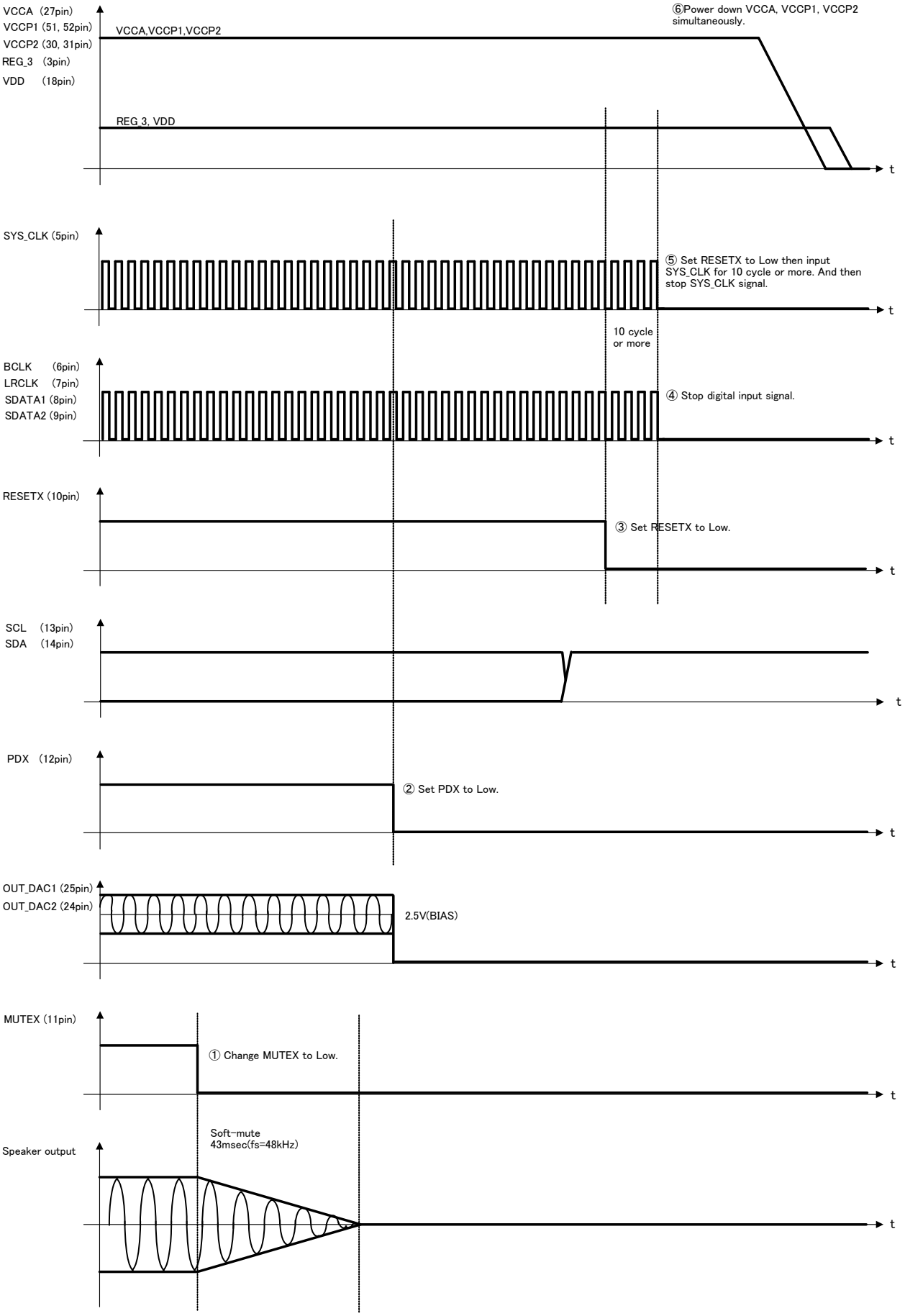
Right-justified data format (48fs)



●Power supply start-up sequence



●Power supply shut-down sequence



●**About the protection function**

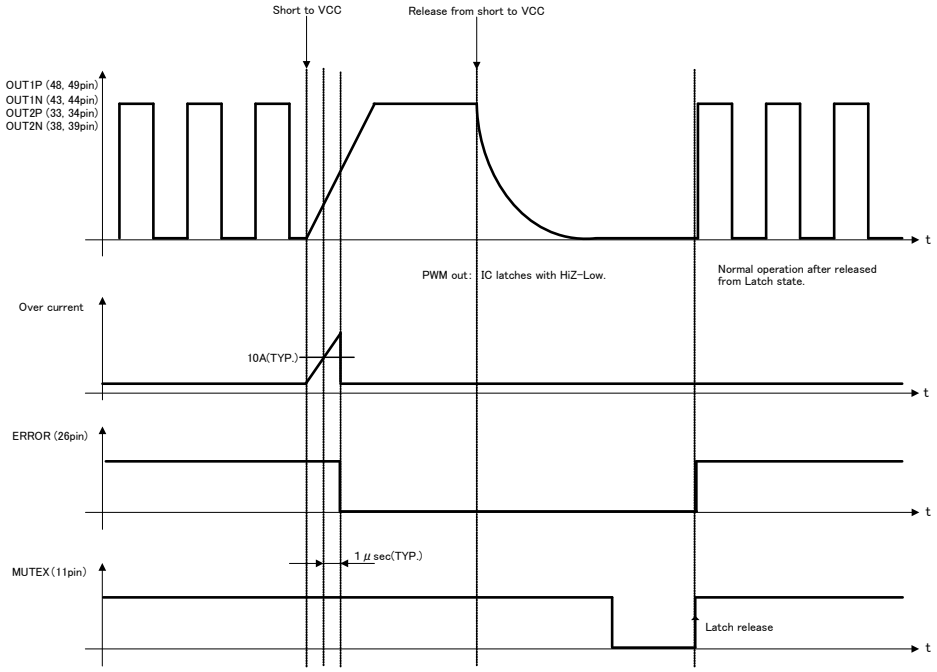
Protection function	Detecting & Releasing condition		DAC Output	PWM Output	ERROR Output
Output short protection	Detecting condition	Detecting current = 10A (TYP.)	Normal operation	HiZ_Low (Latch)	L (Latch)
DC voltage protection in the speaker	Detecting condition	PWM output Duty=0% or 100% 43msec(fs=48kHz) above fixed		HiZ_Low (Latch)	L (Latch)
High temperature protection	Detecting condition	Chip temperature to be above 150℃ (TYP.)	Normal operation	HiZ_Low	H
	Releasing condition	Chip temperature to be below 120℃ (TYP.)		Normal operation	
Under voltage protection	Detecting condition	Power supply voltage to be below 8V (TYP.)	Normal operation	HiZ_Low	H
	Releasing condition	Power supply voltage to be above 9V (TYP.)		Normal operation	
Clock stop protection	Detecting condition	No change to SYS_CLK more than 1usec (TYP.)	Irregular output	HiZ_Low	H
	Releasing condition	Input to SYS_CLK	Normal operation	Normal operation	

1) Output short protection(Short to the power supply)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTE pin is set High and the current that flows in the PWM output pin becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After the MUTEX pin is set Low once, the MUTEX pin is set High again.
②Turning on the power supply again.

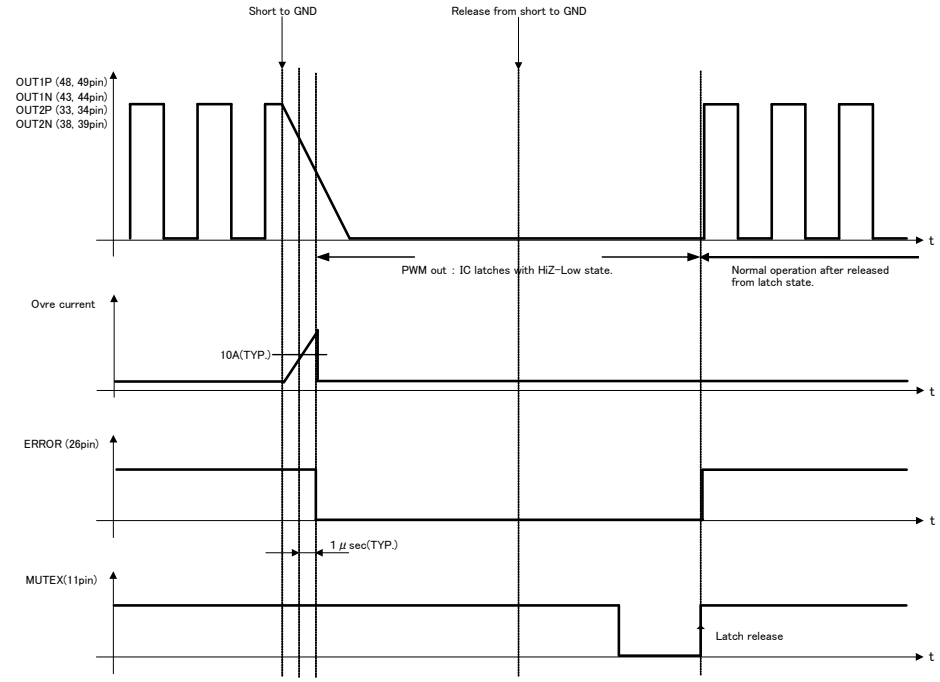


2) Output short protection(Short to GND)

BM5446EFV has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTE pin is set High and the current that flows in the PWM output terminal becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method – ①After the MUTEX pin is set Low once, the MUTEX pin is set High again.
②Turning on the power supply again.

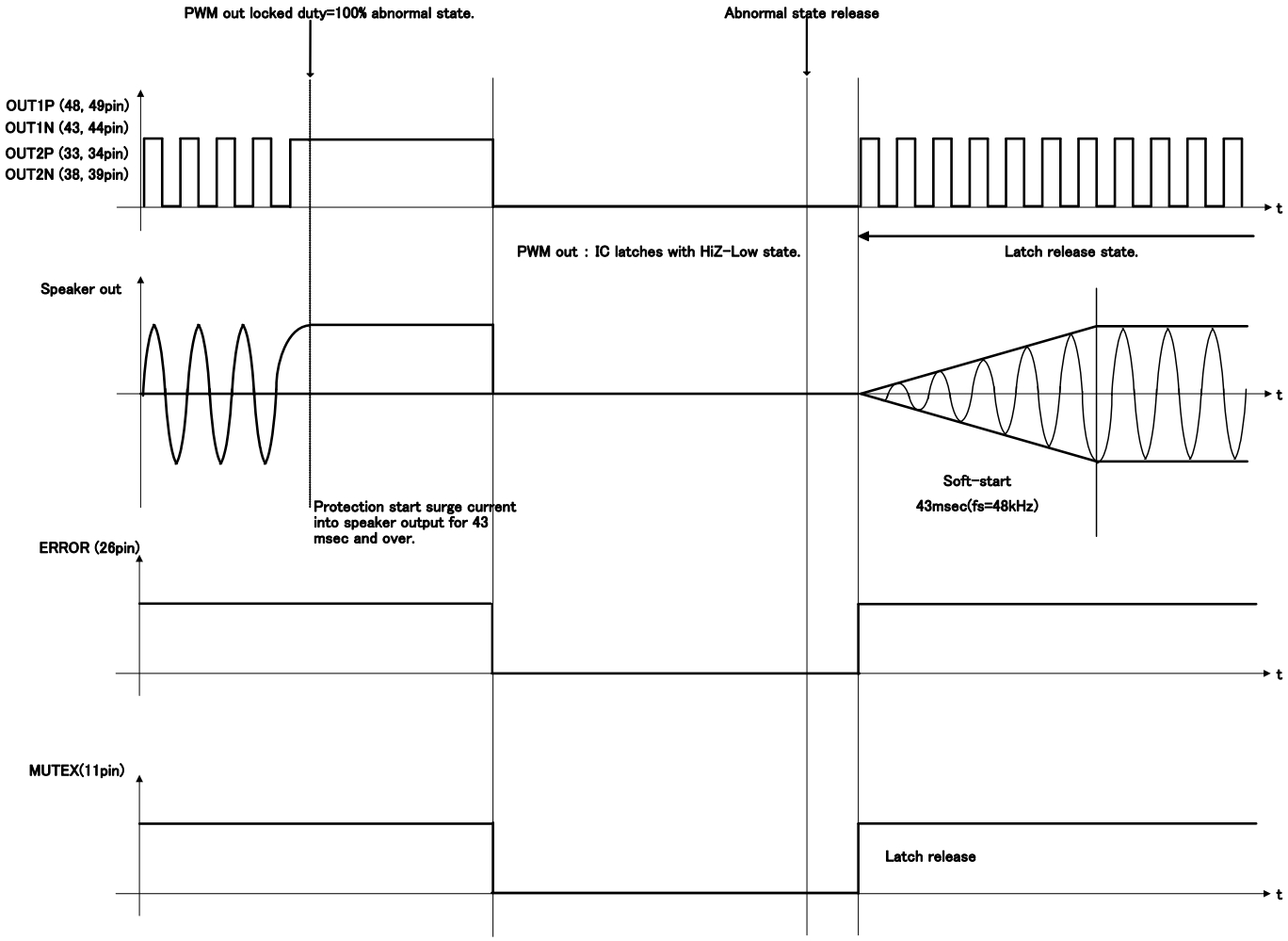


3) DC voltage protection in the speaker

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTE pin is set High and PWM output Duty=0% or 100% , 43msec(fs=48kHz) or above. Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method – ①After the MUTEX pin is set Low once, the MUTEX pin is set High again.
②Turning on the power supply again

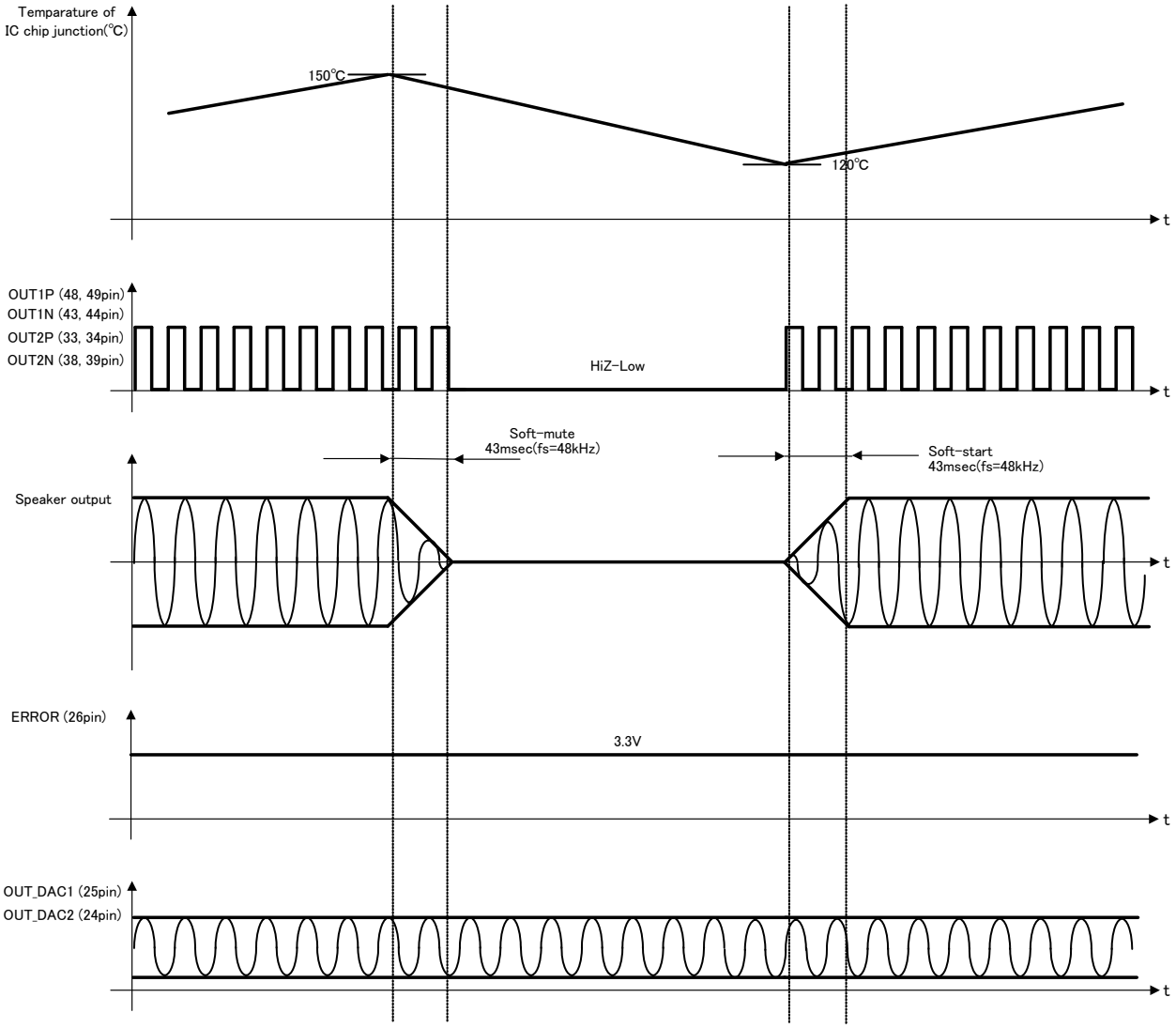


4) High temperature protection

BM5446EFV has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed Tjmax=150℃.

Detecting condition - It will detect when MUTE pin is set High and the temperature of the chip becomes 150℃(TYP.) or more. The speaker output is muted through a soft-mute when detected.

Releasing condition - It will release when MUTE pin is set High and the temperature of the chip becomes 120℃(TYP.) or less. The speaker output is outputted through a soft-start when released.

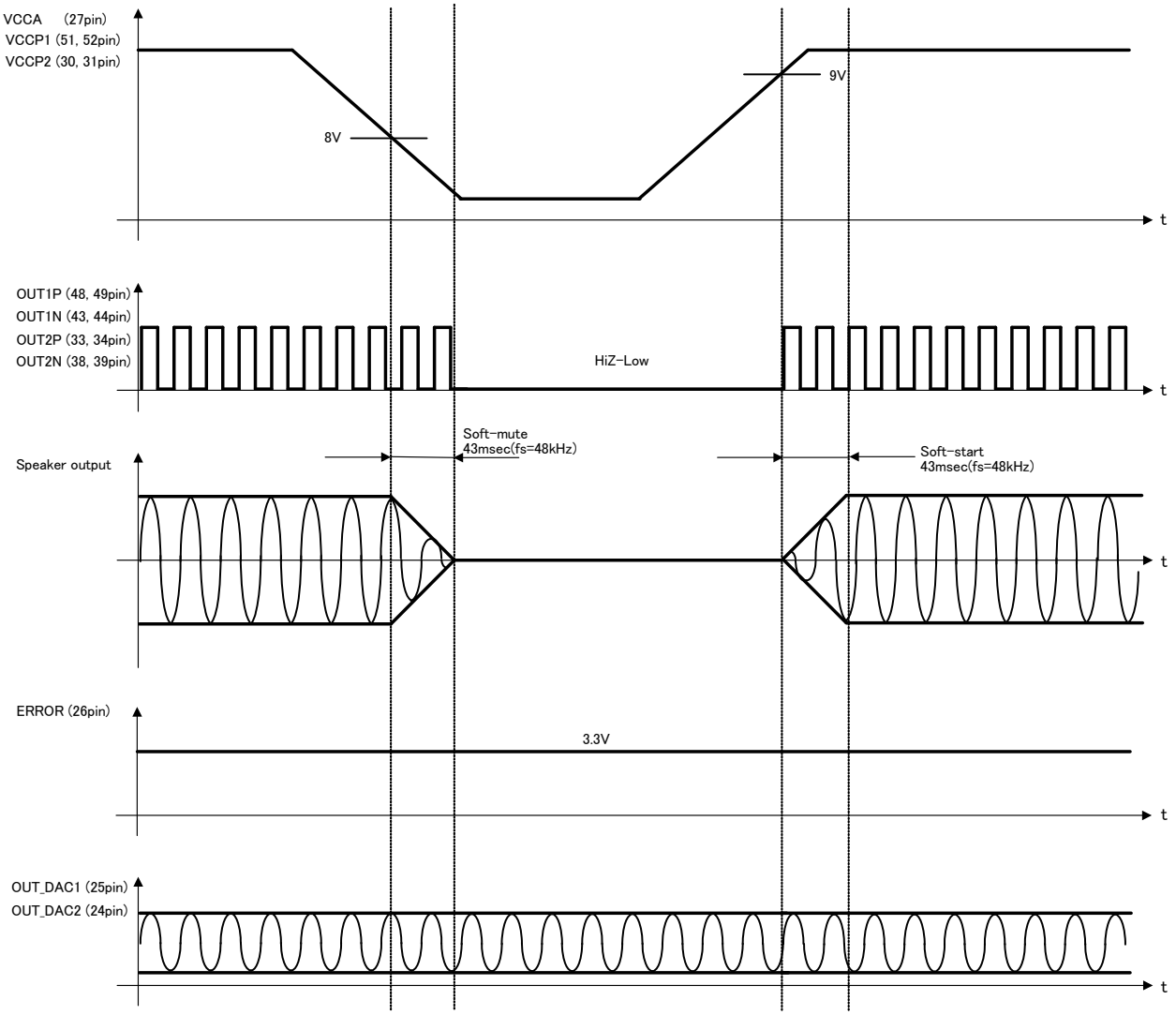


5) Under voltage protection

BM5446EFV has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTE pin is set High and the power supply voltage becomes lower than 8V. The speaker output is muted through a soft-mute when detected.

Releasing condition – It will release when MUTE pin is set High and the power supply voltage becomes more than 9V. The speaker output is outputted through a soft-start when released.

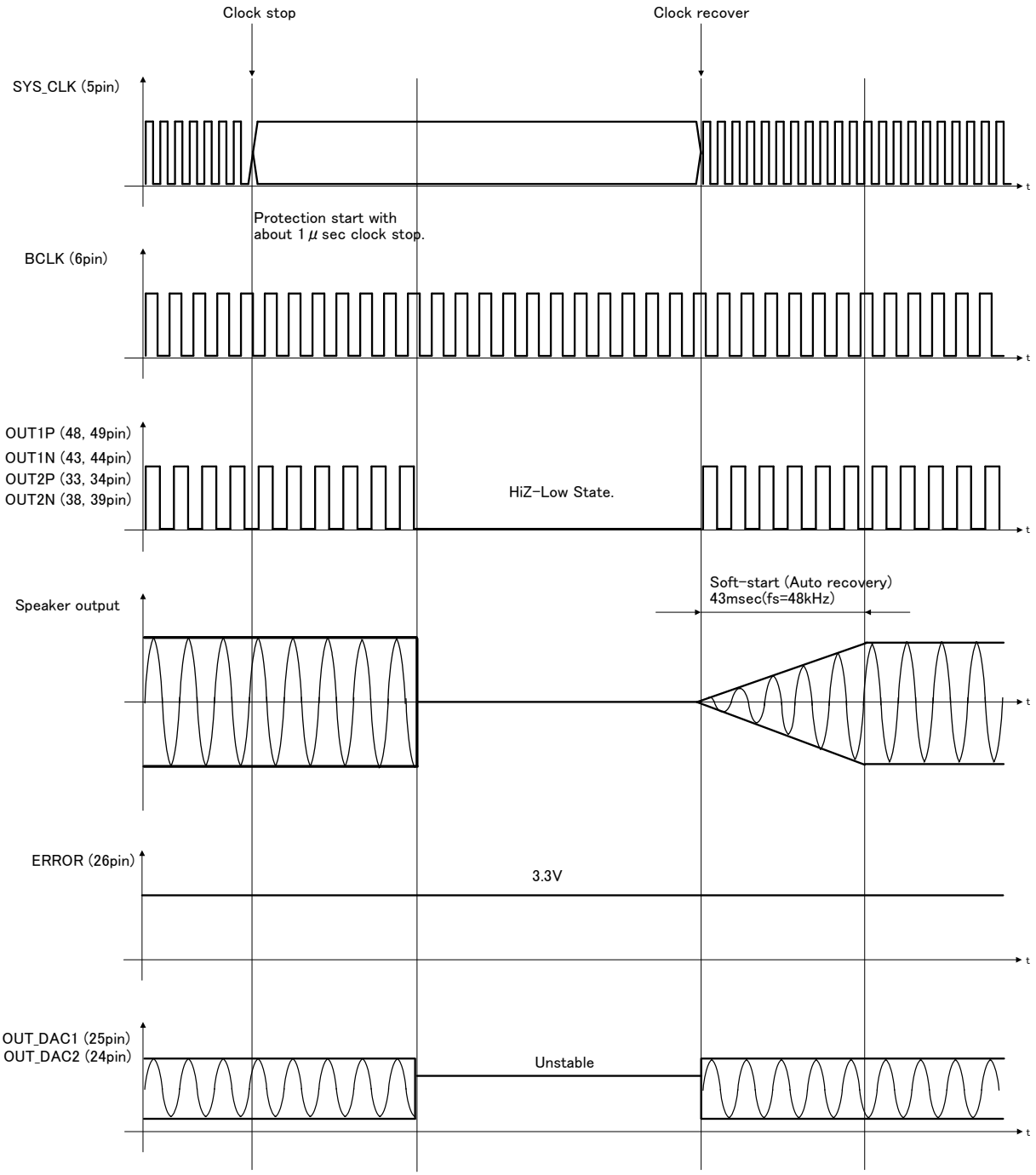


6) Clock stop protection

BM5446EFV has the clock stop protection circuit that make the speaker output mute when the SYS_CLK signal of the digital audio input stops.

Detecting condition - It will detect when MUTE pin is set High and the SYS_CLK signal doesn't change for about 1usec or more. The speaker output is muted through a soft-mute when detected.

Releasing condition - It will release when MUTE pin is set High and the SYS_CLK signal returns to the normal clock operation. The speaker output is outputted through a soft-start when released.



●Application Circuit Example (R_{L_SP}=8Ω)