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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Middle Power Class-D Speaker Amplifier

25W+25W
Full Digital Speaker Amplifier with built-in DSP

BM5449MWV

●General Description

BM5449MWV is a Full Digital Speaker Amplifier with built-in DSP (Digital Sound Processor) designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 25W+25W. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency of 90% (10W+10W output with 8Ω load). In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

●Features

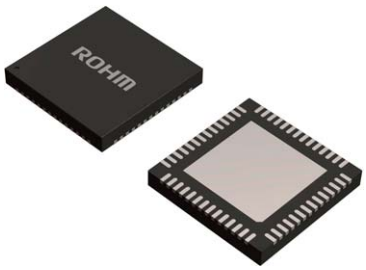
- With wide range of power supply voltage. (V_{CC}=10 to 26V)
- This IC includes the DSP (digital sound processor) for Audio signal processing for Flat TVs.
  Synchronous SRC, Surround, 8 Band EQ, 1 Band EQ (for Sub), Volume, 2 Band DRC, Delay RAM for phase revised Close Over Filter, 512 Taps FIR Filter, P^2Volume, P^2Base+, Higher Sound Complement (High Generator), Soft Clipper, Hard Clipper
- This IC has two inputs systems of digital audio interface.
  I^2S / LJ / RJ format, LRCLK: 8 to 192 kHz, BCLK: 32fs / 48fs / 64fs, SDATA: 16 / 20 / 24bits
  BCLK: 32fs / 48fs / 64fs, SDATA: 16 / 20 / 24bits
- Two Digital Audio Output for Audio DAC and headphone.
- One PWM Output for Subwoofer.
- The sound quality decrease by the power supply variation is prevented with the output feedback circuit. In addition, a low noise and a low distortion are achieved. Mass electrolytic capacitor is unnecessary because it is strong in the power supply variation.
- It contributes to miniaturizing, making to the thin type, and the power saving of the system by highly effective (10W+10W output and 8Ω on-load) 90% and low generation of heat.
- Low current at the Power down Mode.
- The pop noise at power supply on/off is prevented, and a more high-quality soft mute function is built into. Highly reliable design with built-in various protection functions.
- The component side product can be decreased because of small package (UQFN056V7070).
- The maximum output in the stereo is 25W+25W (VCC=20.5V, 8Ω load).
- The maximum output in the monaural(PBTL) is 50W(VCC=20.5V, 4Ω load)

●Key Specifications

- Supply voltage (VCC): 10V to 26V
- Speaker output power (VCC=18V, RL=8Ω): 20W+20W(Typ.)
- THD+N: 0.05 %(Typ.)

●Package

	W (Typ.) x D (Typ.) x H(Max.)
UQFN056V7070	7.00mm x 7.00mm x 1.00mm



●Applications

- Flat Panel TVs(LCD, Plasma)
- Home Audio
- Amusement equipments
- Electronic Music equipments etc.

●Typical Application Circuit

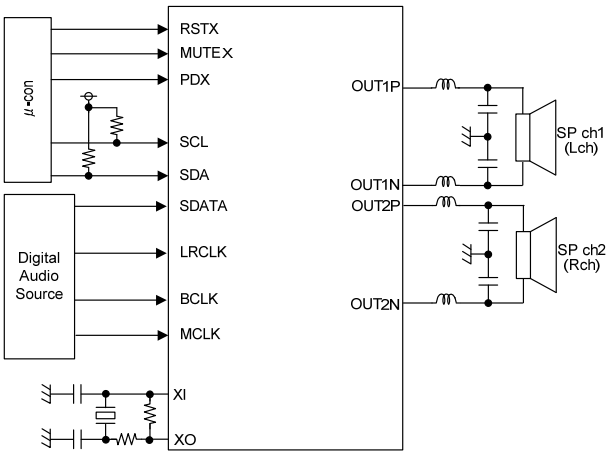


Figure 1. Typical application circuit

●Pin Configuration

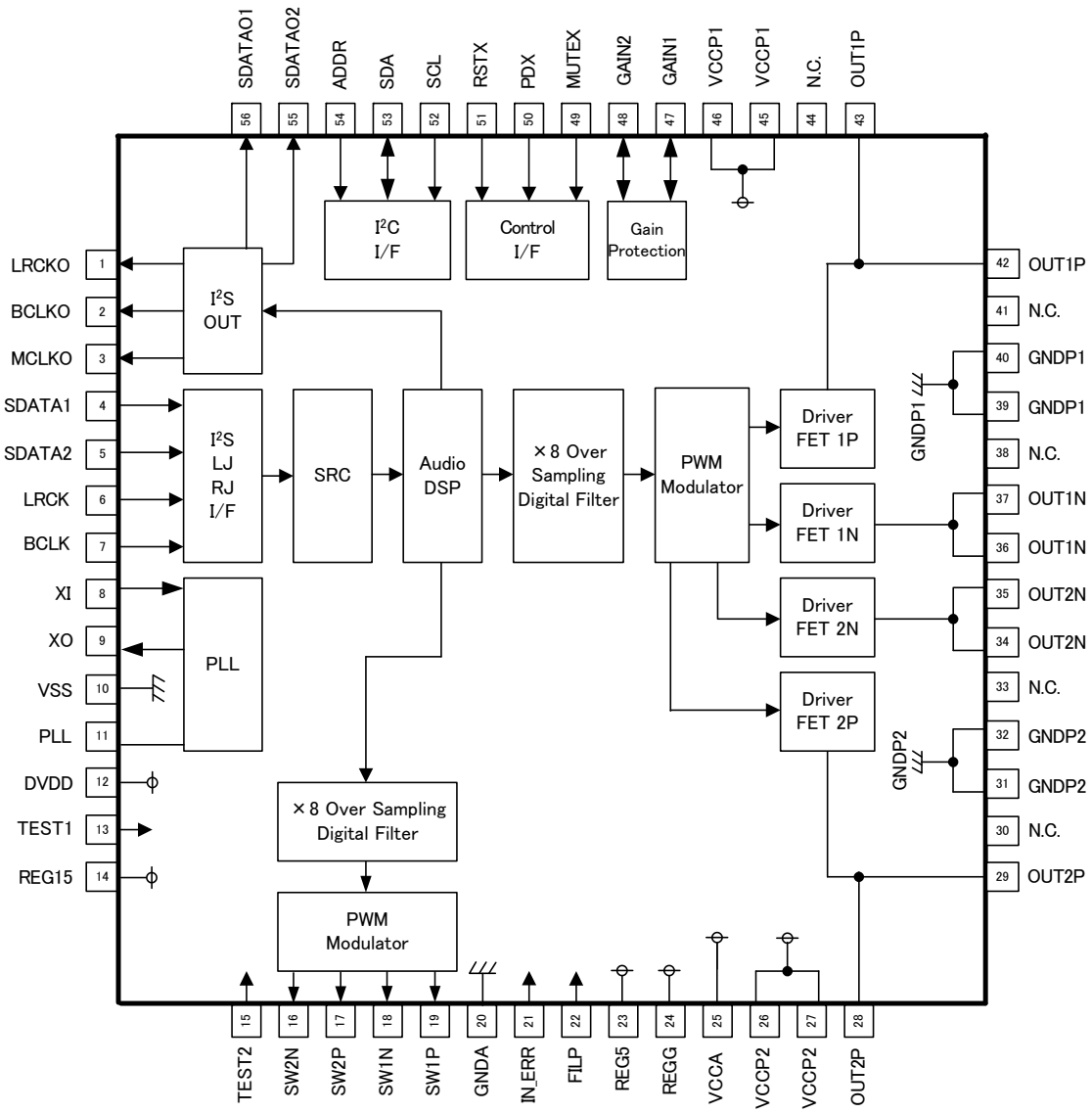


Figure 2. Pin configuration (Top View)

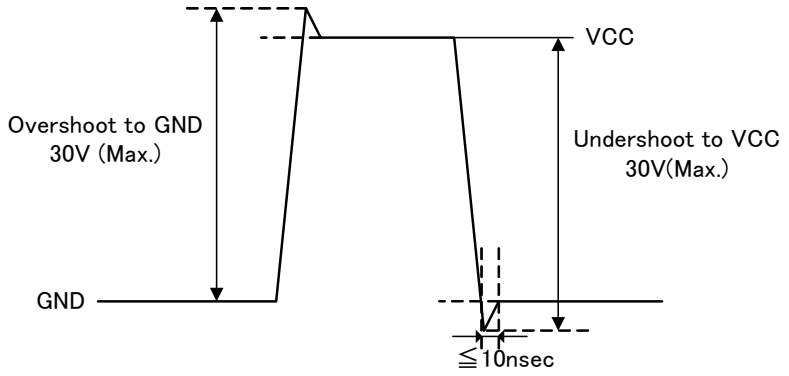
●Pin Description

No.	Name	I/O	No.	Name	I/O	No.	Name	I/O	No.	Name	I/O
1	LRCKO	I/O	15	TEST2	I	29	OUT2P	O	43	OUT1P	O
2	BCLKO	I/O	16	SW2N	O	30	N.C.	-	44	N.C.	-
3	MCLKO	I/O	17	SW2P	O	31	GNDP2	-	45	VCCP1	-
4	SDATA1	I	18	SW1N	O	32	GNDP2	-	46	VCCP1	-
5	SDATA2	I	19	SW1P	O	33	N.C.	-	47	GAIN1	I/O
6	LRCK	I	20	GNDA	-	34	OUT2N	O	48	GAIN2	I/O
7	BCLK	I	21	IN_ERR	I	35	OUT2N	O	49	MUTEX	I
8	XI	I	22	FILP	O	36	OUT1N	O	50	PDX	I
9	XO	O	23	REG5	O	37	OUT1N	O	51	RSTX	I
10	VSS	-	24	REGG	O	38	N.C.	-	52	SCL	I
11	PLL	O	25	VCCA	-	39	GNDP1	-	53	SDA	I/O
12	DVDD	-	26	VCCP2	-	40	GNDP1	-	54	ADDR	I
13	TEST1	I	27	VCCP2	-	41	N.C.	-	55	SDATAO2	I/O
14	REG15	O	28	OUT2P	O	42	OUT1P	O	56	SDATAO1	I/O

●Absolute Maximum Ratings(Ta=25℃)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	V_{CC}	-0.3 to 30	V	Pin 25, 26, 27, 45, 46 *1 *2
	V_{DD}	-0.3 to 4.5		Pin 12 *1 *2
Power dissipation	Pd	4.29	W	*3
		4.83		*4
Input voltage	V_{IN}	-0.3 to 4.5	V	Pin 4 to 8, 13, 15, 49to54 *1
Terminal voltage1	V_{PIN1}	-0.3 to 4.5	V	Pin 1 to 3, 9, 16to19, 47, 48, 55, 56 *1
Terminal voltage 2	V_{PIN2}	-0.3 to 7.0	V	Pin 22 to 24 *1
Terminal voltage 3	V_{PIN3}	-0.3 to 30	V	Pin 28, 29, 34 to 37, 42, 43 *1 *5
Operating temperature range	T_{opr}	-25 to +85	℃	
Storage temperature range	T_{stg}	-55 to +150	℃	
Maximum junction temperature	T_{jmax}	+150	℃	

*1 The voltage that can be applied reference to GND(Pin 10, 20, 31, 32, 39, 40)
*2 Do not, however exceed Pd and Tjmax=150℃.
*3 74.2mm×74.2mm×1.6mm FR4, 4-layer glass epoxy board (Top and bottom layer back copper foil size : 34.09mm^2, 2nd, 3rd layer back copper foil size:5505mm^2)
Derating in done at 34.3 mW/℃ for operating above Ta＝25℃. There are thermal via on the board.
*4 74.2mm×74.2mm×1.6mm F FR4, 4-layer glass epoxy board (Copper area 5505mm2)
Derating in done at 38.6 mW/℃ for operating above Ta＝25℃. There are thermal via on the board.
*5 It should use it below this ratings limit including the AC peak waveform (overshoot) for all conditions.
At only undershoot, it is admitted using at ≦10nse and ≦30V by the VCC reference. (Please refer following figure.)



●RecommendedOperating Ratings (Ta=25℃)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	V_{CC}	10 to 26	V	Pin 25, 26, 27, 45, 46 *1 *2
	V_{DD}	3.0 to 3.6		Pin 12 *1 *2
Minimum load impedance	R_L	3.6	Ω	Vcc≦18V, Stereo BTL mode *6
				Monaural Parallel BTL mode *6
		5.4	Ω	Vcc≦26V, Stereo BTL mode *6

*6 Do not, however exceed Pd.

●Electrical characteristics

(Unless otherwise specified Ta=25℃, Vcc=18V, V_{DD}=3.3V, fin=1kHz, R_L=8Ω, RSTX=3.3V, PDX=3.3V, MUTEX=3.3V
fs= 48kHz, GAIN=20dB, DSP : Through, Output LC filter : L=22μH, C=0.33μF, Cg=0.068μF)

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Total circuit						
Circuit current (Power down mode)	I_{CC1}	-	0.1	0.2	mA	Pin 25, 26, 27, 45, 46 No load RSTX=3.3V, PDX=0V, MUTEX=0V
	I_{DD1}	-	3.7	7.5		Pin 12, Noload RSTX=3.3V, PDX=0V, MUTEX=0V
Circuit current (mute mode)	I_{CC2}	-	7.0	25	mA	Pin 25, 26, 27, 45, 46 No load RSTX=3.3V, PDX=3.3V, MUTEX=0V
	I_{DD2}	-	25	70		Pin 12 Noload RSTX=3.3V, PDX=3.3V, MUTEX=0V
Circuit current (Normal mode)	I_{CC3}	-	50	80	mA	Pin 25, 26, 27, 45, 46 No load RSTX=3.3V, PDX=3.3V, MUTEX=3.3V
	I_{DD3}	-	30	70		Pin 12 Noload RSTX=3.3V, PDX=3.3V, MUTEX=3.3V
Regulator output voltage	V_{REG15}	1.3	1.5	1.7	V	Pin 14
	V_{REG5}	4.7	5.0	5.3		Pin 23
	V_{REGG}	4.7	5.0	5.3		Pin 24
ERROR WARNING terminal L level voltage	V_{ERR}	-	0.4	0.8	V	Pin 47, 48, I_O=0.1mA
H level input voltage	V_{IH}	V_{DD} x0.8	-	-	V	Pin 4 to 7, 13, 15, 21, 49 to 54
L level input voltage	V_{IL}	-	-	V_{DD} x0.2	V	Pin 4 to 7, 13, 15, 21, 49 to 54
Input current (Input pull-up terminal)	I_{IL}	50	100	150	μA	Pin 4 to 7, VIN = 0V
Input current(Input pull-down terminal)	I_{IH}	30	70	105	μA	Pin 49 to 51, 54, VIN = 3.3V
Input current(SCL, SDA terminal)	I_I	-	0	1	μA	Pin 52, 53, VIN = 3.3V
Input current (SCL, SDA terminal)	I_O	-1	0	-	μA	Pin 52, 53, VIN = 0V
Digital Audio Signal Output H level voltage 1	V_{OH1}	V_{DD} -0.5	-	V_{DD}	V	Pin 1 to 3,55,56, Io=1mA
PWM for Subwoofer Output H level voltage 2	V_{OH2}	V_{DD} -0.5	-	V_{DD}	V	Pin 16 to 19, Io=1mA
Digital Audio Signal Output L level voltage 1	V_{OL1}	0	-	0.5	V	Pin 1 to 3,55,56, Io=1mA
PWM for Subwoofer Output L level voltage 2	V_{OL2}	0	-	0.5	V	Pin 16 to 19, Io=1mA

Speaker output						
Maximum output	P_{O1}	-	10	-	W	Vcc=13V, THD+n=10%, Gain=20dB *7
	P_{O2}	-	20	-	W	Vcc=18V, THD+n=10%, Gain=22dB *7
	P_{O3}	-	25	-	W	Vcc=20.5V、THD+n=10%、Gain=23dB*7
Total harmonic distortion	THD	-	0.05	-	%	P_O=1W, BW=20 to 20kHz *7
Crosstalk	CT	60	80	-	dB	P_O=1W, BW=IHF-A *7
PSRR	PSRR	-	70	-	dB	Vripple=1Vrms, f=1KHz *7
Output noise voltage	V_{NO}	-	80	140	μVrms	-∞dBFS, BW=IHF-A *7
PWM sampling frequency	f_{PWM1}	-	384	-	KHz	fs=8kHz, 16kHz, 32kHz *7
	f_{PWM2}	-	352.8	-		fs=11.025kHz, 22.05kHz, 44.1kHz, 88.2kHz *7
	f_{PWM3}	-	384	-		fs=12kHz, 24kHz, 48kHz, 96kHz *7

*7 These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

●Typical Performance Curves

(Ta=25℃,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=8Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=23dB,DSP through)
Measured by ROHM designed 4-layer board.

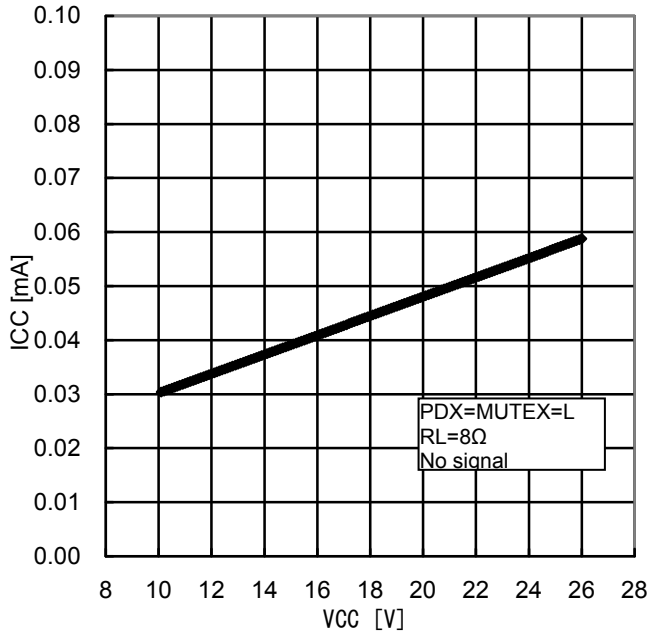


Figure 3.
. Power supply – Current consumption

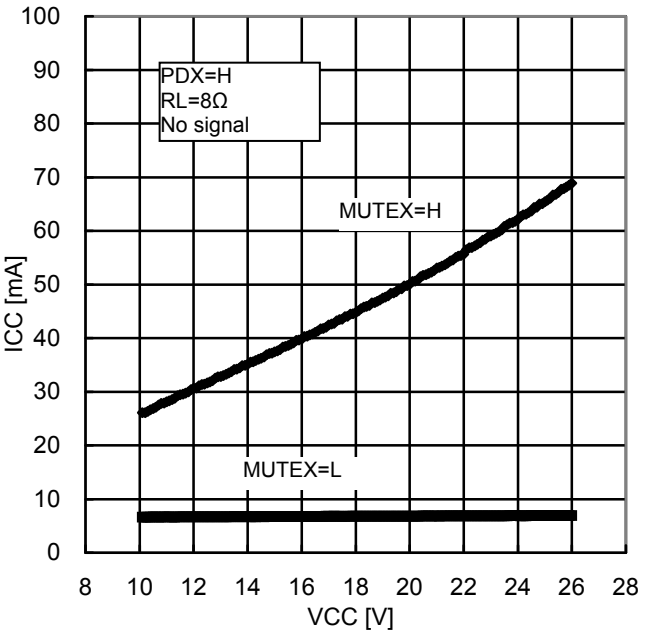


Figure 4.
. Power supply – Current consumption

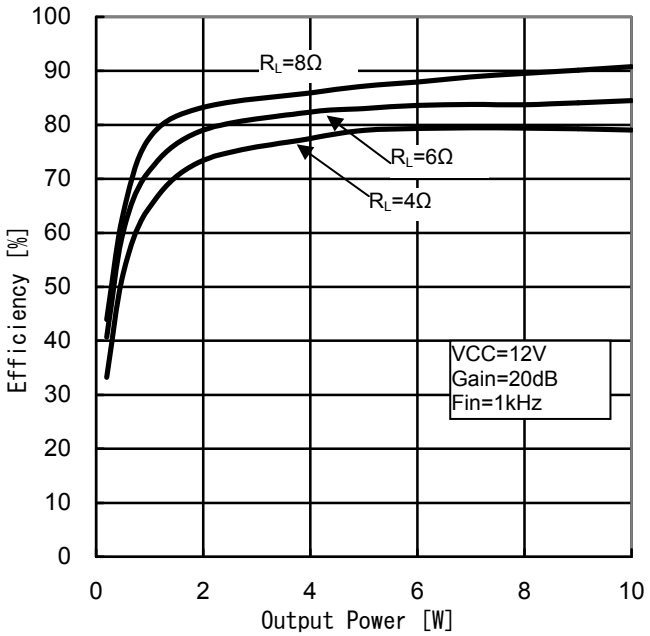


Figure 5.
. Output power – Efficiency

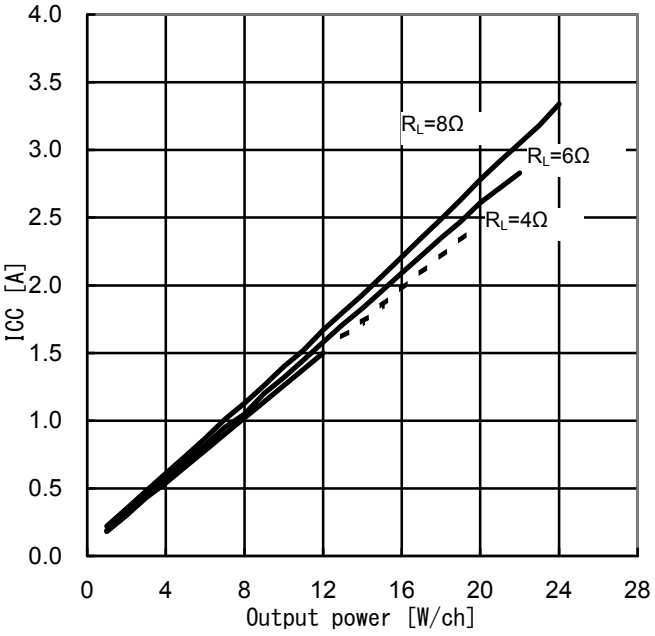


Figure 6.
. Output power – Current consumption

Continued on next page.

※Dotted line means internal dissipation is over package power.

●Typical Performance Curves (Continuation on previous page)

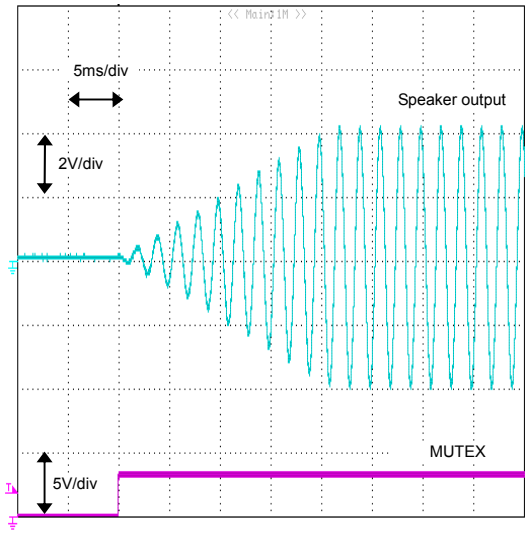


Figure 7.
Waveform at smooth start

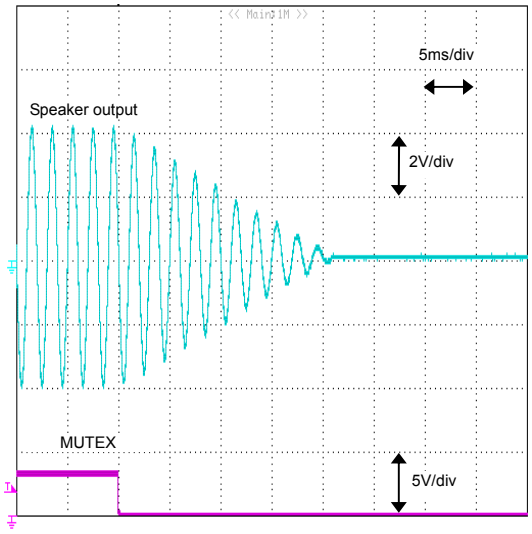


Figure 8.
Waveform at smooth mute

●Typical Performance Curves

(Ta=25℃,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=8Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=23dB,DSP through)
Measured by ROHM designed 4 layer board.

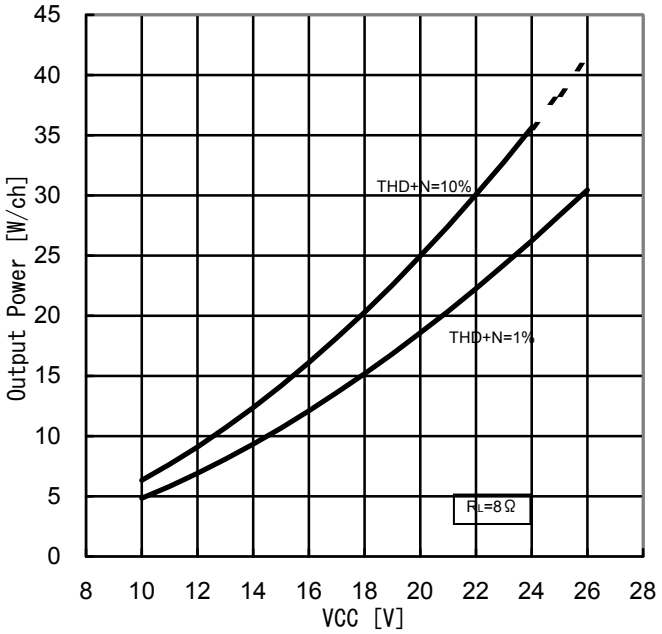


Figure 9.
Output voltage - Power voltage (R_L=8Ω).

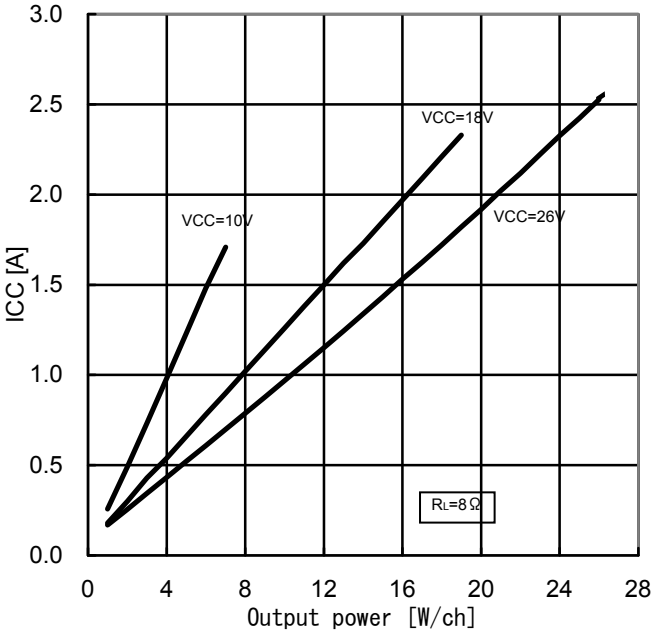


Figure 10.
Output power – Current consumption (R_L=8Ω)

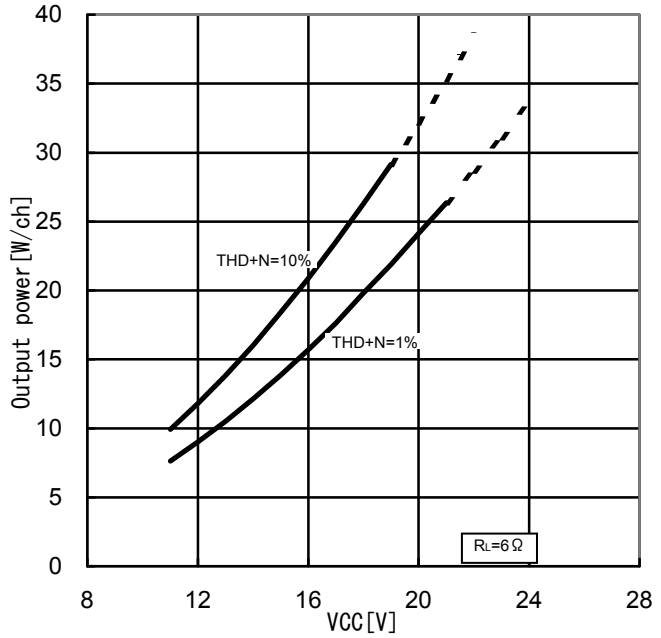


Figure 11.
Output voltage - Power voltage (R_L=6Ω).

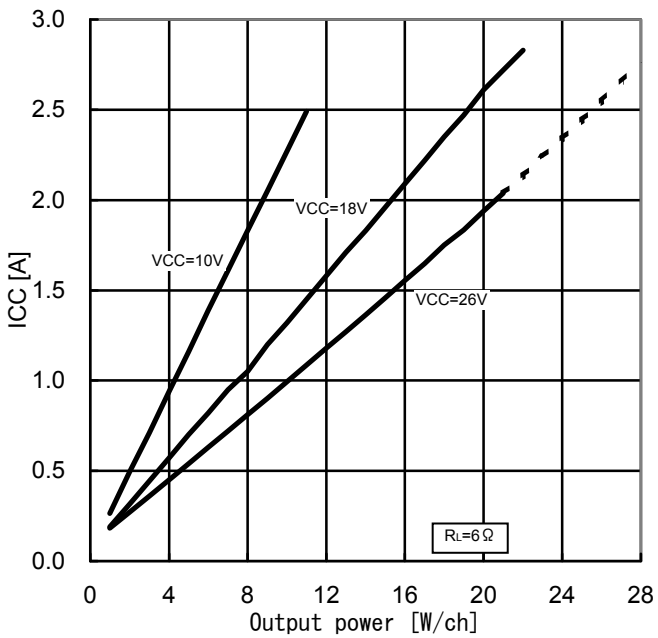


Figure 12.
Output power – Current consumption (R_L=6Ω)

Continued on next page.

※Dotted line means internal dissipation is over package power.

●Typical Performance Curves (Continuation on previous page)

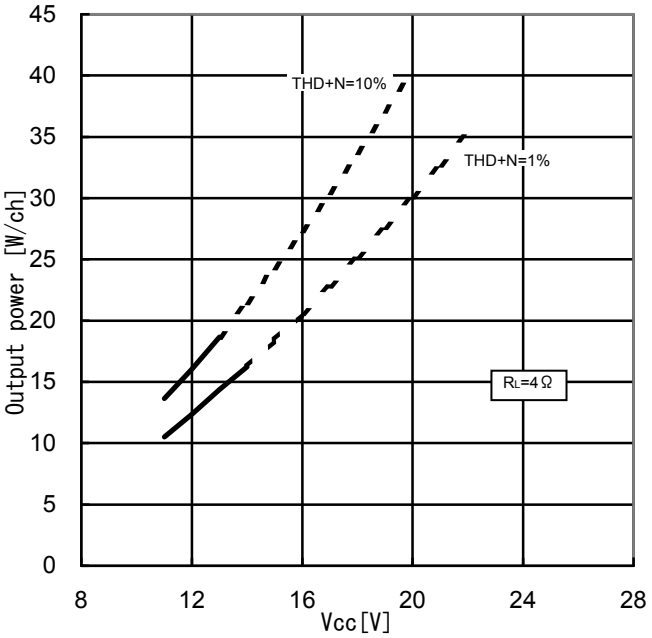


Figure 13.
Output voltage - Power voltage (R_L=4Ω).

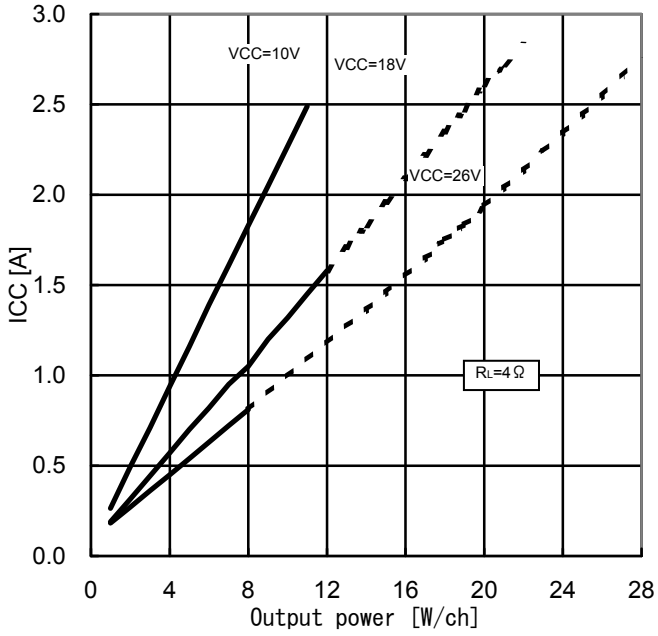


Figure 14.
Output power – Current consumption(R_L=4Ω)

●Typical Performance Curves
(Ta=25℃ ,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=4Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=20dB,DSP through, Output LCfilter:L=10uH,C=0.68uF,Cg=0.15uF, Monaural Parallel BTL mode)
Measured by ROHM designed 4-layer board.

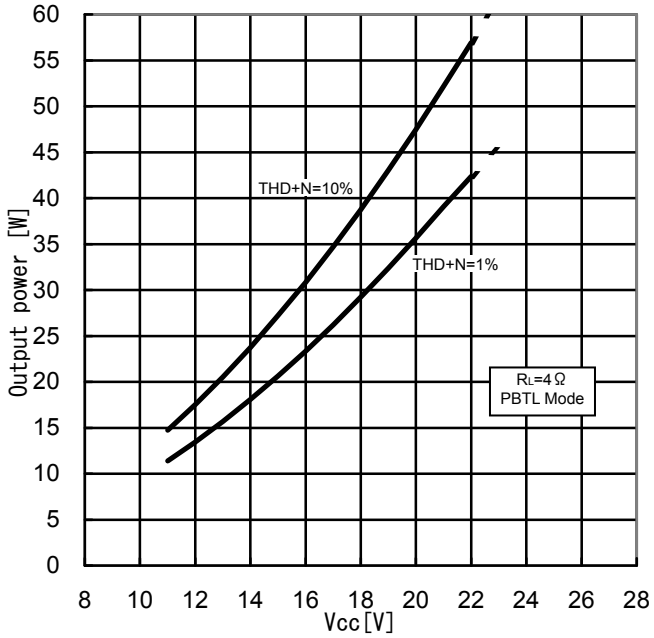


Figure 15.
Output voltage - Power voltage (R_L=4Ω, Monaural Parallel BTL mode)

※Dotted line means internal dissipation is over package power.

●Typical Performance Curves

(Ta=25℃,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=8Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=20dB,DSP through, Output LCfilter:L=22uH,C=0.33uF,Cg=0.068uF)

Measured by ROHM designed 4-layer board.

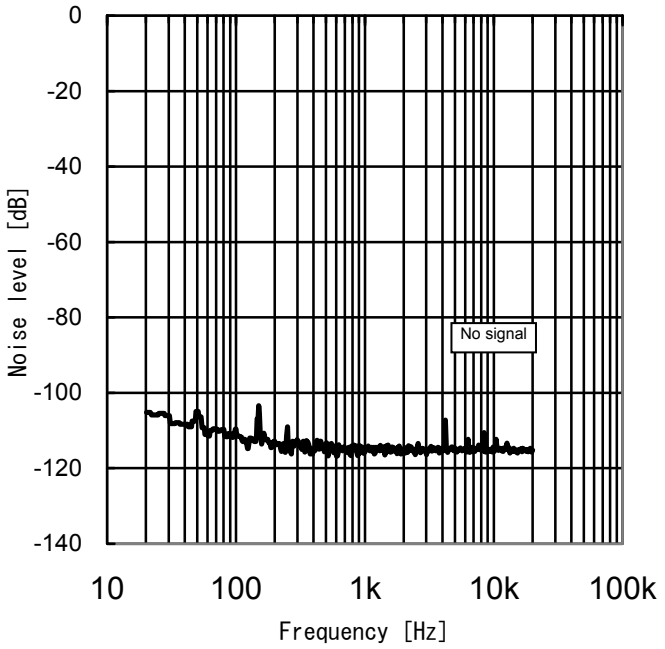


Figure 16.
FFT of output noise voltage (R_L=8Ω)

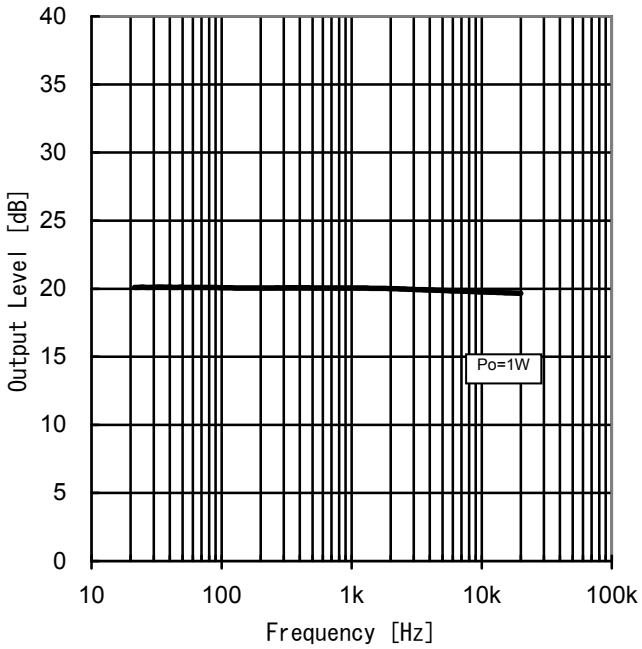


Figure 17.
Frequency – Output power (R_L=8Ω)

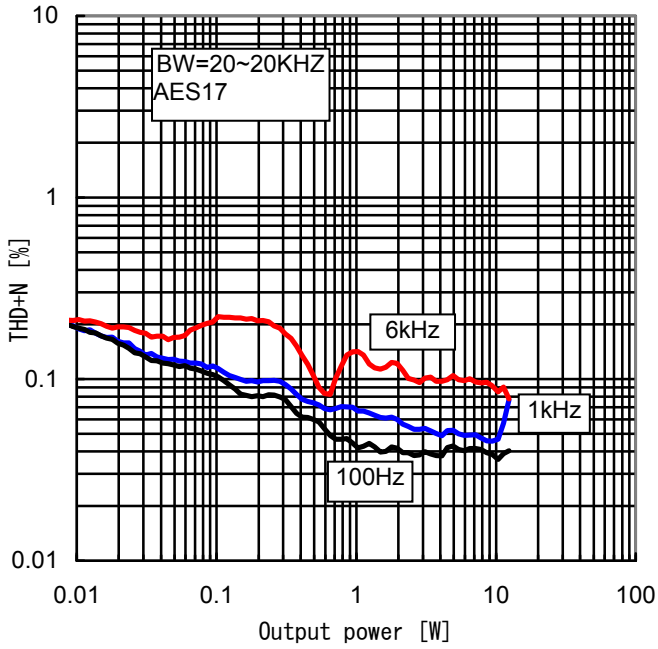


Figure 18.
Output power – THD+N (R_L=8Ω)

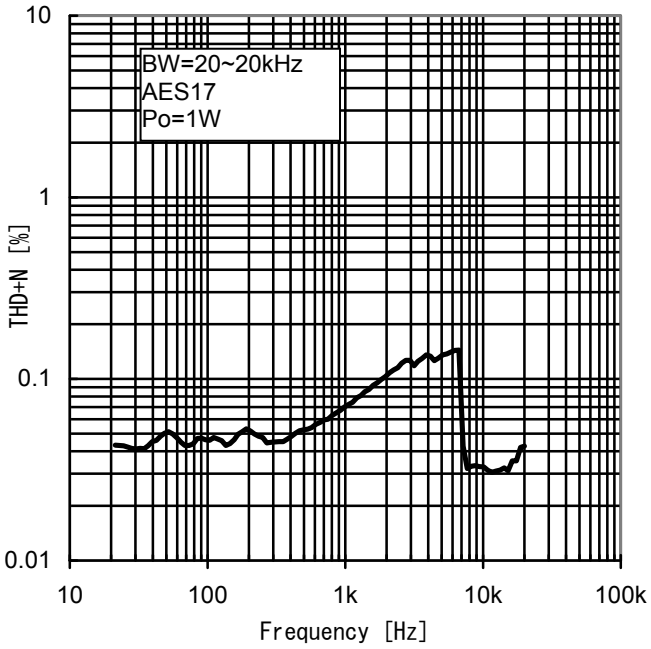


Figure 19.
Frequency – THD+N (R_L=8Ω)

Continued on next page.

●Typical Performance Curves (Continuation on previous page)

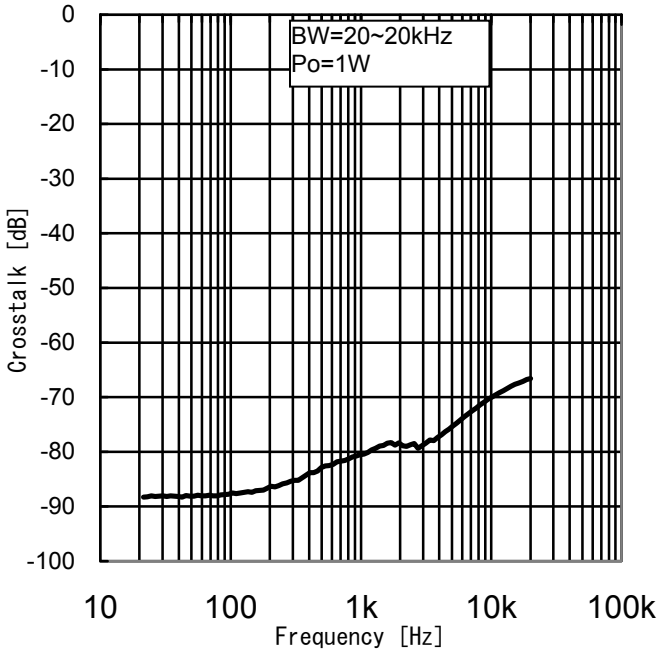


Figure 20.
Frequency – Crosstalk (R_L=8Ω)

●Typical Performance Curves

(Ta=25℃,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=6Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=20dB,DSP through, Output LCfilter:L=15uH,C=0.47uF,Cg=0.1uF)
Measured by ROHM designed 4-layer board.

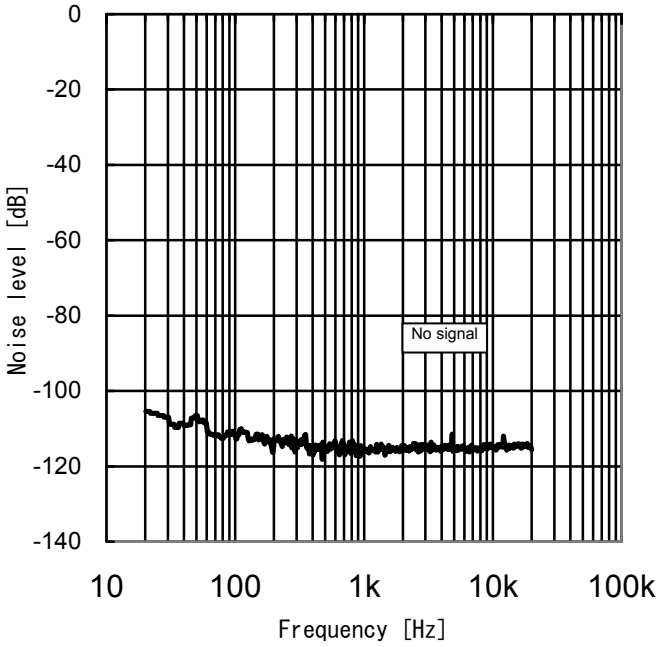


Figure 21.
FFT of output noise voltage (R_L=6Ω)

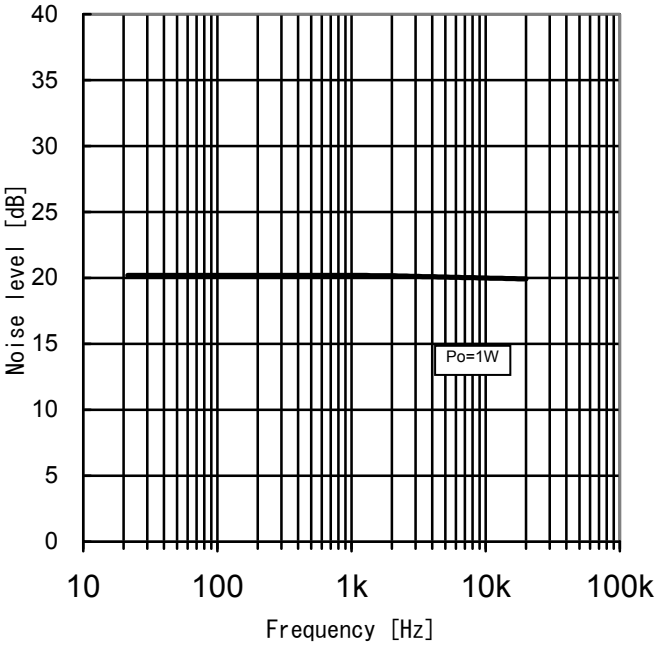


Figure 22.
Frequency – Output power (R_L=6Ω)

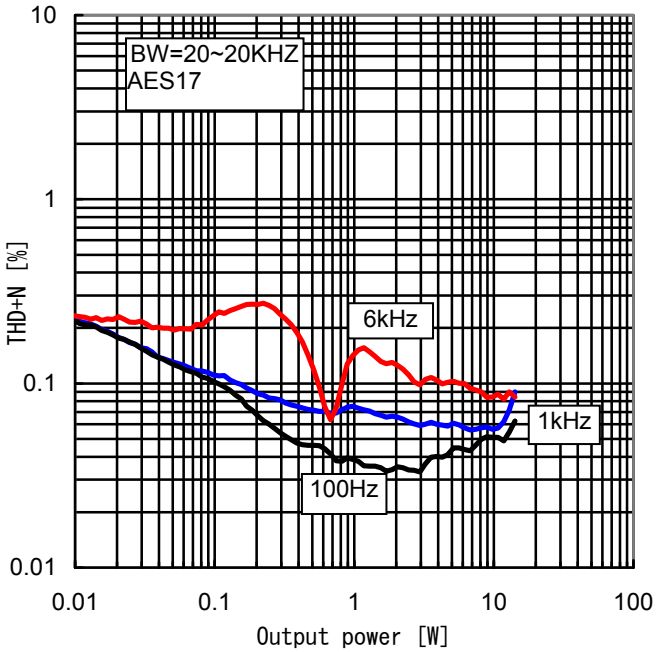


Figure 23.
Output power – THD+N (R_L=6Ω)

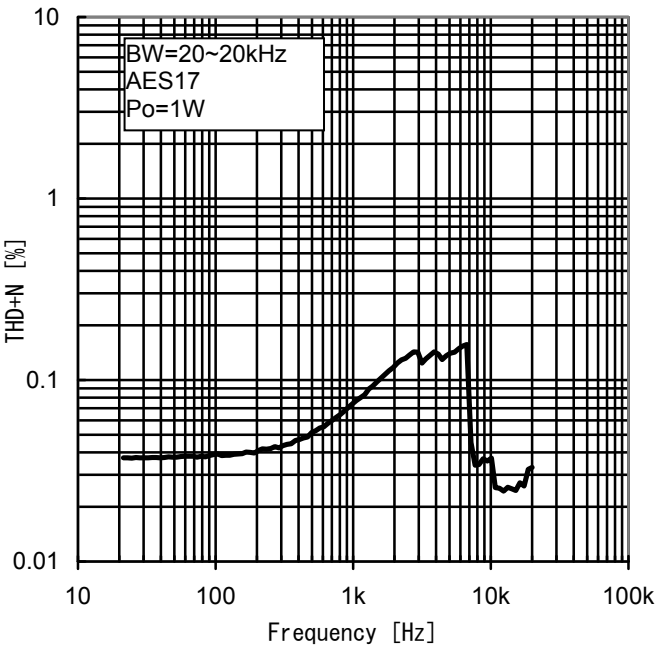


Figure 24.
Frequency – THD+N (R_L=6Ω)

Continued on next page.

●Typical Performance Curves (Continuation on previous page)

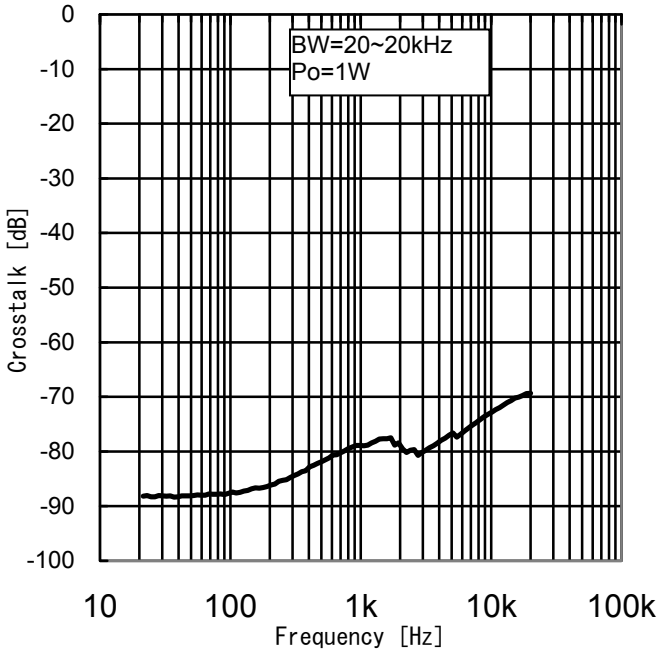


Figure 25.
Frequency – Crosstalk (R_L=6Ω)

●Typical Performance Curves

(Ta=25℃,Vcc=18V,V_{DD}=3.3V,fin=1kHz,R_L=4Ω,RSTX=3.3V,PDX=3.3V,MUTEX=3.3V,fs= 48kHz,GAIN=20dB,DSP through, Output LCfilter:L=10uH,C=0.68uF,Cg=0.15uF)
Measured by ROHM designed 4-layer board.

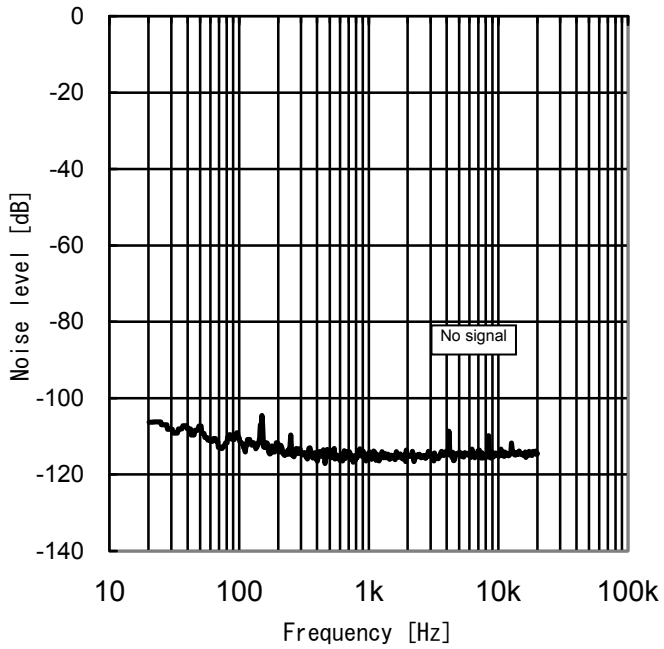


Figure 26.
FFT of output noise voltage (R_L=4Ω)

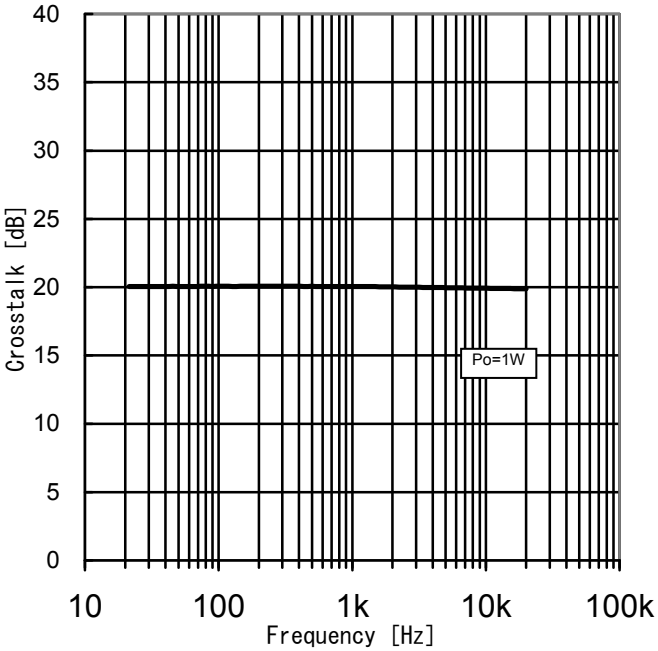


Figure 27.
Frequency – Output power (R_L=4Ω)

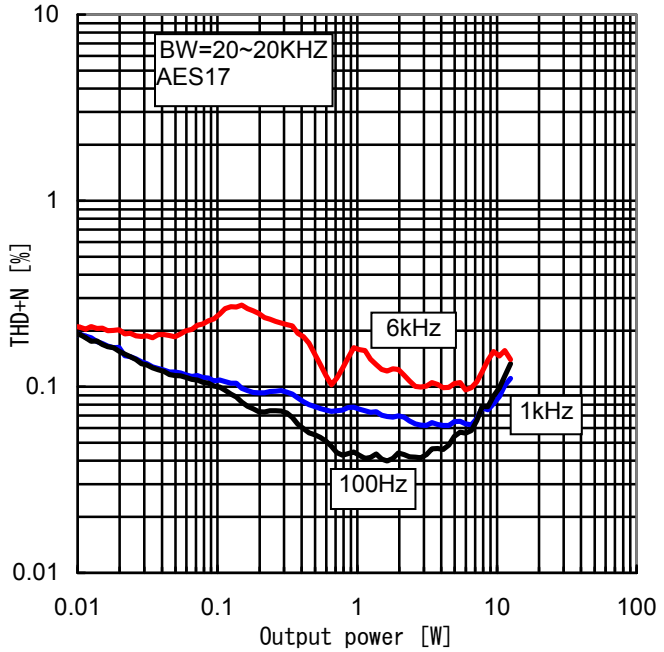


Figure 28.
Output power – THD+N (R_L=4Ω)

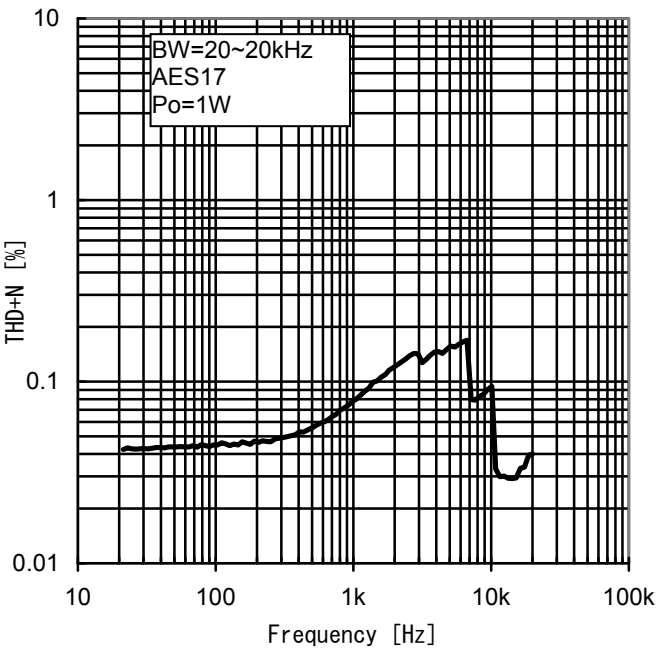


Figure 29.
Frequency – THD+N (R_L=4Ω)

Continued on next page.

●Typical Performance Curves (Continuation on previous page)

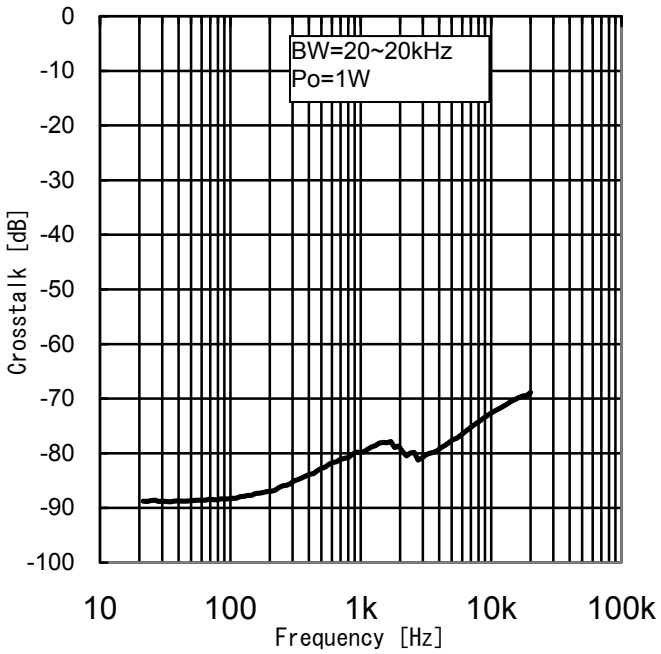


Figure 30.
Frequency – Crosstalk (R_L=4Ω)

●About external setting pin

(1) RSTX pin, PDX pin, MUTEX pin function

RSTX (51pin)	PDX (50pin)	MUTEX (49pin)	Normal state		
			PWM output (OUT1P, 1N, 2P, 2N)	ERROR output	WARNING output
L	L or H	L or H	HiZ_L (Power down mode)	H	H
H	L	L or H	HiZ_L (Power down mode)	H	H
H	H	L	HiZ_L (MUTE ON)	H	H
H	H	H	Normal (MUTE OFF)	H	H

RSTX (51pin)	PDX (50pin)	MUTEX (49pin)	ERROR detection		
			PWM output (OUT1P, 1N, 2P, 2N)	ERROR output	WARNING output
L	L or H	L or H	HiZ_L (Power down mode)	H	H
H	L	L or H	HiZ_L (Power down mode)	H	H
H	H	L	HiZ_L (MUTE ON)	H	H
H	H	H	HiZ_L (Latch)	L	H

RSTX (51pin)	PDX (50pin)	MUTEX (49pin)	WARNING detection		
			PWM output (OUT1P, 1N, 2P, 2N)	ERROR output	WARNING output
L	L or H	L or H	HiZ_L (Power down mode)	H	H
H	L	L or H	HiZ_L (Power down mode)	H	H
H	H	L	HiZ_L (MUTE ON)	H	H
H	H	H	HiZ_L	H	L

* RSTX, PDX and MUTEX pin are set Low, internal registers are initialized.

(2) ADDR pin function

ADDR (54pin)	I^2C BUS Slave address
L	80(hex)
H	82(hex)

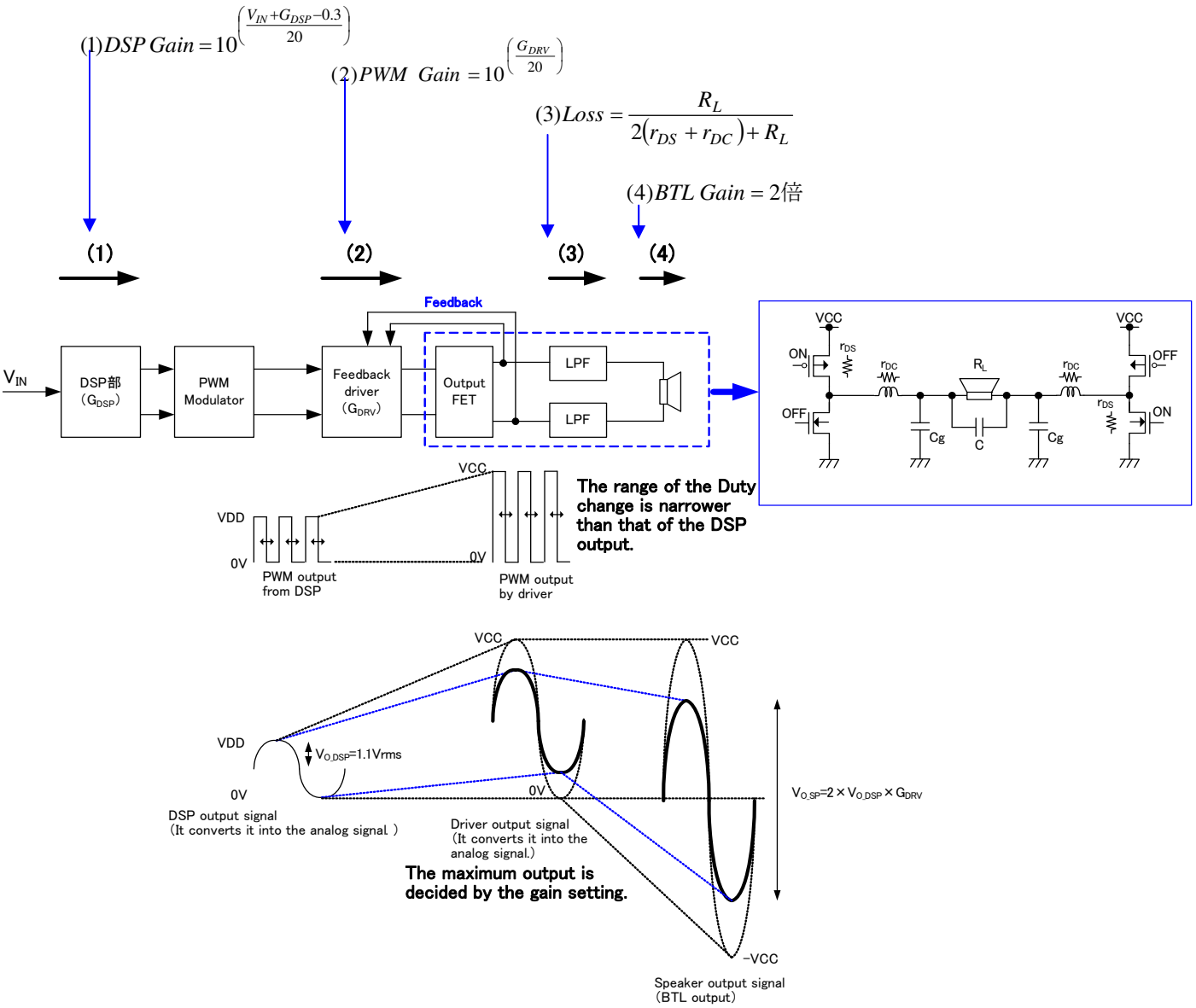
* ADDR pin is set to low level, internal resisters are initialized

(3) GAIN pin function

GAIN2 (48pin)	GAIN1 (47pin)	Speaker output setting gain	Speaker output limitation power (*1)
L	L	13.7dB	3.3W (THD+n=1%)
L	H	18.9dB	11.0W(THD+n=1%)
H	L	15.9dB	5.5W (THD+n=1%)
H	H	20.7dB	16.5W (THD+n=1%)

*1: It provides for the limitation power in the speaker output by the speaker maximum output when RL=8Ω, DSP=0dB, 0dBFS corresponding is input. Please set it according to the speaker used. 18dB, 20dB, 22dB, and 23dB can be set by the command besides the above-mentioned, set gain.

(4) Level diagram



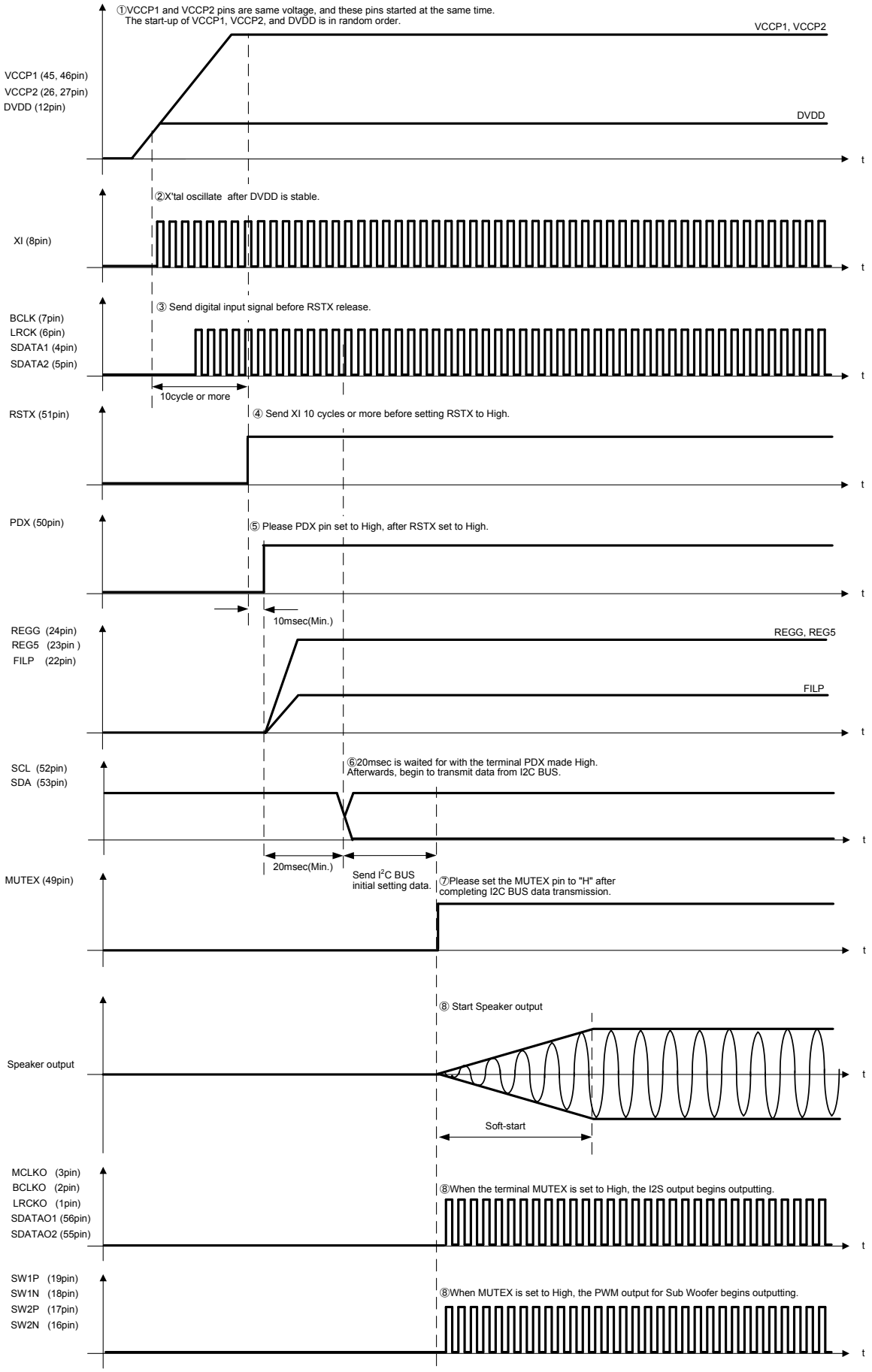
$$V_{O\_DSP} = \frac{VDD}{2\sqrt{2}}\left(10^{\frac{V_{IN}+G_{DSP}-0.3}{20}}\right) \quad [\text{Vrms}]$$

$$V_{O\_SP} = V_{O\_DSP} \times 10^{\left(\frac{G_{DRV}}{20}\right)} \times \frac{R_L}{2(r_{DS}+r_{DC})+R_L} \times 2 \quad [\text{Vrms}]$$

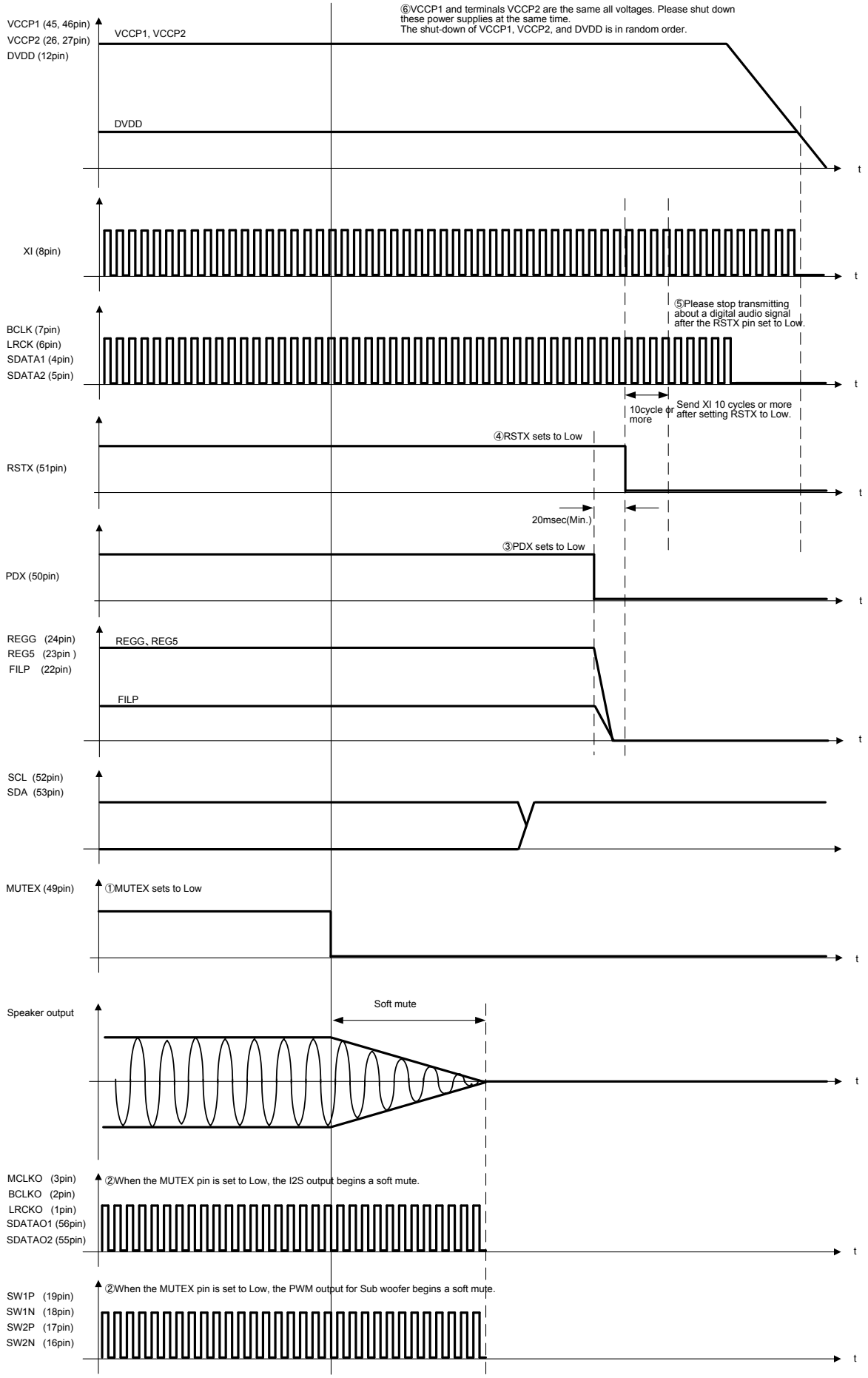
$$P_{O(THD=1\%)} = \frac{\left[\frac{VDD}{2\sqrt{2}}\left(10^{\frac{V_{IN}+G_{DSP}-0.3}{20}}\right) \times 10^{\left(\frac{G_{DRV}}{20}\right)} \times \frac{R_L}{2(r_{DS}+r_{DC})+R_L}[\text{W}] \times 2\right]^2}{R_L}$$

V_{IN} : I^2S input level [dBFS]
G_{DSP} : DSP gain [dB]
G_{DRV} : Feedback driver gain [dB]
VCC : Power supply for power amp [V]
VDD : Power supply for DSP [V]
R_L : Speaker load resistance [Ω]
r_{DS} : Output FET resistance[Ω] (TYP = 0.16Ω)
r_{DC} : Direct current resistance of coil [Ω]

●Power supply start-up sequence



●Power supply start-up sequence



●About the protection function

Protection function	Detecting & Releasing condition		Speaker PWM output	ERROR flag output	WARNING flag output
Output short protection	Detecting condition	Detecting current = 10A (TYP.)	HiZ_Low (Latch)	L	H
DC voltage protection	Detecting condition	Speaker PWM output fixes 40msec or more by Duty=0% or 100%.	HiZ_Low (Latch)	L	H
High temperature protection	Detecting condition	Chip temperature to be over 150℃ (TYP.)	HiZ_Low (Auto return)	H	L
	Releasing condition	Chip temperature to be under 120℃ (TYP.)	Normal		H
Under voltage protection	Detecting condition	Power supply voltage to be below 8V (TYP.)	HiZ_Low (Auto return)	H	L
	Releasing condition	Power supply voltage to be above 9V (TYP.)	Normal		H
Over voltage protection	Detecting condition	Power supply voltage to be above 29V (TYP.)	HiZ_Low (Auto return)	H	L
	Releasing condition	Power supply voltage to be below 28V (TYP.)	Normal		H
Clock stop protection	Detecting condition	BCLK or LRCK stops 100μsec (default) or more stops.	HiZ_Low (Auto return)	H	L
	Releasing condition	BCLK and LRCK normal input it.	Normal		H

* It doesn't return automatically even if abnormal state is released when becoming a latch state. It is possible to release it by the method of the following ①or②.
  ①After the terminal MUTEX is made Low (10 time maintained in Low = msec(Min.)) once, it returns it to High again.
  ②Please reenter the power supply after it drops to power-supply voltage Vcc<3V that the internal power-on reset circuit operates (10msec(Min.) maintenance).
* GAIN1 and GAIN2 pin can respectively be changed to the WARNING flag output pin and the ERROR flag output pin by the command.
* The stop detection time of BCLK and LRCK can respectively be changed with &h09 and &h08.

●Output selection of Stereo or Monaural on Main side.
Main side output can be set to stereo or monaural output. Initial value is set to “stereo output”.

Default = 0h

Select Address	Value	Explanation of operation	R/W
&hF0 [7]	0	Stereo output on main side. (Normal BTL Output)	R/W
	1	Monaural output on main side. (Parallel BTL Output)	

Please refer to the item of “Change of GAIN1 and GAIN2 pin “for other bits.

Default = 01h

Select Address	Value	Explanation of operation	R/W
&hF1 [7]	0	Reserved. (This bit should be set to “0”)	R/W
&hF1 [6]	0	Stereo output on main side. (Normal BTL Output)	R/W
	1	Monaural output on main side. (Parallel BT Output)	
&hF1 [5:3]	0	Reserved. (This bit should be set to “0”)	R/W
&hF1 [2:0]	1	Transmit address	R

After it sets it as follows, Channel Mixer 2 is set to set it to monaural.
(1) Write 1h to &hF0 [7] register.
(2) Write 41h to &hF1 [7:0] register.
(3) Write 01h to &hF8 [7:0] register.

When the Main side is output by the monaural output, the output of the DSP side is set to the monaural output with Channel Mixer 2. The example of setting that time is as follows.

(1) When you use L ch as a monaural output
&h26 = 19h : L out set to L in, R out set to inverse L in.

(2) When you use R ch as a monaural output
&h26 = 2Ah : L out set to R in, R out set to inverse R in.

(3) When you use L ch as a monaural output
&h26 = 3Bh : L out set to (Lch + Rch)/2, R out set to inverse (Lch + Rch)/2.

*Changing the stereo or monaural should be done after MUTEX terminal set to “L”.

Please refer to "4-11. The channel setting with the phase reversing function" for details of Channel Mixer 2.

●Output selection of Stereo or Monaural on Sub side.
The output of the Sub side can be set to the stereo or monaural as well as the Main side. An initial value is a stereo output.
If the Sub side is monaural output, it should be set to monaural output by Channel Mixer 3 of the DSP.
The example of setting that time is as follows.

(1) When you use L ch as a monaural output
&h27 = 19h : L out set to L in, R out set to inverse L in.

(2) When you use R ch as a monaural output
&h27 = 2Ah : L out set to R in, R out set to inverse R in.

(3) When you use L ch as a monaural output
&h27 = 3Bh : L out set to (Lch + Rch)/2, R out set to inverse (Lch + Rch)/2

*Changing the stereo or monaural should be done after MUTEX terminal set to “L”.

Please refer to "4-11. The channel setting with the phase reversing function" for details of Channel Mixer 3.

●Change of GAIN1 and GAIN2 pin

After address &hF0 [3] is set to 1, it is necessary to set to 1 in &hF8 [0] to change the terminal GAIN1 and the terminal GAIN2 to the WARNING flag output and the ERROR flag output terminal respectively.

Moreover, the gain value can be changed by writing 1 in &hF8 [0] after the speaker output setting gain value also similarly sets the gain value to &hF0 [6:4]. Please set &hF0 [3] to 1 when you set the gain by this command.

Restrictions on output power supply for 3W speaker

Default=00h

Select Address	Value	Explanation of operation	R/W
&hF0 [6 : 4]	0	13.7dB (Output power limitter for 3W speaker)	R/W
	1	19.0dB (Output power limitter for 10W speaker)	
	2	15.9dB (Output power limitter for 5W speaker)	
	3	20.7dB (Output power limitter for 15W speaker)	
	4	18.0dB	
	5	20.0dB	
	6	22.0dB	
	7	23.0dB	
&hF0 [3]	0	Gain setting by external pin	R/W
	1	Output flag setting for WARNING/ERROR	
&hF0 [2:0]	0	Transmit address	R

Default=0h

Select Address	Value	Explanation of operation	R/W
&hF8 [1]	0	Force stop transmission invalid	R/W
	1	Force stop transmission valid	
&hF8 [0]	0	Stop transmission	R/W
	1	Start transmission (This bit is cleared 0 by automatically)	

*The address from &hF1 to &hF7 is register for LSI test. Please don't access these register.

●Reading of ERROR and WARNING flag with I^2C

It is also possible to read it through I^2C I/F though WARNING and the ERROR flag can be output to the terminal GAIN1 and the terminal GAIN2 respectively. The reading address is as follows.

Select Address	Value	Explanation of operation	R/W
&hE8 [7]	0	ERROR state	R
	1	Normal	
&hE8 [6]	0	WARNING state	R
	1	Normal	

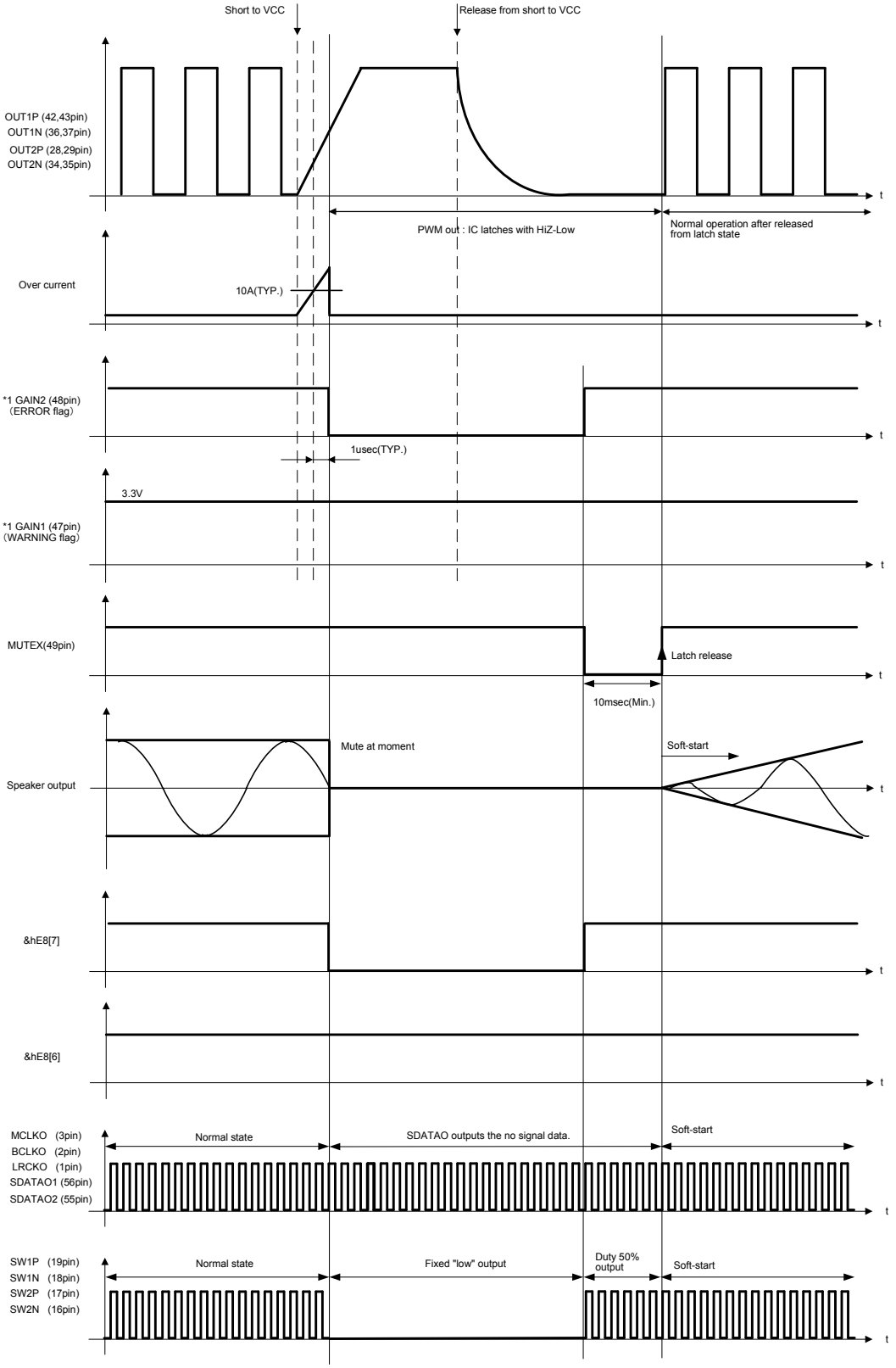
●Output short protection (Short to the power supply)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output pin becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After MUTEX pin is set Low once over the soft mute transition time(Min.:10msec), MUTEX pin is returned to High again.

②Turning on the power supply again (Vcc<3V, 10ms(min)).



(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

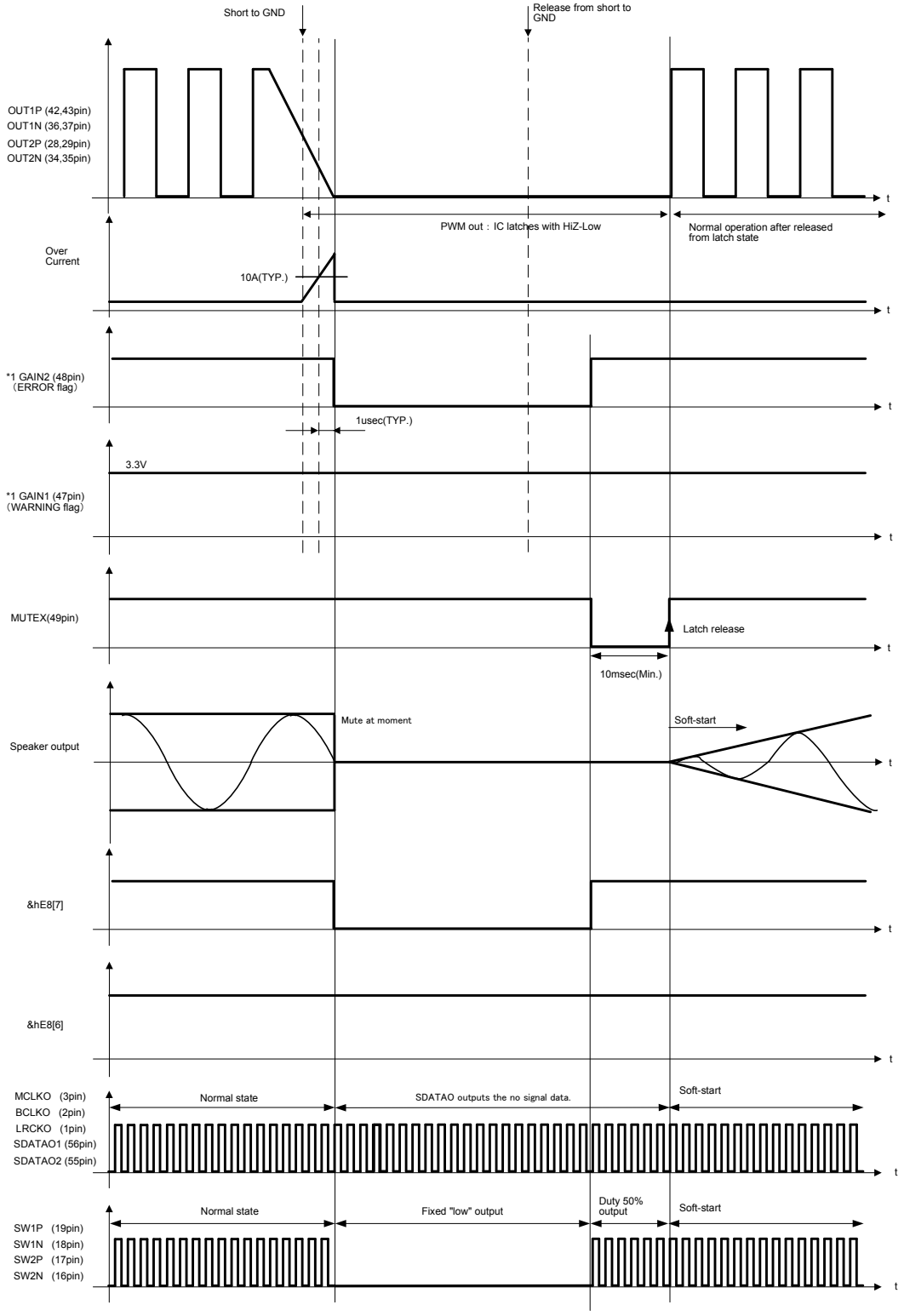
●Output short protection (Short to GND)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output terminal becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method – ①After MUTEX pin is set Low once over the soft mute transition time(10msec(Min.)), MUTEX pin is returned to High again.

②Turning on the power supply again (Vcc<3V, 10msec(Min.))



(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

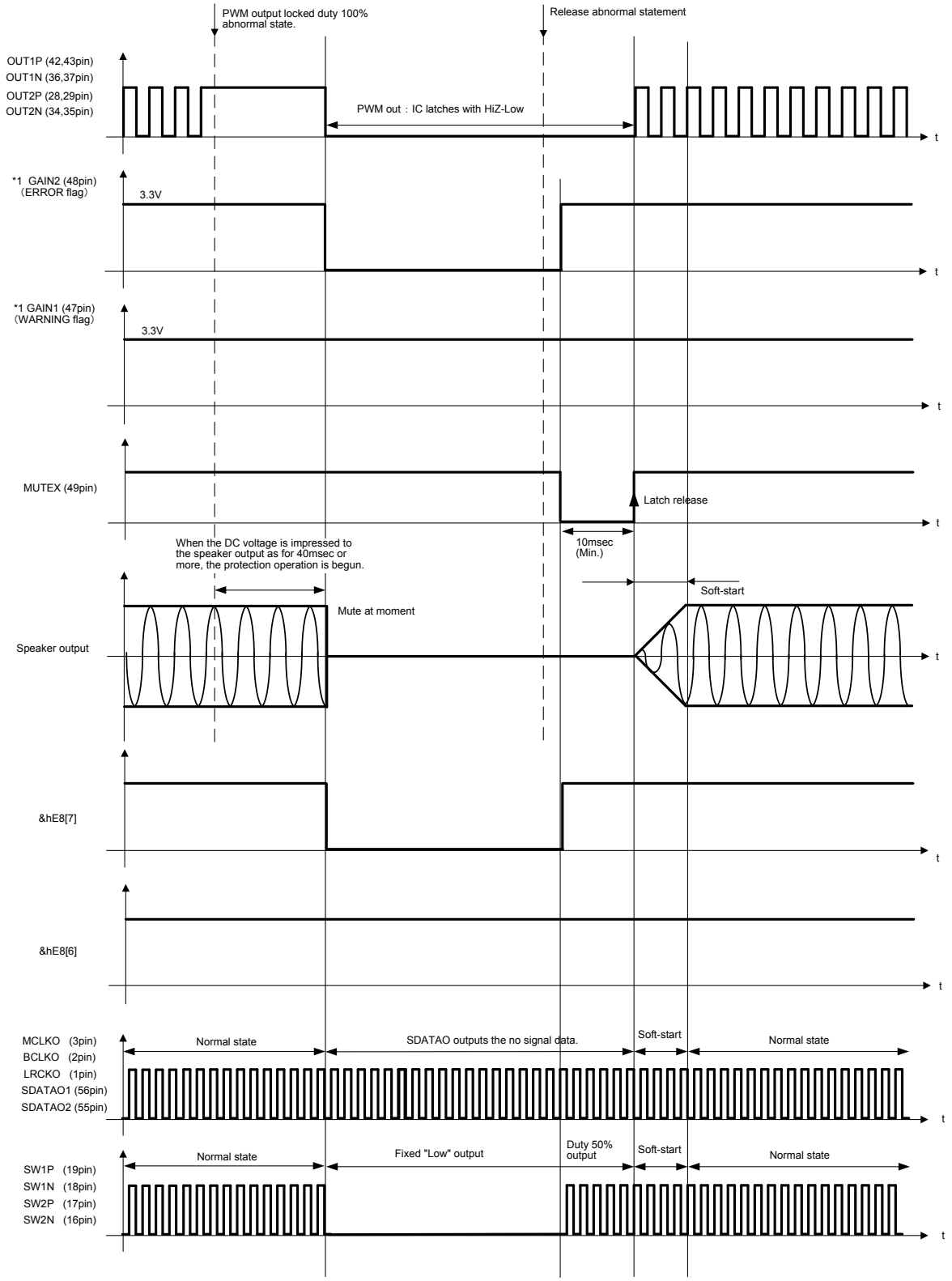
●DC voltage protection in the speaker

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTEX pin is set High and PWM output Duty=0% or 100% over 40msec. Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method – ①After MUTEX pin is set Low once over the soft mute transition time(10msec(Min.)), MUTEX pin is returned to High again.

②Turning on the power supply again (Vcc<3V, 10msec(Min)).



(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.