Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Gate Driver Providing Galvanic isolation Series

Isolation voltage 2500Vrms 1ch Gate Driver Providing Galvanic Isolation

BM60014FV-C

General Description

The BM60014FV-C is a gate driver with an isolation voltage of 2500Vrms, I/O delay time of 120ns, and minimum input pulse width of 70ns. It incorporates the fault signal output functions, Under-voltage Lockout (UVLO) function and Miller clamp function.

Key Specifications

- Isolation voltage: 2500Vrms
- Maximum gate drive voltage: 24V
- I/O delay time: 120ns(Max)
- Minimum input pulse width: 70ns(Max)

Features

- AEC-Q100 Qualified(Note1)
- Providing Galvanic Isolation
- Active Miller Clamping
- Fault signal output function
- Under-voltage Lockout function
- UL1577 Recognized:File No. E356010

(Note1: Grade1)

Package

SSOP-B20W — W(Typ) x D(Typ) x H(Max) 6.50mm x 8.10mm x 2.01mm

Applications

- IGBT Gate Driver
- MOSFET Gate Driver

Typical Application Circuits

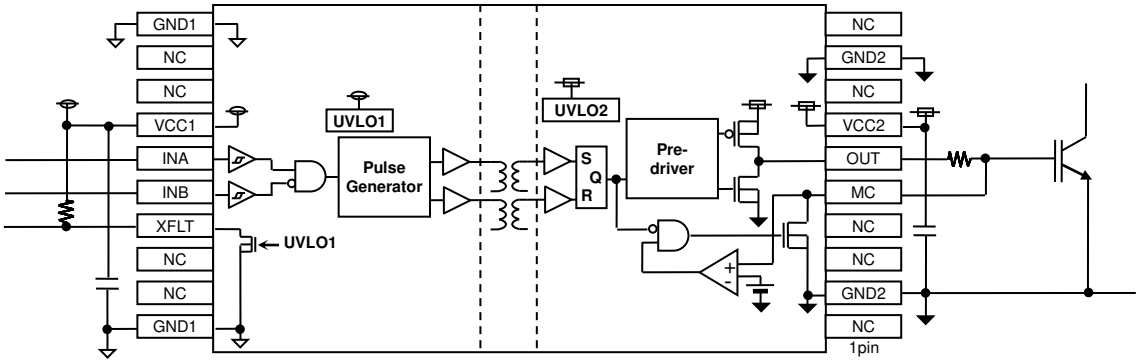


Figure 1. Application Circuits (IGBT Gate Driver)

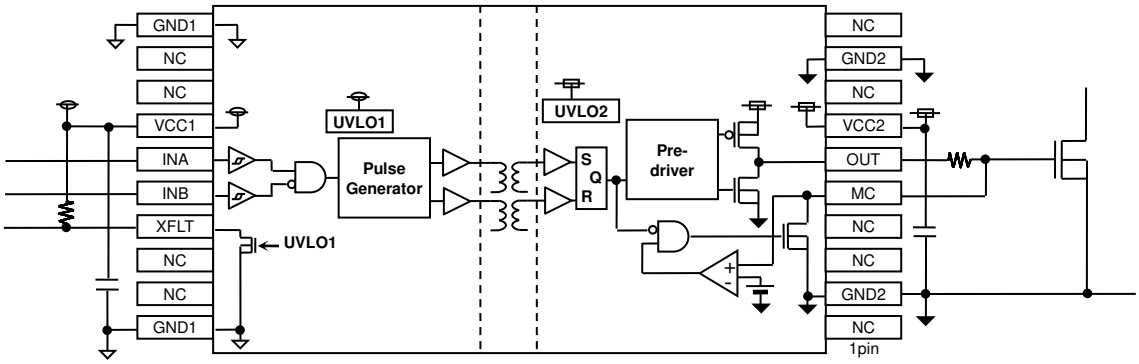


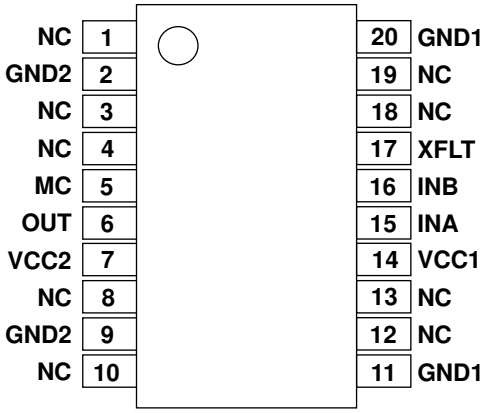
Figure 2. Application Circuits (MOSFET Gate Driver)

Recommended Range of External Constants

Pin Name	Symbol	Recommended Value			Unit
		Min.	Typ.	Max.	
VCC1	C_{VCC1}	0.1	1.0	-	µF
VCC2	C_{VCC2}	0.33	-	-	µF

Pin Configurations

(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1	NC	No Connection
2	GND2	Output-side ground pin
3	NC	No Connection
4	NC	No Connection
5	MC	Output pin for Miller Clamp
6	OUT	Output pin
7	VCC2	Output-side power supply pin
8	NC	No Connection
9	GND2	Output-side ground pin
10	NC	No Connection
11	GND1	Input-side ground pin
12	NC	No Connection
13	NC	No Connection
14	VCC1	Input-side power supply pin
15	INA	Control input pin A
16	INB	Control input pin B
17	XFLT	Fault signal output pin
18	NC	No Connection
19	NC	No Connection
20	GND1	Input-side ground pin

Description of pins and cautions on layout of board

1) VCC1 (Input-side power supply pin)
The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2) GND1 (Input-side ground pin)
The GND1 pin is a ground pin on the input side.

3) VCC2 (Output-side positive power supply pin)
The VCC2 pin is a power supply pin on the output side. To reduce voltage fluctuations due to OUT pin output current, connect a bypass capacitor between the VCC2 and the GND2 pins.

4) GND2 (Output-side ground pin)
The GND2 pin is a ground pin on the output side.

5) INA, INB (Control input terminal)
The INA and INB pins are used to determine output logic.

INB	INA	OUT
H	L	L
H	H	L
L	L	L
L	H	H

6) OUT (Output pin)
The OUT pin is used to drive the gate of a power device.

7) MC (Output pin for Miller Clamp)
The MC pin is for preventing the increase in gate voltage due to the Miller current of the power device connected to the OUT pin. If the Miller Clamp function is not used, short-circuit the MC pin to the GND2 pin.

8) XFLT (Fault signal output pin)
The XFLT pin is an open drain pin used to output a fault signal when a fault occurs (i.e., when the Under-voltage Lockout function (UVLO1) is activated).

Conditions	XFLT
While in normal operation	L
When an Fault occurs (When UVLO1 is activated)	Hi-Z

Description of functions and examples of constant setting

1) Miller Clamp function

When INA=L and OUT pin voltage < V_{MCON} (typ 2V), the internal MOSFET of the MC pin is turned ON.

INA	MC	Internal MOSFET of the MC pin
L	less than V_{MCON}	ON
H	X	OFF

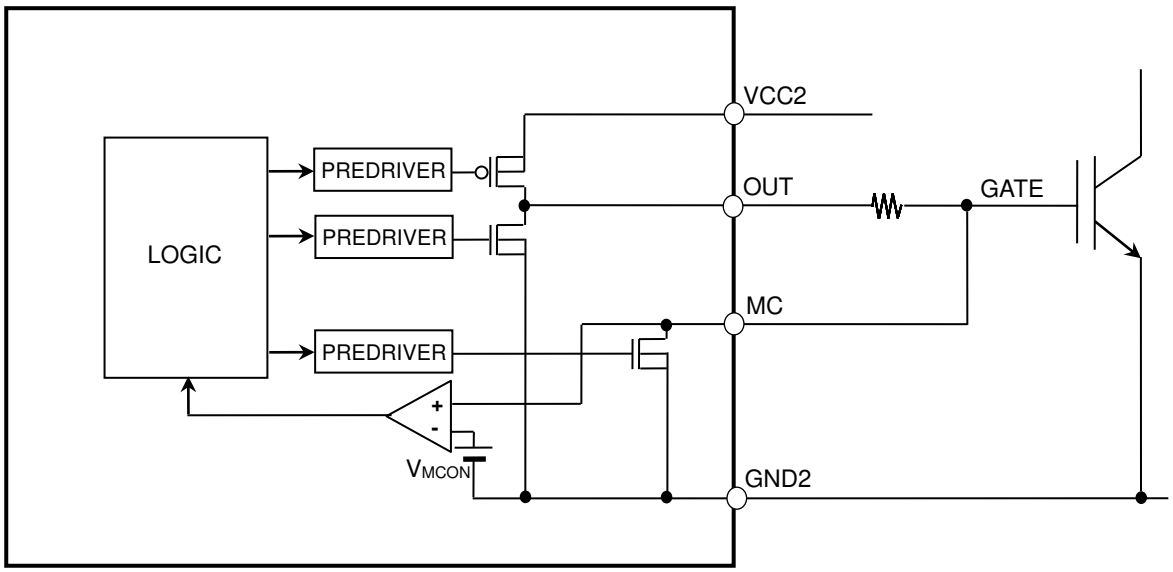


Figure 3. Block diagram of Miller Clamp function.

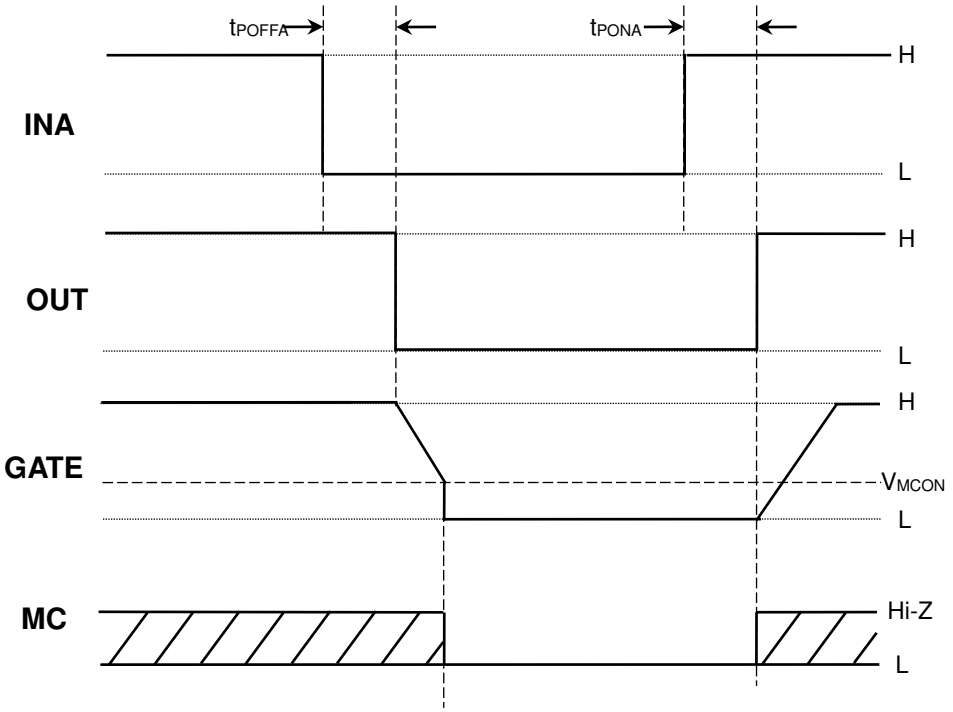


Figure 4. Timing chart of Miller Clamp function

2) Under-voltage Lockout (UVLO) function

The BM60014FV-C incorporates the Under-voltage Lockout (UVLO) function both on the low and the high voltage sides. When the power supply voltage drops to the UVLO ON voltage (low voltage side typ 3.4V, high voltage side voltage typ 9.5V), the OUT pin will output the “L” signal. In addition, to prevent malfunctions due to noises, a mask time of $t_{UVLO1MSK}$ (typ 2.5µs) and $t_{UVLO2MSK}$ (typ 2.85µs) are set on both the low and the high voltage sides.

This IC does not have a function which feeds back the high voltage side state to the low voltage side. After the high voltage side UVLO is released, the input signal will take effect from the time after the input signal switches.

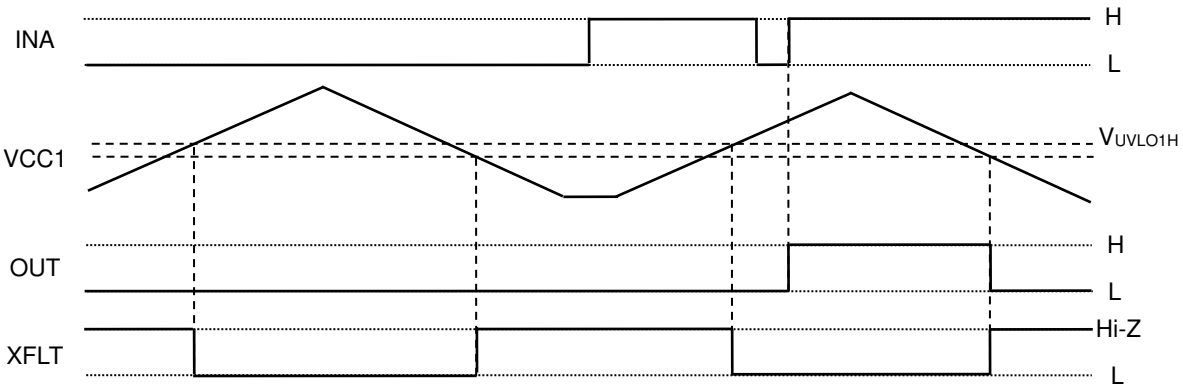


Figure 5. Input-side UVLO Function Operation Timing Chart

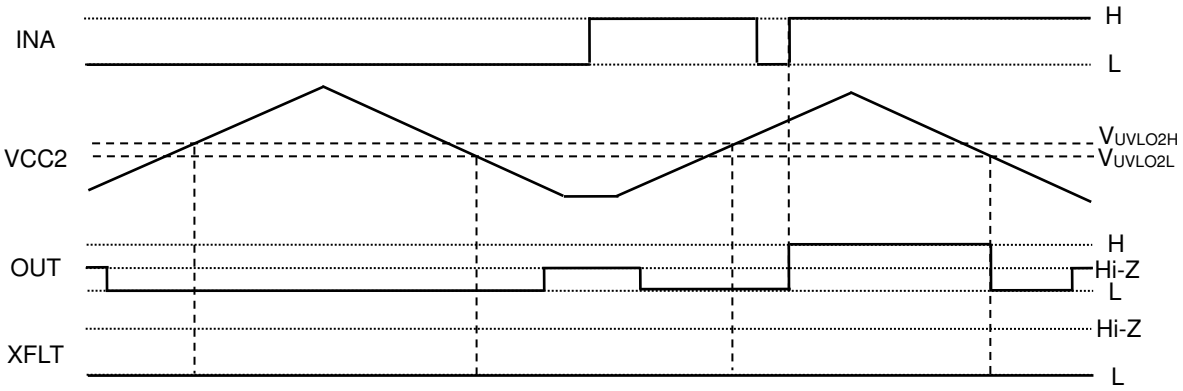


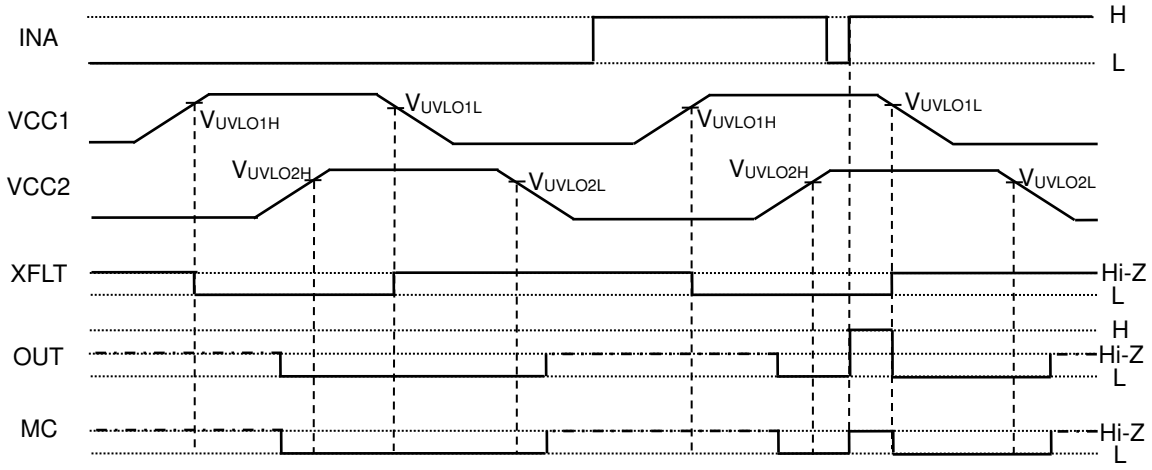
Figure 6. Output-side UVLO Function Operation Timing Chart

3）I/O condition table

No.	Status	Input				Output		
		VCC1	VCC2	INB	INA	OUT	MC	XFLT
1	VCC1UVLO	UVLO	X	X	X	L	L	H
2	VCC2UVLO	X	UVLO	X	X	L	L	L
3	INB Active	○	○	H	X	L	L	L
4	Normal operation L input	○	○	L	L	L	L	L
5	Normal operation H input	○	○	L	H	H	Hi-Z	L

○: VCC1 or VCC2 > UVLO, X:Don't care

4) Power supply startup / shutoff sequence



- - - - - - : Since the VCC2 to GND2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z.

Figure 7. Power Supply Startup / Shutoff Sequence

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input-side supply voltage	V_{CC1}	-0.3～+7.0(Note 1)	V
Output-side supply voltage	V_{CC2}	-0.3～+30.0(Note 2)	V
INA pin input voltage	V_{INA}	-0.3～+VCC1+0.3 or +7.0(Note 3)	V
INB pin input voltage	V_{INB}	-0.3～+VCC1+0.3 or +7.0(Note1)	V
OUT pin output current (Peak 10μs)	$I_{OUTPEAK}$	5.0(Note 3)	A
XFLT pin output current	I_{XFLT}	10	mA
Power dissipation	Pd	1.19(Note 4)	W
Operating temperature range	Topr	-40～+125	°C
Storage temperature range	Tstg	-55～+150	°C
Junction temperature	Tjmax	+150	°C

(Note 1) Relative to GND1.
(Note 2) Relative to GND2.
(Note 3) Should not exceed Pd and Tj=150°C
(Note 4) Derate by 9.5mW/°C when operating above Ta=25°C. Mounted on a glass epoxy of 70mm ×70mm ×1.6mm.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Ratings

Parameter	Symbol	Min.	Max.	Units
Input-side supply voltage	V_{CC1}(Note 5)	4.5	5.5	V_{CC1}(Note 5)
Output-side supply voltage	V_{CC2}(Note 6)	10	24	V_{CC2}(Note 6)

(Note 5) Relative to GND1.
(Note 6) Relative to GND2.

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Units
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1sec	V_{ISO}	3000	Vrms

Electrical Characteristics

(Unless otherwise specified T_a=-40°C to 125°C, V_{CC1}=4.5V to 5.5V, V_{CC2}=10V to 24V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
General						
Input side circuit current 1	I_{CC11}	0.06	0.14	0.22	mA	
Input side circuit current 2	I_{CC12}	0.10	0.20	0.30	mA	INA =10kHz, Duty=50%
Input side circuit current 3	I_{CC13}	0.15	0.30	0.45	mA	INA =20kHz, Duty=50%
Output side circuit current 1	I_{CC21}	0.26	0.44	0.62	mA	OUT=L
Output side circuit current 2	I_{CC22}	0.22	0.38	0.57	mA	OUT=H
Logic block						
Logic high level input voltage	V_{INH}	2.0	-	V_{CC1}	V	INA, INB
Logic low level input voltage	V_{INL}	0	-	0.8	V	INA, INB
Logic pull-down resistance	R_{IND}	25	50	100	kΩ	INA, INB
Logic input minimum pulse width	t_{INMIN}	-	-	70	ns	INA, INB
Output						
OUT ON resistance (Source)	R_{ONH}	0.4	0.9	2.0	Ω	I_{OUT}=-40mA
OUT ON resistance (Sink)	R_{ONL}	0.2	0.6	1.3	Ω	I_{OUT}=40mA
OUT maximum current (Source)	$I_{OUTMAXH}$	3.0	4.5	-	A	VCC2=15V, Guaranteed by design
OUT maximum current (Sink)	$I_{OUTMAXL}$	3.0	3.9	-	A	VCC2=15V, Guaranteed by design
Turn ON time	t_{PONA}	70	90	120	ns	INA=PWM, INB=L
	t_{PONB}	65	85	115	ns	INA=H, INB=PWM
Turn OFF time	t_{POFFA}	70	90	120	ns	INA=PWM, INB=L
	t_{POFFB}	75	95	125	ns	INA=H, INB=PWM
Propagation distortion	t_{PDISTA}	-25	0	25	ns	$t_{POFFA} - t_{PONA}$
	t_{PDISTB}	-15	10	35	ns	$t_{POFFB} - t_{PONB}$
Rise time	t_{RISE}	-	50	-	ns	10nF between OUT-GND2
Fall time	t_{FALL}	-	50	-	ns	10nF between OUT-GND2
MC ON resistance	R_{ONMC}	0.20	0.65	1.40	Ω	I_{MC}=40mA
MC ON threshold voltage	V_{MCON}	1.8	2	2.2	V	
Common Mode Transient Immunity	CM	100	-	-	kV/µs	Guaranteed by design
Protection functions						
VCC1 UVLO OFF voltage	V_{UVLO1H}	3.35	3.50	3.65	V	
VCC1 UVLO ON voltage	V_{UVLO1L}	3.25	3.40	3.55	V	
VCC1 UVLO mask time	$t_{UVLO1MSK}$	1.0	2.5	5.0	µs	
VCC2 UVLO OFF voltage	V_{UVLO2H}	9.0	9.5	10.0	V	
VCC2 UVLO ON voltage	V_{UVLO2L}	8.0	8.5	9.0	V	
VCC2 UVLO mask time	$t_{UVLO2MSK}$	1.00	2.85	5.00	µs	
XFLT output L voltage	V_{XFLT}	-	0.10	0.25	V	I_{XFLT}=5mA

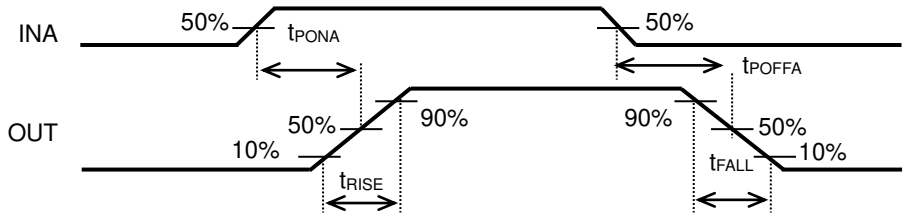


Figure 8. IN-OUT Timing Chart

UL1577 Ratings Table

Following values are described in UL Report.

Parameter	Values	Units	Conditions
Side 1 (Input Side) Circuit Current	0.14	mA	VCC1=5.0V, OUT=L
Side 2 (Output Side) Circuit Current	0.44	mA	VCC2=V, OUT=L
Side 1 (Input Side) Consumption Power	0.7	mW	VCC1=5.0V, OUT=L
Side 2 (Output Side) Consumption Power	6.6	mW	VCC2=15V, OUT=L
Isolation Voltage	2500	Vrms	
Maximum Operating (Ambient) Temperature	125	℃	
Maximum Junction Temperature	150	℃	
Maximum Strage Temperature	150	℃	
Maximum Data Transmission Rate	2.5	MHz	

Typical Performance Curves

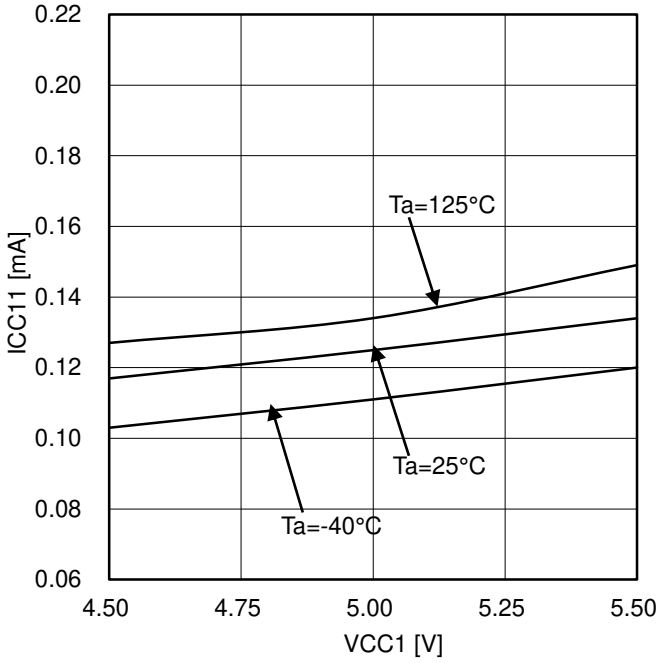


Figure 9. Input Side Circuit Current vs Input Side Supply Voltage

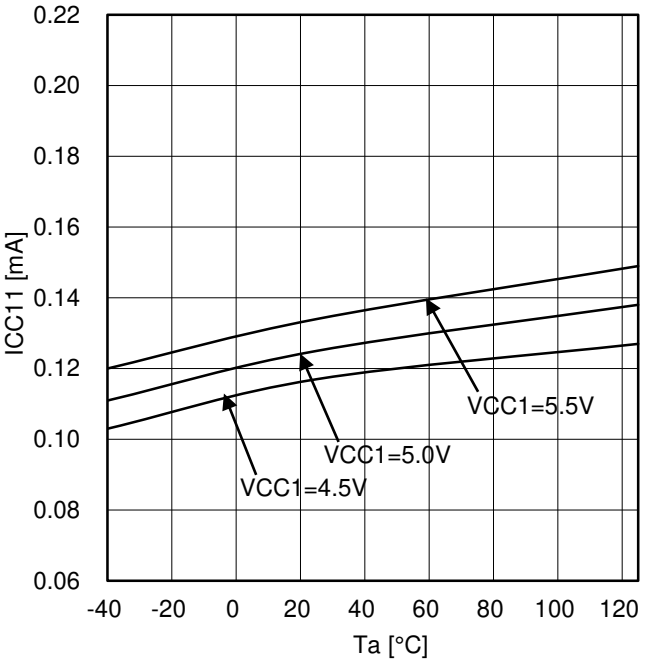


Figure 10. Input Side Circuit Current vs Temperature

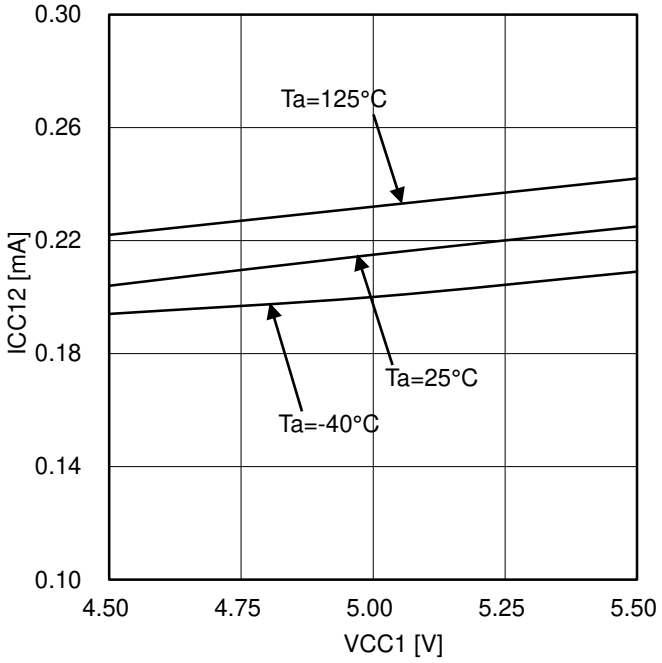


Figure 11. Input Side Circuit Current vs Input Side Supply Voltage (at INA=10kHz, Duty=50%)

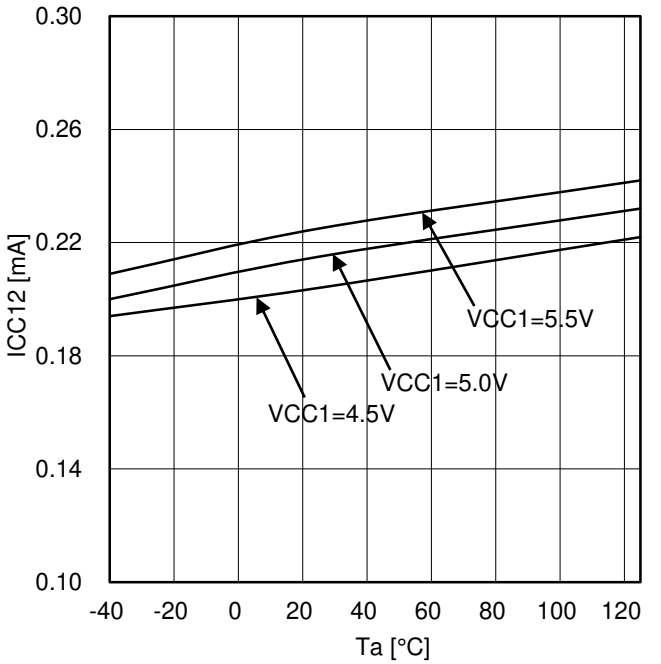


Figure 12. Input Side Circuit Current vs Temperature (at INA=10kHz, Duty=50%)

Typical Performance Curves - continued

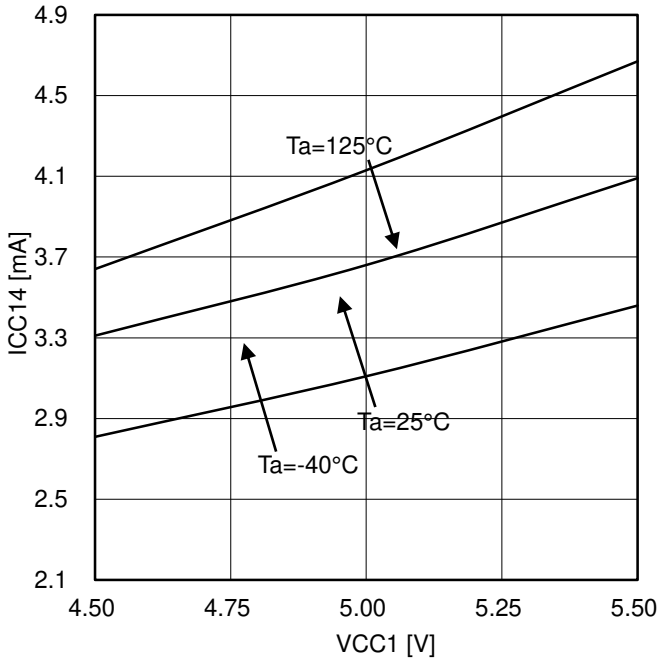


Figure 13. Input Side Circuit Current vs Input Side Supply Voltage (INA=20kHz, Duty=50%)

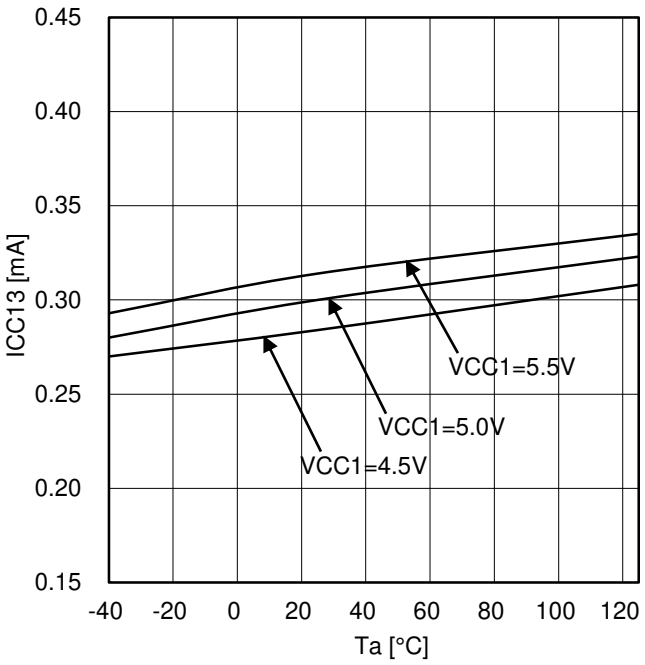


Figure 14. Input Side Circuit Current vs Temperature (INA=20kHz, Duty=50%)

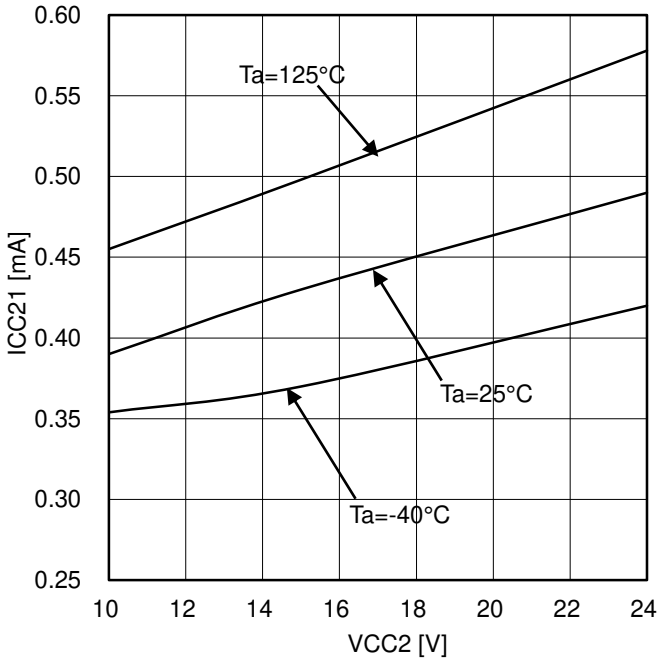


Figure 15. Output Side Circuit Current vs Output Side Supply Voltage (at OUT=L)

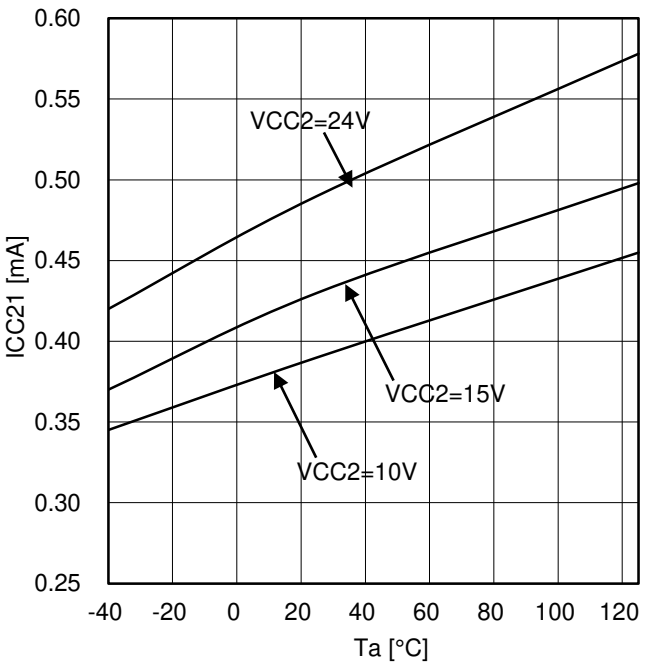


Figure 16. Output Side Circuit Current vs Temperature (at OUT=L)

Typical Performance Curves - continued

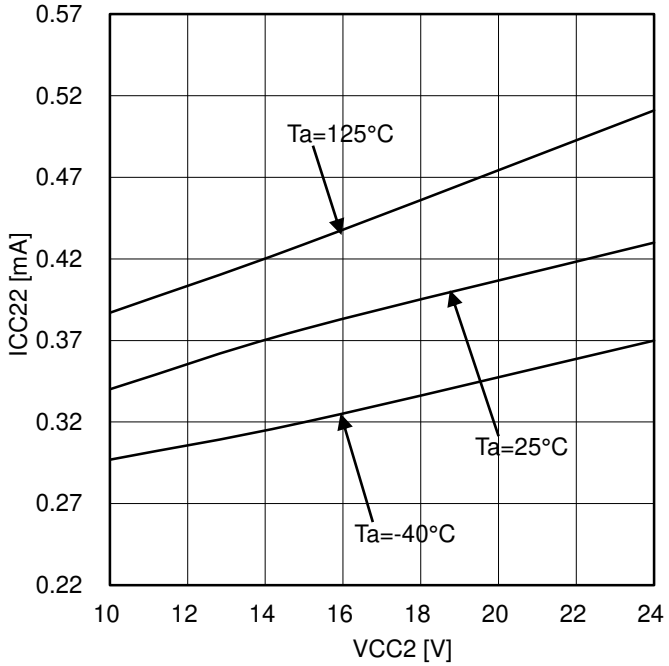


Figure 17. Output Side Circuit Current vs Output Side Supply Voltage (at OUT=H)

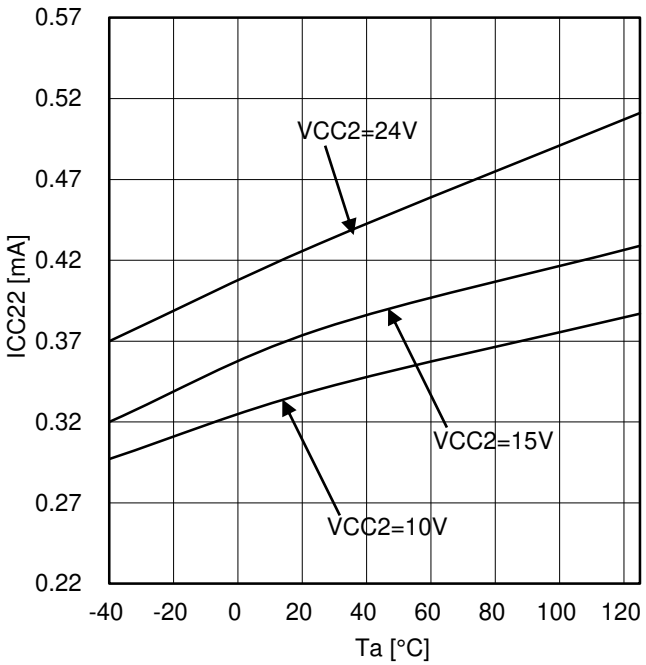


Figure 18. Output Side Circuit Current vs Temperature (at OUT=H)

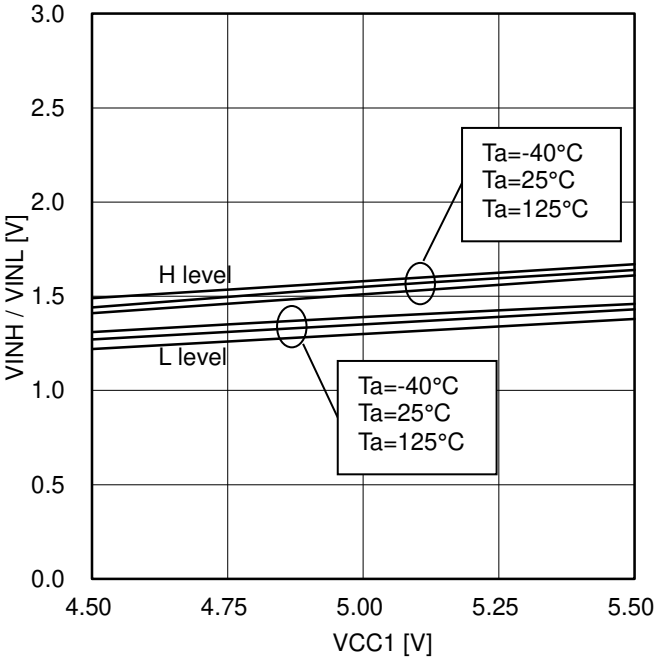


Figure 19. Logic (INA/INB) High/Low Level Voltage vs Input Side Supply Voltage

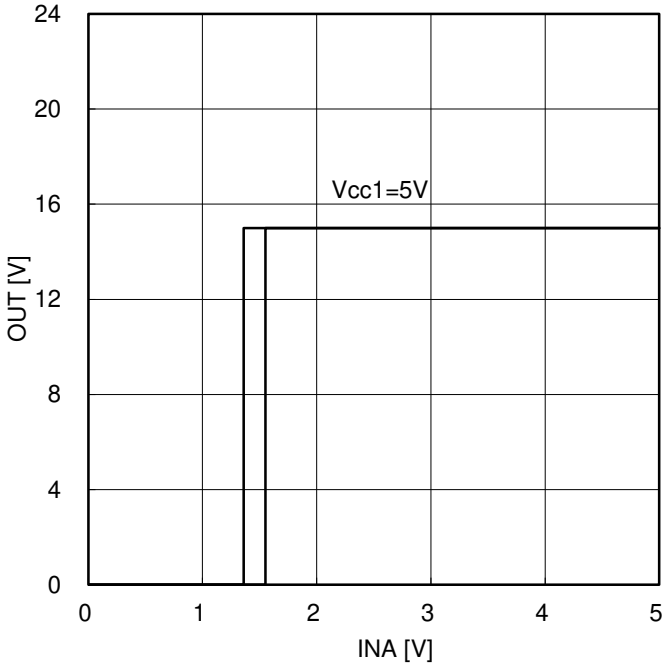


Figure 20. OUT vs Logic (INA) Input Voltage (VCC1=5V, VCC2=15V, Ta=25°C)

Typical Performance Curves - continued

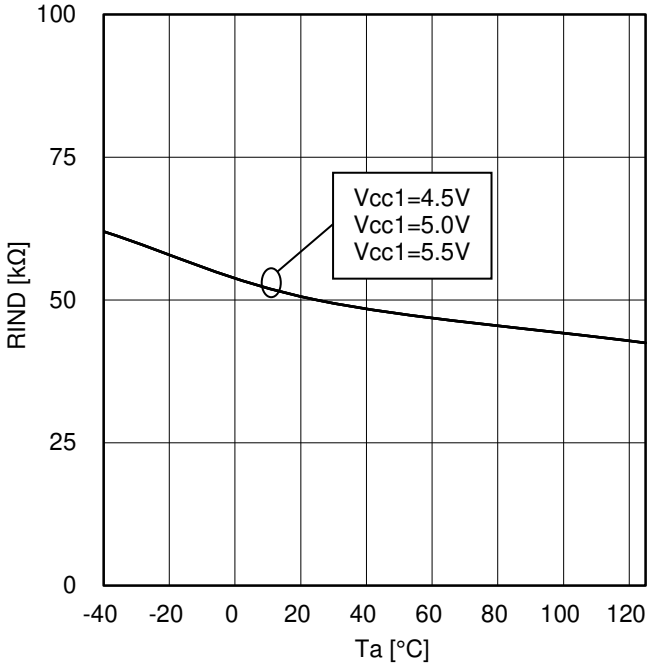


Figure 21. Logic Pull-down Resistance vs Temperature

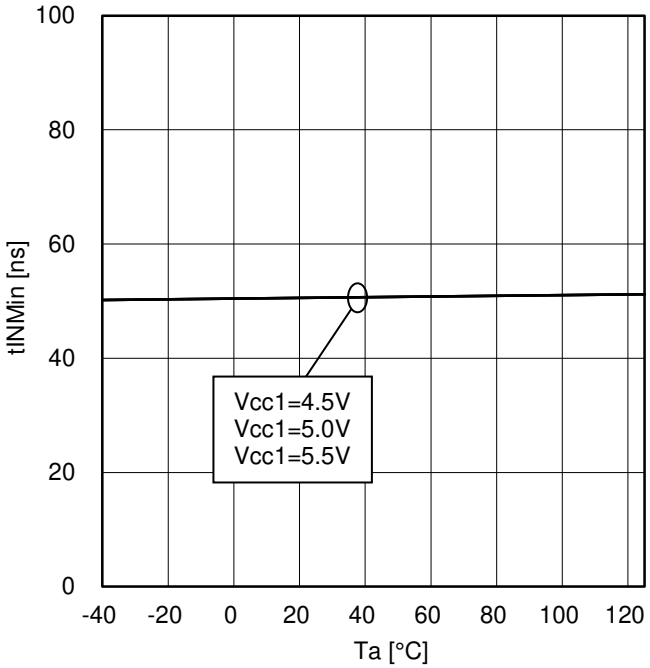


Figure 22. Logic (INA) Input Minimum Pulse Width vs Temperature

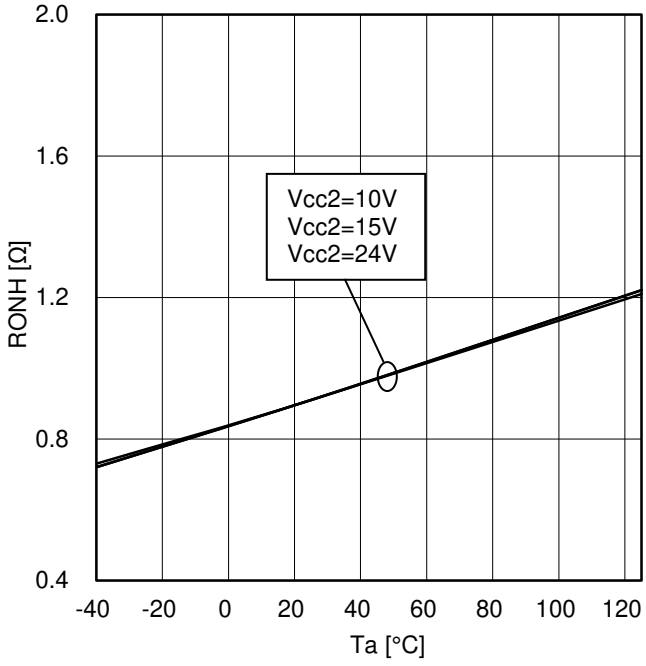


Figure 23. OUT ON Resistance (Source) vs Temperature

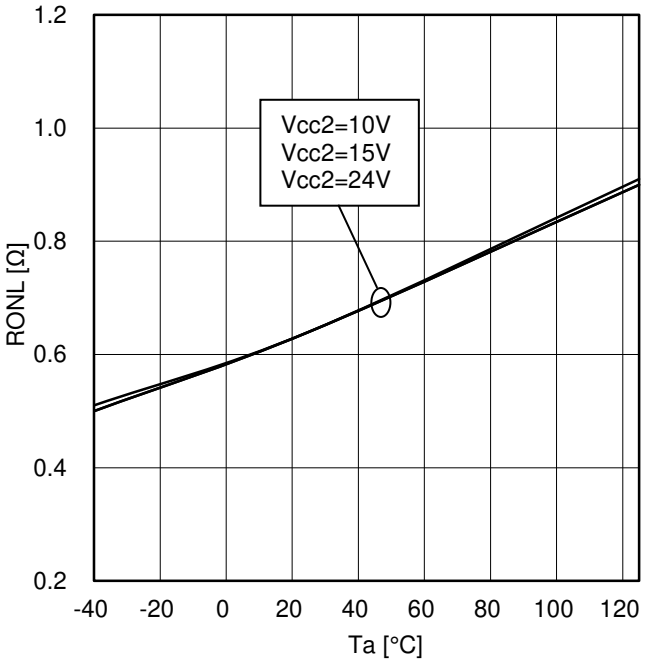


Figure 24. OUT ON Resistance (Sink) vs Temperature

Typical Performance Curves - continued

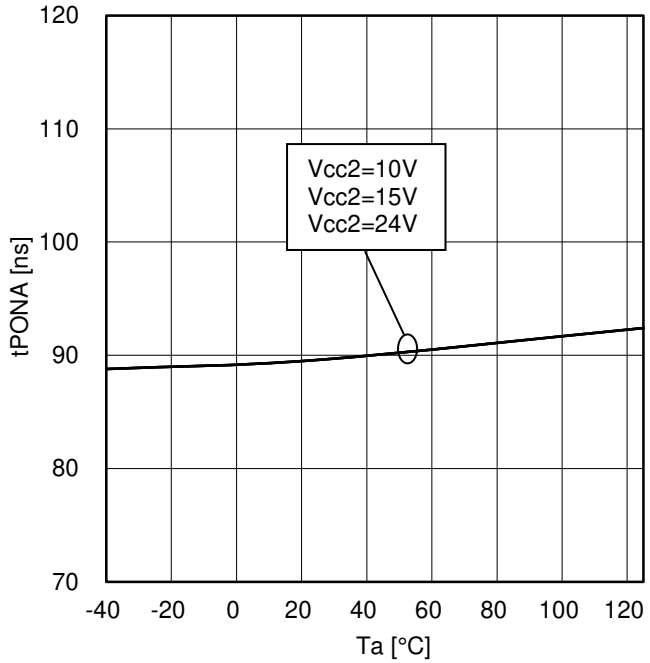


Figure 25. Turn ON Time vs Temperature
(INA=PWM, INB=L)

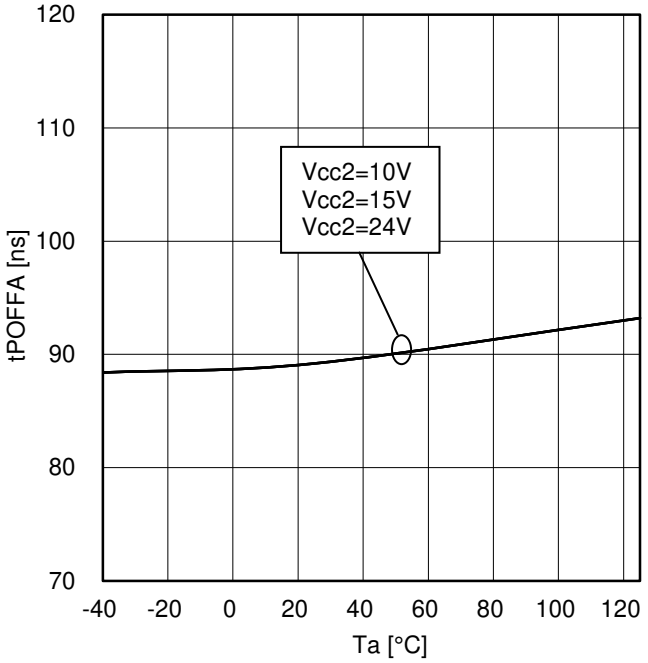


Figure 26. Turn OFF Time vs Temperature
(INA=PWM, INB=L)

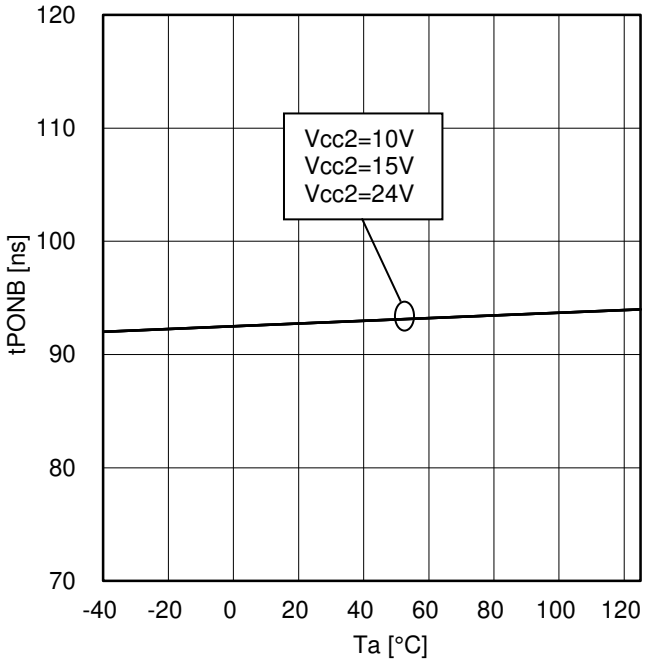


Figure 27. Turn ON Time vs Temperature
(INA=H, INB=PWM)

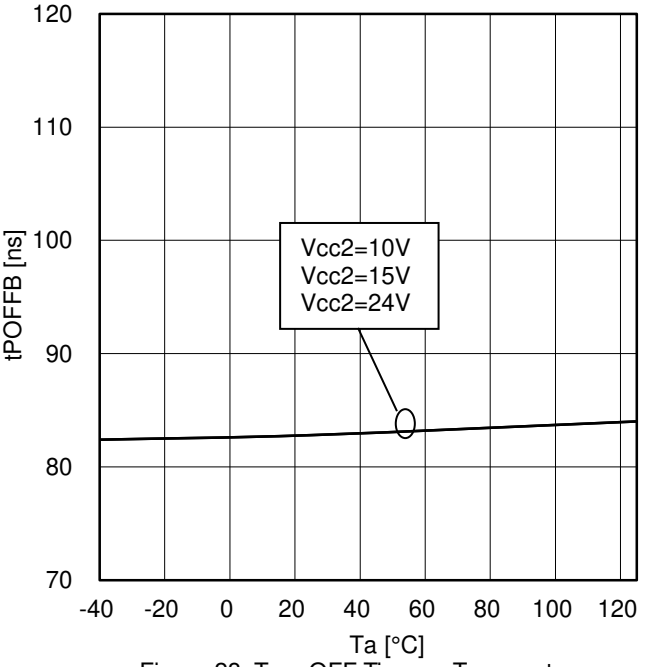


Figure 28. Turn OFF Time vs Temperature
(INA=H, INB=PWM)

Typical Performance Curves - continued

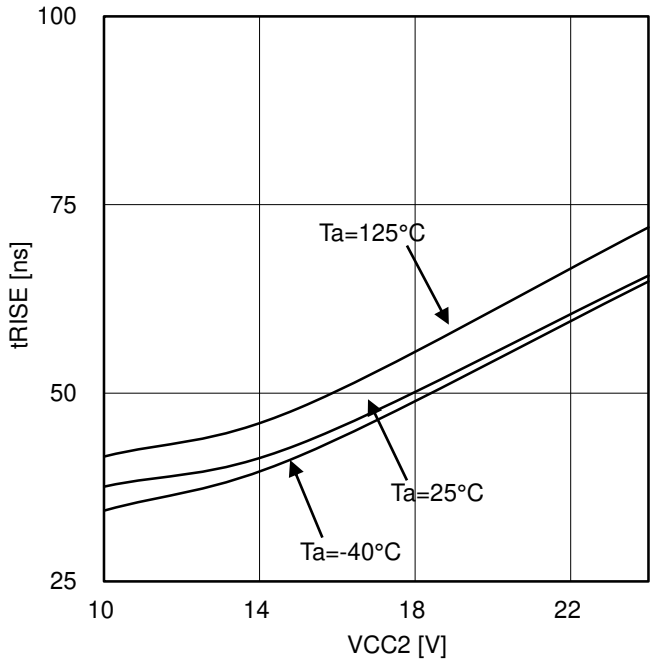


Figure 29. Rise Time vs Output Side Supply Voltage (10nF between OUT-GND2)

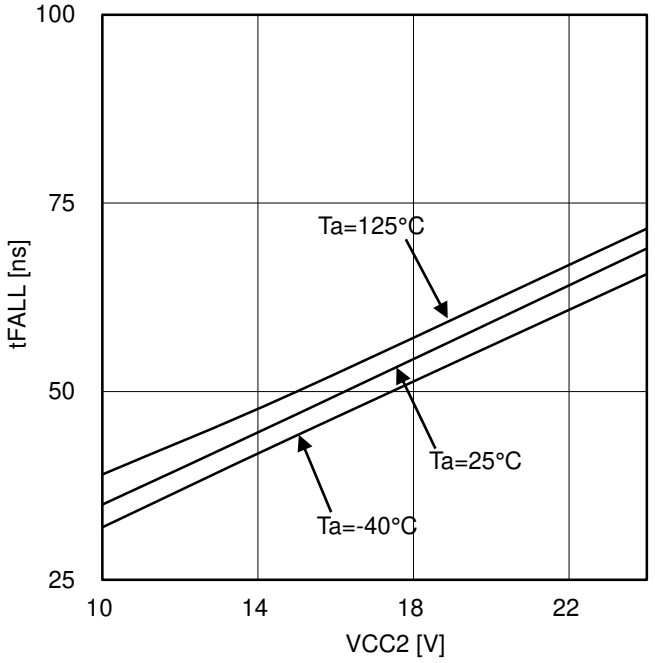


Figure 30. Fall Time vs Output Side Supply Voltage (10nF between OUT-GND2)

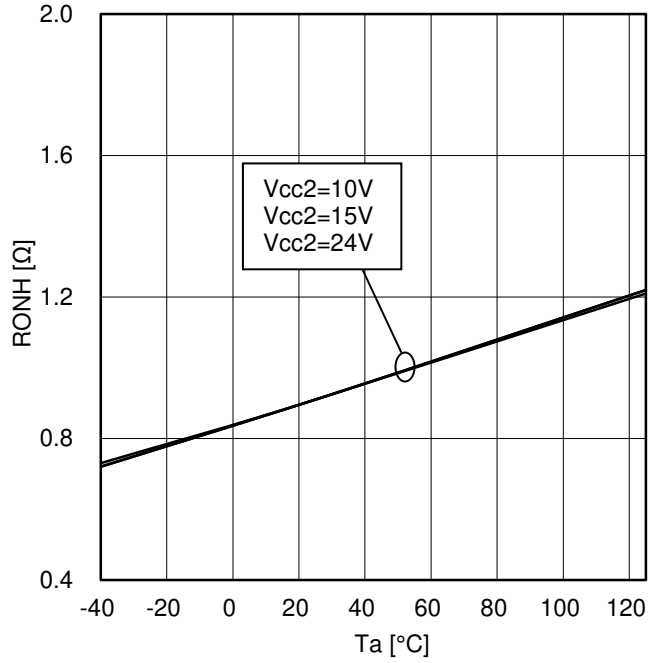


Figure 31. MC ON Resistance vs Temperature

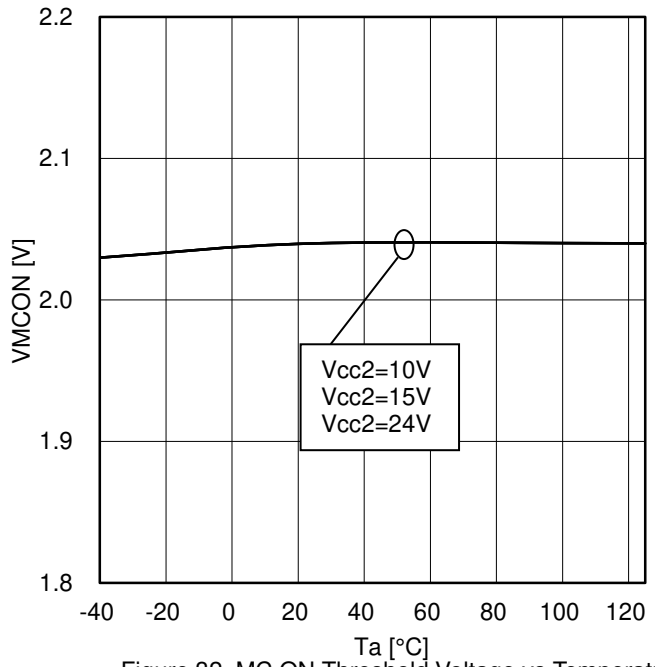


Figure 32. MC ON Threshold Voltage vs Temperature

Typical Performance Curves - continued

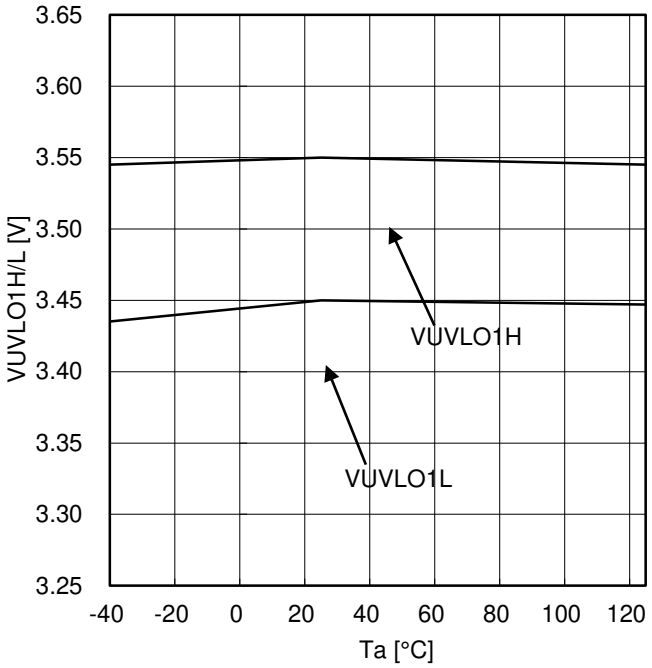


Figure 33. Input Side UVLO ON/OFF Voltage vs Temperature

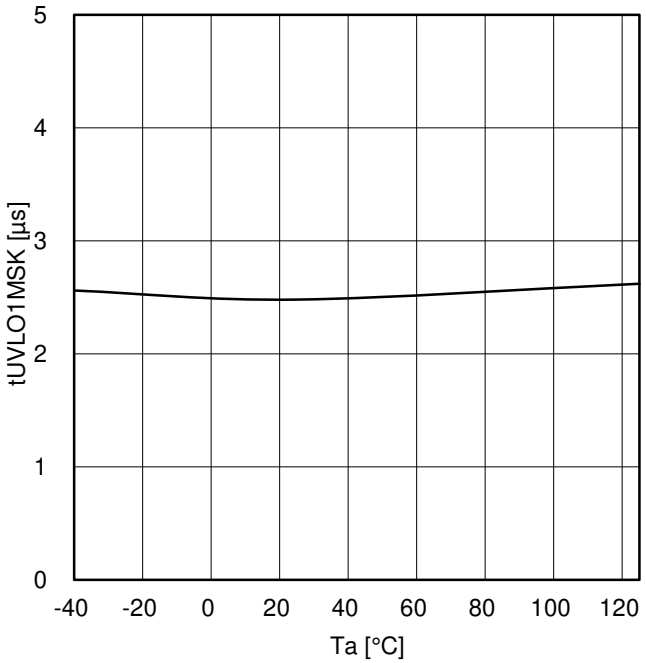


Figure 34. Input Side UVLO Mask Time vs Temperature

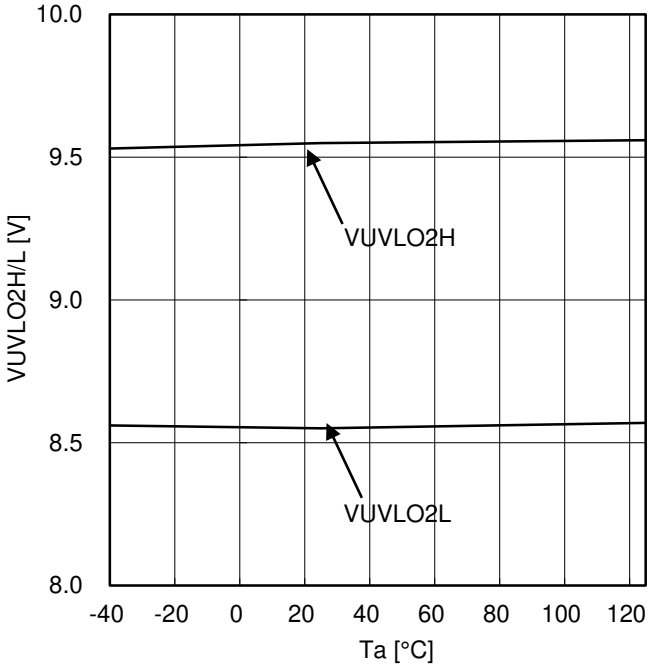


Figure 35. Output Side UVLO ON/OFF voltage vs Temperature

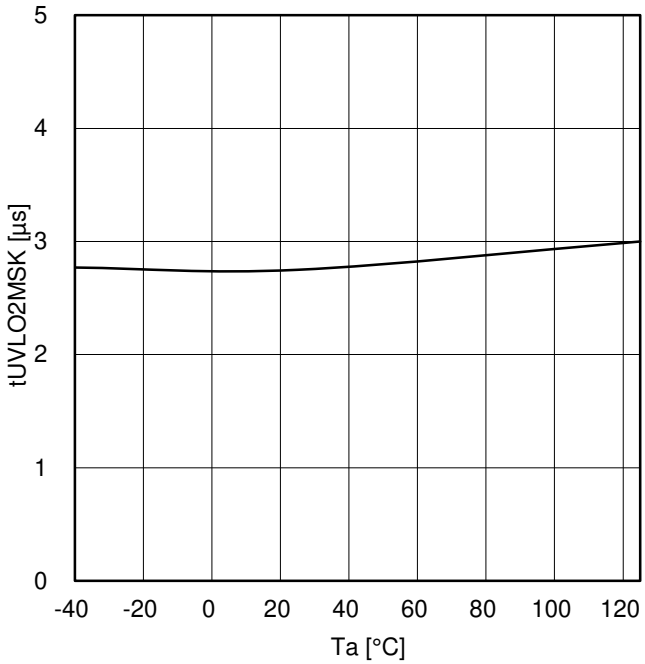


Figure 36. Output Side UVLO Mask Time vs Temperature

Typical Performance Curves - continued

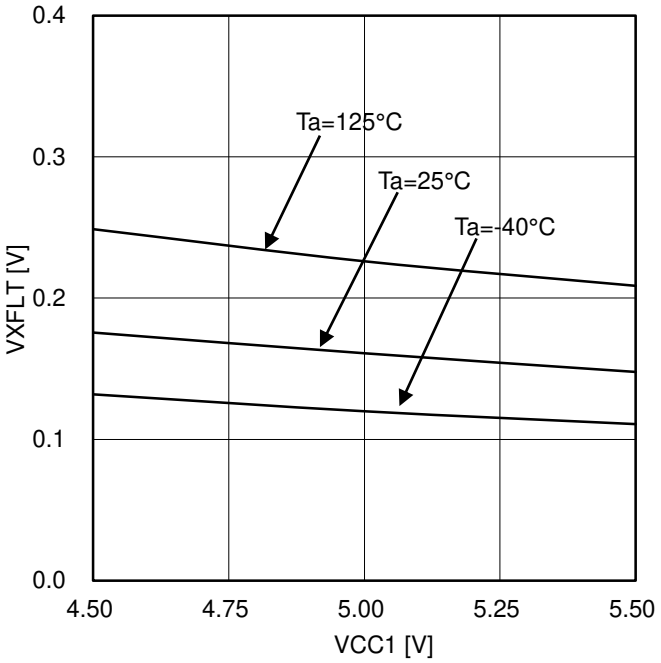


Figure 37. Output Low Voltage vs Input Side Supply Voltage (IXFLT=5mA)

Selection of Components Externally Connected

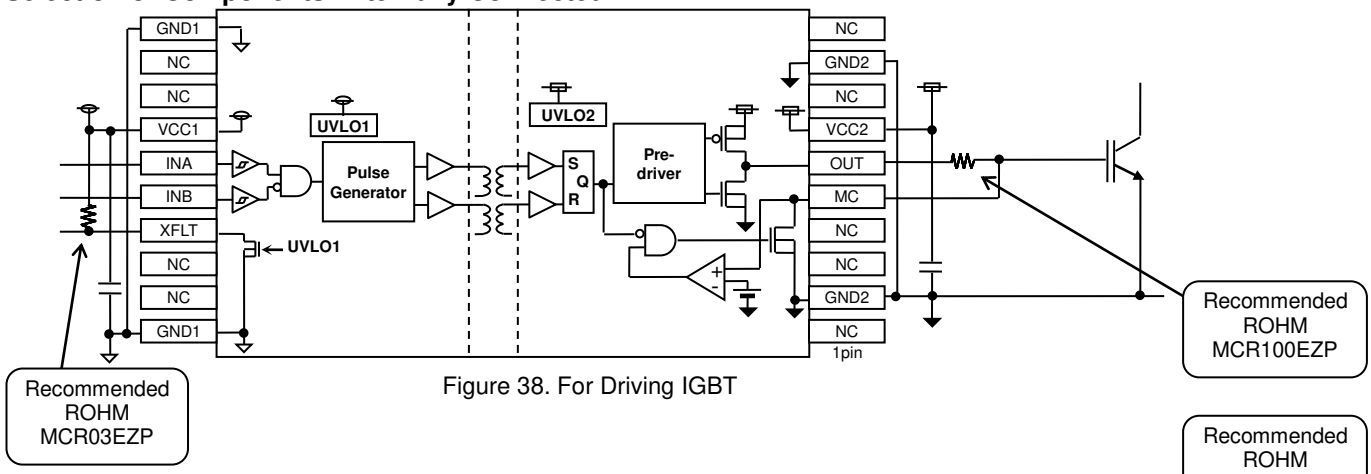


Figure 38. For Driving IGBT

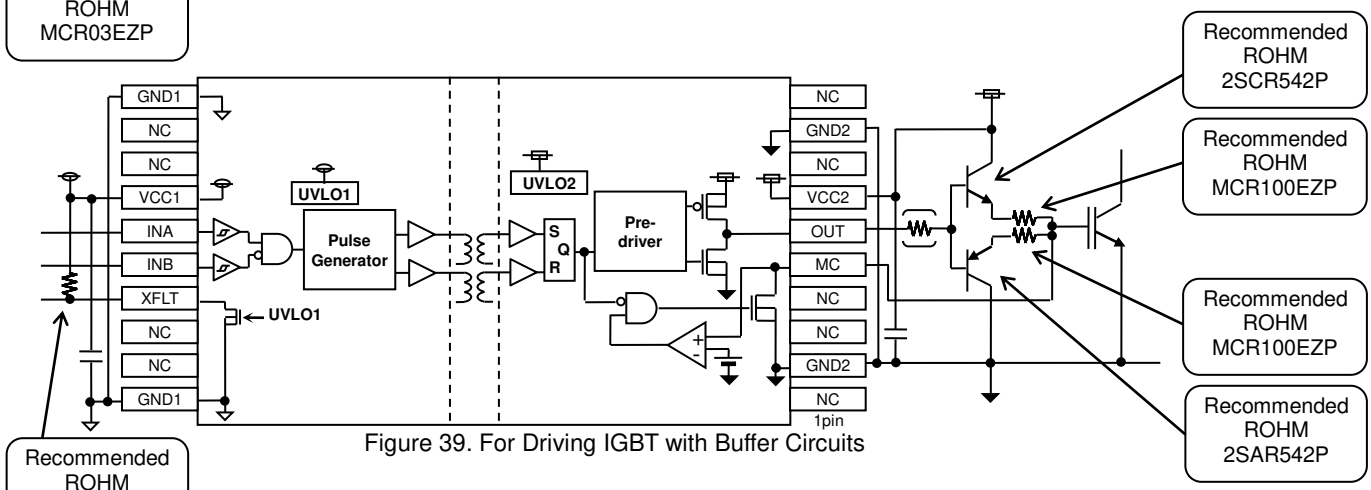


Figure 39. For Driving IGBT with Buffer Circuits

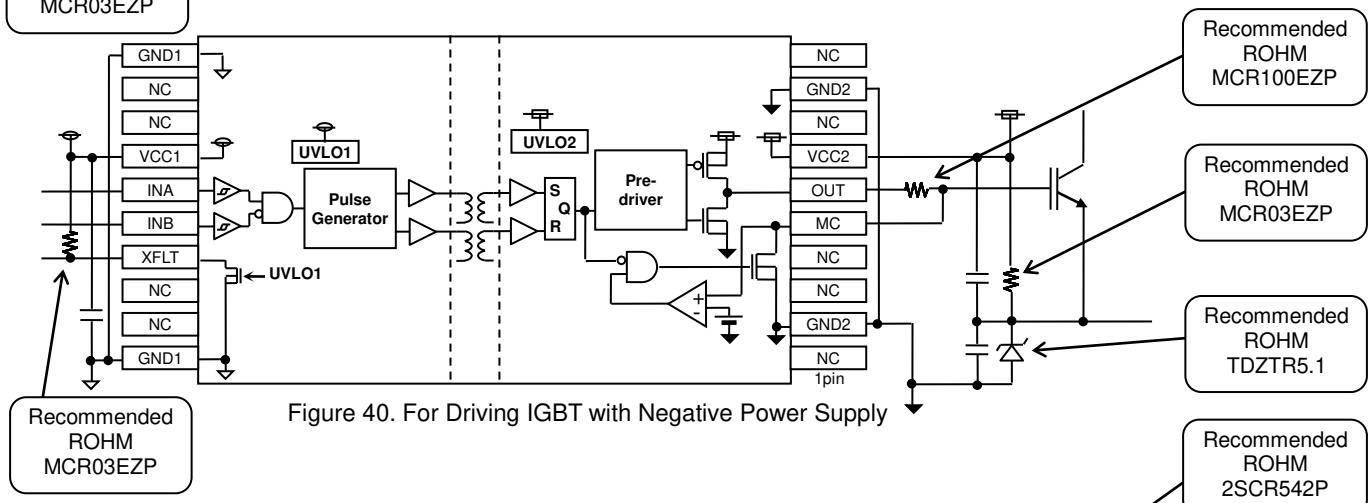


Figure 40. For Driving IGBT with Negative Power Supply

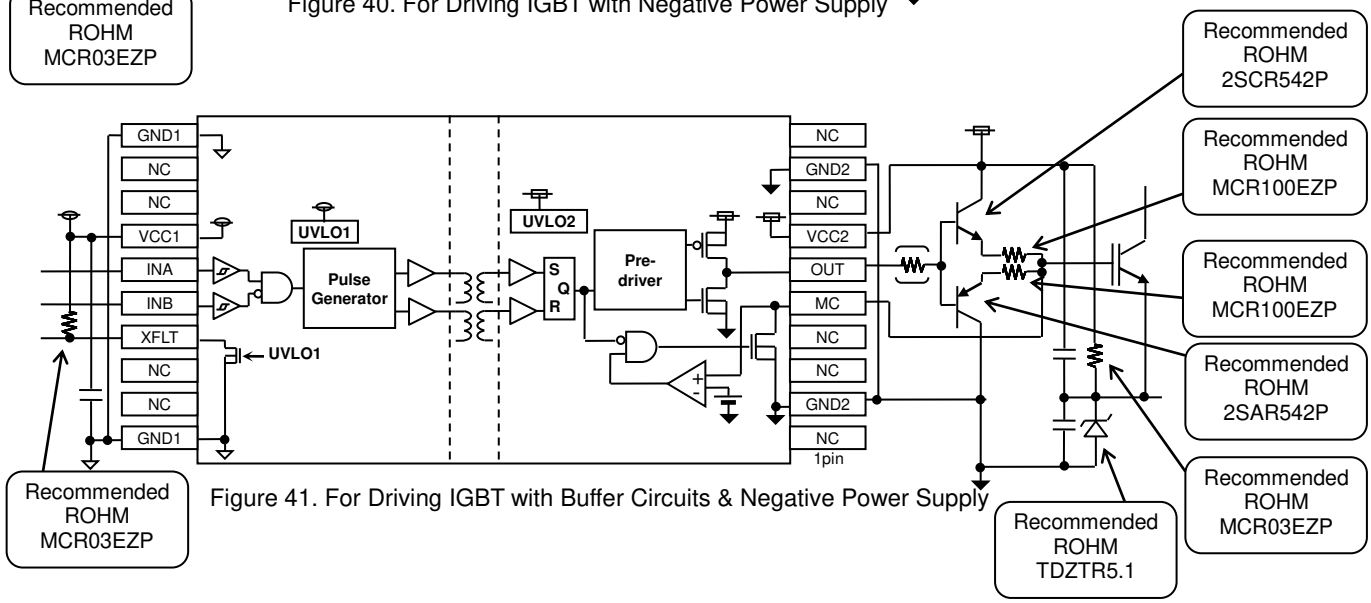


Figure 41. For Driving IGBT with Buffer Circuits & Negative Power Supply

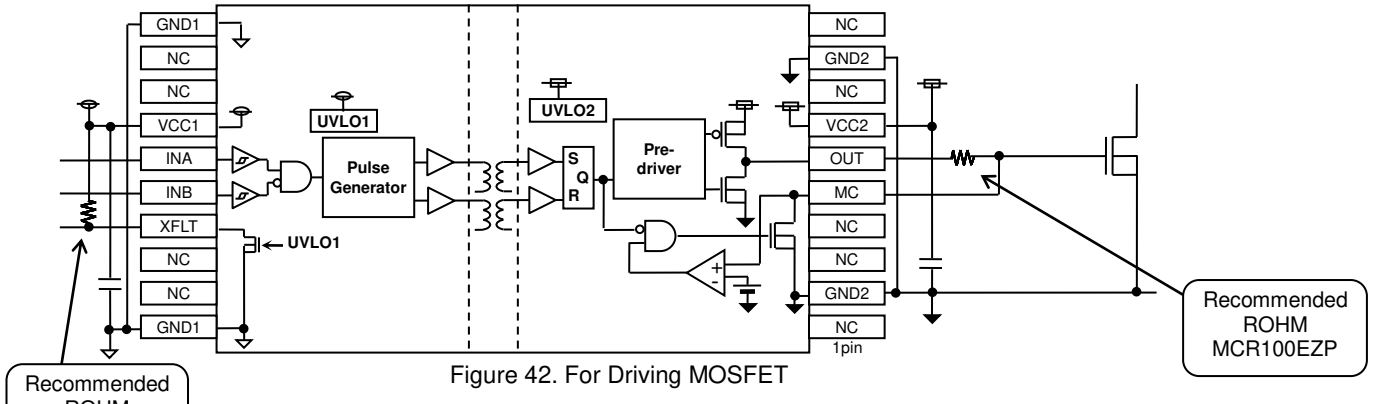


Figure 42. For Driving MOSFET

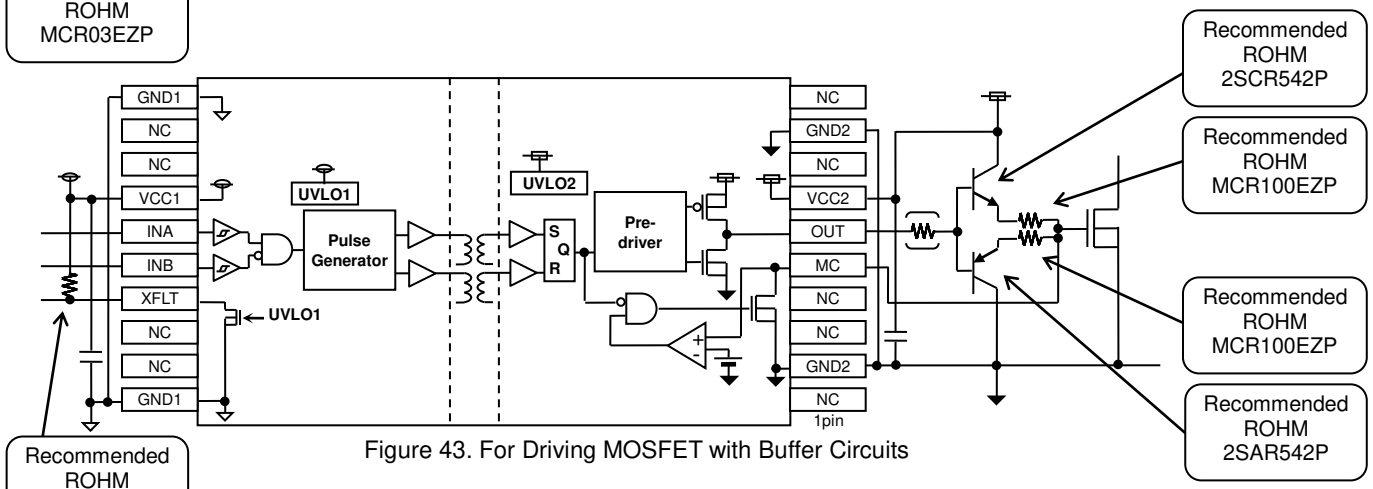


Figure 43. For Driving MOSFET with Buffer Circuits

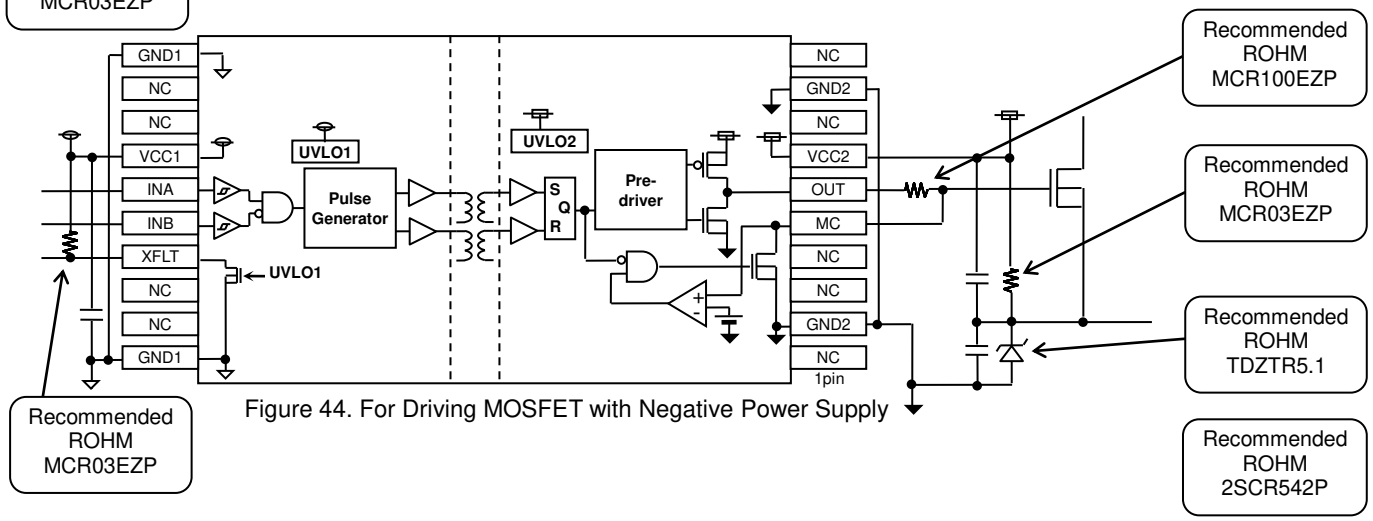


Figure 44. For Driving MOSFET with Negative Power Supply

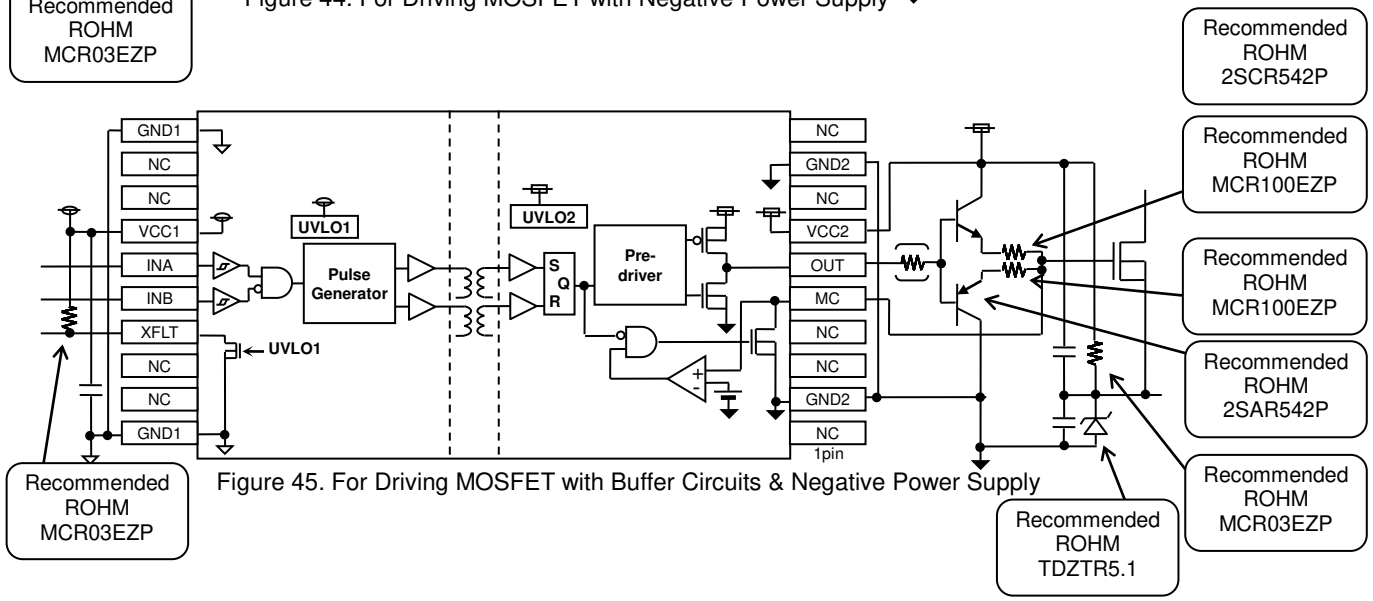


Figure 45. For Driving MOSFET with Buffer Circuits & Negative Power Supply

Power Dissipation

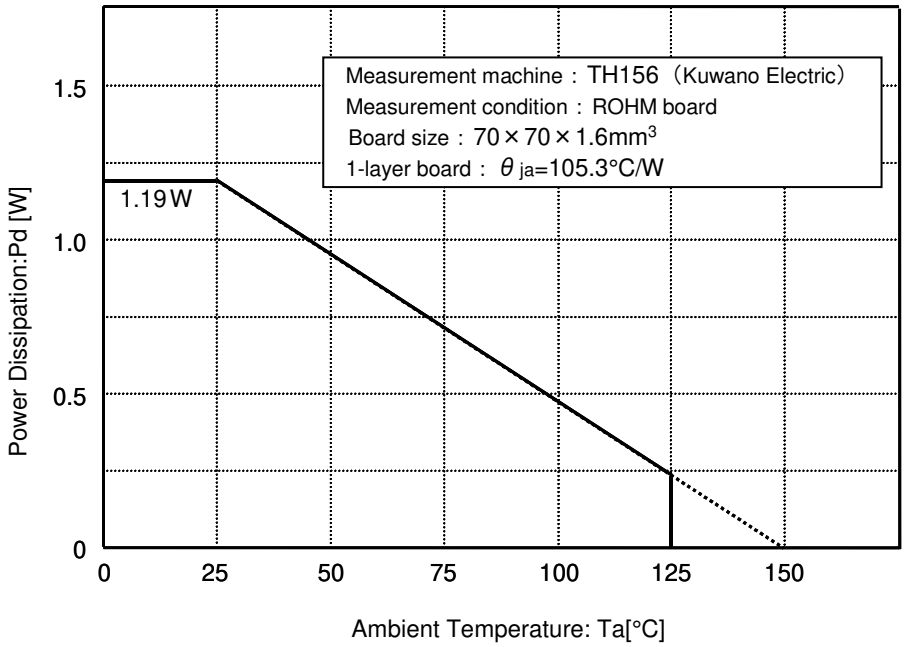
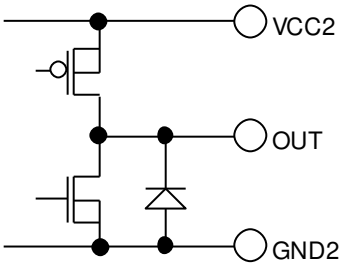
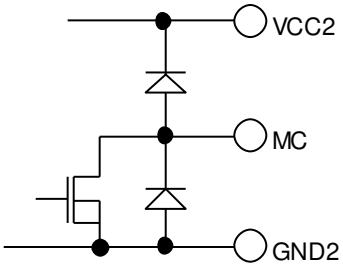
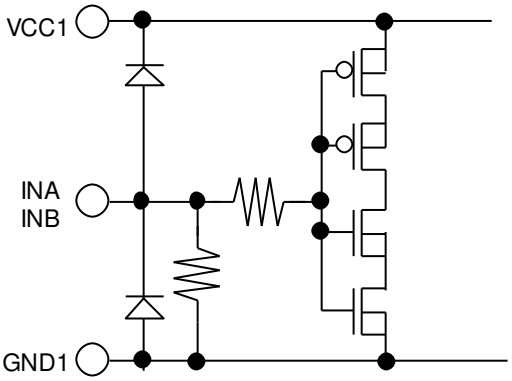
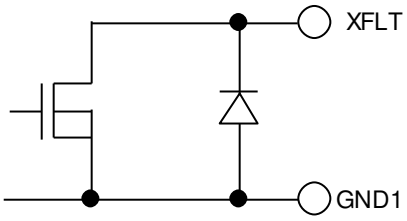


Figure 46. SSOP-B20W Derating Curve

Thermal Design

Please make sure that the IC's chip temperature Tj is not over 150°C, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150°C is exceeded, the function as a semiconductor will not operate and some problems (ex. Abnormal operation of various parasitic elements and increasing of leak current) occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. Tjmax=150°C must be strictly followed under all circumstances.

I/O Equivalent Circuits

Pin No	Name / Function	I/O equivalence circuits
1	OUT Output pin	
2	MC Output pin for Miller clamp	
3	INA Control input pin A INB Control input pin B	
4	XFLT Fault signal output pin	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

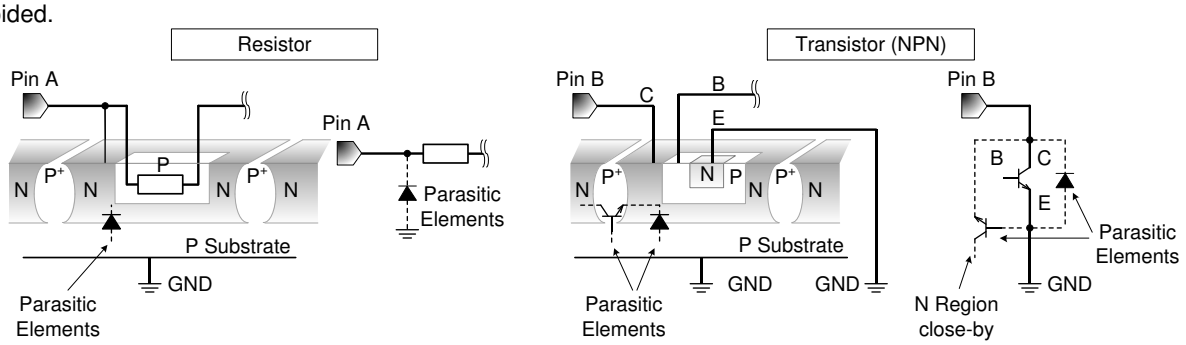


Figure 47. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

Ordering Information

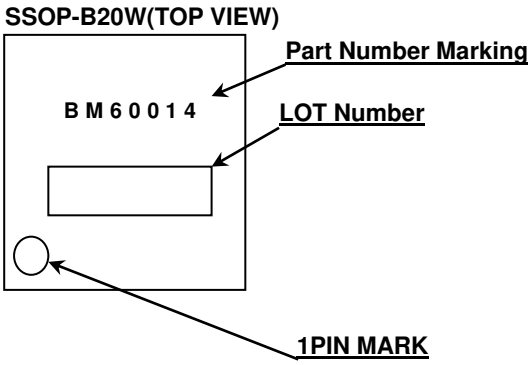
B M 6 0 0 1 4 F V	-	CE 2

Part Number

Package
FV:SSOP-B20W

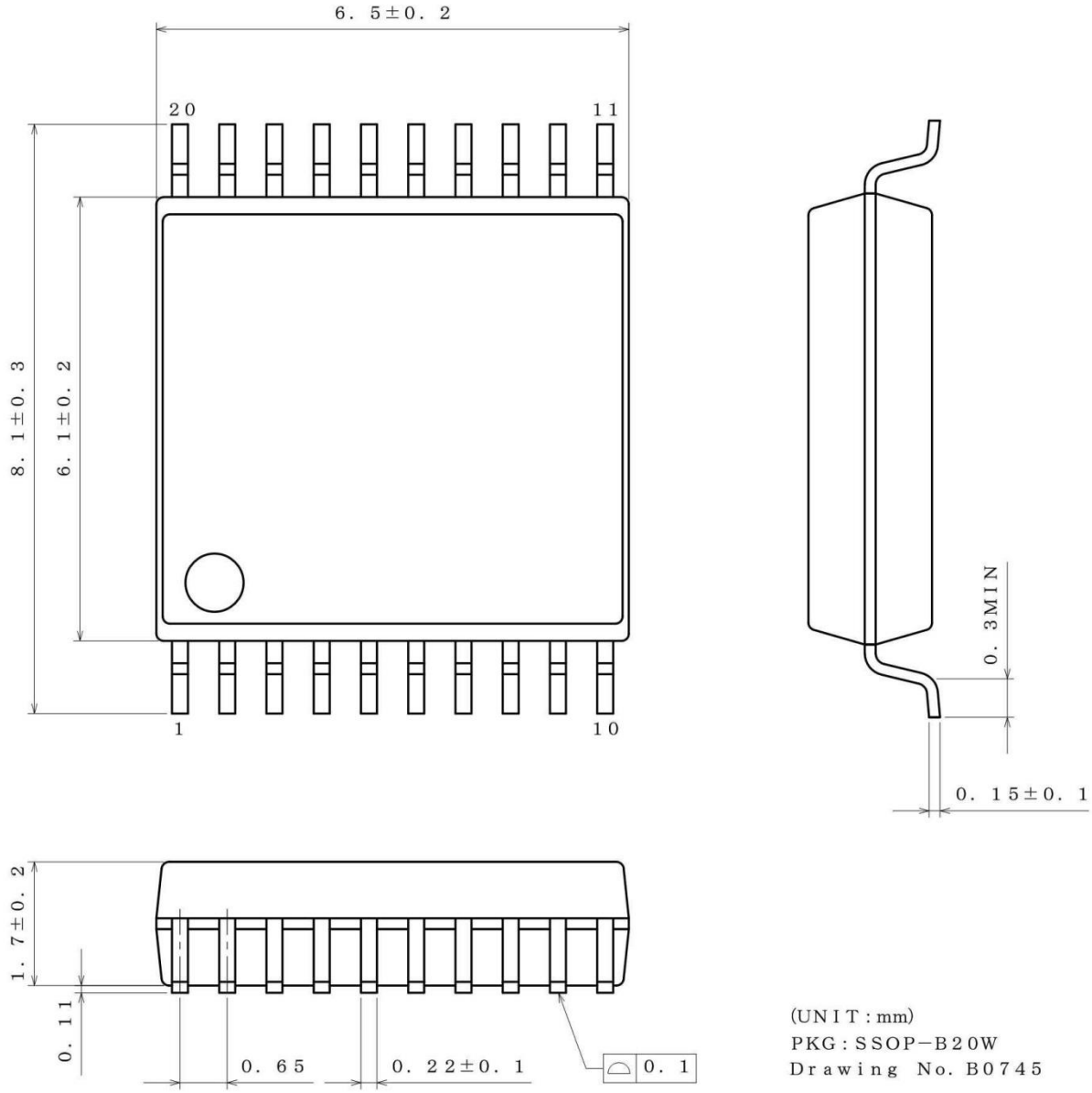
Product class
C: for Automotive applications
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagrams



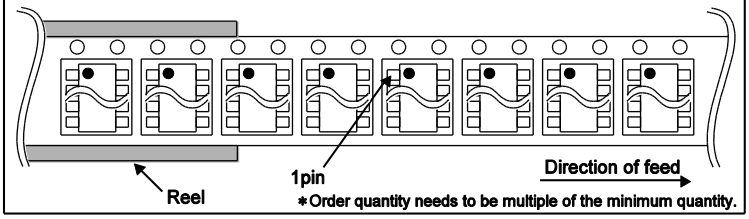
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B20W



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.