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Gate Driver Providing Galvanic isolation Series

Isolation voltage 2500Vrms 1ch Gate Driver Providing Galvanic Isolation

BM6104FV-C

General Description

The BM6104FV-C is a gate driver with isolation voltage 2500Vrms, I/O delay time of 150ns, and minimum input pulse width of 90ns, and incorporates the fault signal output functions, undervoltage lockout (UVLO) function, and short current protection (SCP, DESAT) function.

Features

- Providing Galvanic Isolation
- Active Miller Clamping
- Fault Signal Output Function (Adjustable Output Holding Time)
- Undervoltage Lockout Function
- Short Current Protection Function (Adjustable Reset Time)
- Soft Turn-Off Function For Short Current Protection (Adjustable Turn-Off Time)
- Supporting Negative VEE2
- Output State Feedback Function
- UL1577 Recognized:File No. E356010
- AEC-Q100 Qualified(Note 1) (Note 1:Grade1)

Key Specifications

- Isolation Voltage: 2500Vrms
- Maximum Gate Drive Voltage: 24V
- I/O Delay Time: 150ns(Max)
- Minimum Input Pulse Width: 90ns(Max)

Package

	W(Typ) x D(Typ) x H(Max)
SSOP-B20W	6.50mm x 8.10mm x 2.01mm

Applications

- IGBT Gate Driver
- MOSFET Gate Driver

Typical Application Circuits

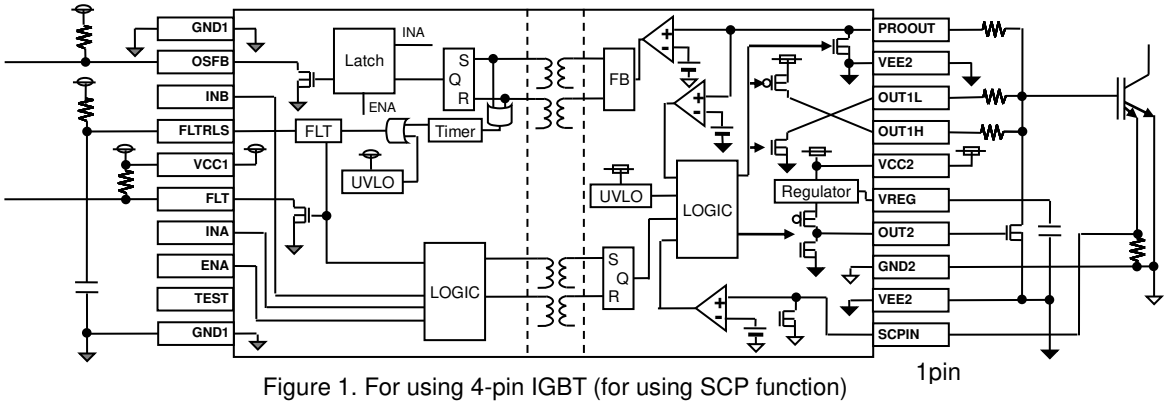


Figure 1. For using 4-pin IGBT (for using SCP function)

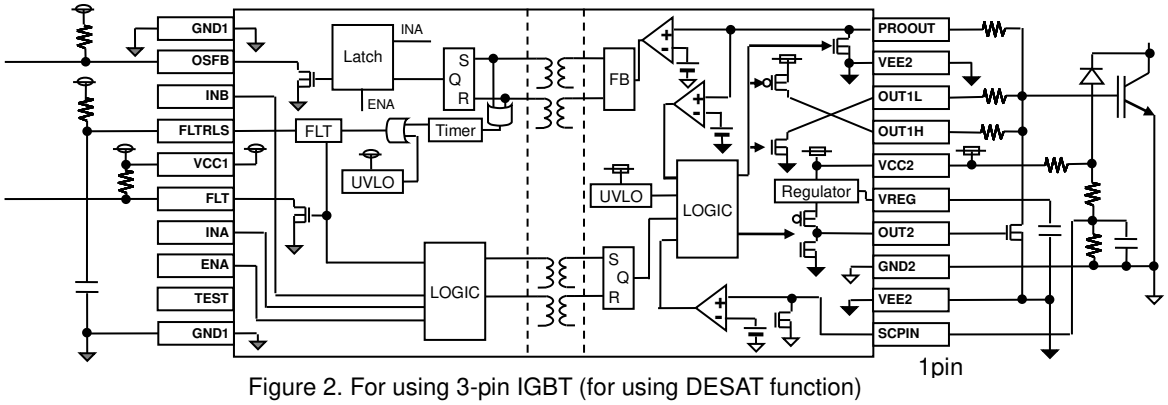


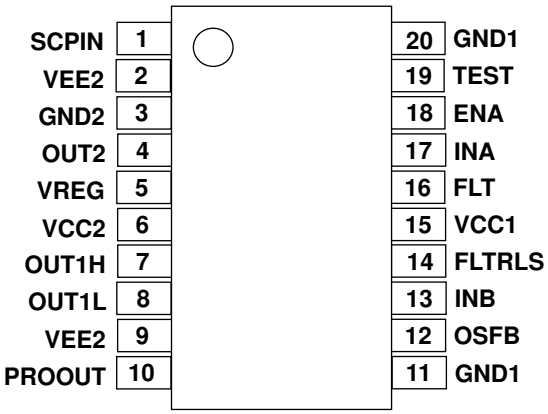
Figure 2. For using 3-pin IGBT (for using DESAT function)

Recommended Range Of External Constants

Pin Name	Symbol	Recommended Value			Unit
		Min	Typ	Max	
FLTRLS	C_{FLTRLS}	-	0.01	0.47	µF
	R_{FLTRLS}	50	200	1000	kΩ
VREG	C_{VREG}	1.0	3.3	10.0	µF
VCC1	C_{VCC1}	0.1	1.0	-	µF
VCC2	C_{VCC2}	0.33	-	-	µF

Pin Configurations

(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1	SCPIN	Short current detection pin
2	VEE2	Output-side negative power supply pin
3	GND2	Output-side ground pin
4	OUT2	MOSFET control pin for Miller Clamp
5	VREG	Power supply pin for driving MOSFET for Miller Clamp
6	VCC2	Output-side positive power supply pin
7	OUT1H	Source side output pin
8	OUT1L	Sink side output pin
9	VEE2	Output-side negative power supply pin
10	PROOUT	Soft turn-off pin
11	GND1	Input-side ground pin
12	OSFB	Output state feedback output pin
13	INB	Control input pin B
14	FLTRLS	Fault output holding time setting pin
15	VCC1	Input-side power supply pin
16	FLT	Fault output pin
17	INA	Control input pin A
18	ENA	Input enabling signal input pin
19	TEST	Mode setting pin
20	GND1	Input-side ground pin

Description of pins and cautions on layout of board

1) VCC1 (Input-side power supply pin)
The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2) GND1 (Input-side ground pin)
The GND1 pin is a ground pin on the input side.

3) VCC2 (Output-side positive power supply pin)
The VCC2 pin is a positive power supply pin on the output side. To reduce voltage fluctuations due to OUT1H/L pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VCC2 and the GND2 pins.

4) VEE2 (Output-side negative power supply pin)
The VEE2 pin is a power supply pin on the output side. To suppress voltage fluctuations due to OUT1H/L pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VEE2 and the GND2 pins. To use no negative power supply, connect the VEE2 pin to the GND2 pin.

5) GND2 (Output-side ground pin)
The GND2 pin is a ground pin on the output side. Connect the GND2 pin to the emitter / source of a power device.

6) IN (Control input terminal)
The IN is a pin used to determine output logic.

ENA	INB	INA	OUT1H	OUT1L
H	X	X	Hi-Z	L
L	H	L	Hi-Z	L
L	H	H	Hi-Z	L
L	L	L	Hi-Z	L
L	L	H	H	Hi-Z

7) FLT (Fault output pin)
The FLT pin is an open drain pin used to output a fault signal when a fault occurs (i.e., when the undervoltage lockout function (UVLO) or short current protection function (SCP) is activated).

Pin	FLT
While in normal operation	Hi-Z
When an Fault occurs (When UVLO or SCP is activated)	L

8) FLTRLS (Fault output holding time setting pin)
The FLTRLS is a pin used to make setting of time to hold a Fault signal. Connect a capacitor between the FLTRLS pin and the GND1 pin, and a resistor between it and the VCC1 pin.
The Fault signal is held until the FLTRLS pin voltage exceeds a voltage set with the V_{FLTRLS} parameter. To set holding time to 0 ms, do not connect the capacitor. Short-circuiting the FLTRLS pin to the VCC1 pin will cause a high current to flow in the FLTRLS pin and, in an open state, may cause the IC to malfunction. To avoid such trouble, be sure to connect a resistor between the FLTRLS and the VCC1 pins.

9) OUT1H, OUT1L (Output pin)
The OUT1H pin is a source side pin used to drive the gate of a power device, and the OUT1L pin is a sink side pin used to drive the gate of a power device.

10) OUT2 (MOSFET control pin for Miller Clamp)
The OUT2 is a pin for controlling the external MOS switch to prevent the increase in gate voltage due to the miller current of the power device connected to OUT1H/L pin.

11) VREG (Power supply pin for driving the MOSFET for Miller Clamp)
The VREG pin is a power supply pin for Miller Clamp (typ 10V). Be sure to connect a capacitor between VREG pin and VEE2 pin to prevent oscillation and to reduce voltage fluctuations due to OUT2 pin output current.

12) PROOUT (Soft turn-off pin)
The PROOUT is a pin used to put the soft turn-off function of a power device in operation when the SCP function is activated. This pin combines with the gate voltage monitoring pin for Miller Clamp function and OSFB function which output the gate state.

13) SCPIN (Short current detection pin)
The SCPIN is a pin used to detect current for short current protection. When the SCPIN pin voltage exceeds V_{SCDET} (typ 0.7V), the SCP function will be activated. This may cause the IC to malfunction in an open state. To avoid such trouble, short-circuit the SCPIN pin to the GND2 pin if the short current protection is not used. In order to prevent the wrong detection due to noise, the noise mask time t_{SCPMSK} (typ 0.8µs) is set.

14) OSFB (Output state feedback output pin)
The OSFB pin is an open drain pin used to output the gate state. If the IN and the OUT1H/L pin are at the same level, the OSFB pin output the “Hi-Z” level, otherwise the OSFB pin output the “L” level and hold “L” until ENA=H or UVLO on low voltage side is activated.

15) TEST(Mode setting pin)
The TEST pin is an operation mode setting pin. This pin is usually connected to GND1 pin. If the TEST pin is connected to the VCC1 pin, Input-side UVLO function is disabled.

Description of functions and examples of constant setting

1) Miller Clamp function
When OUT1H/L=Hi-Z/L and PROOUT pin voltage < V_{OUT2ON} (typ 2V), H is output from OUT2 pin and the external MOS switch is turned ON. When OUT1H/L=H/Hi-Z, L is output from OUT2 pin and the external MOS switch is turned OFF. While the short-circuit protection function is activated, L is output from OUT2 pin and the external MOS switch is turned OFF.

Short current	SCPIN	IN	PROOUT	OUT2
Detected	Not less than V_{SCDET}	X	X	L
Not detected	X	L	Not less than V_{OUT2ON}	L
	X	L	less than V_{OUT2ON}	H
	X	H	X	L

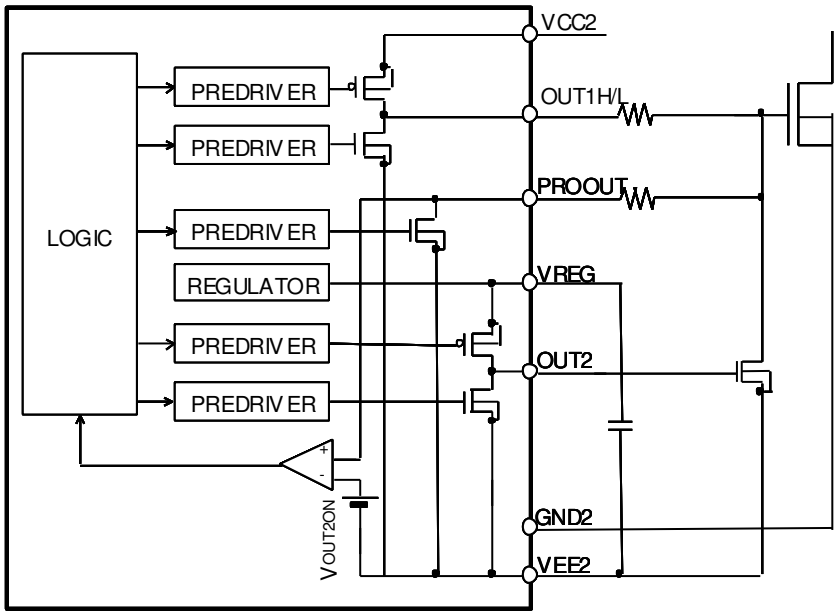


Figure 3. Block diagram of Miller Clamp function.

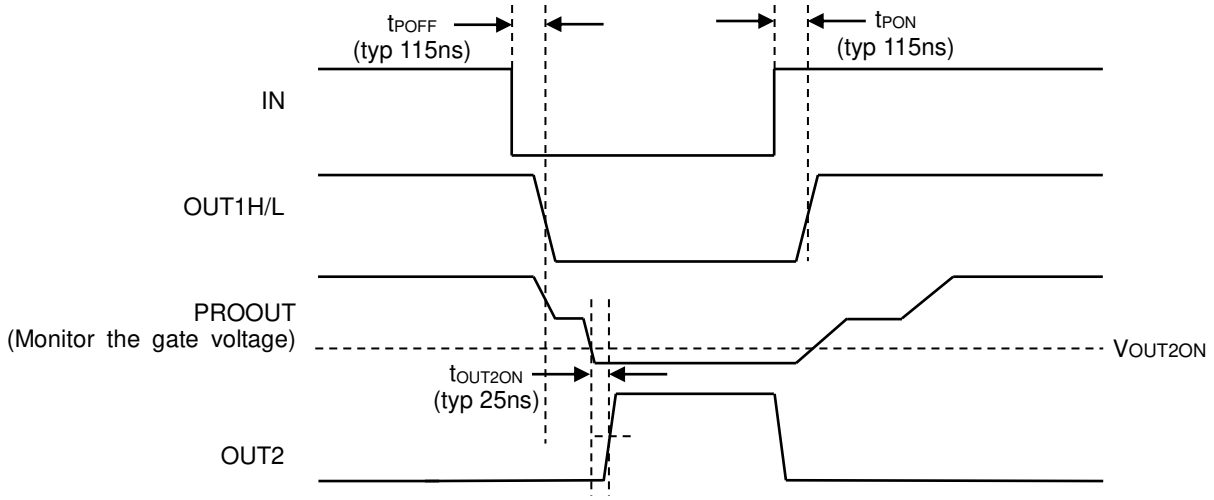


Figure 4. Timing chart of Miller Clamp function

2) Fault status output

This function is used to output a fault signal from the FLT pin when a fault occurs (i.e., when the undervoltage lockout function (UVLO) or short current protection function (SCP) is activated) and hold the Fault signal until the set Fault output holding time is completed. The Fault output holding time t_{FLTRLS} is given as the following equation with the settings of capacitor C_{FLTRLS} and resistor R_{FLTRLS} connected to the FLTRLS pin. For example, when C_{FLTRLS} is set to 0.01μF and R_{FLTRLS} is set to 200kΩ, the holding time will be set to 2 ms.

t_{FLTRLS} [ms]= C_{FLTRLS} [µF]•R_{FLTRLS} [kΩ]

To set the fault output holding time to “0” ms, only connect the resistor R_{FLTRLS}.

Status	FLT pin
Normal	Hi-Z
Fault occurs	L

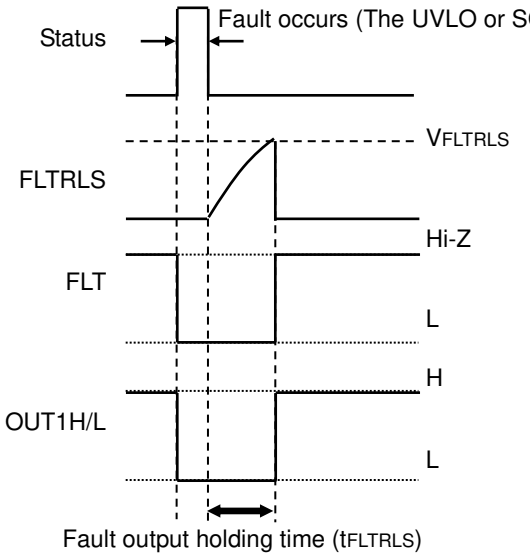


Figure 5. Fault Status Output Timing Chart

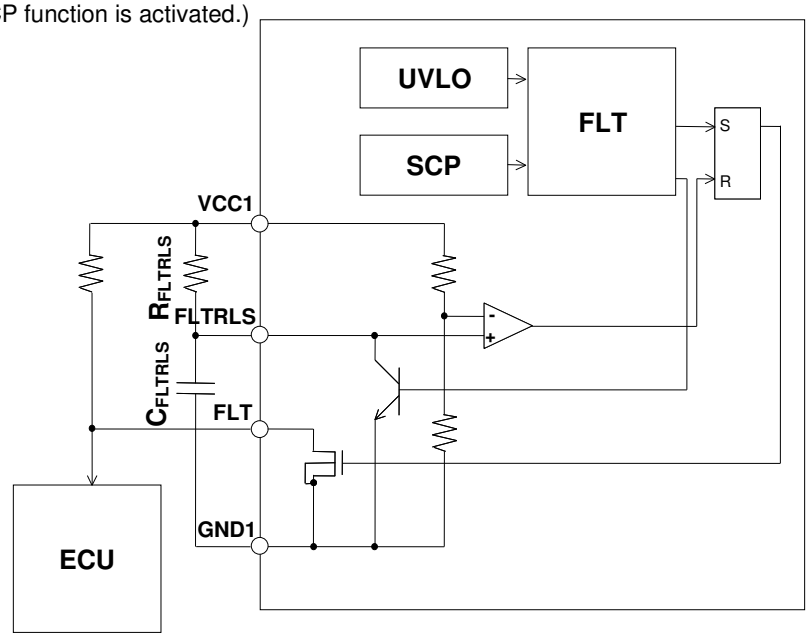


Figure 6. Fault Output Block Diagram

3) Undervoltage Lockout (UVLO) function

The BM6104FV-C incorporates the undervoltage lockout (UVLO) function both on the low and the high voltage sides. When the power supply voltage drops to the UVLO ON voltage (low voltage side typ 3.4V, high voltage side typ 9.05V), the OUT1 and the FLT pin both will output the “L” signal. When the power supply voltage rises to the UVLO OFF voltage (low voltage side typ 3.5V, high voltage side typ 9.55V), these pins will be reset. However, during the fault output holding time set in “2) Fault status output” section, the OUT1 pin and the FLT pin will hold the “L” signal. In addition, to prevent malfunctions due to noises, mask time $t_{UVLO1MSK}$ (typ 10µs) and $t_{UVLO2MSK}$ (typ 10µs) are set on both low and high voltage sides.

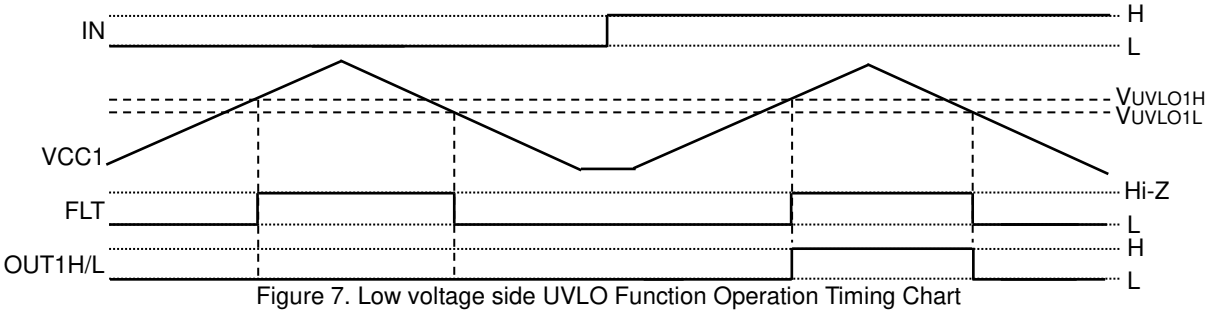


Figure 7. Low voltage side UVLO Function Operation Timing Chart

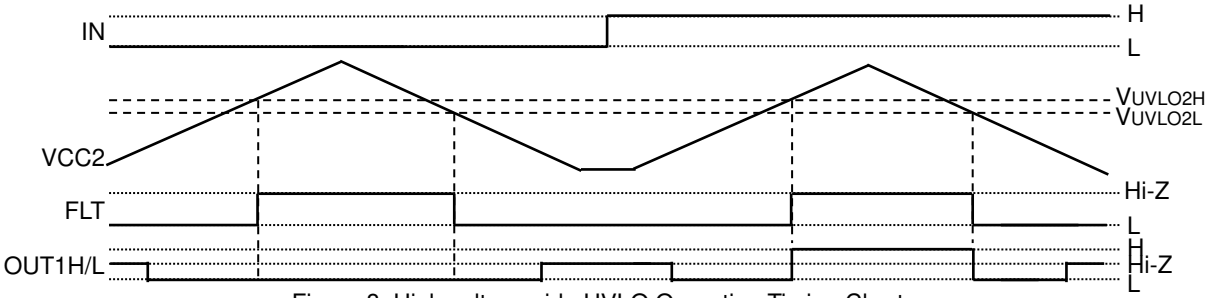


Figure 8. High voltage side UVLO Operation Timing Chart

4) Short current protection function (SCP, DESAT)

When the SCPIN pin voltage exceeds V_{SCDET} (typ 0.7V), the SCP function will be activated. When the SCP function is activated, the OUT1H/L pin voltage will be set to the “Hi-Z/HiZ” level first, and then the PROOUT pin voltage to the “L” level (soft turn-off).Next, after t_{STO} (min 30µs, max 110µs) has passed after the short-circuit current falls below the threshold value, OUT1H/L pin becomes HiZ/L and PROOUT pin becomes L. Finally, when the fault output holding time set in “2) fault status output” section on page 5 is completed, the SCP function will be released.

$V_{COLLECTOR}/V_{DRAIN}$ which Desaturation Protection starts operation (V_{DESAT}) and the blanking time (t_{BLANK}) can be calculated by the formula below;

$$V_{DESAT}[V] = V_{SCDET} \bullet \frac{R3+R2}{R3} - V_{F_{D1}}$$

$$V_{CC2_{MIN}}[V] > V_{SCDET} \bullet \frac{R3+R2+R1}{R3}$$

$$t_{BLANKoutemal}[s] = -\frac{R2+R1}{R3+R2+R1} \bullet R3 \bullet (C_{BLANK} + 24 \bullet 10^{-12}) \bullet \ln(1 - \frac{R3+R2+R1}{R3} \bullet \frac{V_{SCDET}}{V_{CC2}}) + 0.2 \bullet 10^{-6}$$

V_{DESAT}	Reference Value		
	R1	R2	R3
4.0V	15 kΩ	39 kΩ	6.8 kΩ
4.5V	15 kΩ	43 kΩ	6.8 kΩ
5.0V	15 kΩ	36 kΩ	5.1 kΩ
5.5V	15 kΩ	39 kΩ	5.1 kΩ
6.0V	15 kΩ	43 kΩ	5.1 kΩ
6.5V	15 kΩ	62 kΩ	6.8 kΩ
7.0V	15 kΩ	68 kΩ	6.8 kΩ
7.5V	15 kΩ	82 kΩ	7.5 kΩ
8.0V	15 kΩ	91 kΩ	8.2 kΩ
8.5V	15 kΩ	82 kΩ	6.8 kΩ
9.0V	15 kΩ	130 kΩ	10 kΩ
9.5V	15 kΩ	91 kΩ	6.8 kΩ
10.0V	15 kΩ	130 kΩ	9.1 kΩ

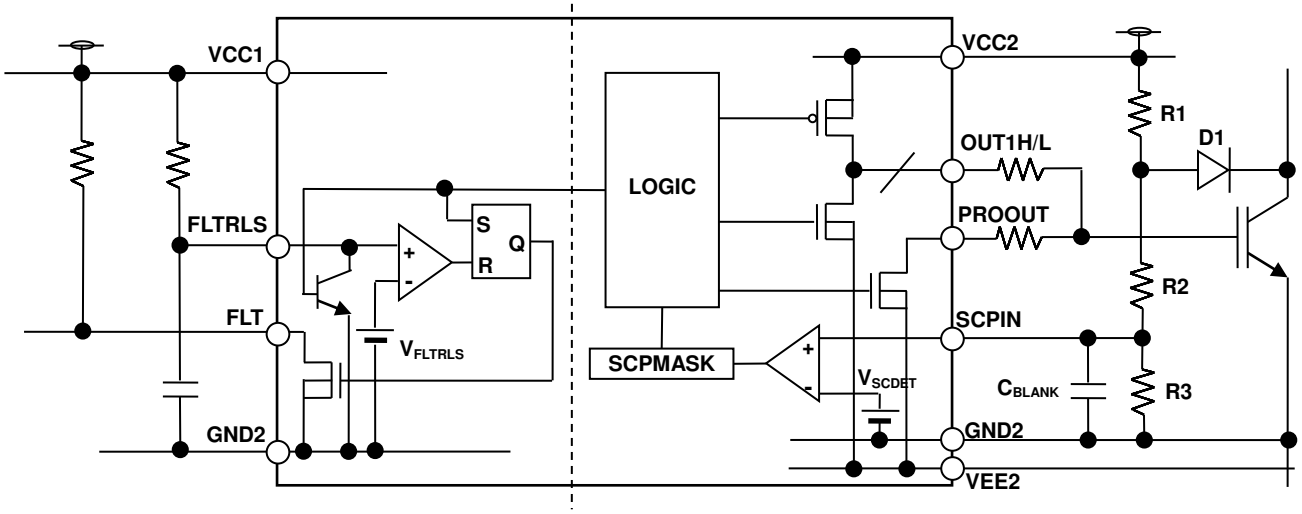


Figure 9. Block Diagram for DESAT

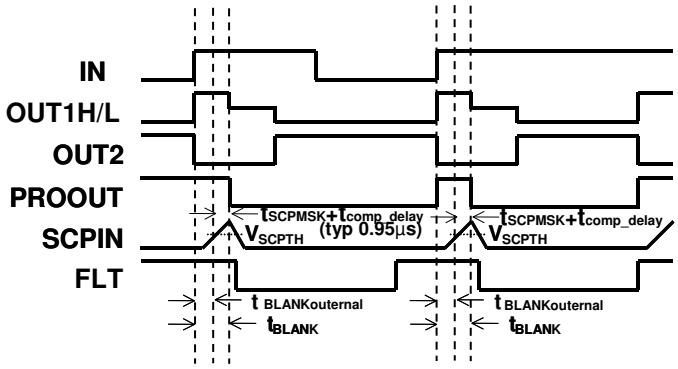
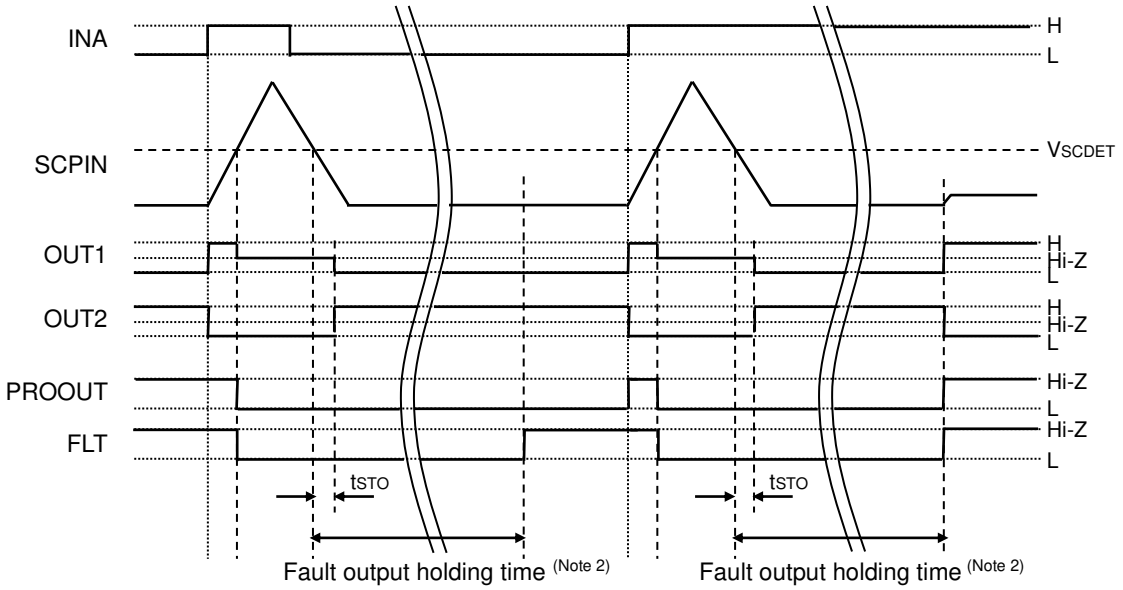


Figure 10. DESAT Operation Timing Chart



(Note 2): "2) Fault status output" section on page 5

Figure 11. SCP Operation Timing Chart

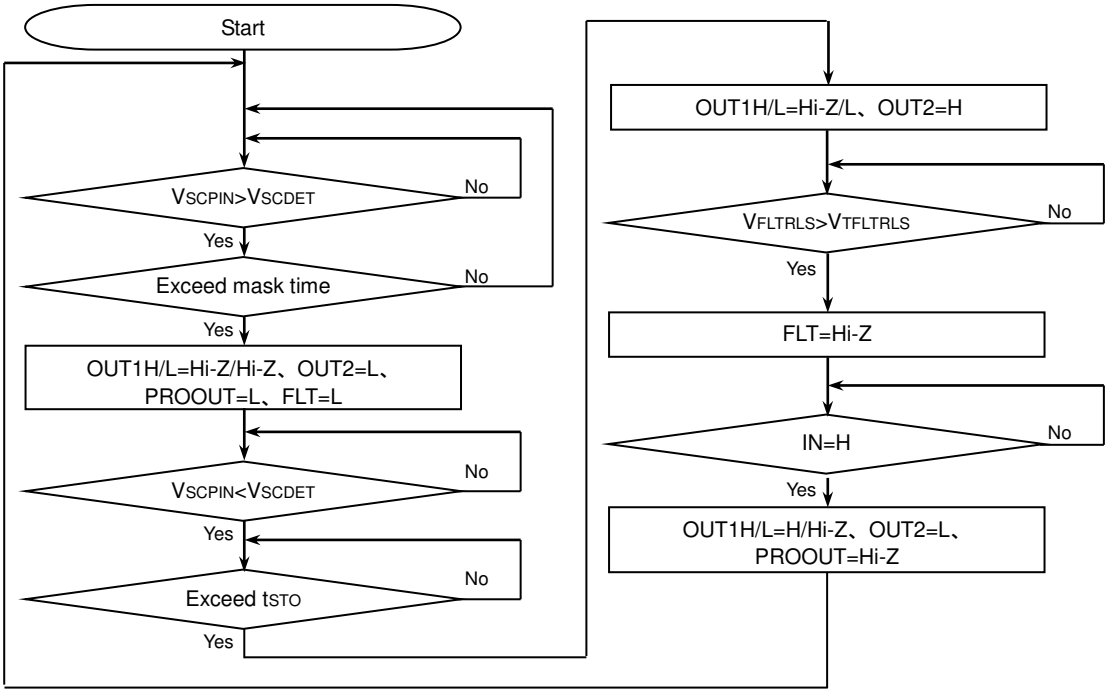


Figure 12. SCP Operation Status Transition Diagram

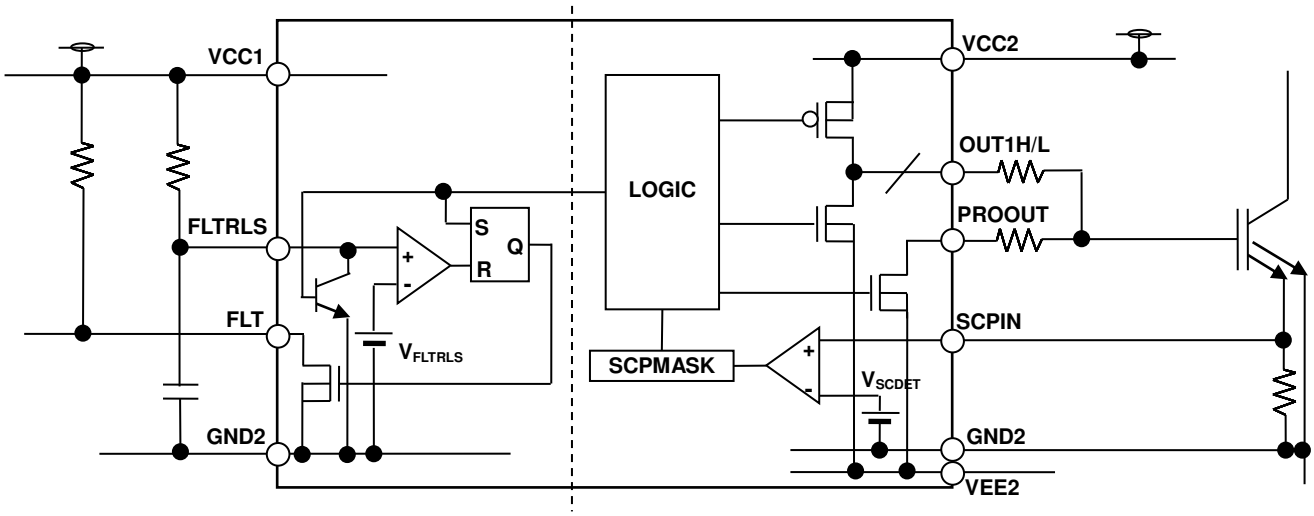


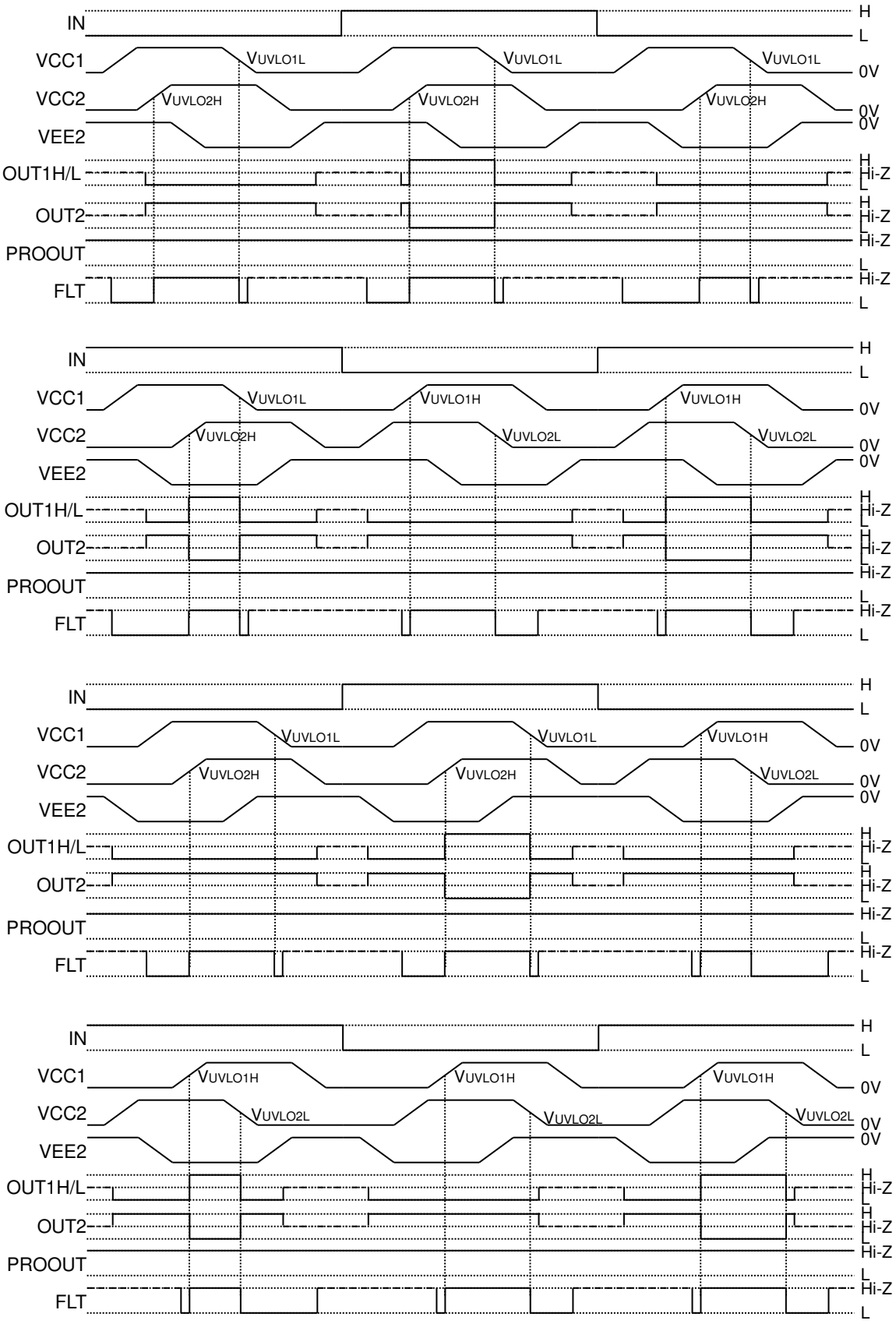
Figure 13. Block Diagram for SCP

5）I/O condition table

No.	Status	Input							Output					
		VCC1	VCC2	SCPIN	ENA	INB	INA	PROOUT	OUT1H	OUT1L	OUT2	PROOUT	FLT	OSFB
1	SCP	○	○	H	L	L	H	X	Hi-Z	Hi-Z	L	L	L	Hi-Z
2	VCC1UVLO	UVLO	X	L	X	X	X	H	Hi-Z	L	L	Hi-Z	L	Hi-Z
3		UVLO	X	L	X	X	X	L	Hi-Z	L	H	Hi-Z	L	Hi-Z
4	VCC2UVLO	X	UVLO	L	X	X	X	H	Hi-Z	L	L	Hi-Z	L	Hi-Z
5		X	UVLO	L	X	X	X	L	Hi-Z	L	H	Hi-Z	L	Hi-Z
6	Disable	○	○	L	H	X	X	H	Hi-Z	L	L	Hi-Z	Hi-Z	Hi-Z
7		○	○	L	H	X	X	L	Hi-Z	L	H	Hi-Z	Hi-Z	Hi-Z
8	INB Active	○	○	L	L	H	X	H	Hi-Z	L	L	Hi-Z	Hi-Z	L
9		○	○	L	L	H	X	L	Hi-Z	L	H	Hi-Z	Hi-Z	Hi-Z
10	Normal Operation L Input	○	○	L	L	L	L	H	Hi-Z	L	L	Hi-Z	Hi-Z	L
11		○	○	L	L	L	L	L	Hi-Z	L	H	Hi-Z	Hi-Z	Hi-Z
12	Normal Operation H Input	○	○	L	L	L	H	H	H	Hi-Z	L	Hi-Z	Hi-Z	Hi-Z
13		○	○	L	L	L	H	L	H	Hi-Z	L	Hi-Z	Hi-Z	L

○: VCC1 or VCC2 > UVLO, X:Don't care

6) Power supply startup / shutoff sequence



: Since the VCC2 to VEE2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z conditions.

: Since the VCC1 pin voltage is low and the FLT output MOS does not turn ON, the output pins become Hi-Z conditions.

Figure 14. Power supply startup / shutoff sequence

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input-Side Supply Voltage	V_{CC1}	-0.3～+7.0(Note 3)	V
Output-Side Positive Supply Voltage	V_{CC2}	-0.3～+30.0(Note 4)	V
Output-Side Negative Supply Voltage	V_{EE2}	-15.0～+0.3(Note 4)	V
Maximum Difference Between Output-Side Positive and Negative Voltages	V_{MAX2}	36.0	V
INA, INB, ENA Pin Input Voltage	V_{IN}	-0.3～+VCC1+0.3 or 7.0(Note 3)	V
OSFB, FLT Pin Input Voltage	V_{FLT}	-0.3～+VCC1+0.3 or 7.0(Note 3)	V
FLTRLS Pin Input Voltage	V_{FLTRLS}	-0.3～+VCC1+0.3 or 7.0(Note 3)	V
SCPIN Pin Input Voltage	V_{SCPIN}	-0.3~VCC2+0.3(Note 4)	V
VREG Pin Output Current	I_{VREG}	10	mA
OUT1H, OUT1L, PROOUT Pin Output Current (Peak 10μs)	$I_{OUT1PEAK}$	5.0(Note 5)	A
OUT2 Pin Output Current (Peak 10μs)	$I_{OUT2PEAK}$	1.0(Note 5)	A
OSFB Output Current	I_{OSFB}	10	mA
FLT Output Current	I_{FLT}	10	mA
Power Dissipation	P_d	1.19(Note 6)	W
Operating Temperature Range	T_{opr}	-40～+125	°C
Storage Temperature Range	T_{stg}	-55～+150	°C
Junction Temperature	T_{jmax}	+150	°C

(Note 3) Relative to GND1.
(Note 4) Relative to GND2.
(Note 5) Should not exceed Pd and Tj=150°C.
(Note 6) Derate above Ta=25°C at a rate of 9.5mW/°C. Mounted on a glass epoxy of 70 mm × 70 mm × 1.6 mm.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Ratings

Parameter	Symbol	Min	Max	Units
Input-Side Supply Voltage(Note 7)	V_{CC1}	4.5	5.5	V
Output-Side Positive Supply Voltage(Note 8)	V_{CC2}	10	24	V
Output-Side Negative Supply Voltage(Note 8)	V_{EE2}	-12	0	V
Maximum Difference Between Output-Side Positive and Negative Voltages	V_{MAX2}	10	32	V

(Note 7) Relative to GND1.
(Note 8) Relative to GND2.

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Units
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1sec	V_{ISO}	3000	Vrms

Electrical Characteristics

（Unless otherwise specified T_a=-40°C~125°C, V_{CC1}=4.5V~5.5V, V_{CC2}=10V~24V, V_{EE2}=-12V~0V）

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Input Side Circuit Current 1	I_{CC11}	0.38	0.51	0.64	mA	OUT1=L
Input Side Circuit Current 2	I_{CC12}	0.38	0.51	0.64	mA	OUT1=H
Input Side Circuit Current 3	I_{CC13}	0.47	0.62	0.77	mA	INA=10kHz, Duty=50%
Input Side Circuit Current 4	I_{CC14}	0.54	0.72	0.90	mA	INA=20kHz, Duty=50%
Output Side Circuit Current 1	I_{CC21}	1.5	2.0	2.5	mA	VCC2=14V, OUT1=L
Output Side Circuit Current 2	I_{CC22}	1.3	1.8	2.3	mA	VCC2=14V, OUT1=H
Output Side Circuit Current 3	I_{CC23}	1.6	2.2	2.8	mA	VCC2=18V, OUT1=L
Output Side Circuit Current 4	I_{CC24}	1.3	1.9	2.5	mA	VCC2=18V, OUT1=H
Output Side Circuit Current 5	I_{CC25}	1.8	2.5	3.2	mA	VCC2=24V, OUT1=L
Output Side Circuit Current 6	I_{CC26}	1.5	2.1	2.7	mA	VCC2=24V, OUT1=H
Logic Block						
Logic High Level Input Voltage	V_{INH}	2.0	-	V_{CC1}	V	INA, INB, ENA
Logic Low Level Input Voltage	V_{INL}	0	-	0.8	V	INA, INB, ENA
Logic Pull-Down Resistance	R_{IND}	25	50	100	kΩ	INA, INB
Logic Pull-Up Resistance	R_{INU}	25	50	100	kΩ	ENA
Logic Input Mask Time	t_{INMSK}	-	-	90	ns	INA, INB
ENA Mask Time	t_{ENAMSK}	4	10	20	µs	ENA
Output						
OUT1H ON Resistance	R_{ONH}	0.7	1.8	4.0	Ω	I_{OUT1H}=40mA
OUT1L ON Resistance	R_{ONL}	0.4	0.9	2.0	Ω	I_{OUT1L}=40mA
OUT1 Maximum Current	I_{OUTMAX}	3.0	4.5	-	A	VCC2=18V Guaranteed by design
PROOUT ON Resistance	R_{ONPRO}	0.4	0.9	2.0	Ω	I_{PROOUT}=40mA
Turn ON Time	t_{PONA}	90	115	150	ns	INA=PWM, INB=L
	t_{PONB}	100	125	160	ns	INA=H, INB=PWM
Turn OFF Time	t_{POFFA}	90	115	150	ns	INA=PWM, INB=L
	t_{POFFB}	80	105	140	ns	INA=H, INB=PWM
Propagation Distortion	t_{PDISTA}	-25	0	20	ns	t_{POFFA} - t_{PONA}
	t_{PDISTB}	-45	-20	0	ns	t_{POFFB} - t_{PONB}
Rise Time	t_{RISE}	-	50	-	ns	10nF between OUT1-VEE2
Fall Time	t_{FALL}	-	50	-	ns	10nF between OUT1-VEE2
OUT2 ON Resistance (Source)	R_{ON2H}	2.0	4.5	9.0	Ω	I_{OUT2}=10mA
OUT2 ON Resistance (Sink)	R_{ON2L}	1.5	3.5	7.0	Ω	I_{OUT2}=10mA
OUT2 ON Threshold Voltage	V_{OUT2ON}	1.8	2	2.2	V	Relative to VEE2
OUT2 Output Delay Time	t_{OUT2ON}	-	25	50	ns	
VREG Output Voltage	V_{REG}	9	10	11	V	Relative to VEE2
Common Mode Transient Immunity	CM	100	-	-	kV/µs	Design assurance

Electrical Characteristics

（Unless otherwise specified Ta=-40°C~125°C, V_{CC1}=4.5V~5.5V, V_{CC2}=10V~24V, V_{EE2}=-12V~0V）

Protection functions						
VCC1 UVLO OFF Voltage	V_{UVLO1H}	3.35	3.50	3.65	V	
VCC1 UVLO ON Voltage	V_{UVLO1L}	3.25	3.40	3.55	V	
VCC1 UVLO Mask Time	$t_{UVLO1MSK}$	4	10	30	μs	
VCC2 UVLO OFF Voltage	V_{UVLO2H}	8.95	9.55	10.15	V	
VCC2 UVLO ON Voltage	V_{UVLO2L}	8.45	9.05	9.65	V	
VCC2 UVLO Mask Time	$t_{UVLO2MSK}$	4	10	30	μs	
SCPIN Input Voltage	V_{SCPIN}	-	0.1	0.22	V	I_{SCPIN}=1mA
SCP Threshold Voltage	V_{SCDET}	0.665	0.700	0.735	V	
SCP Detection Mask Time	t_{SCPMSK}	0.55	0.8	1.05	μs	
Soft Turn OFF Release Time	t_{STO}	30		110	μs	
OSFB Threshold Voltage H	V_{OSFBH}	4.5	5.0	5.5	V	Respective to GND2
OSFB Threshold Voltage L	V_{OSFBL}	4.0	4.5	5.0	V	Respective to GND2
OSFB Output Low Voltage	V_{OSFBOL}	-	0.18	0.40	V	I_{OSFB}=5mA
OSFB Filter Time	t_{OSFBON}	1.5	2.0	2.6	μs	
FLT Output Low Voltage	V_{FLTL}	-	0.18	0.40	V	I_{FLT}=5mA
FLTRLS Threshold	$V_{TFLTRLS}$	0.64 × V_{CC1} -0.1	0.64 × V_{CC1}	0.64 × V_{CC1} +0.1	V	

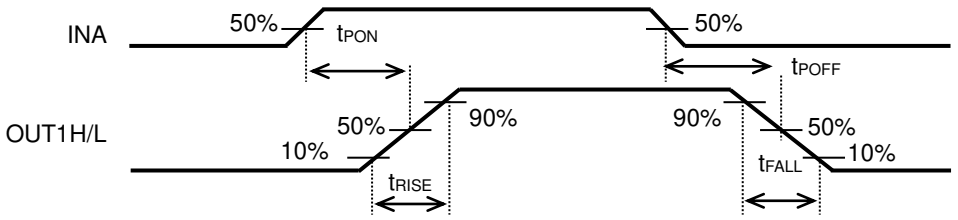


Figure 15. INA-OUT1 Timing Chart

UL1577 Ratings Table

Following values are described in UL Report.

Parameter	Values	Units	Conditions
Side 1 (Input Side) Circuit Current	0.51	mA	VCC1=5.0V, OUT1H/L=L
Side 2 (Output Side) Circuit Current	2.2	mA	VCC2=18V, VEE2=0V, UT1H/L=L
Side 1 (Input Side) Consumption Power	2.55	mW	VCC1=5.0V, OUT1H/L=L
Side 2 (Output Side) Consumption Power	39.6	mW	VCC2=18V, VEE2=0V, OUT1H/L=L
Isolation Voltage	2500	Vrms	
Maximum Operating (Ambient) Temperature	125	℃	
Maximum Junction Temperature	150	℃	
Maximum Strage Temperature	150	℃	
Maximum Data Transmission Rate	2.5	MHz	

Typical Performance Curves

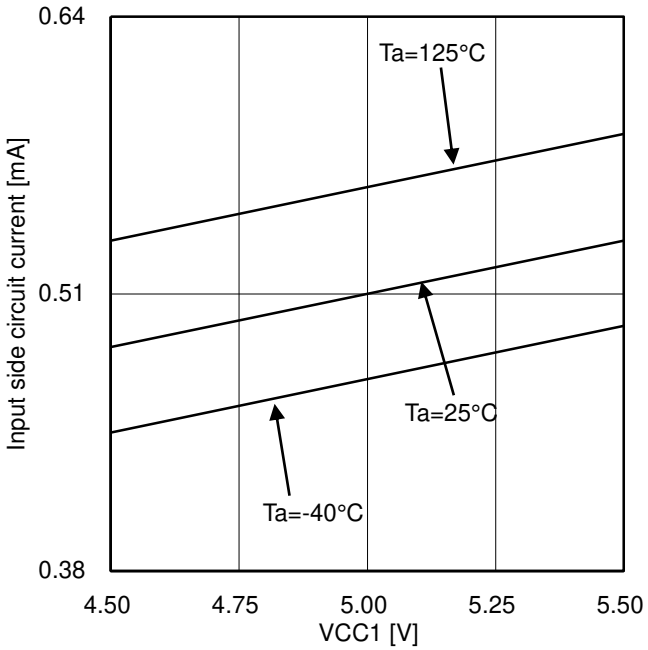


Figure 16. Input side circuit current vs. VCC1
(OUT1=L)

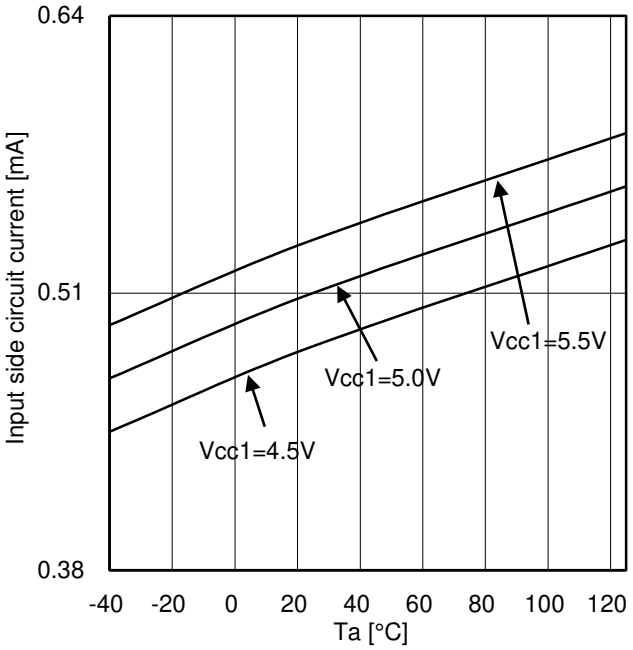


Figure 17. Input side circuit current vs. Temperature
(OUT1=L)

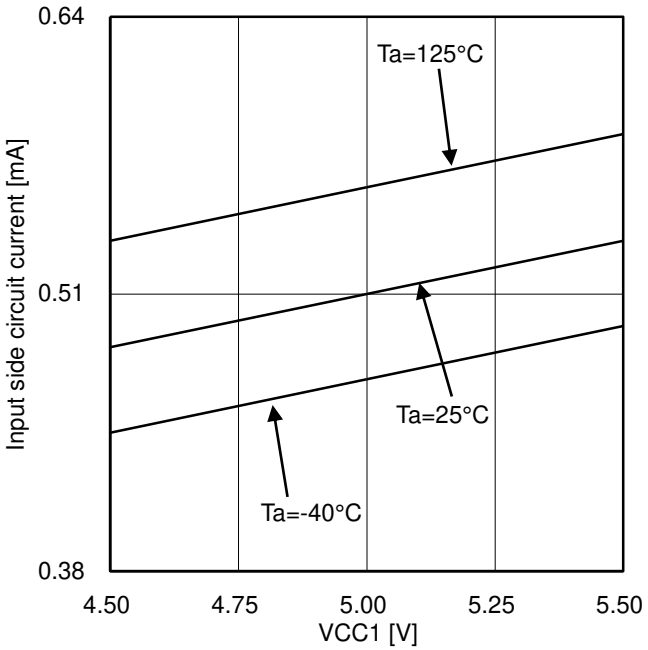


Figure 18. Input side circuit current vs. VCC1
(OUT1=H)

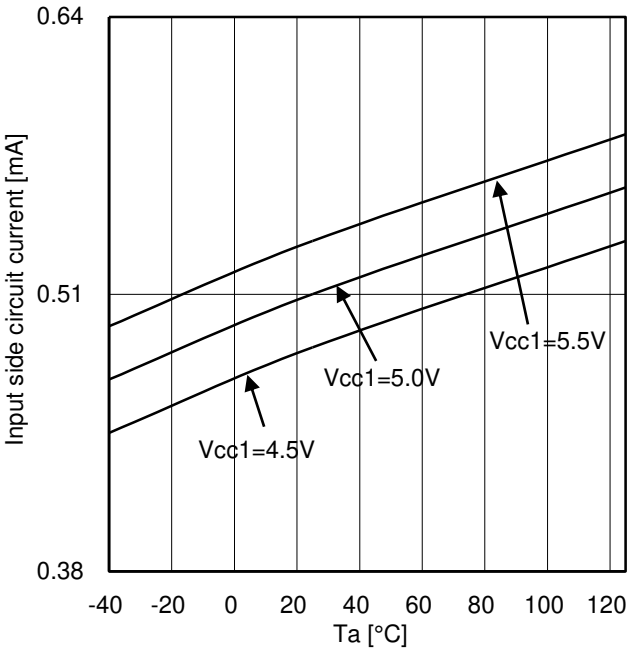


Figure 19. Input side circuit current vs. Temperature
(OUT1=H)

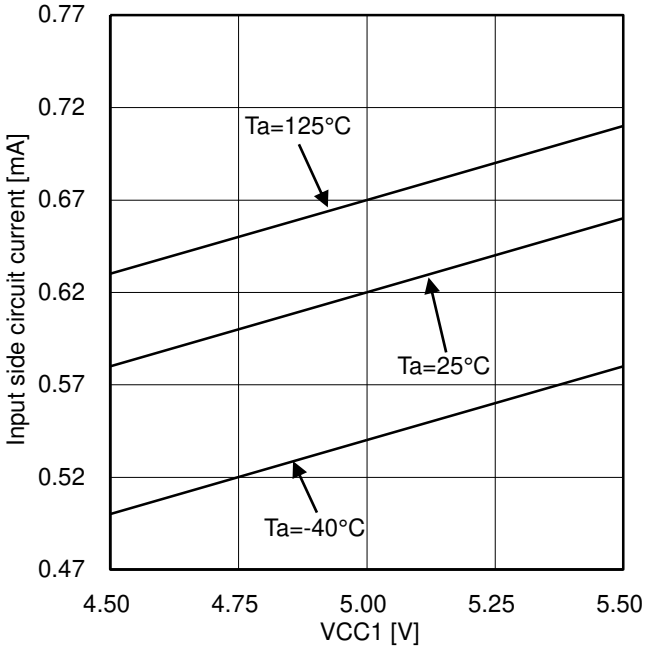


Figure 20. Input side circuit current vs. VCC1
(INA=10 kHz, Duty=50%)

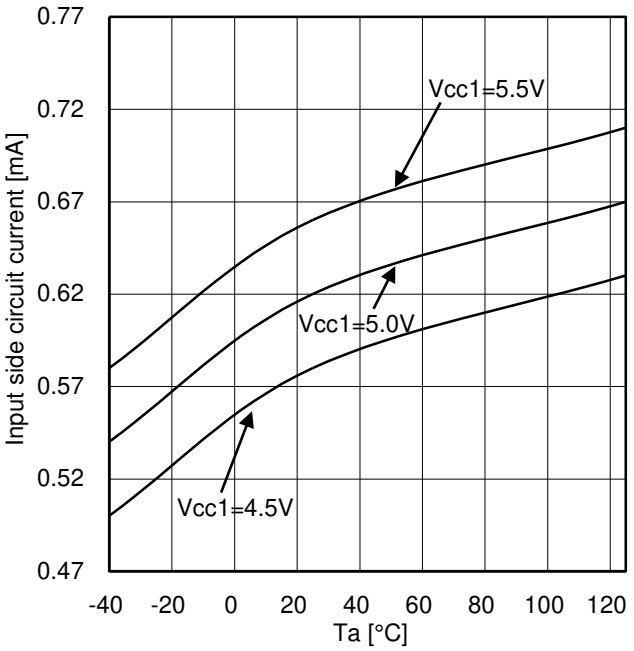


Figure 21. Input side circuit current vs. Temperature
(INA=10 kHz, Duty=50%)

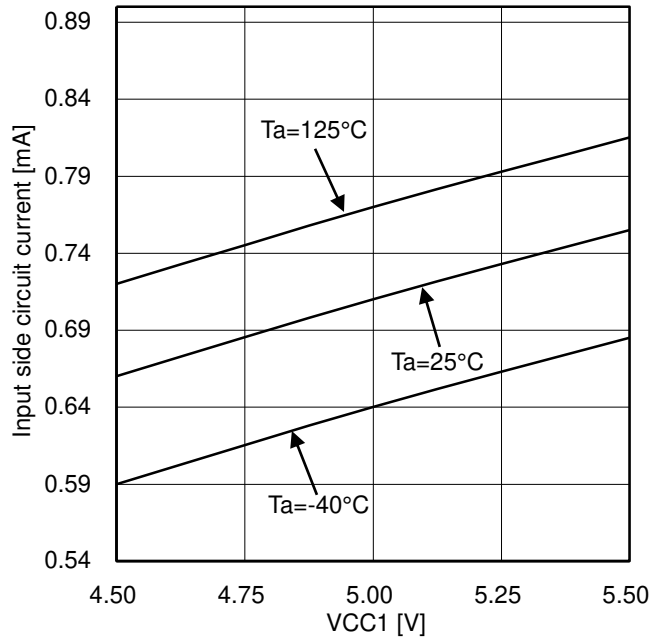


Figure 22. Input side circuit current vs. VCC1
(INA=20 kHz, Duty=50%)

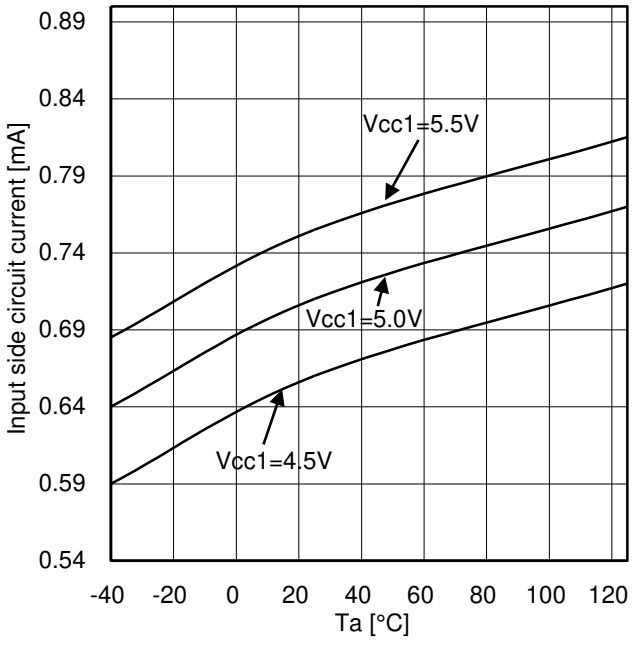


Figure 23. Input side circuit current vs. Temperature
(INA=20 kHz, Duty=50%)

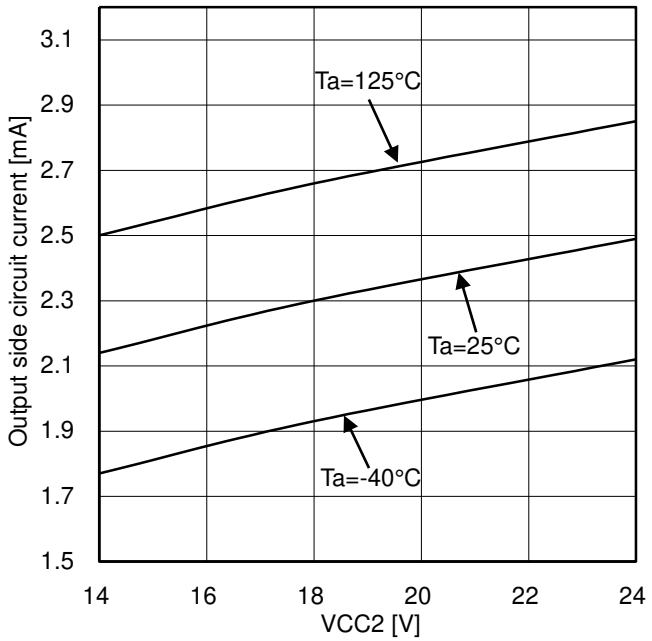


Figure 24. Output side circuit current vs. VCC2
(OUT1=L)

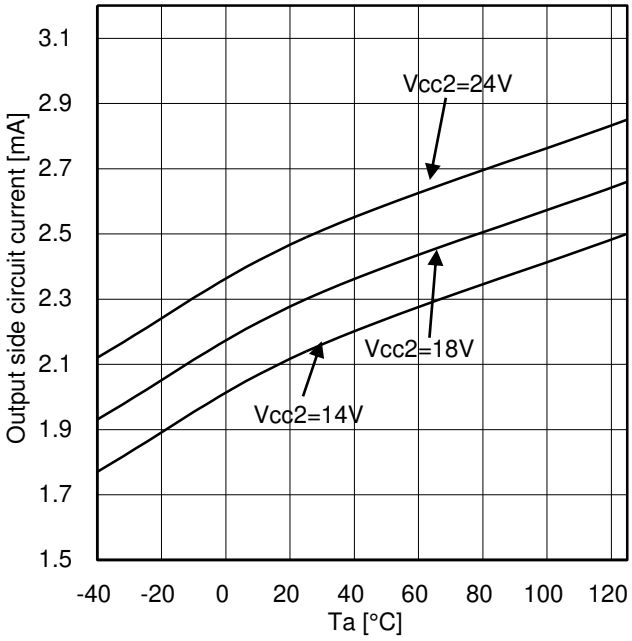


Figure 25. Output side circuit current vs. Temperature
(OUT1=L)

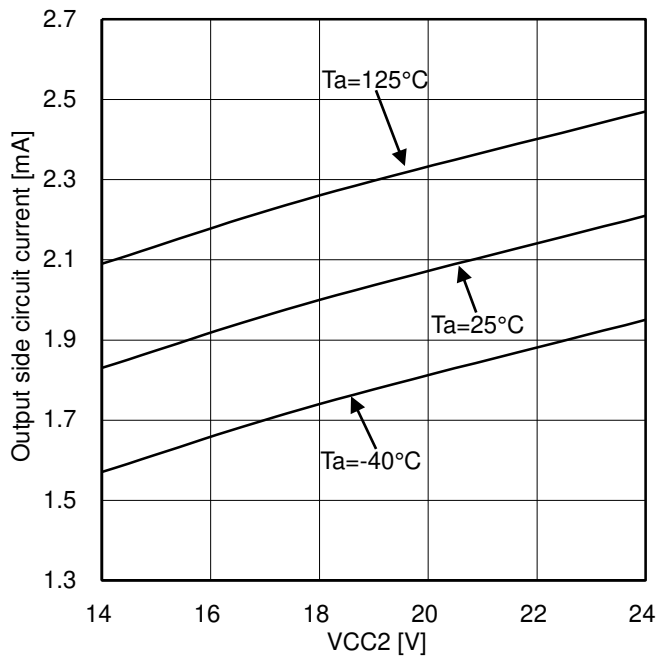


Figure 26. Output side circuit current vs. VCC2
(OUT1=H)

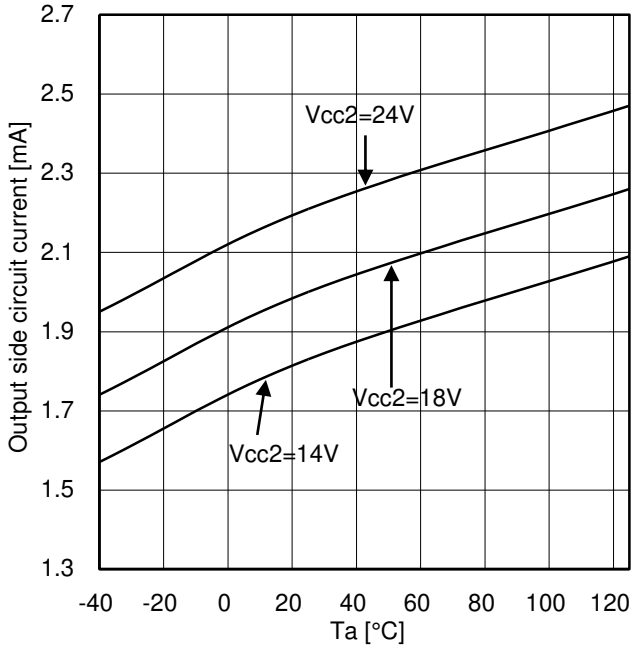


Figure 27. Output side circuit current vs. Temperature
(OUT1=H)

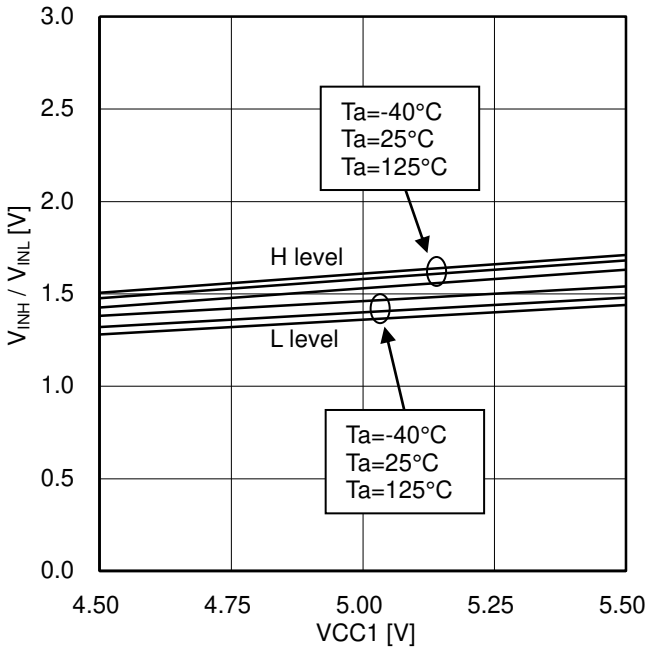


Figure 28. Logic (INA/INB/ENA) High/Low level input voltage vs. VCC1

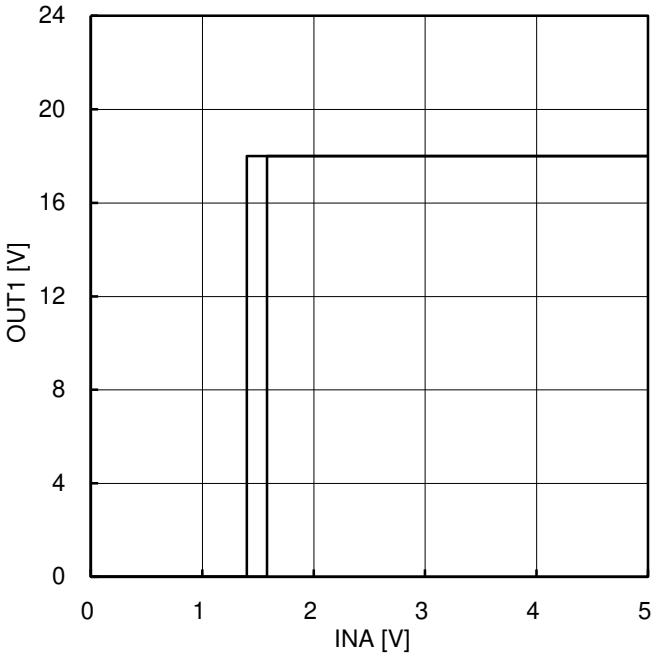


Figure 29. OUT1 vs. INA input voltage (VCC1=5V, VCC2=18V, Ta=25°C)

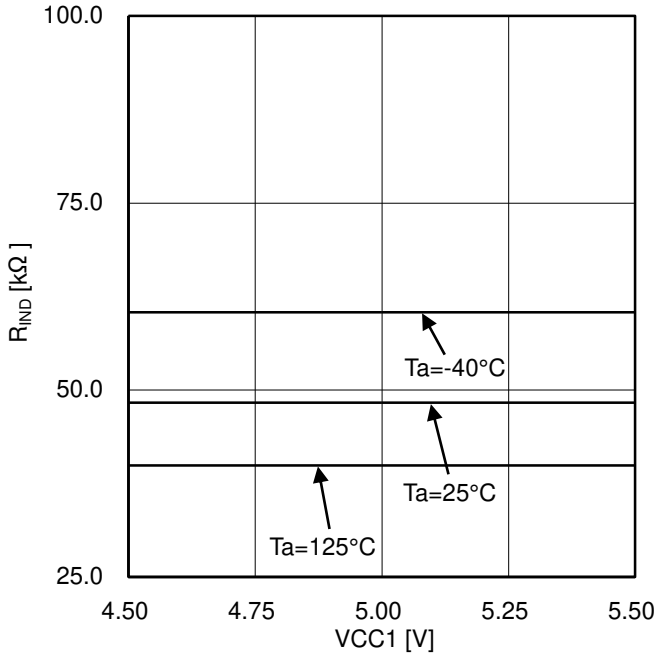


Figure 30. Logic pull-down resistance vs. VCC1

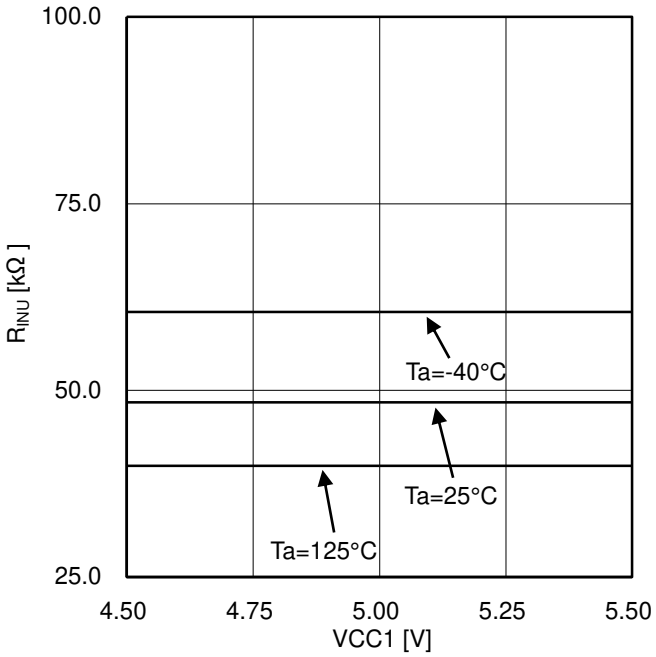


Figure 31. Logic pull-up resistance vs. VCC1

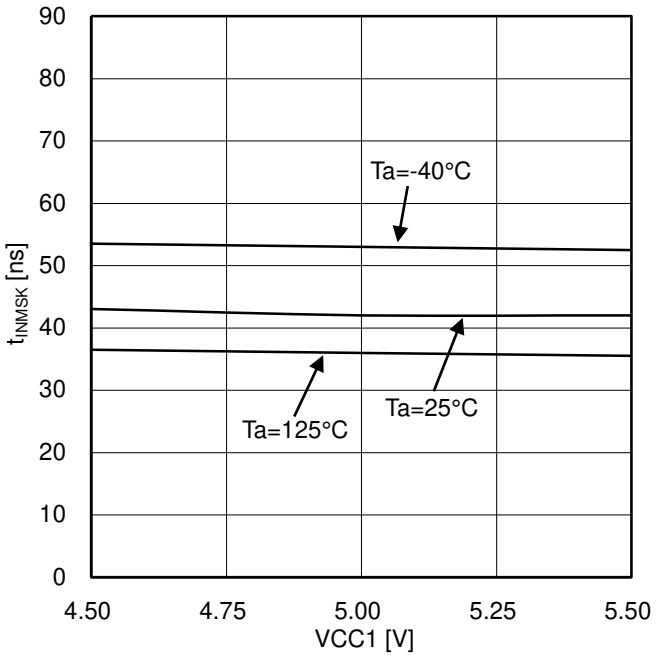


Figure 32. Logic (INA/INB) input mask time vs. VCC1 (High pulse)

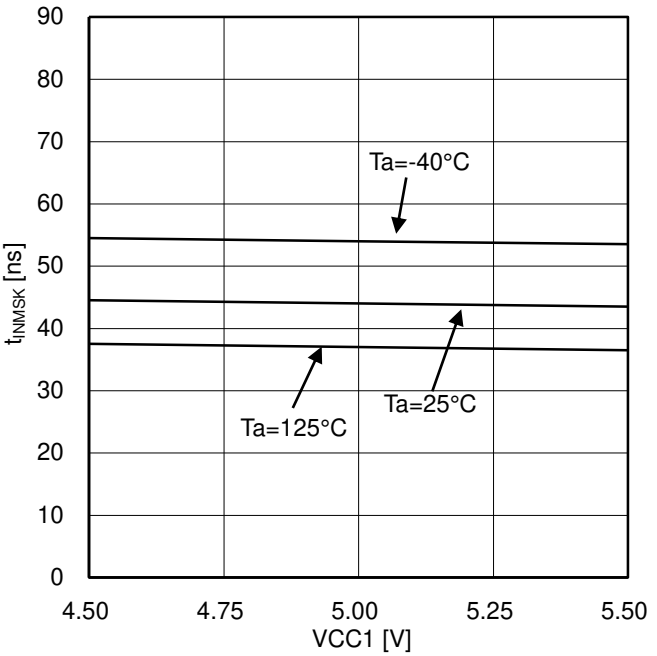


Figure 33. Logic (INA/INB) input mask time vs. VCC1 (Low pulse)

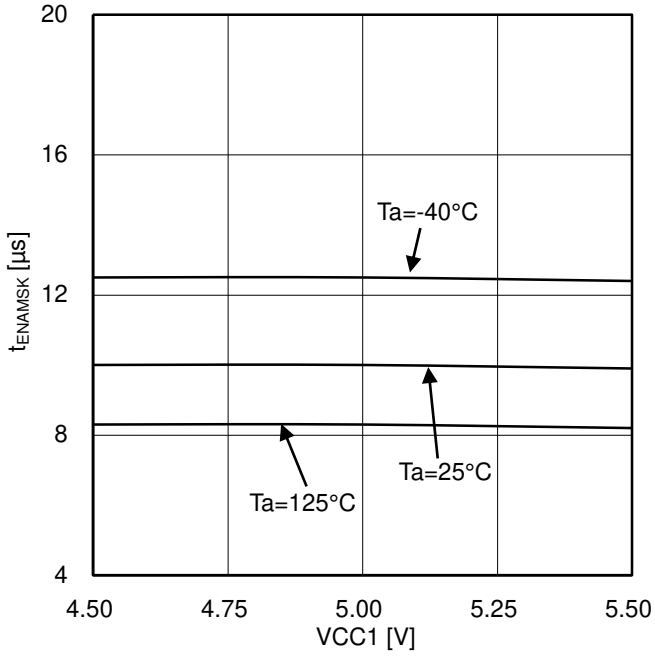


Figure 34. ENA mask time vs. VCC1

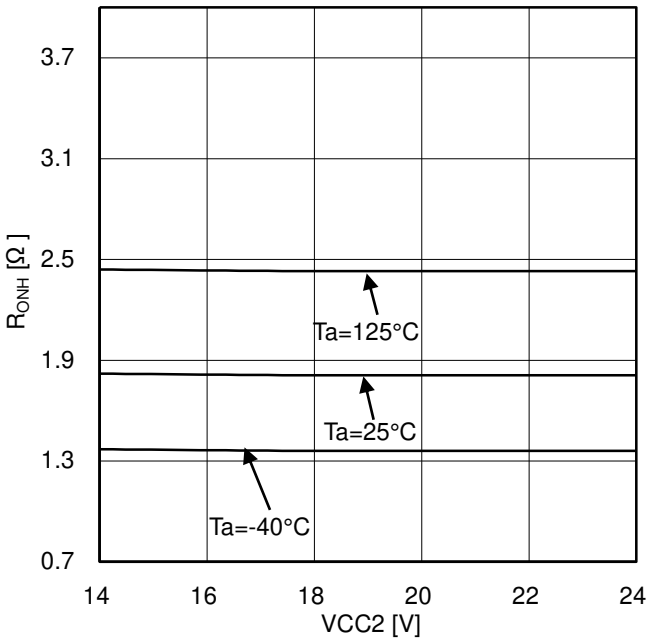


Figure 35. OUT1H ON resistance vs. VCC2

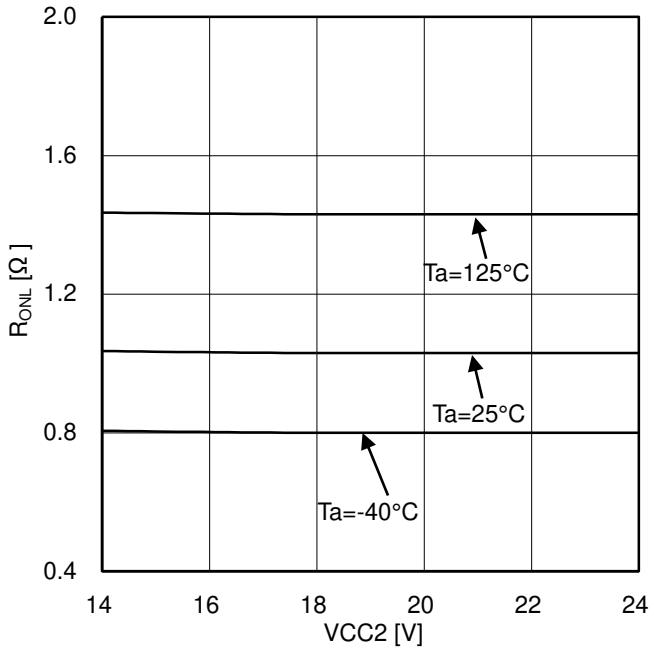


Figure 36. OUT1L ON resistance vs. VCC2

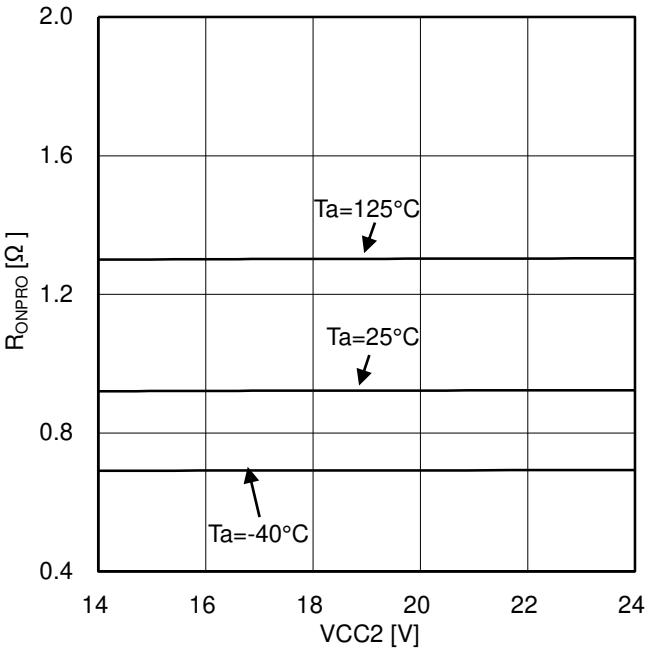


Figure 37. PROOUT ON resistance vs. VCC2

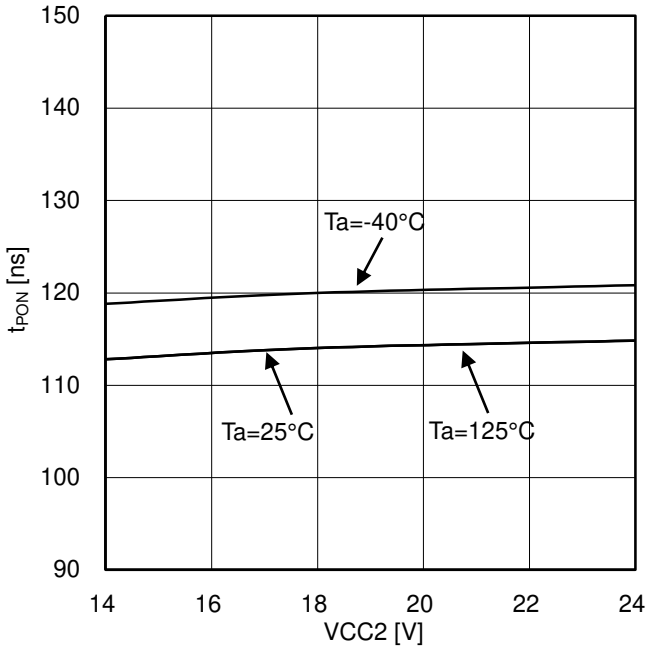


Figure 38. Turn ON time vs VCC2
(INA=PWM, INB=L)

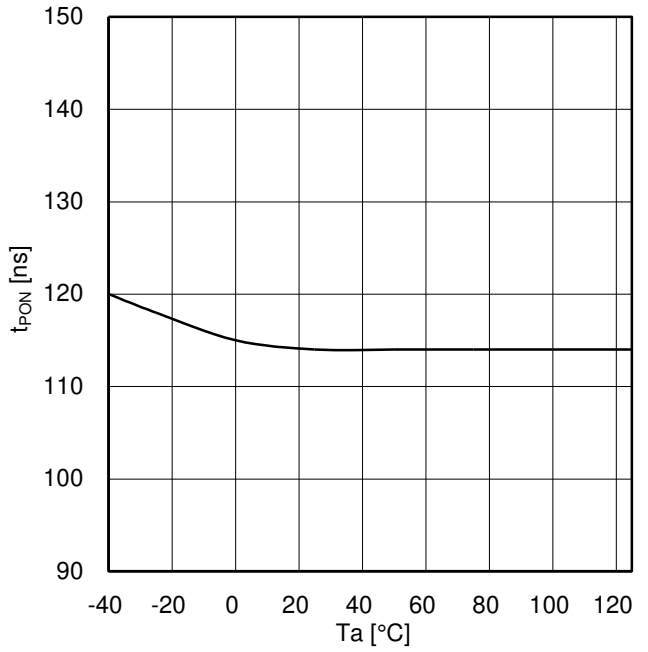


Figure 39. Turn ON time vs Temperature
(VCC2=24V, INA=PWM, INB=L)

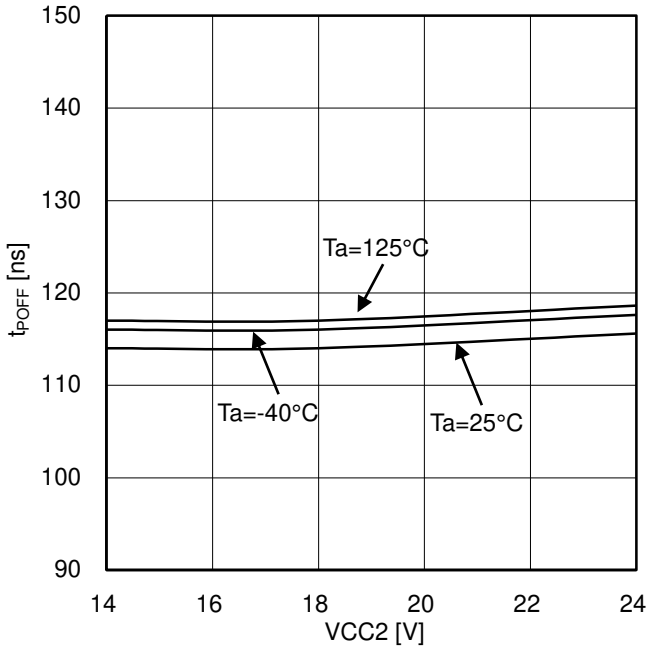


Figure 40. Turn OFF time vs. VCC2
(INA=PWM, INB=L)

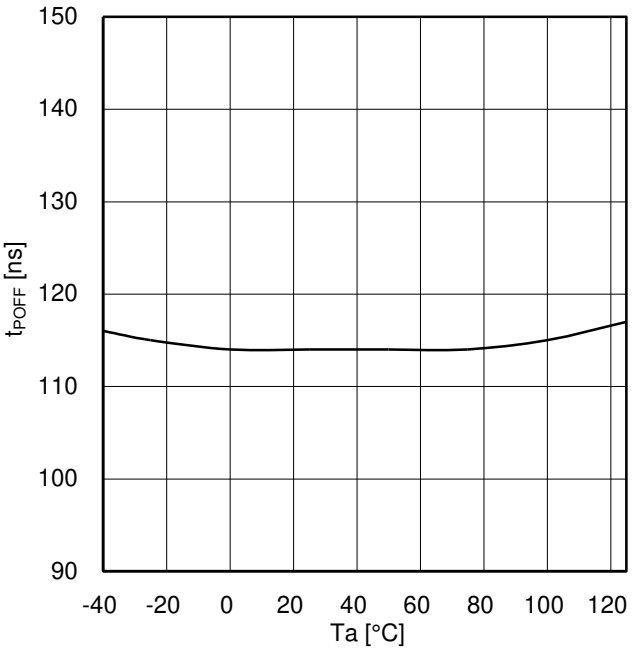


Figure 41. Turn OFF time vs. Temperature
(VCC2=24V, INA=PWM, INB=L)

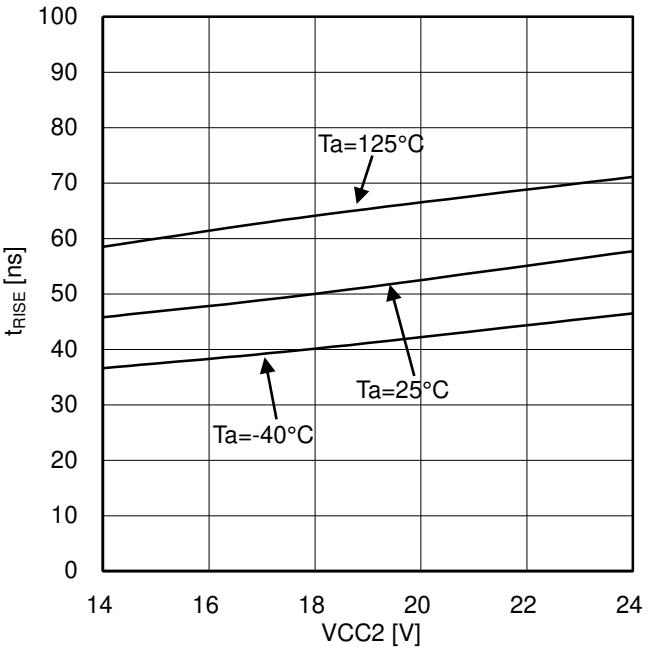


Figure 42. Rise time vs. VCC2
(10nF between OUT1-VEE2)

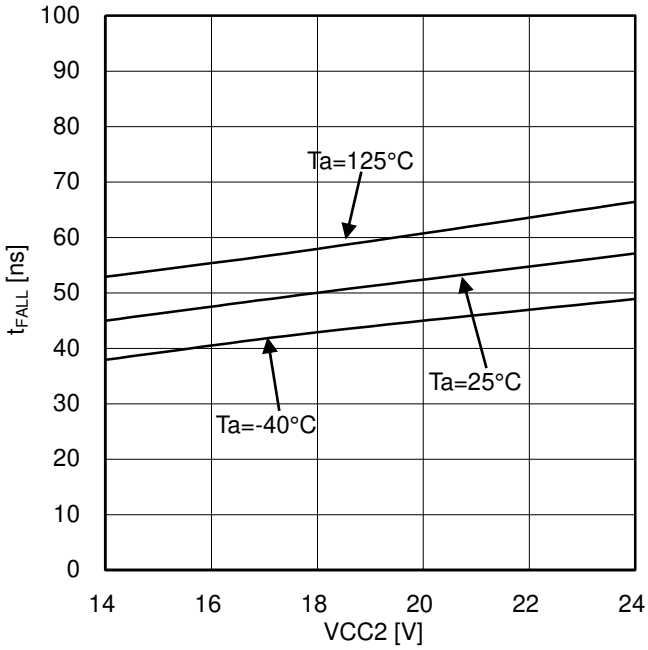


Figure 43. Fall time vs. VCC2
(10nF between OUT1-VEE2)

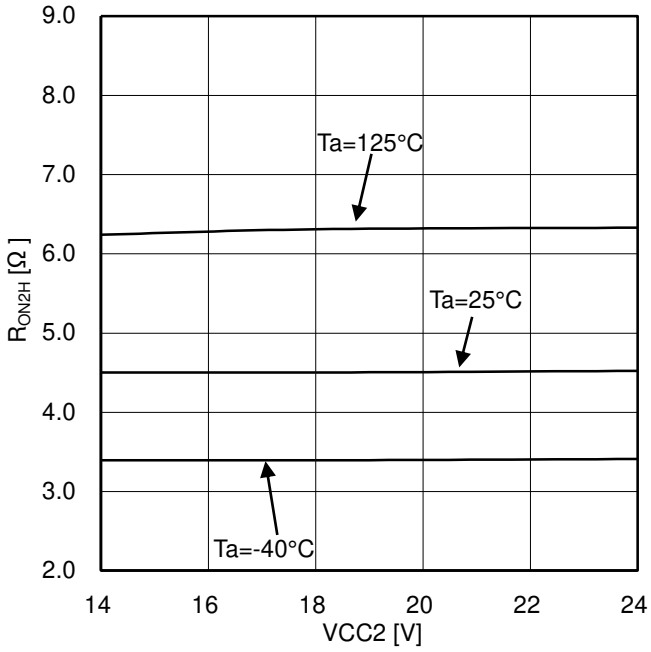


Figure 44. OUT2 ON resistance (Source) vs. VCC2

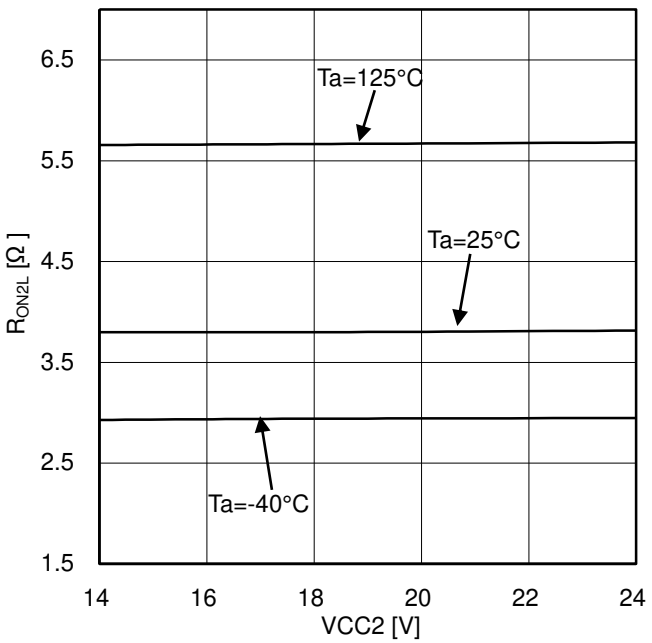


Figure 45. OUT2 ON resistance (Sink) vs. VCC2

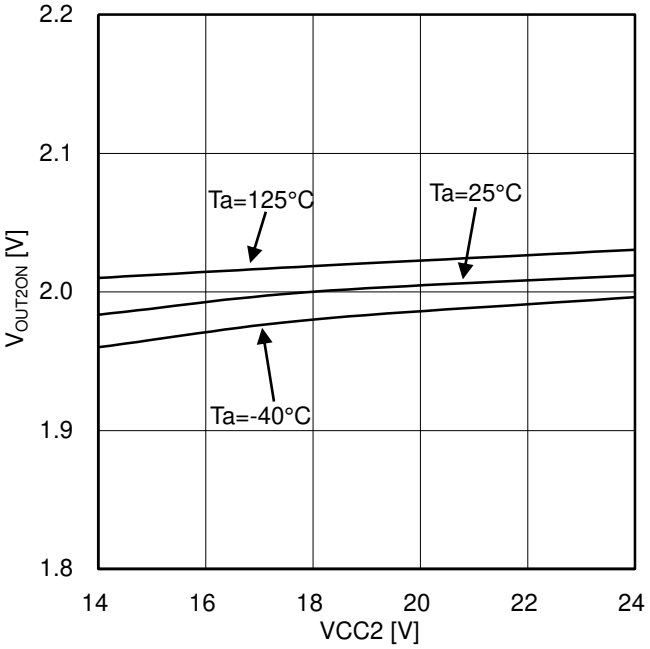


Figure 46. OUT2 ON threshold voltage vs. VCC2

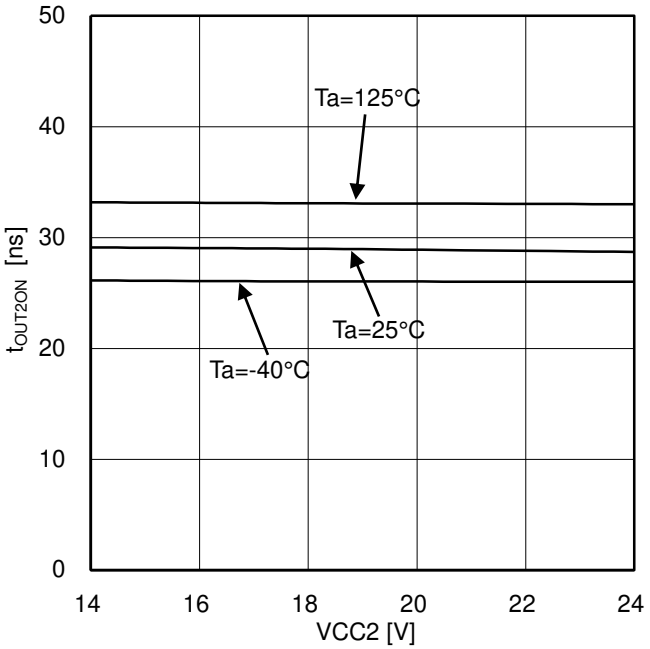


Figure 47. OUT2 output delay time vs. VCC2

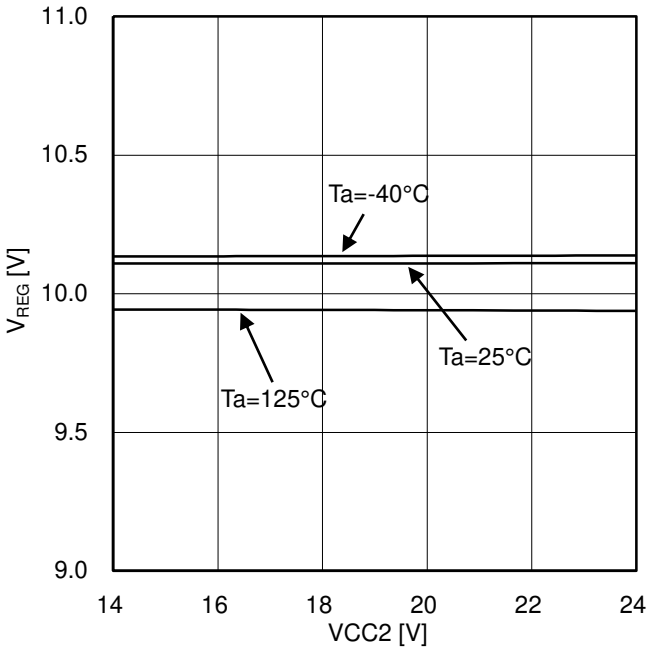


Figure 48. VREG output voltage vs. VCC2

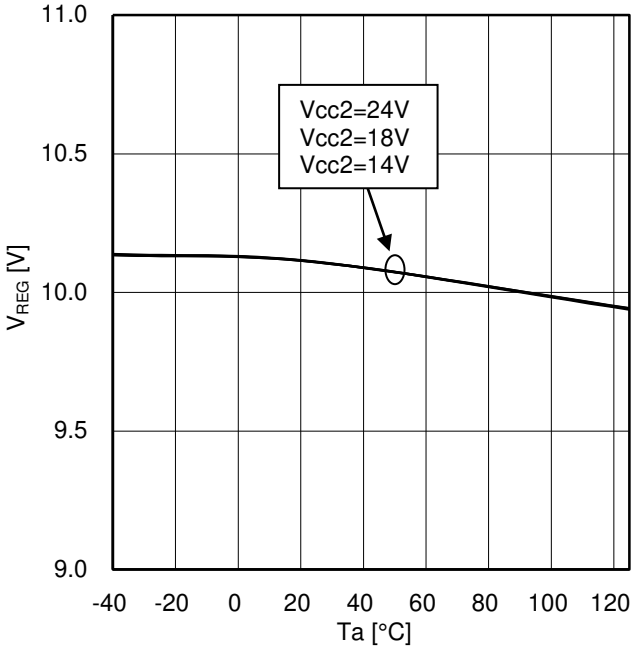


Figure 49. VREG output voltage vs. Temperature

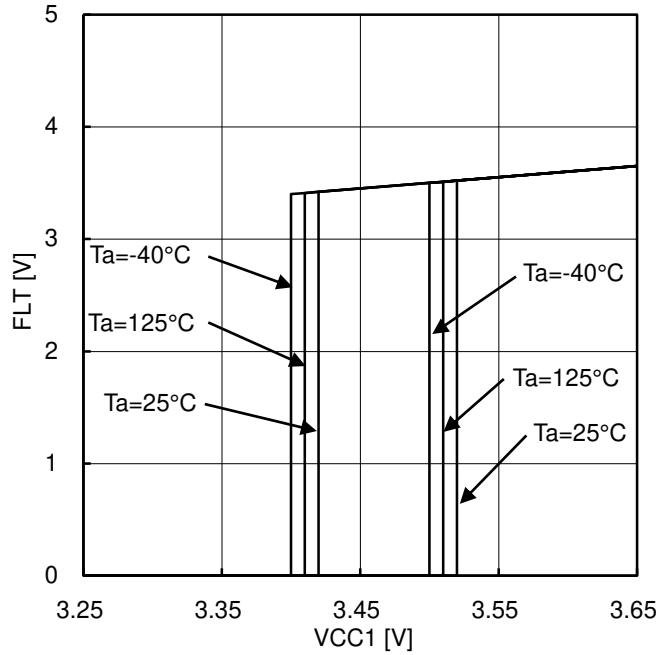


Figure 50. FLT vs. VCC1
(VCC1 UVLO ON/OFF voltage)

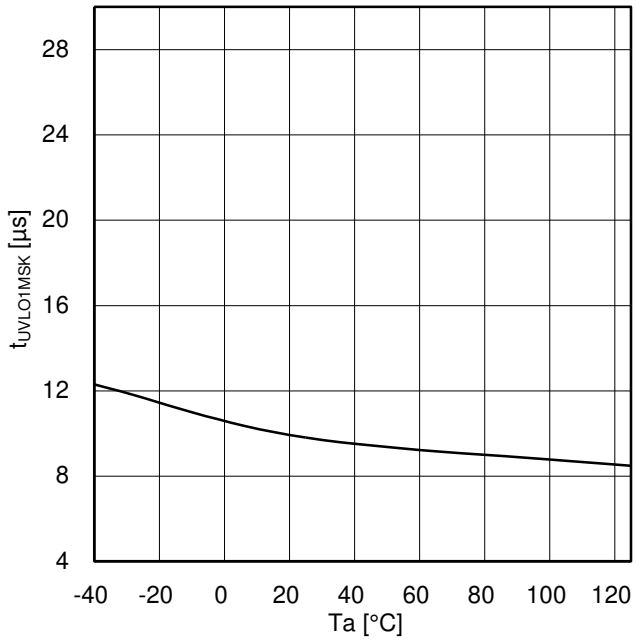


Figure 51. VCC1 UVLO mask time vs. Temperature

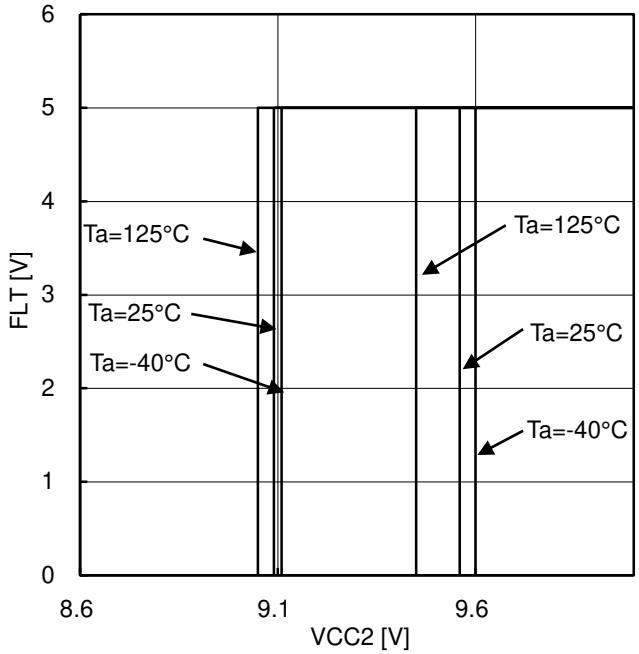


Figure 52. FLT vs. VCC2
(VCC2 UVLO ON/OFF voltage, VCC1=5V)

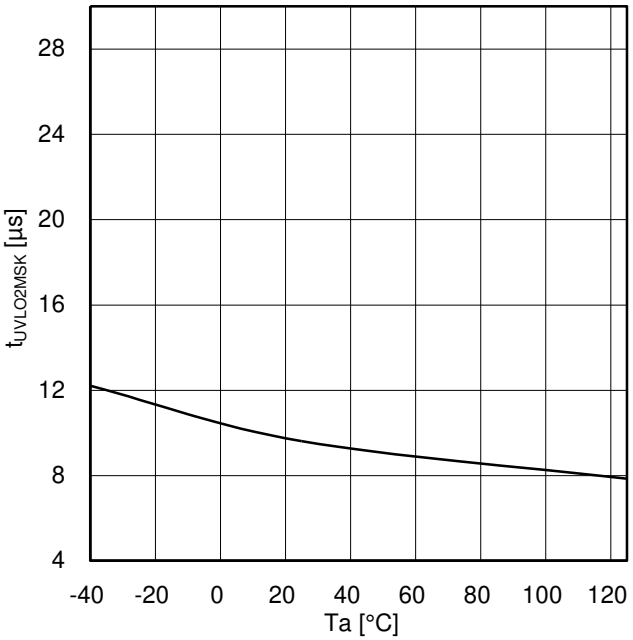


Figure 53. VCC2 UVLO mask time vs. Temperature

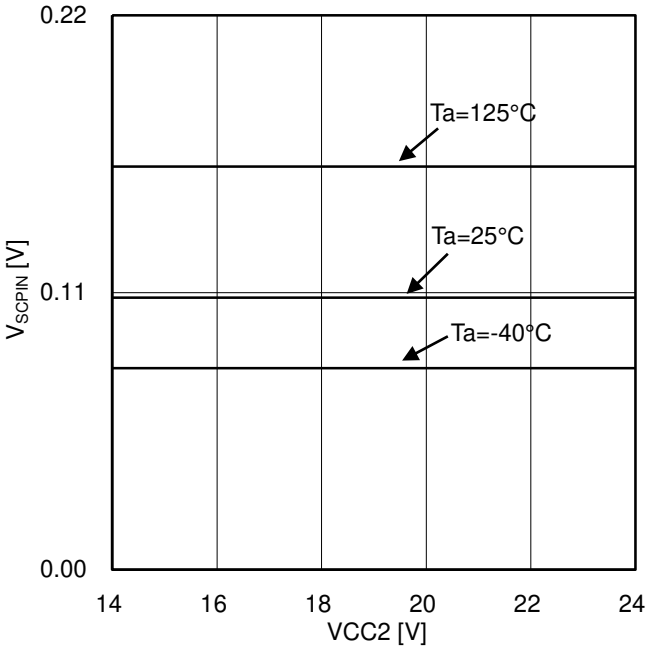


Figure 54. SCPIN Input voltage vs. VCC2
(ISCPIN=1mA)

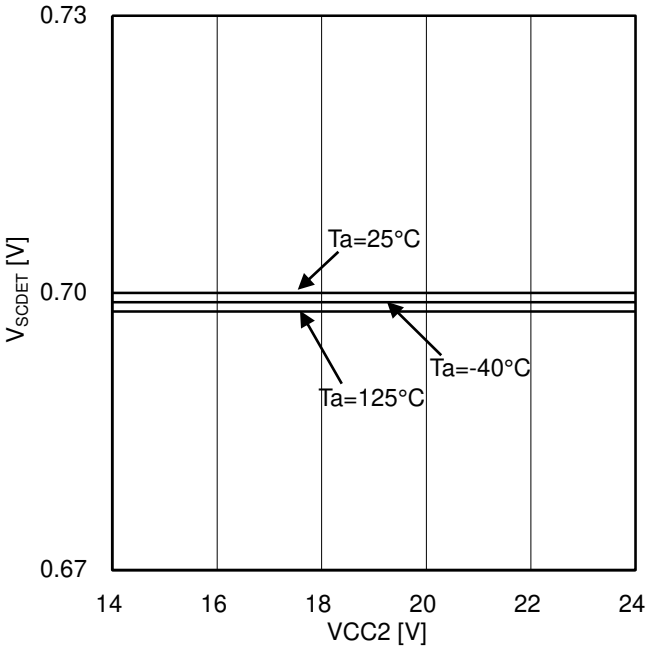


Figure 55. SCP threshold voltage vs. VCC2

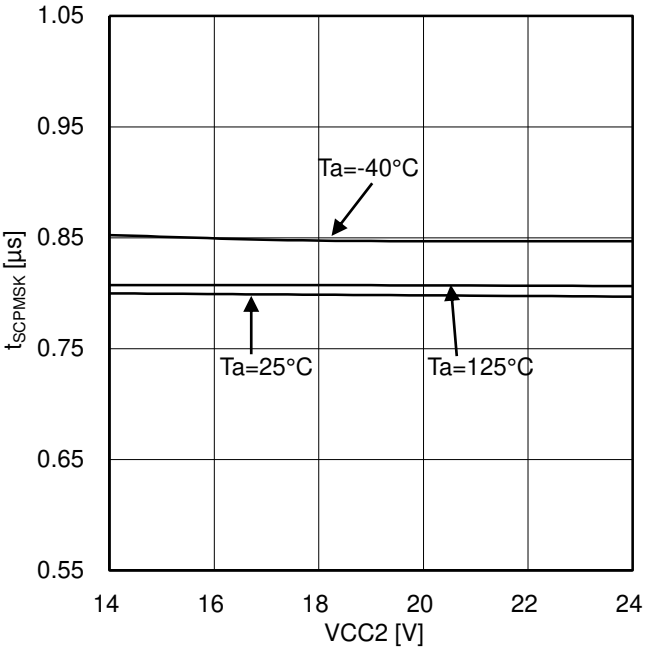


Figure 56. SCP detection mask time vs. VCC2

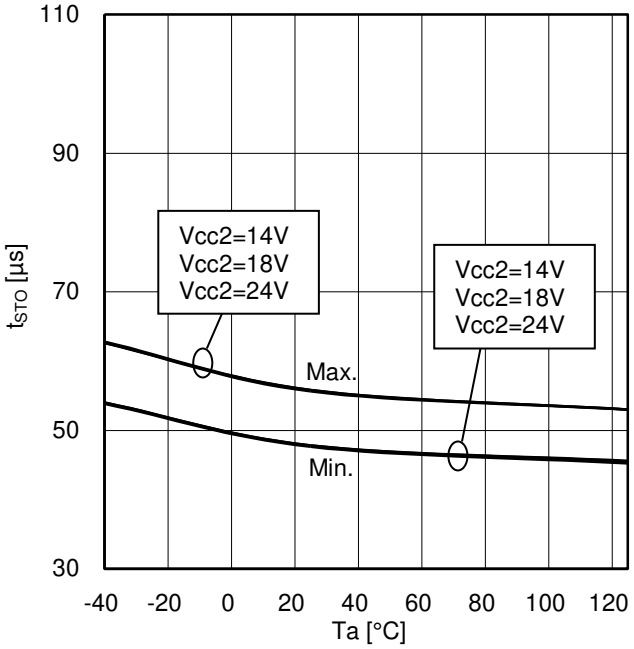


Figure 57. Soft turn OFF release time vs. Temperature

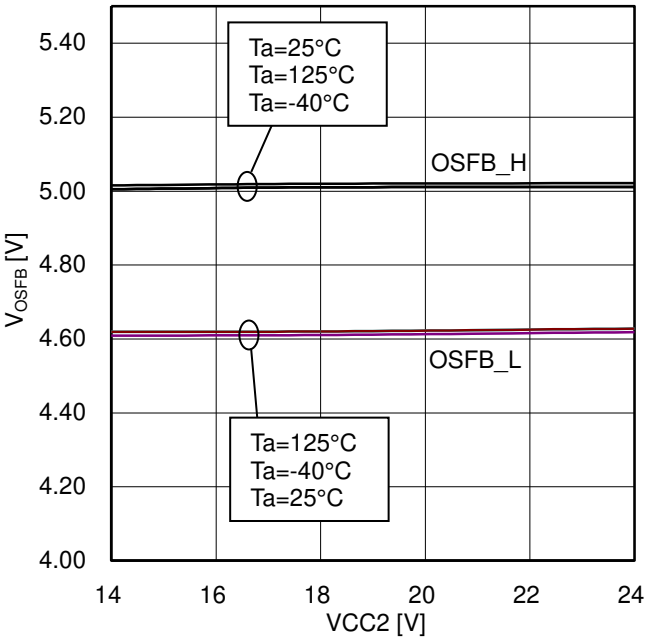


Figure 58. OSFB threshold voltage H/L vs. VCC2

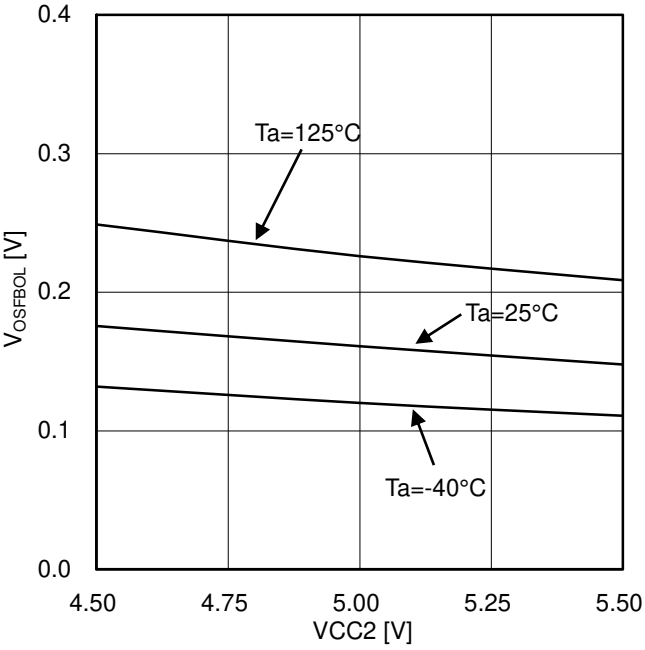


Figure 59. OSFB output low voltage vs. VCC2
(IOSFB=5mA)

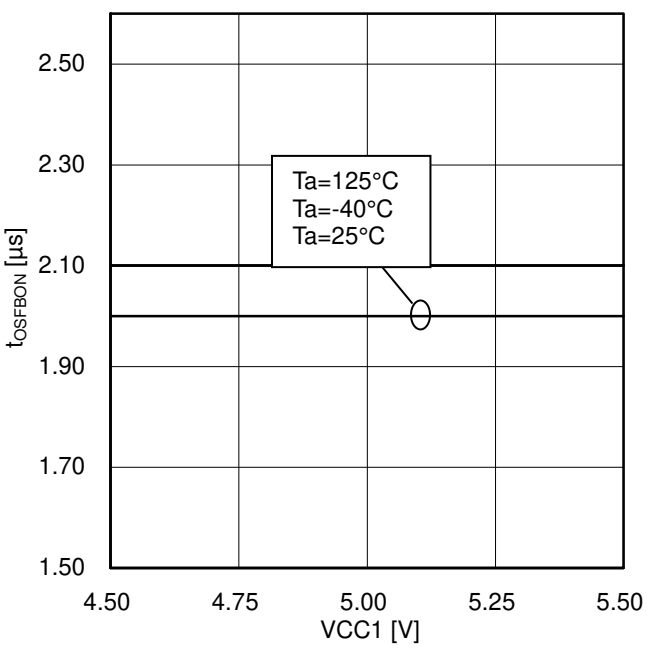


Figure 60. OSFB filter time vs. VCC1

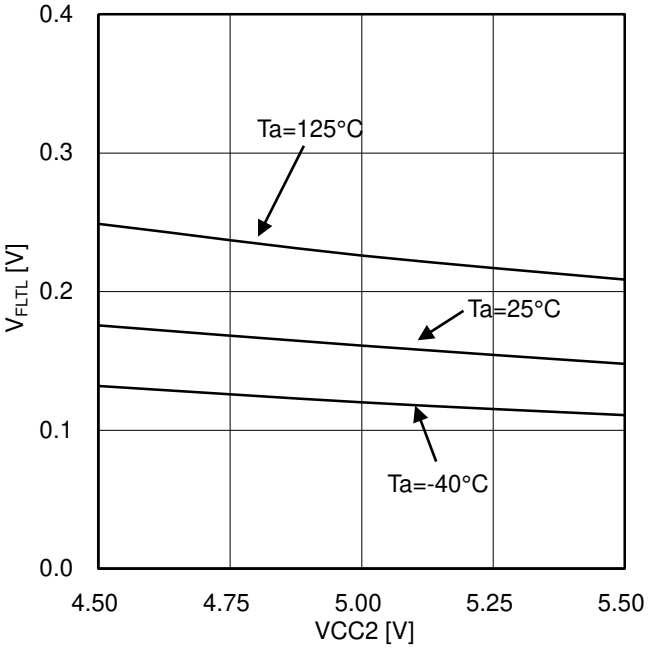


Figure 61. FLT output low voltage vs. VCC2 (IFLT=5mA)

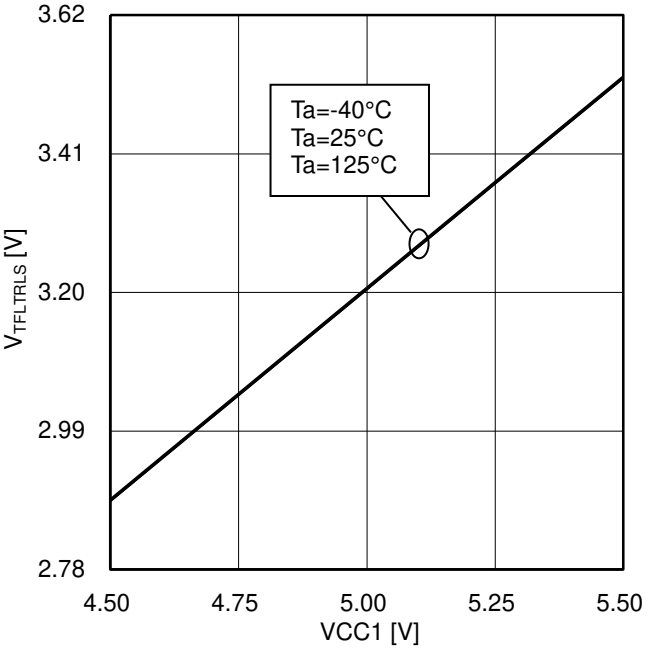


Figure 62. FLTRLS threshold vs. VCC1