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Datasheet

For Air-Conditioner Fan Motor

3-Phase Brushless Fan Motor Driver

BM6206FS

General Description

This motor driver IC adopts PrestoMOS™ as the output transistor, and put in a small full molding package with the 150° commutation controller chip and the high voltage gate driver chip. The protection circuits for overcurrent, overheating, under voltage lock out and the high voltage bootstrap diode with current regulation are built-in. It provides optimum motor drive system and downsizing the built-in PCB of the motor.

Features

- 600V PrestoMOS™ built-in
- Output current 1.5A
- Bootstrap operation by floating high side driver (including diode)
- 150° commutation logic
- PWM control (Upper arm switching)
- Phase control supported from 0° to +30° at 1° intervals
- Rotational direction switch
- FG signal output with pulse number switch (4 or 12)
- VREG output (5V/30mA)
- Protection circuits provided: CL, OCP, TSD, UVLO, MLP and the external fault input
- Fault output (open drain)

Applications

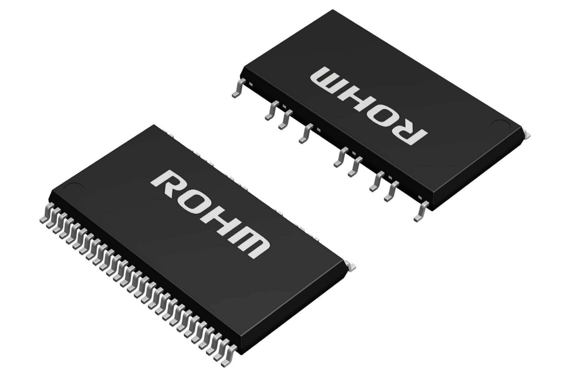
- Air conditioners; air purifiers; water pumps; dishwashers; washing machines

Key Specifications

Output MOSFET Voltage:	600V
Driver Output Current (DC):	±1.5A (Max)
Driver output Current (Pulse):	±2.5A (Max)
Output MOSFET DC On Resistance:	2.7Ω (Typ)
Duty Control Voltage Range:	2.1V to 5.4V
Phase Control Range:	0° to +30°
Operating Case Temperature:	-20°C to +100°C
Junction Temperature:	+150°C
Power Dissipation:	3.00W

Package

	W (Typ) x D (Typ) x H (Max)
SSOP-A54_36	22.0 mm x 14.1 mm x 2.4 mm



SSOP-A54_36

Typical Application Circuit

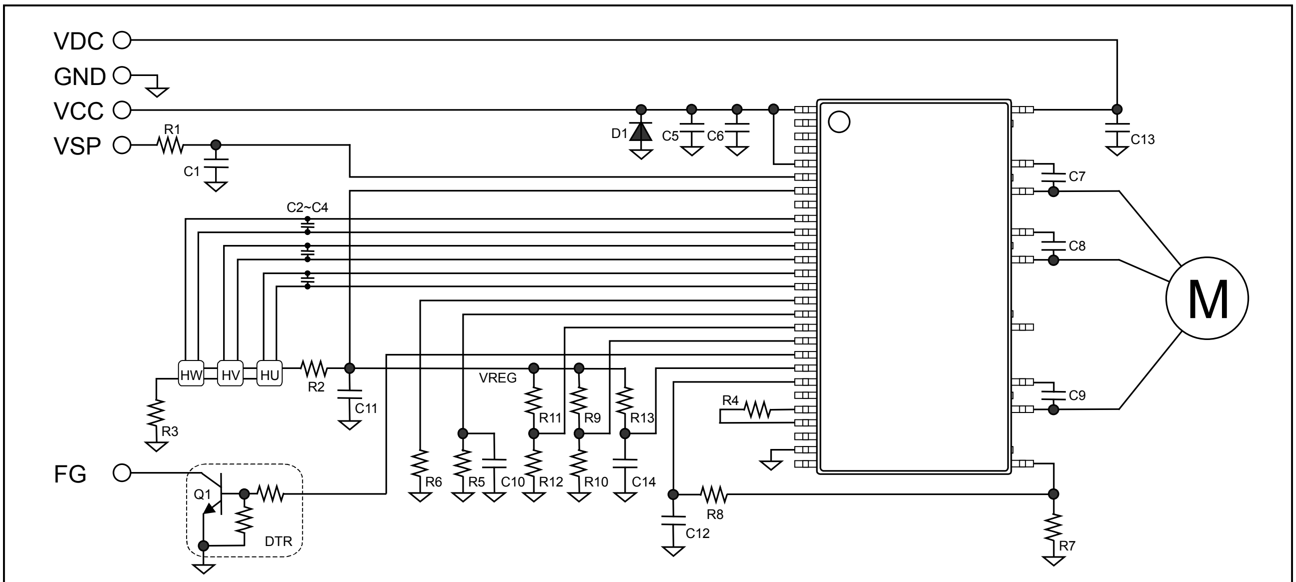


Figure 1. Application Circuit Example

○Product structure : Semiconductor IC ○This product is not designed protection against radioactive rays

Block Diagram and Pin Configuration

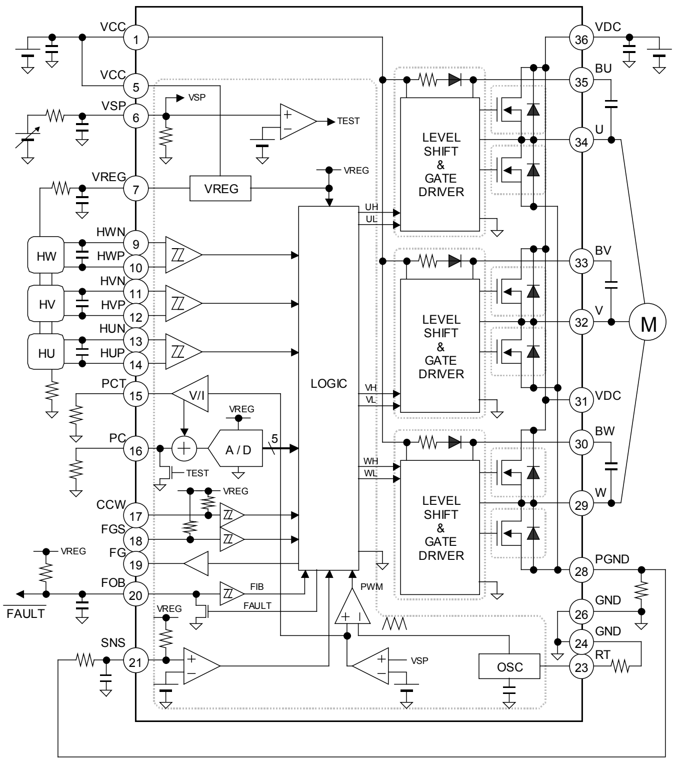


Figure 2. Block Diagram

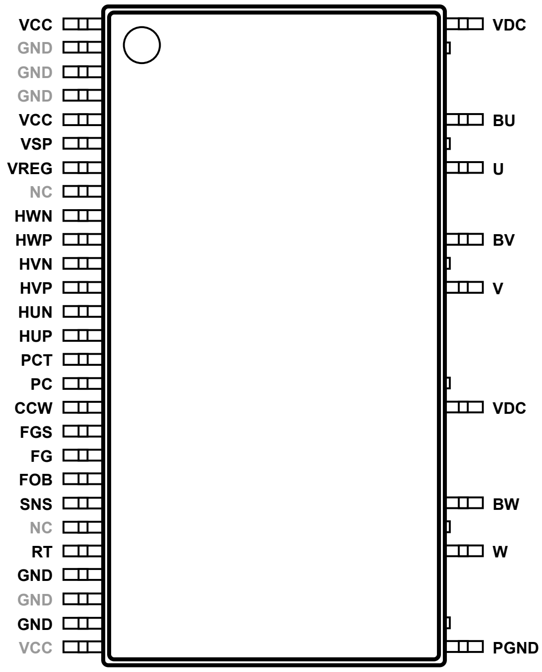


Figure 3. Pin Configuration
(Top View)

Pin Descriptions (NC: No Connection)

Pin	Name	Function	Pin	Name	Function
1	VCC	Low voltage power supply	36	VDC	High voltage power supply
2	GND	Ground	-	VDC	
3	GND	Ground			
4	GND	Ground			
5	VCC	Low voltage power supply	35	BU	Phase U floating power supply
6	VSP	Duty control voltage input pin	-	U	
7	VREG	Regulator output	34	U	Phase U output
8	NC				
9	HWN	Hall input pin phase W-			
10	HWP	Hall input pin phase W+	33	BV	Phase V floating power supply
11	HVN	Hall input pin phase V-	-	V	
12	HVP	Hall input pin phase V+	32	V	Phase V output
13	HUN	Hall input pin phase U-			
14	HUP	Hall input pin phase U+			
15	PCT	VSP offset voltage output pin			
16	PC	Phase control input pin	-	VDC	
17	CCW	Direction switch (H:CCW)	31	VDC	High voltage power supply
18	FGS	FG pulse # switch (H:12, L:4)			
19	FG	FG signal output			
20	FOB	Fault signal output (open drain)			
21	SNS	Over current sense pin	30	BW	Phase W floating power supply
22	NC		-	W	
23	RT	Carrier frequency setting pin	29	W	Phase W output
24	GND	Ground			
25	GND	Ground			
26	GND	Ground	-	PGND	
27	VCC	Low voltage power supply	28	PGND	Ground (current sense pin)

Note) All pin cut surfaces visible from the side of package are no connected, except the pin number is expressed as a “-”.

Description of Blocks

1. Commutation Logic

When the hall frequency is about 1.4-Hz or less (e.g. when the motor starts up), the commutation mode is 120° square wave drive with upper and lower switching (no lead angle). The controller monitors the hall frequency, and switches to 150° commutation drive when the hall frequency reaches or exceeds about 1.4-Hz over four consecutive cycles. Refer to the timing charts in figures 13 and 14.

Table 1. 120° Commutation (Six-State) Truth Table

HU	HV	HW	UH	VH	WH	UL	VL	WL
H	L	H	L	PWM	L	H	$\overline{PWM}$	L
H	L	L	L	L	PWM	H	L	$\overline{PWM}$
H	H	L	L	L	PWM	L	H	$\overline{PWM}$
L	H	L	PWM	L	L	$\overline{PWM}$	H	L
L	H	H	PWM	L	L	$\overline{PWM}$	L	H
L	L	H	L	PWM	L	L	$\overline{PWM}$	H

2. Duty Control

The switching duty can be controlled by forcing DC voltage with value from V_{SPMIN} to V_{SPMAX} to the VSP pin. When the VSP voltage is higher than V_{SPTST}, the controller forces PC pin voltage to ground (Testing mode, maximum duty and no lead angle). The VSP pin is pulled down internally by a 200 kΩ resistor. Therefore, note the impedance when setting the VSP voltage with a resistance voltage divider.

3. Carrier Frequency Setting

The carrier frequency setting can be freely adjusted by connecting an external resistor between the RT pin and ground. The RT pin is biased to a constant voltage, which determines the charge current to the internal capacitor. Carrier frequencies can be set within a range from about 16 kHz to 50 kHz. Refer to the formula to the right.

$$f_{OSC}[kHz] = \frac{400}{R_T[kohm]}$$

4. FG Signal Output

The number of FG output pulses can be switched in accordance with the number of poles and the rotational speed of the motor. The FG signal is output from the FG pin. The 12-pulse signal is generated from the three hall signals (exclusive NOR), and the 4-pulse signal is the same as hall U signal. It is recommended to pull up FGS pin to VREG voltage when malfunctioning because of the noise.

FGS	No. of pulse
H	12
L	4

5. Direction of Motor Rotation Setting

The direction of rotation can be switched by the CCW pin. When CCW pin is “H” or open, the motor rotates at CCW direction. When the real direction is different from the setting, the commutation mode is 120° square wave drive (no lead angle). It is recommended to pull up CCW pin to VREG voltage when malfunctioning because of the noise.

CCW	Direction
H	CCW
L	CW

6. Hall Signal Comparator

The hall comparator provides voltage hysteresis to prevent noise malfunctions. The bias current to the hall elements should be set to the input voltage amplitude from the element, at a value higher than the minimum input voltage, $V_{HALLMIN}$. We recommend connecting a ceramic capacitor with value from 100 pF to 0.01 µF, between the differential input pins of the hall comparator. Note that the bias to hall elements must be set within the common mode input voltage range V_{HALLCM}.

7. **Output Duty Pulse Width Limiter**
Pulse width duty is controlled during PWM switching in order to ensure the operation of internal power transistor. The controller doesn't output pulse of less than T_{MIN} (0.8μs minimum), nor output a duty pulse of D_{MAX} or more. Dead time is forcibly provided to prevent internal power transistors to turn-on simultaneously in upper and lower side in gate driver output (for example, UH and UL) of each arm. This will not overlap the minimum time T_{DT} (1.6μs minimum). Because of this, the maximum duty of 120° square wave drive at start up is 84% (typical).

8. **Phase Control Setting**
The driving signal phase can be advanced to the hall signal for phase control. The lead angle is set by forcing DC voltage to the PC pin. The input voltage is converted digitally by a 6-bit A/D converter, in which internal VREG voltage is assumed to be full-scale, and the converted data is processed by a logic circuit. The lead angle can be set from 0° to +30° at 1° intervals, and updated fourth hall cycle of phase W falling edge. Phase control function only operates at 150° commutation mode. However, the controller forces PC pin voltage to ground (no lead angle) during testing mode. The VSP offset voltage (Figure 33) is buffered to PCT pin, to connect an external resistor between PCT pin and ground. The internal bias current is determined by PCT voltage and the resistor value - V_{PCT} / R_{PCT} -, and mixed to PC pin. As a result, the lead angle setting is followed with the duty control voltage, and the performance of the motor can be improved. Please select the R_{PCT} value from 50 kΩ to 200 kΩ in the range on the basis of 100 kΩ, because the PCT pin current capability is a 100 μA or less.

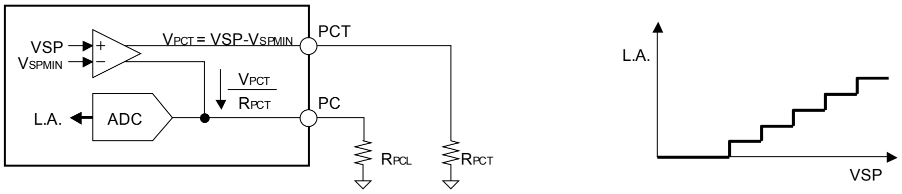


Figure 4. Phase Control Setting Example 1

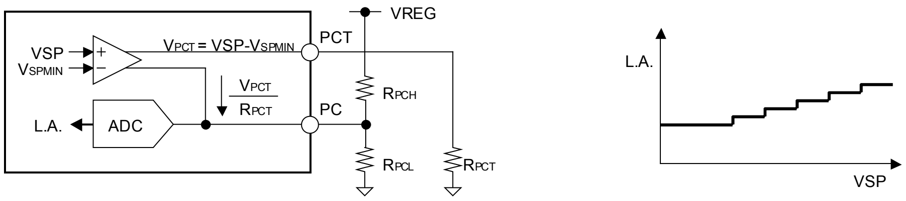


Figure 5. Phase Control Setting Example 2

9. **Current Limiter (CL) Circuit and Overcurrent Protection (OCP) Circuit**
The current limiter circuit can be activated by connecting a low value resistor for current detection between the output stage ground (PGND) and the controller ground (GND). When the SNS pin voltage reaches or surpasses the threshold value (V_{SNS}, 0.5V typical), the controller forces all the upper switching arm inputs low (UH, VH, WH = L, L, L), thus initiating the current limiter operation. When the SNS pin voltage swings below the ground, it is recommended to insert a resistor - 1.5 kΩ or more - between SNS pin and PGND pin to prevent malfunction. Since this limiter circuit is not a latch type, it returns to normal operation - synchronizing with the carrier frequency - once the SNS pin voltage falls below the threshold voltage. A filter is built into the overcurrent detection circuit to prevent malfunctions, and does not activate when a short pulse of less than T_{MASK} is present at the input.
When the SNS pin voltage reaches or surpasses the threshold value (V_{OVER}, 0.9V typical) because of the power fault or the short circuit except the ground fault, the gate driver outputs low to the gate of all output MOSFETs, thus initiating the overcurrent protection operation. Since this protection circuit is also not a latch type, it returns to normal operation synchronizing with the carrier frequency.

10. Under Voltage Lock Out (UVLO) Circuit

To secure the lowest power supply voltage necessary to operate the controller and the driver, and to prevent under voltage malfunctions, the UVLO circuits are independently built into the upper side floating driver, the lower side driver and the controller. When the supply voltage falls to V_{UVL} or below, the controller forces driver outputs low. When the voltage rises to V_{UVH} or above, the UVLO circuit ends the lockout operation and returns the chip only after 32 carrier frequency periods (1.6ms for the default 20kHz frequency) to normal operation. Even if the controller returns to normal operation, the output begins from the following control input signal.

The voltage monitor circuit (4.0V nominal) is built-in for the VREG voltage. Therefore, the UVLO circuit does not release operation when the VREG voltage rising is delayed behind the VCC voltage rising even if VCC voltage becomes V_{UVH} or more.

11. Thermal Shutdown (TSD) Circuit

The TSD circuit operates when the junction temperature of the controller exceeds the preset temperature (125°C nominal). At this time, the controller forces all driver outputs low. Since thermal hysteresis is provided in the TSD circuit, the chip returns to normal operation when the junction temperature falls below the preset temperature (100°C nominal). The TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation in the presence of extreme heat. Do not continue to use the IC after the TSD circuit is activated, and do not use the IC in an environment where activation of the circuit is assumed.

Moreover, it is not possible to follow the output MOSFET junction temperature rising rapidly because it is a gate driver chip that monitors the temperature and it is likely not to function effectively.

12. Motor Lock Protection (MLP) Circuit

When the controller detects the motor locking during fixed time of 4 seconds nominal when each edge of the hall signal doesn't input either, the controller forces all driver outputs low under a fixed time 20 seconds nominal, and self-returns to normal operation. This circuit is enabled if the voltage force to VSP is over the duty minimum voltage V_{SPMIN}, and note that the motor cannot start up when the controller doesn’t detect the motor rotation by the minimum duty control. Even if the edge of the hall signal is inputted within range of the OFF state by this protection circuit, it is ignored. But if the VSP is forced to ground level once, the protection can be canceled immediately.

13. Hall Signal Wrong Input Detection

Hall element abnormalities may cause incorrect inputs that vary from the normal logic. When all hall input signals go high or low, the hall signal wrong input detection circuit forces all driver outputs low. And when the controller detects the abnormal hall signals continuously for four times or more motor rotation, the controller forces all driver outputs low and latches the state. It is released if the duty control voltage VSP is forced to ground level once.

14. Internal Voltage Regulator

The internal voltage regulator VREG is output for the bias of the hall element and the phase control setting. However, when using the VREG function, be aware of the I_{OMAX} value. If a capacitor is connected to the ground in order to stabilize output, a value of 1 µF or more should be used. In this case, be sure to confirm that there is no oscillation in the output.

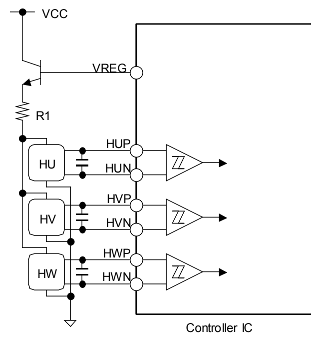


Figure 6. VREG Output Pin Application Example

15. Bootstrap Operation

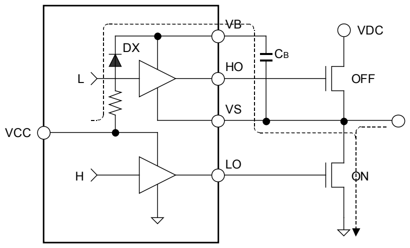


Figure 7. Charging Period

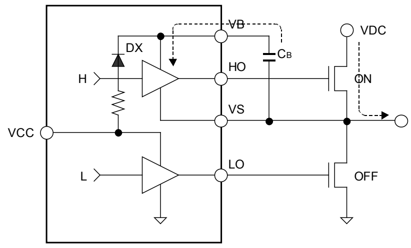


Figure 8. Discharging Period

The bootstrap is operated by the charge period and the discharge period being alternately repeated for bootstrap capacitor (CB) as shown in the figure above. In a word, this operation is repeated while the output of an external transistor is switching with synchronous rectification. Because the supply voltage of the floating driver is charged from the VCC power supply to CB through prevention of backflow diode DX, it is approximately (VCC-1V). The resistance series connection with DX has the impedance of approximately 200 Ω. Because the total gate charge is needed only by the carrier frequency in the upper switching section of 150° commutation driving, please set it after confirming actual application operation.

16. Fault Signal Output

When the controller detects either state that should be protected the overcurrent (OCP) and the over temperature (TSD), the FOB pin outputs low (open drain) and it returns to normal operation synchronizing with the carrier frequency. Even when this function is not used, the FOB pin is pull-up to the voltage of 3V or more and at least a resistor with a value 10k Ω or more. A filter is built into the fault signal input circuit to prevent malfunctions by the switching noise, and does not activate when a short pulse of less than T_{MASK} is present at the input. The time to the fault operation is the sum total of the propagation delay time of the detection circuit and the filter time, 1.6μs (typical).

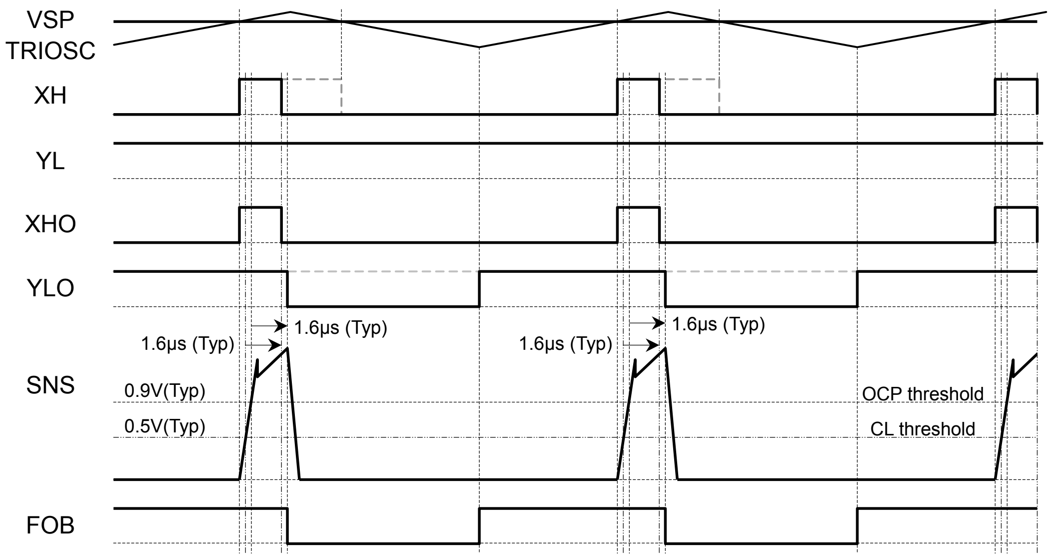


Figure 9. Fault Operation ~ OCP ~ Timing Chart

The release time from the protection operation can be changed by inserting an external capacitor. Refer to the formula below. Release time of 5ms or more is recommended.

$$t = -ln(1 - \frac{2.3}{V_{REG}}) \cdot R \cdot C \quad [s]$$

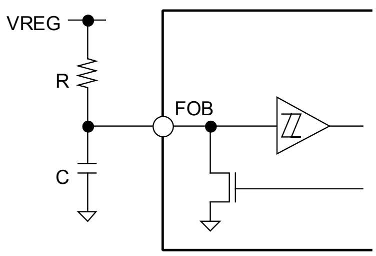


Figure 10. Release Time Setting Application Circuit

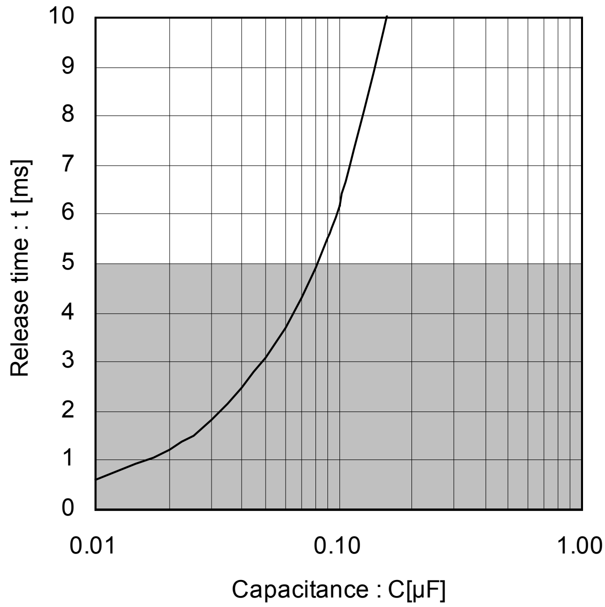


Figure 11. Release Time (Reference Data @R=100kΩ)

17. Switching Time

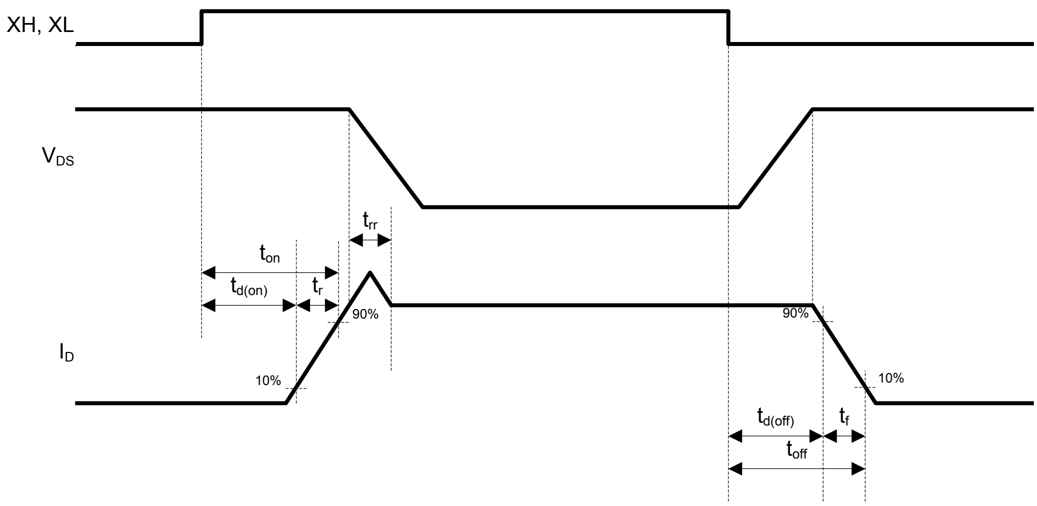


Figure 12. Switching Time Definition

Parameter	Symbol	Reference	Unit	Conditions
High Side Switching Time	$t_{dH(on)}$	790	ns	VDC=300V, VCC=15V, I_D=0.75A Inductive load The propagation delay time: Internal gate driver input stage to the driver IC output.
	t_{rH}	110	ns	
	t_{rrH}	200	ns	
	$t_{dH(off)}$	490	ns	
	t_{fH}	15	ns	
Low Side Switching Time	$t_{dL(on)}$	830	ns	
	t_{rL}	110	ns	
	t_{rrL}	160	ns	
	$t_{dL(off)}$	570	ns	
	t_{fL}	80	ns	

Timing Chart (CW)

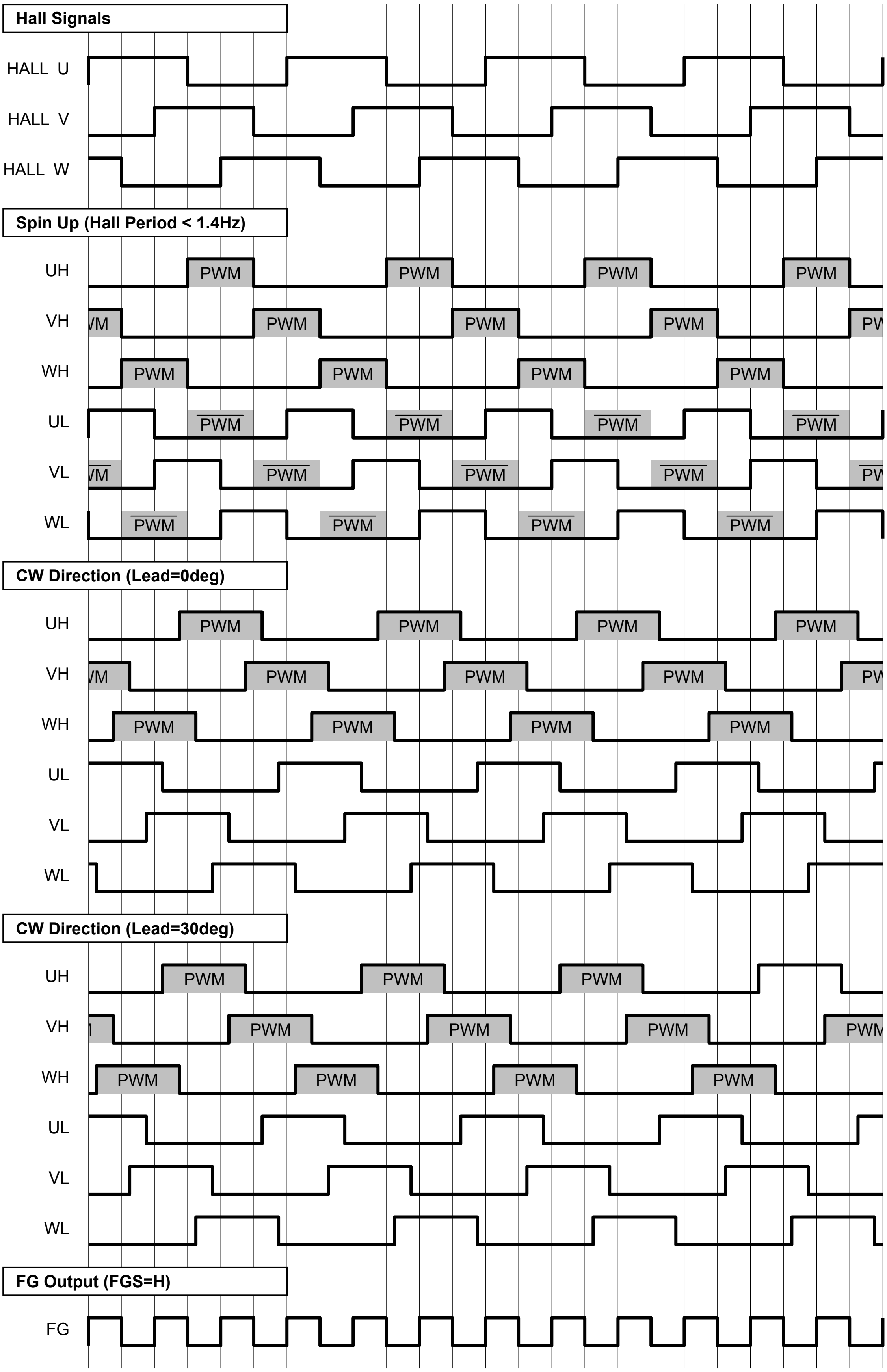


Figure 13. Timing Chart (Clockwise)

Timing Chart (CCW)

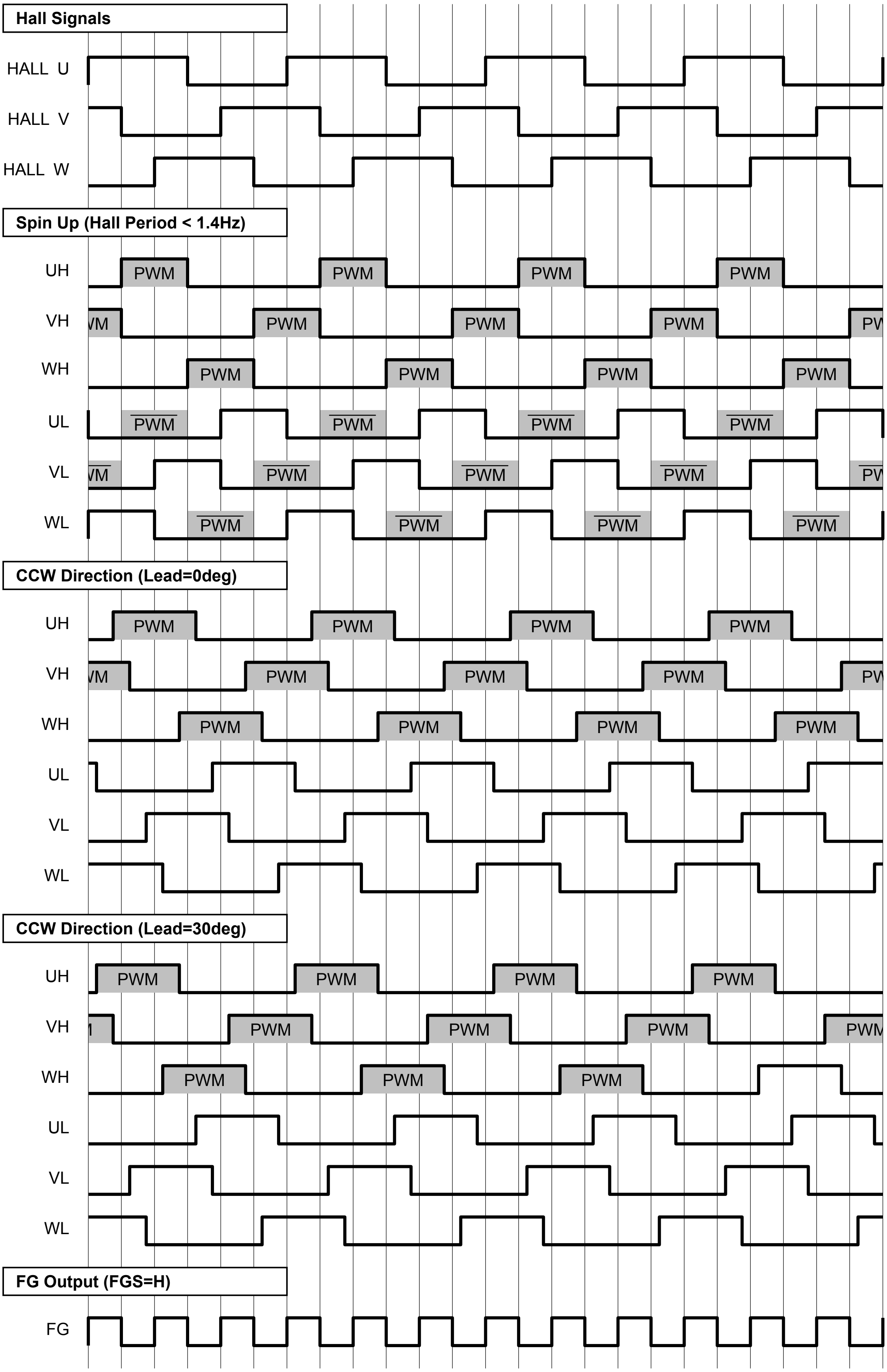


Figure 14. Timing Chart (Counter Clockwise)

Controller Outputs and Operation Mode Summary

Conditions	Detected direction	Forward (CW:U~V~W, CCW:U~W~V)		Reverse (CW:U~W~V, CCW:U~V~W)	
	Hall sensor frequency	< 1.4Hz	1.4Hz <	< 1.4Hz	1.4Hz <
Normal operation	VSP < V_{SPMIN} (Duty off)	Upper and lower arm off			
	V_{SPMIN} < VSP < V_{SPMAX} (Control range)	120° Upper and lower switching	150° Upper switching	120° Upper and lower switching	120° Upper switching
	V_{SPTST} < VSP (Testing mode)		150° Upper switching (No lead angle)		
Protect operation	Current limiter (Note 1)	Upper arm off			Upper and lower arm off
	Overcurrent (Note 2)	Upper and lower arm off			
	TSD (Note 2)				
	External input (Note 2)				
	UVLO (Note 3)				
	Motor lock				
	Hall sensor abnormally	Upper and lower arm off and latch			

(Note) The controller monitors both edges of three hall sensors for detecting period.
(Note) Phase control function only operates at 150° commutation mode. However, the controller forces no lead angle during the testing mode.
(Note 1) It returns to normal operation by the carrier frequency synchronization.
(Note 2) It works together with the fault operation, and returns after the release time synchronizing with the carrier frequency.
(Note 3) It returns to normal operation after 32 cycles of the carrier oscillation period.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Output MOSFET	V_{DSS}	600 (Note 1)	V
Supply Voltage	V_{DC}	-0.3 to +600 (Note 1)	V
Output Voltage	V_U, V_V, V_W	-0.3 to +600 (Note 1)	V
High Side Supply Pin Voltage	V_{BU}, V_{BV}, V_{BW}	-0.3 to +600 (Note 1)	V
High Side Floating Supply Voltage	V_{BU}-V_U, V_{BV}-V_V, V_{BW}-V_W	-0.3 to +20	V
Low Side Supply Voltage	V_{CC}	-0.3 to +20	V
Duty Control Voltage	V_{SP}	-0.3 to +20	V
All Others	$V_{I/O}$	-0.3 to +5.5	V
Driver Outputs (DC)	$I_{OMAX(DC)}$	±1.5 (Note 1)	A
Driver Outputs (Pulse)	$I_{OMAX(PLS)}$	±2.5 (Note 1, 2)	A
Fault Signal Output	$I_{OMAX(FOB)}$	15 (Note 1)	mA
Power Dissipation	Pd	3.00 (Note 3)	W
Thermal Resistance	R_{thj-c}	15	°C/W
Operating Case Temperature	T_C	-20 to +100	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Junction Temperature	T_{jmax}	150	°C

(Note) All voltages are with respect to ground.
(Note 1) Do not, however, exceed Pd or ASO.
(Note 2) Pw ≤ 10μs, Duty cycle ≤ 1%
(Note 3) Mounted on a 70mm x 70mm x 1.6mm FR4 glass-epoxy board with less than 3% copper foil. Derated at 24mW/°C above 25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Tc=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DC}	-	310	400	V
High Side Floating Supply Voltage	V_{BU}-V_U, V_{BV}-V_V, V_{BW}-V_W	13.5	15	16.5	V
Low Side Supply Voltage	V_{CC}	13.5	15	16.5	V
Bootstrap Capacitor	C_B	1.0	-	-	μF
VREG Bypass Capacitor	C_{VREG}	1.0	-	-	μF
Shunt Resistor (PGND)	R_S	0.6	-	-	Ω
Junction Temperature	T_j	-	-	125	°C

(Note) All voltages are with respect to ground.

Electrical Characteristics (Driver part, unless otherwise specified, Ta=25°C and VCC=15V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply						
HS Quiescence Current	I_{BBQ}	30	70	150	μA	VSP=0V, each phase
LS Quiescence Current	I_{CCQ}	0.2	0.7	1.3	mA	VSP=0V
Output MOSFET						
D-S Breakdown Voltage	$V_{(BR)DSS}$	600	-	-	V	I_D=1mA, VSP=0V
Leak Current	I_{DSS}	-	-	100	μA	V_{DS}=600V, VSP=0V
DC On Resistance	$R_{DS(ON)}$	-	2.7	3.5	Ω	I_D=0.75A
Diode Forward Voltage	V_{SD}	-	1.1	1.5	V	I_D=0.75A
Bootstrap Diode						
Leak Current	I_{LBD}	-	-	10	μA	V_{BX}=600V
Forward Voltage	V_{FBD}	1.5	1.8	2.1	V	I_{BD}=-5mA, including series-R
Series Resistance	R_{BD}	-	200	-	Ω	
Under Voltage Lock Out						
HS Release Voltage	V_{BUVH}	9.5	10.0	10.5	V	V_{BX} - V_X
HS Lockout Voltage	V_{BUVL}	8.5	9.0	9.5	V	V_{BX} - V_X

Electrical Characteristics (Controller part, unless otherwise specified, Ta=25°C and VCC=15V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply						
Supply Current	I_{CC}	0.8	1.7	3.0	mA	VSP=0V
VREG Voltage	V_{REG}	4.5	5.0	5.5	V	I_O=-30mA
Hall Comparators						
Input Bias Current	I_{HALL}	-2.0	-0.1	2.0	μA	V_{IN}=0V
Common Mode Input	V_{HALLCM}	0	-	V_{REG}-1.5	V	
Minimum Input Level	$V_{HALLMIN}$	50	-	-	mV_{p-p}	
Hysteresis Voltage P	$V_{HALLHY+}$	5	13	23	mV	
Hysteresis Voltage N	$V_{HALLHY-}$	-23	-13	-5	mV	
Duty Control						
Input Bias Current	I_{SP}	15	25	35	μA	V_{IN}=5V
Duty Minimum Voltage	V_{SPMIN}	1.8	2.1	2.4	V	
Duty Maximum Voltage	V_{SPMAX}	5.1	5.4	5.7	V	
Testing Operation Range	V_{SPTST}	8.2	-	18	V	
Minimum Output Duty	D_{MIN}	-	2	-	%	F_{OSC}=20kHz
Maximum Output Duty	D_{MAX}	-	95	-	%	F_{OSC}=20kHz
Mode Switch - FGS and CCW						
Input Bias Current	I_{IN}	-70	-50	-30	μA	V_{IN}=0V
Input High Voltage	V_{INH}	3	-	V_{REG}	V	
Input Low Voltage	V_{INL}	0	-	1	V	
Fault Input/Output - FOB						
Input High Voltage	V_{FOBIH}	3	-	V_{REG}	V	
Input Low Voltage	V_{FOBIL}	0	-	1	V	
Output Low Voltage	V_{FOBOL}	0	0.07	0.60	V	I_O=5mA
Monitor Output - FG						
Output High Voltage	V_{MONH}	V_{REG}-0.40	V_{REG}-0.08	V_{REG}	V	I_O=-2mA
Output Low Voltage	V_{MONL}	0	0.02	0.40	V	I_O=2mA
Current Detection						
Input Bias Current	I_{SNS}	-30	-20	-10	μA	V_{IN}=0V
Current Limiter Voltage	V_{SNS}	0.48	0.50	0.52	V	
Overcurrent Voltage	V_{OVER}	0.84	0.90	0.96	V	
Noise Masking Time	T_{MASK}	0.8	1.0	1.2	μs	
Phase Control						
Minimum Lead Angle	P_{MIN}	-	0	1	deg	V_{PC}=0V
Maximum Lead Angle	P_{MAX}	29	30	-	deg	V_{PC}=1/2·V_{REG}
Carrier Frequency Oscillator						
Carrier Frequency	F_{OSC}	18	20	22	kHz	R_T=20kΩ
Under Voltage Lock Out						
LS Release Voltage	V_{CCUVH}	11.5	12.0	12.5	V	
LS Lockout Voltage	V_{CCUVL}	10.5	11.0	11.5	V	

Typical Performance Curves (Reference data)

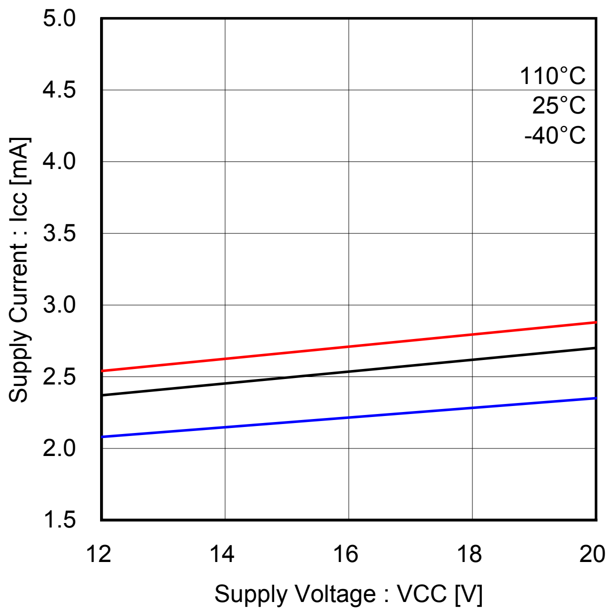


Figure 15. Quiscence Current
(Low Side Drivers)

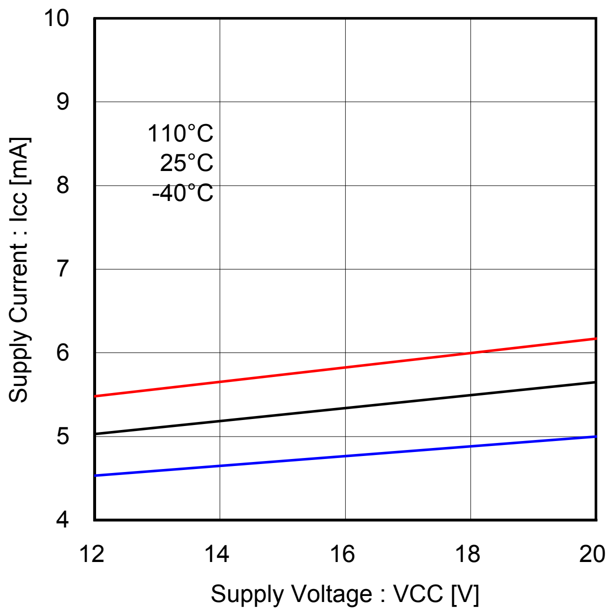


Figure 16. Low Side Drivers Operating Current
(F_{PWM}: 20kHz)

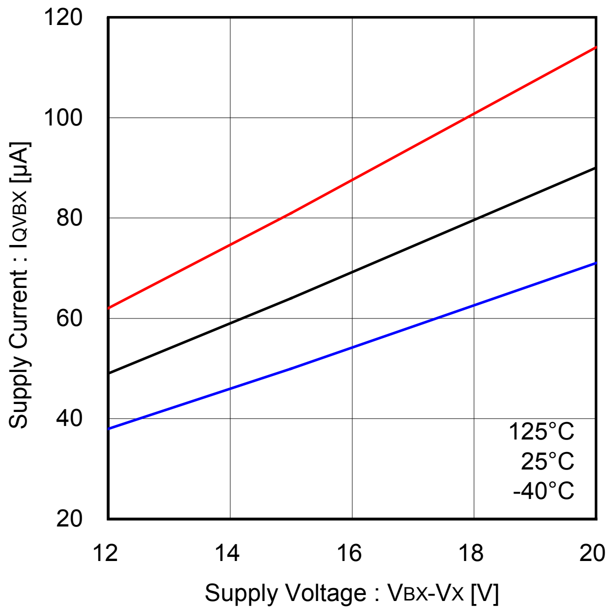


Figure 17. Quiescence Current
(High Side Driver, Each Phase)

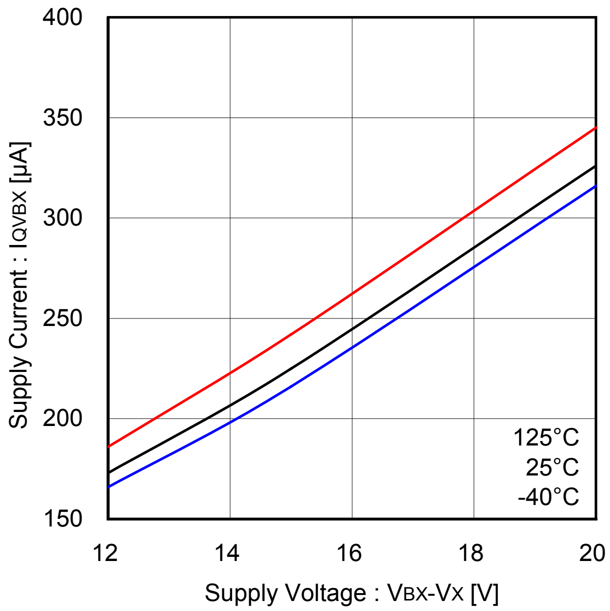


Figure 18. High Side Driver Operating Current
(F_{PWM}: 20kHz, Each Phase)

Typical Performance Curves (Reference data) - Continued

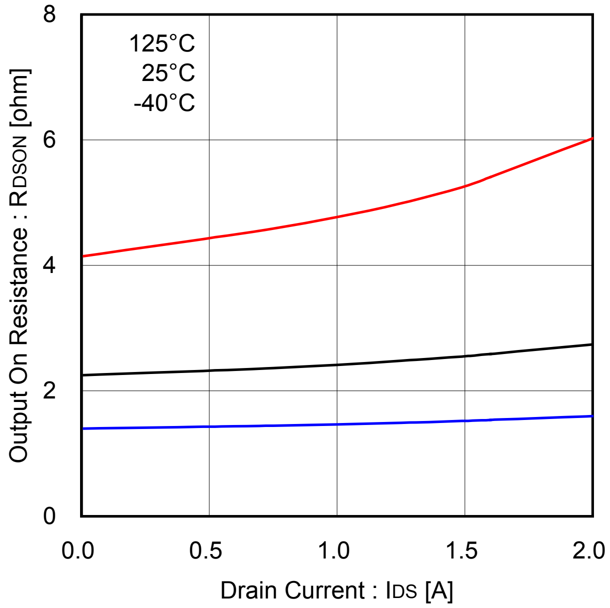


Figure 19. Output MOSFET ON Resistance

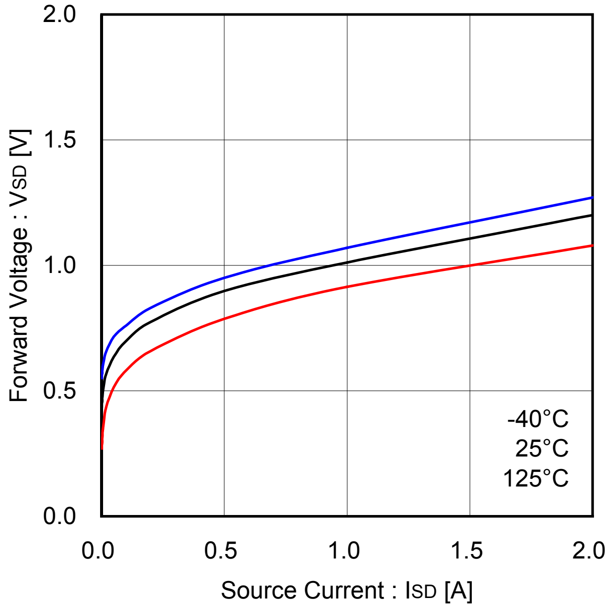


Figure 20. Output MOSFET Body Diode

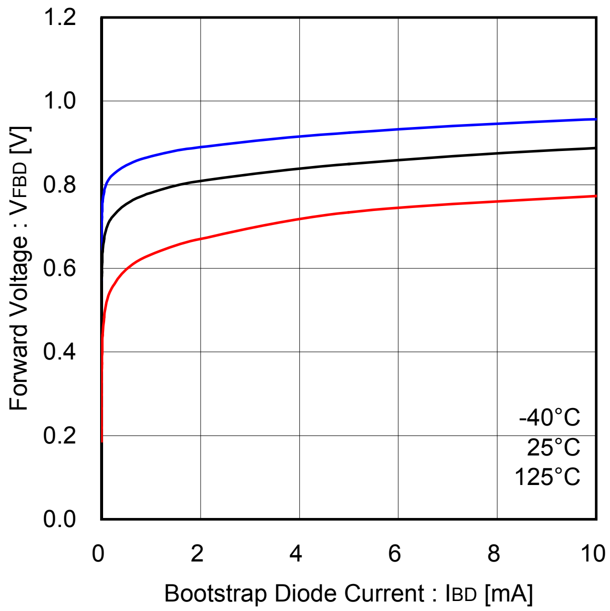


Figure 21. Bootstrap Diode Forward Voltage

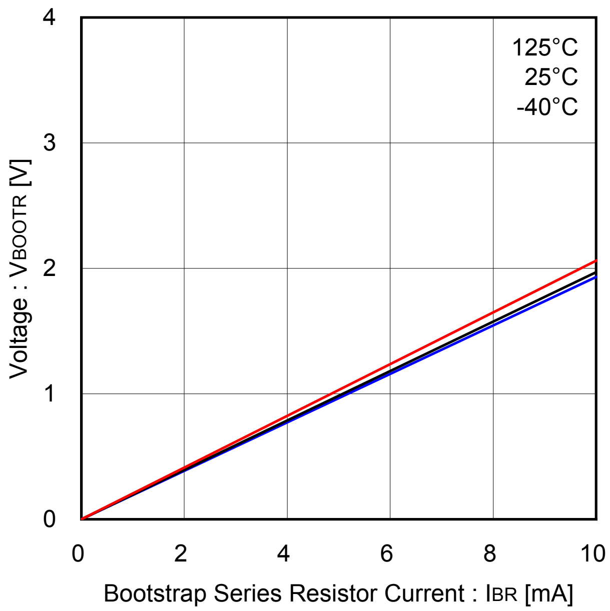


Figure 22. Bootstrap Series Resistor

Typical Performance Curves (Reference data) - Continued

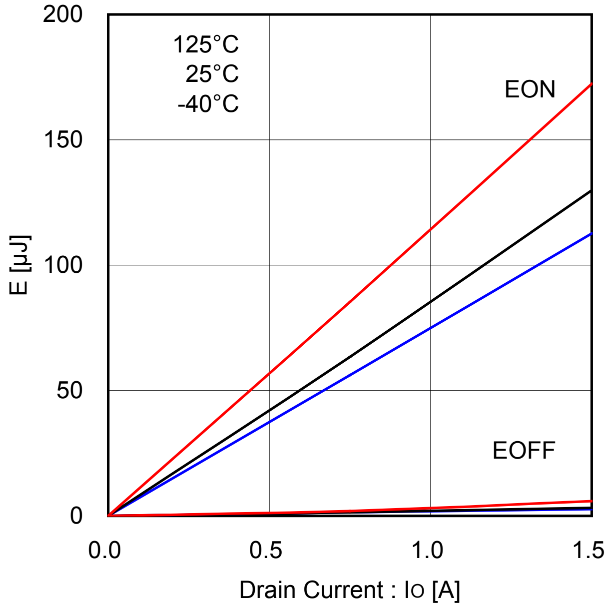


Figure 23. High Side Switching Loss (VDC=300V)

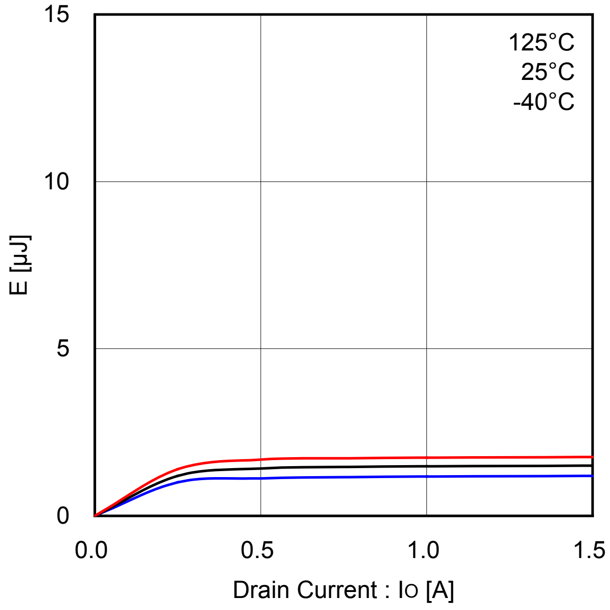


Figure 24. High Side Recovery Loss (VDC=300V)

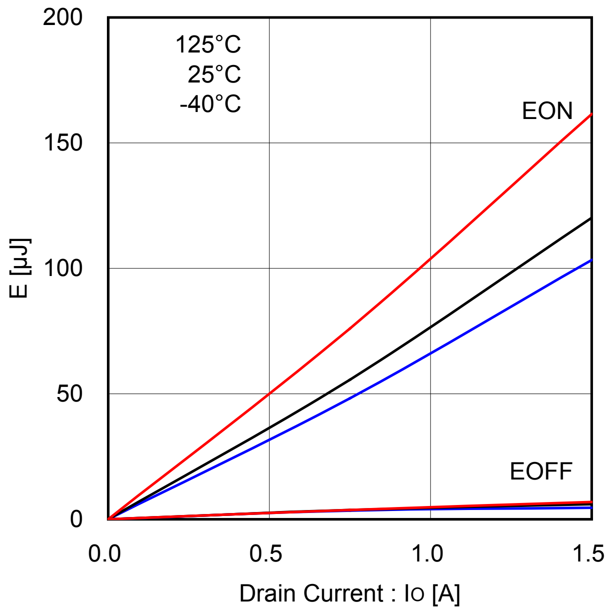


Figure 25. Low Side Switching Loss (VDC=300V)

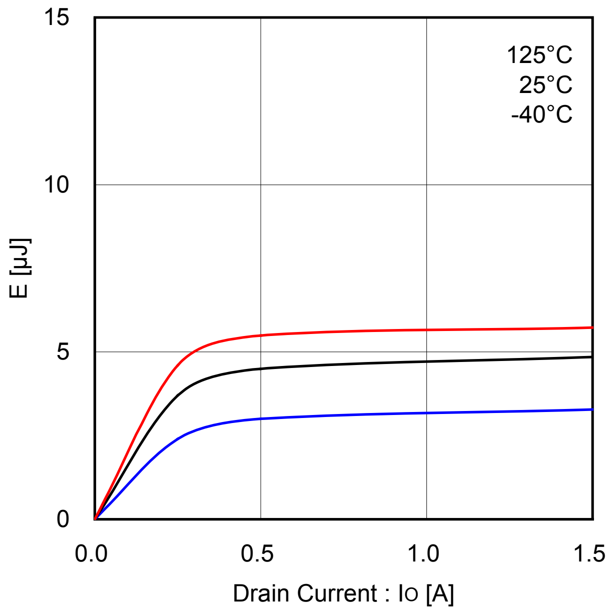


Figure 26. Low Side Recovery Loss (VDC=300V)

Typical Performance Curves (Reference data) - Continued

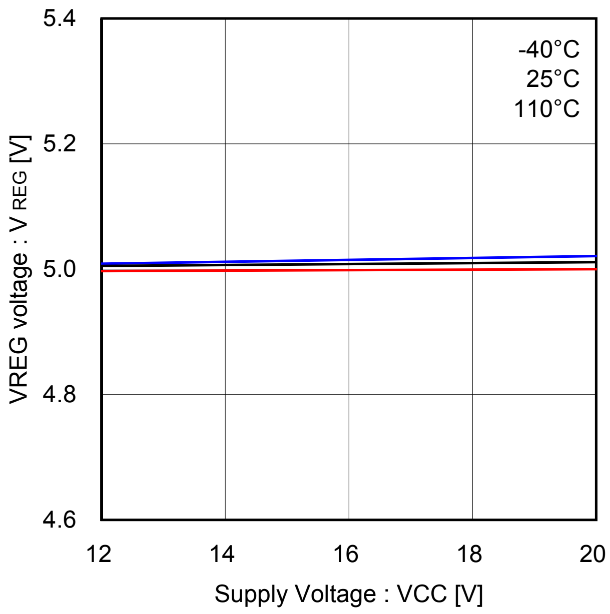


Figure 27. VREG - VCC

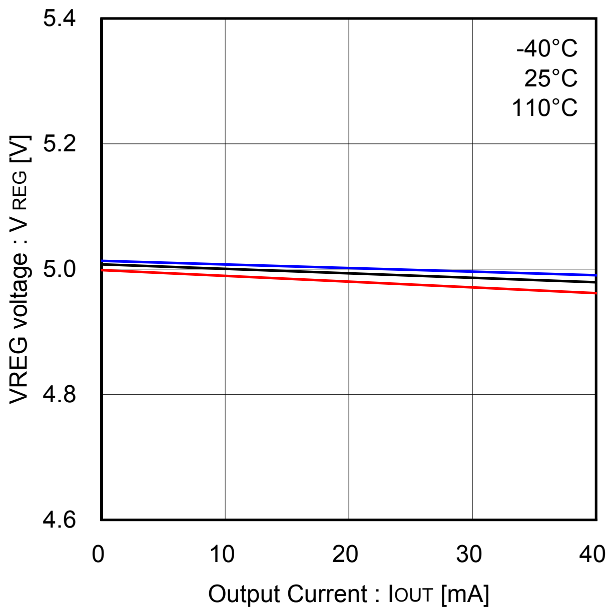


Figure 28. VREG Drive Capability

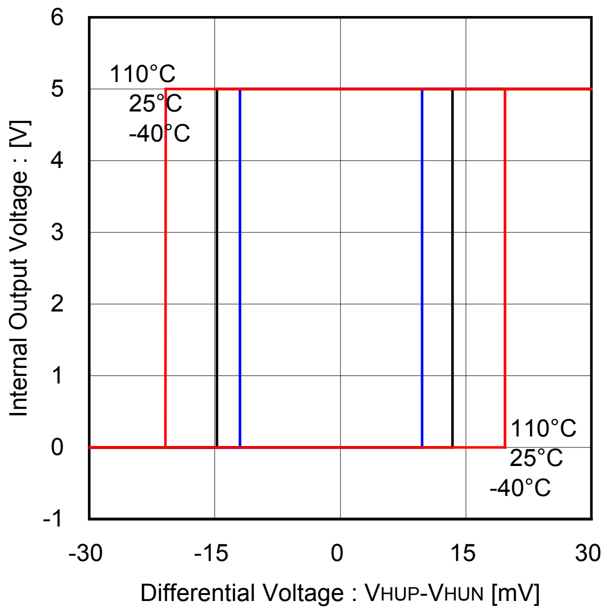


Figure 29. Hall Comparator Hysteresis Voltage

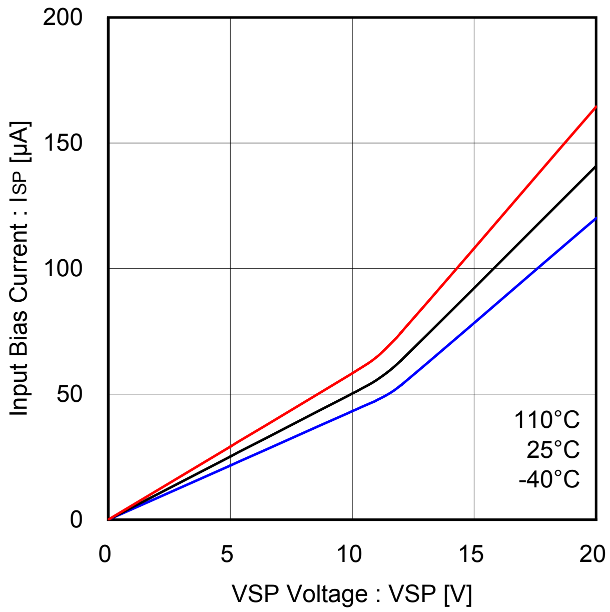


Figure 30. VSP Input Bias Current

Typical Performance Curves (Reference data) - Continued

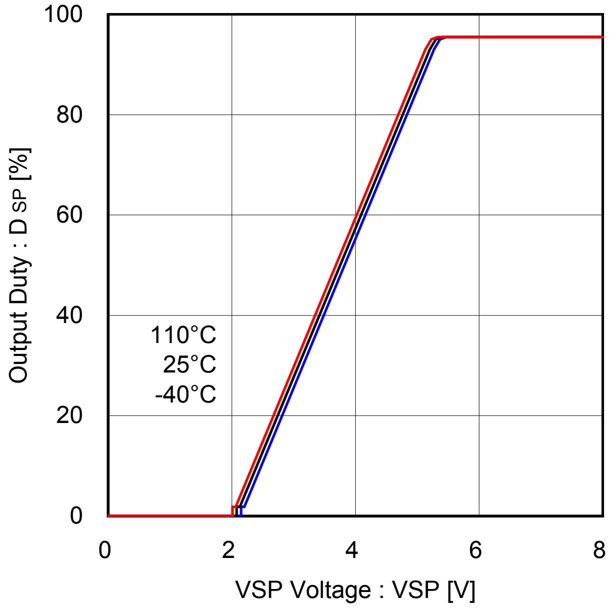


Figure 31. Output Duty - VSP Voltage

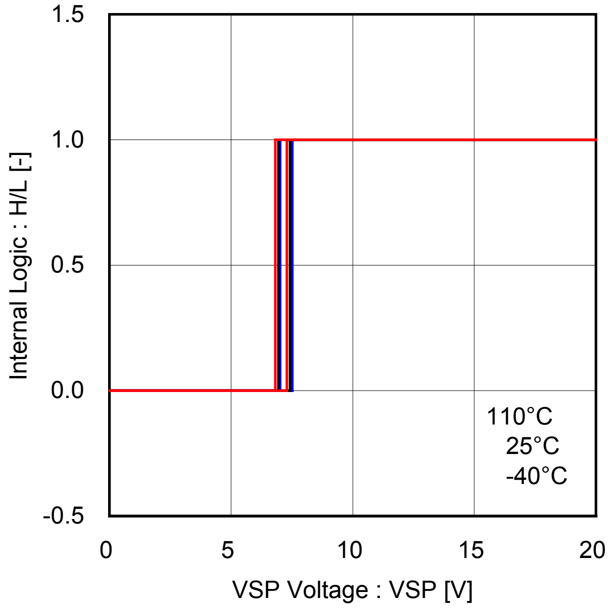


Figure 32. Testing Mode Threshold Voltage

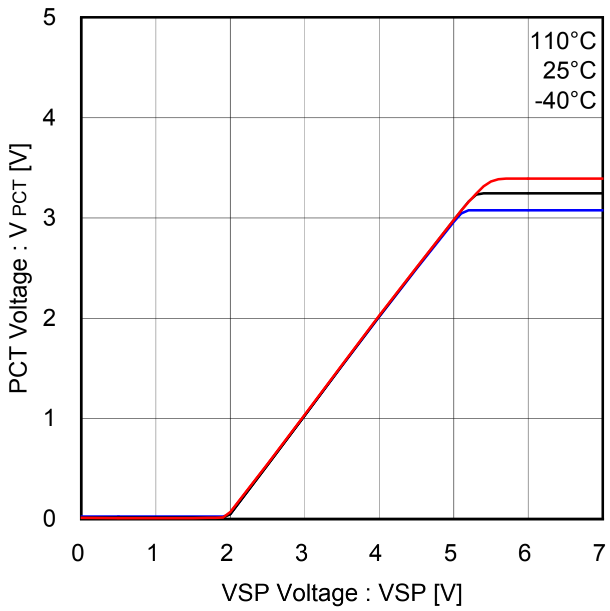


Figure 33. VSP - PCT Offset Voltage

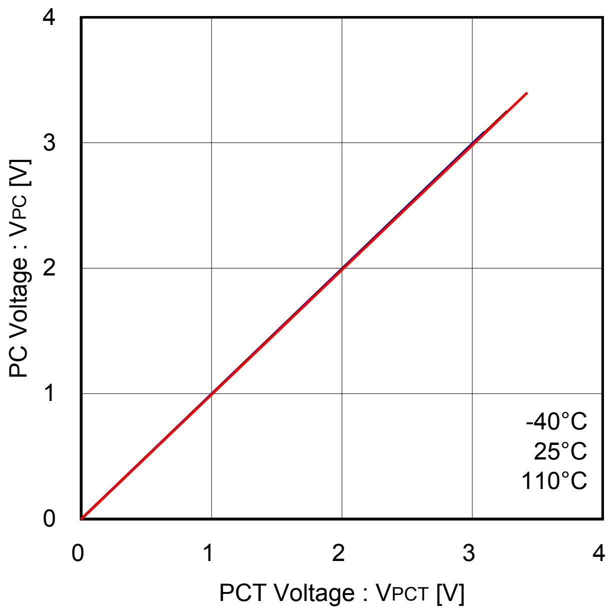


Figure 34. PCT - PC Linearity
($R_{PCT}=R_{PC}=100k\Omega$)

Typical Performance Curves (Reference data) - Continued

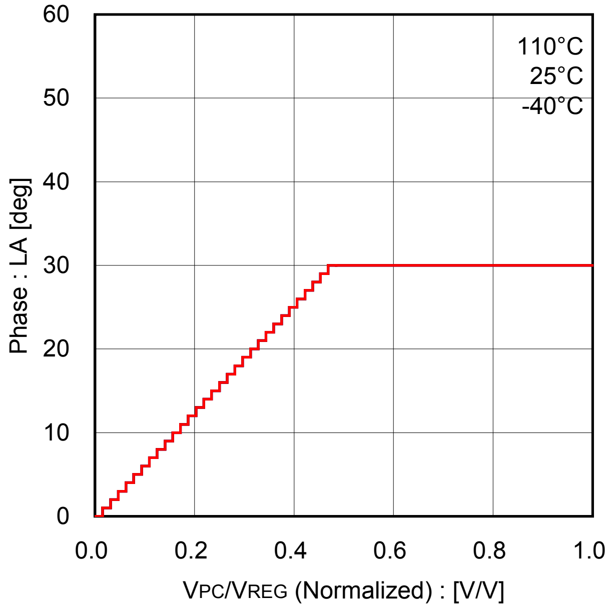


Figure 35. PC Voltage Normalized - Lead Angle

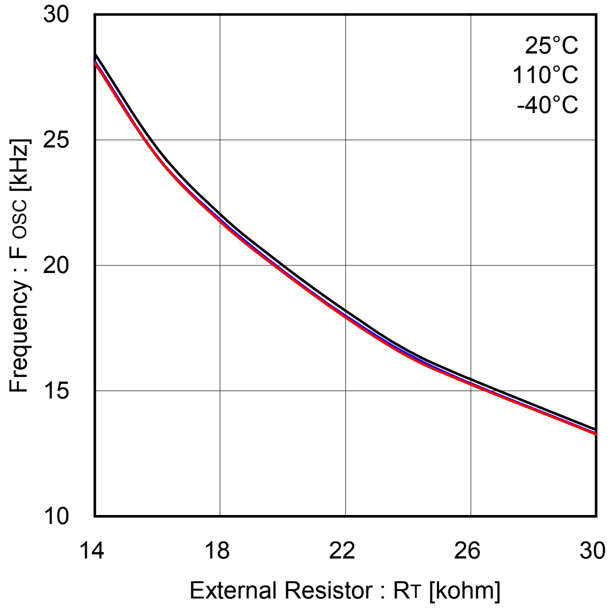


Figure 36. Carrier Frequency - RT

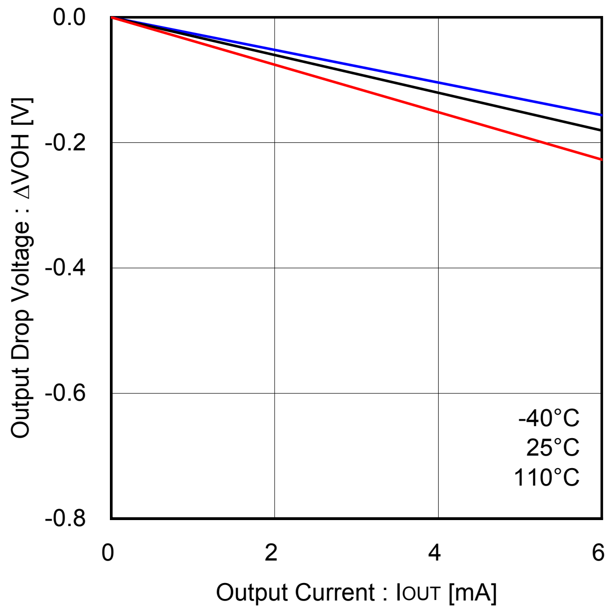


Figure 37. High Side Output Voltage (FG)

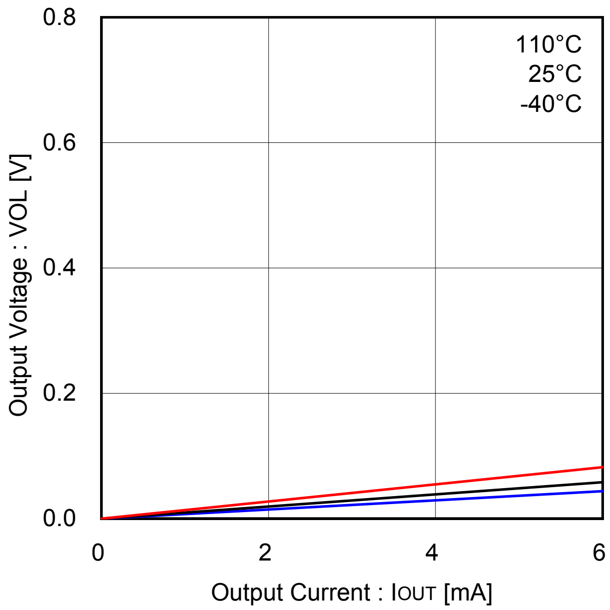


Figure 38. Low Side Output Voltage (FG)

Typical Performance Curves (Reference data) - Continued

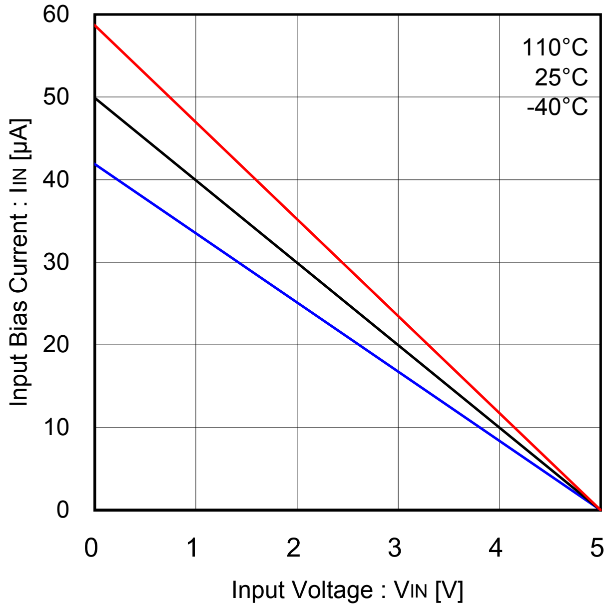


Figure 39. Input Bias Current
(CCW, FGS)

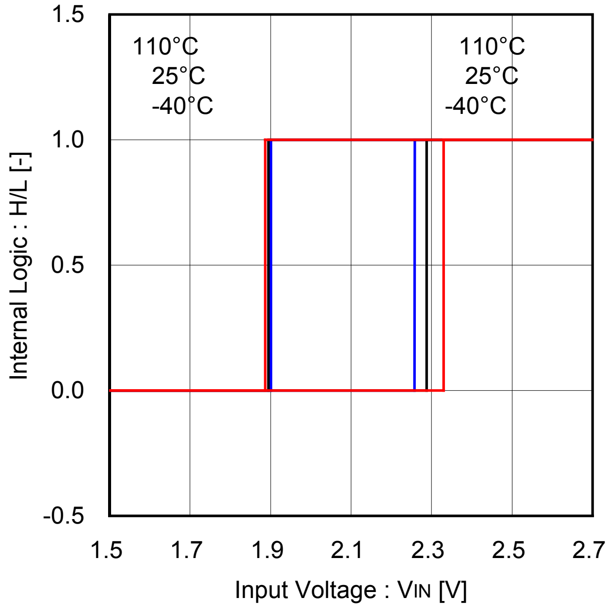


Figure 40. Input Threshold Voltage
(CCW, FGS, FOB)

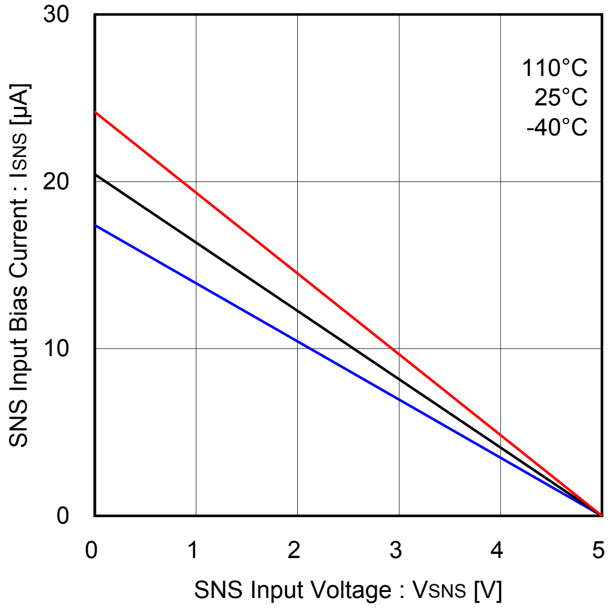


Figure 41. SNS Input Bias Current

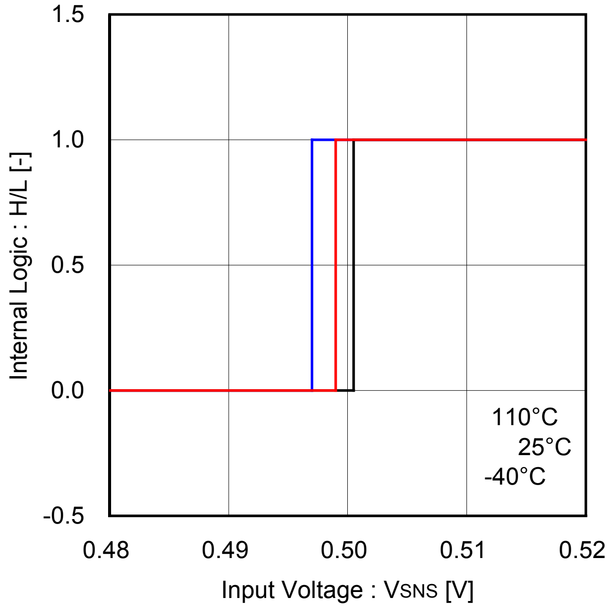


Figure 42. Current Limiter Input Threshold Voltage
(SNS)

Typical Performance Curves (Reference data) - Continued

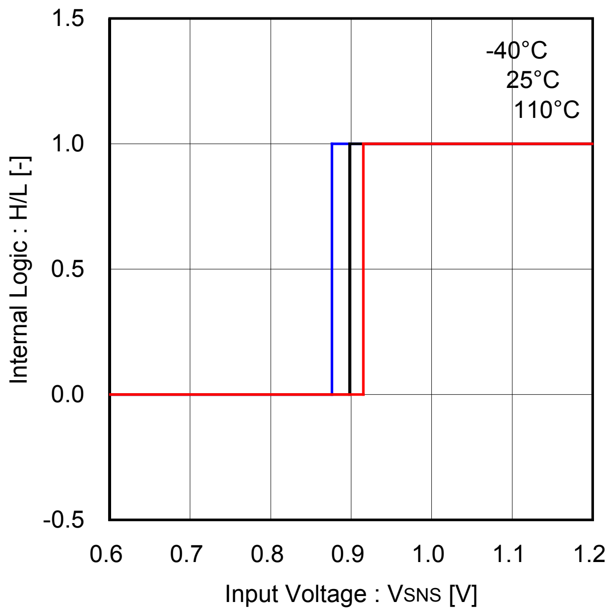


Figure 43. OCP Input Threshold Voltage (SNS)

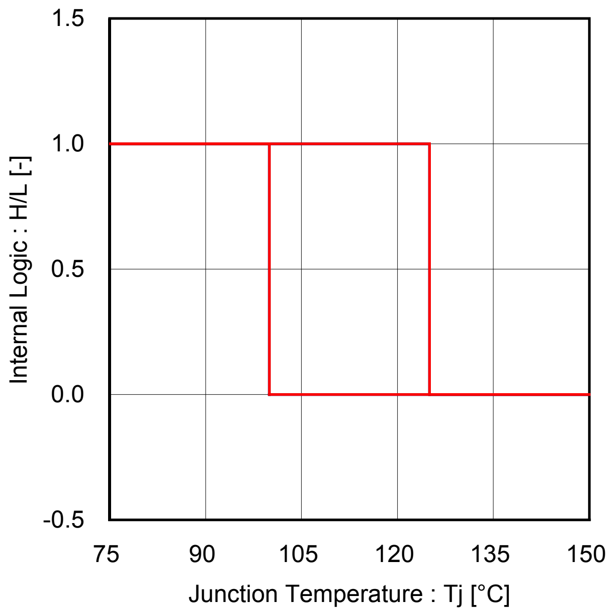


Figure 44. Thermal Shutdown

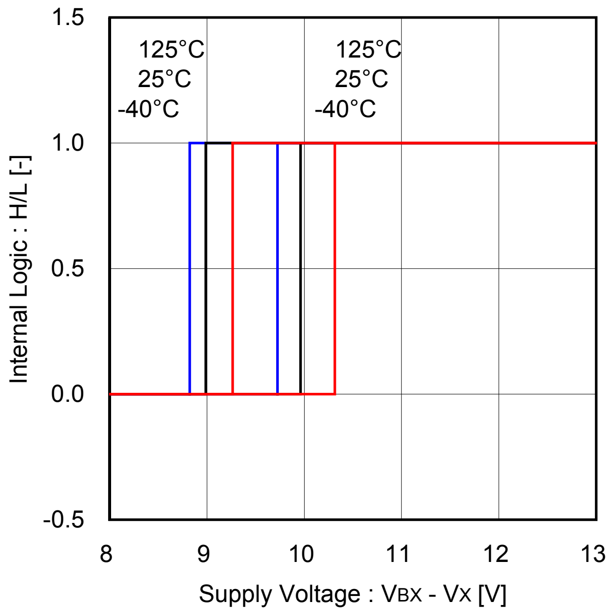


Figure 45. Under Voltage Lock Out (High Side Driver, Each Phase)

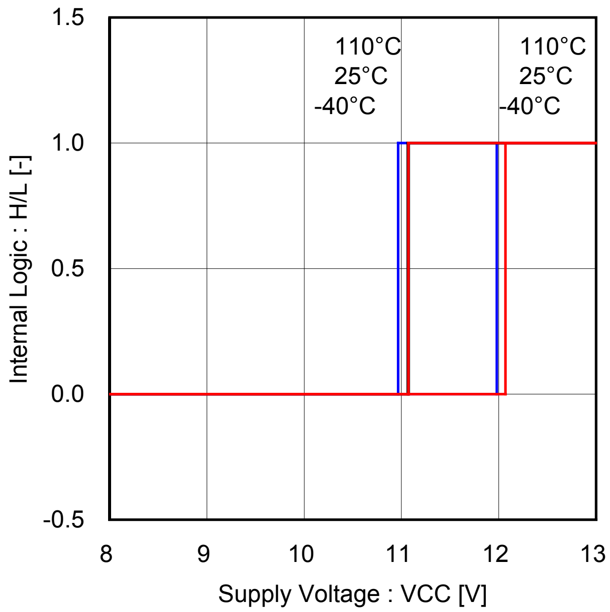


Figure 46. Under Voltage Lock Out (Low Side Drivers)

Application Example

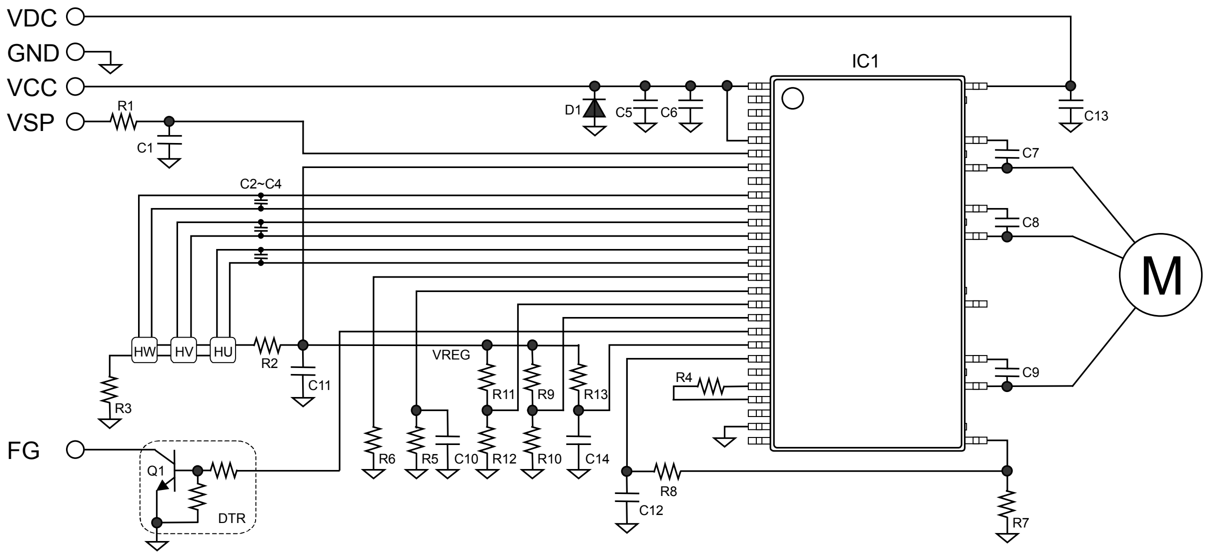


Figure 47. Application Example (150° Commutation Driver)

Parts List

Parts	Value	Manufacturer	Type	Parts	Value	Ratings	Type
IC1	-	ROHM	BM6206FS	C1	0.1µF	50V	Ceramic
R1	1kΩ	ROHM	MCR18EZPF1001	C2	2200pF	50V	Ceramic
R2	150Ω	ROHM	MCR18EZPJ151	C3	2200pF	50V	Ceramic
R3	150Ω	ROHM	MCR18EZPJ151	C4	2200pF	50V	Ceramic
R4	20kΩ	ROHM	MCR18EZPF2002	C5	10 µF	50V	Ceramic
R5	51kΩ	ROHM	MCR18EZPF5102	C6	10 µF	50V	Ceramic
R6	100kΩ	ROHM	MCR18EZPF1003	C7	2.2µF	50V	Ceramic
R7	0.6Ω	ROHM	MCR50JZHFL1R80 x 3	C8	2.2µF	50V	Ceramic
R8	10kΩ	ROHM	MCR18EZPF1002	C9	2.2µF	50V	Ceramic
R9	0Ω	ROHM	MCR18EZPJ000	C10	0.1µF	50V	Ceramic
R10	-	-	-	C11	2.2µF	50V	Ceramic
R11	0Ω	ROHM	MCR18EZPJ000	C12	100pF	50V	Ceramic
R12	-	-	-	C13	0.1µF	630V	Ceramic
R13	100kΩ	ROHM	MCR18EZPF1003	C14	0.1µF	50V	Ceramic
Q1	-	ROHM	DTC124EUA	HX	-	-	Hall elements
D1	-	ROHM	KDZ20B				

I/O Equivalence Circuits

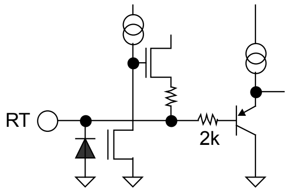


Figure 48. RT

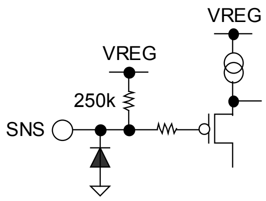


Figure 49. SNS

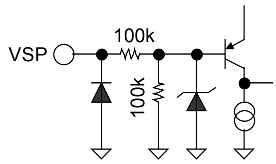


Figure 50. VSP

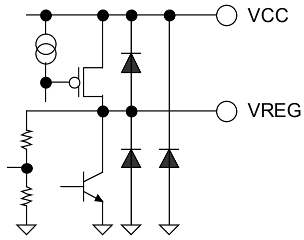


Figure 51. VREG, VCC

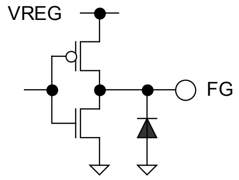


Figure 52. FG

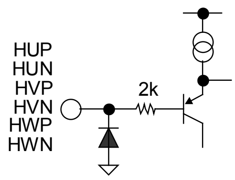


Figure 53. HXP, HXN

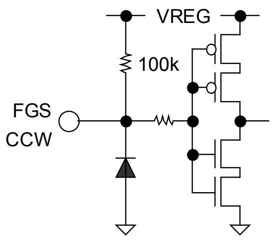


Figure 54. FGS, CCW

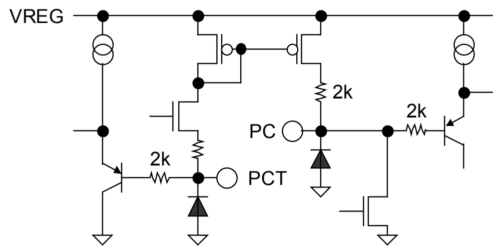


Figure 55. PC, PCT

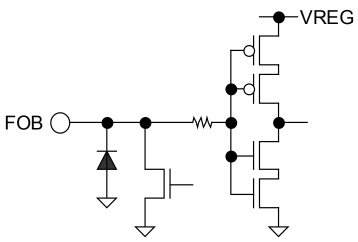


Figure 56. FOB

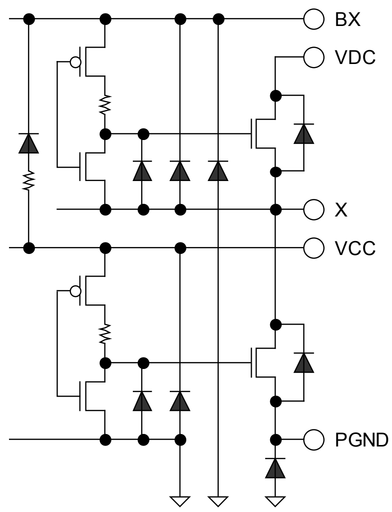


Figure 57. VCC, PGND, VDC, BX(BU/BV/BW), X(U/V/W)

Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

Do not force voltage to the input pins when the power does not supply to the IC. Also, do not force voltage to the input pins that exceed the supply voltage or in the guaranteed the absolute maximum rating value even if the power is supplied to the IC.

When using this IC, the high voltage pins VDC, BU/U, BV/V and BW/W need a resin coating between these pins. It is judged that the inter-pins distance is not enough. If any special mode in excess of absolute maximum ratings is to be implemented with this product or its application circuits, it is important to take physical safety measures, such as providing voltage-clamping diodes or fuses. And, set the output transistor so that it does not exceed absolute maximum ratings or ASO. In the event a large capacitor is connected between the output and ground, and if VCC and VDC are short-circuited with 0V or ground for any reason, the current charged in the capacitor flows into the output and may destroy the IC.

This IC contains the controller chip, P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

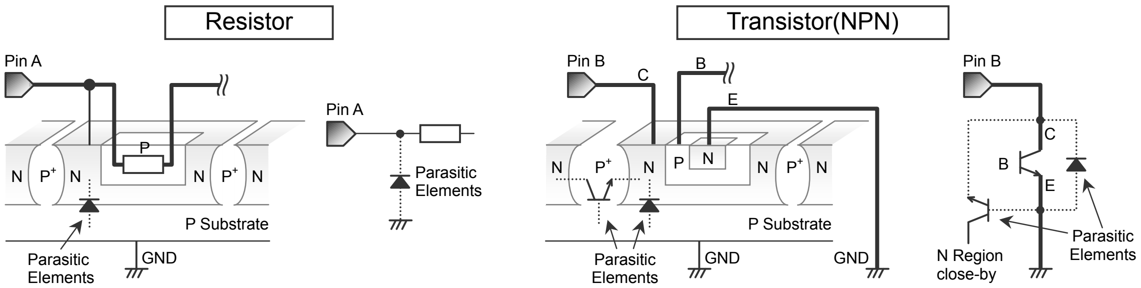


Figure A-1. Example of IC structure

13. Ceramic Capacitor

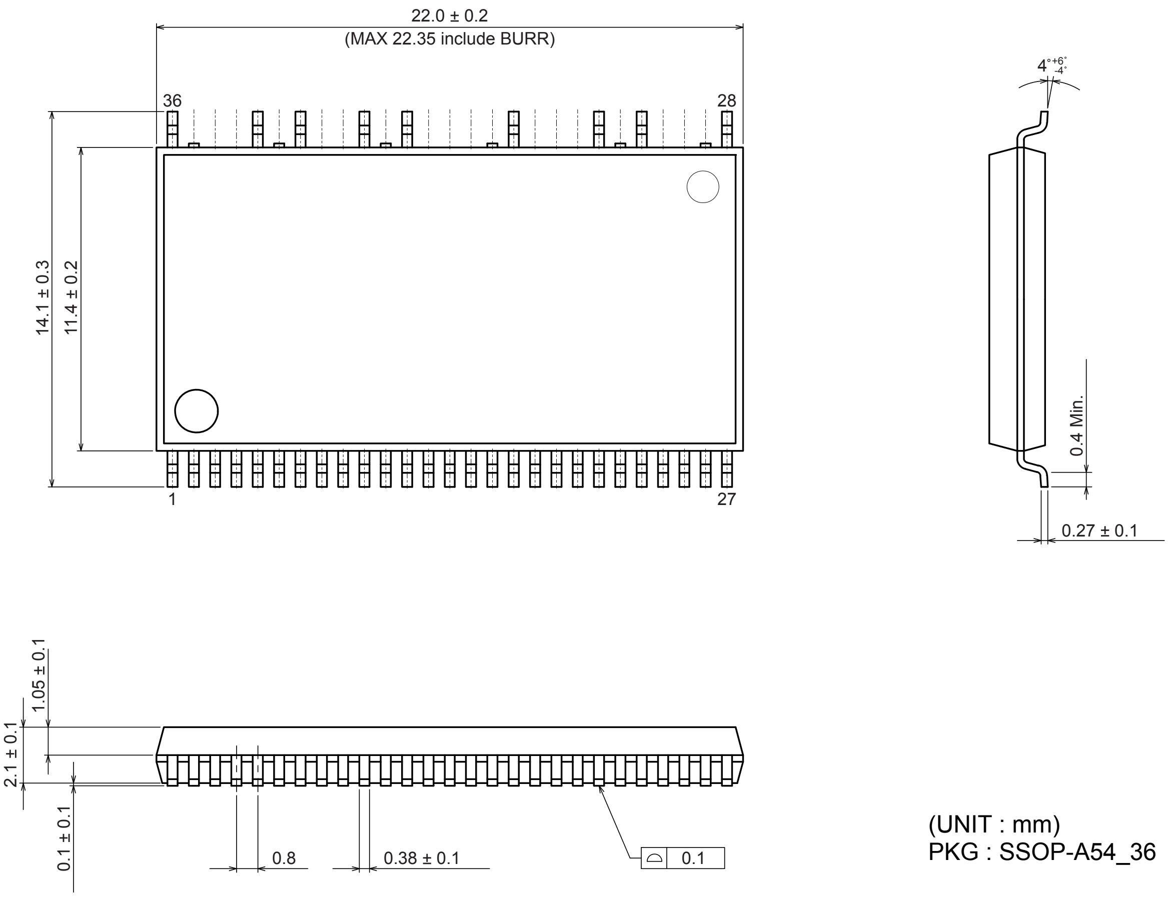
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

Physical Dimension, Tape and Reel Information

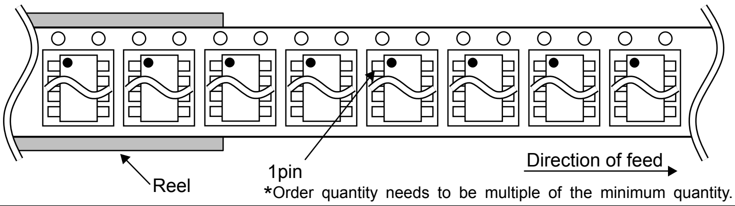
Package Name	SSOP-A54_36



(UNIT : mm)
PKG : SSOP-A54_36

<Tape and Reel Information>

Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.