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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Power supply IC series for TFT-LCD panels

12V Input Multi-Channel System Power Supply IC

BM81004MUV

General Description

BM81004MUV is a system power supply for TFT-LCD panels used for liquid crystal TVs. This IC is incorporated with Negative and Positive charge pump controller and Gate Pulse Modulation (GPM) function. It also features built-in EEPROM to contain each setting voltage, soft start time etc.

Features

- Step-up DC/DC converter (AVDD). (Synchronous rectification, Built-in load switch).
- Step-down DC/DC converter 1(VIO). (Non-synchronous rectification).
- Step-down DC/DC converter 2(VCORE).
- Step-down DC/DC converter 3(HAVDD). (Synchronous rectification).
- Positive charge pump controller (VGH).
- Negative charge pump controller (VGL).
- Gate Pulse Modulation (GPM) function.
- High Voltage LDO (50mA)
- 10 bit DAC-controlled Gamma Amplifier 4ch
- 8 bit DAC-controlled VCOM Amplifier
- Output voltage control by I2C.
- Built-in EEPROM.
- Switching Frequency 750kHz (AVDD, VIO).
- Switching Frequency 1MHz (VCORE, HAVDD).

Applications

- TFT-LCD panel

Key Specifications

- Input voltage range : 8.6V to 14.0V
- AVDD Output voltage range : 11.7V to 18.0V
- VIO Output voltage range : 2.2V to 3.7V
- HAVDD Output voltage range : 4.8V to 11.1V
- VGH Output voltage range : 25V to 40.5V
- VGL Output voltage range : -10.2V to -4.0V
- Switching Frequency : 750kHz(Typ) 1MHz(Typ)
- Operating temperature range : -40℃ to +105℃

Package

	W(Typ) x D(Typ) x H(Max)
VQFN48V7070A	7.00mm x 7.00mm x 1.0mm

Typical Application Circuit 1 （TOP VIEW）

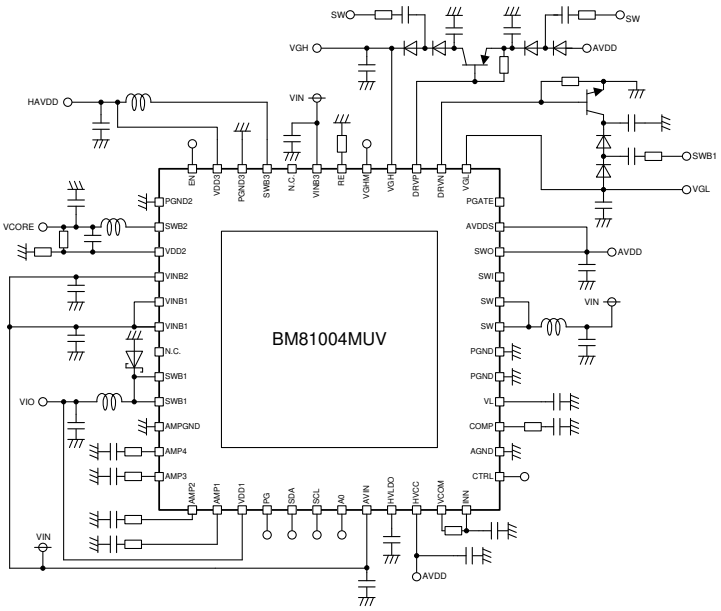

Figure 1. Application Circuit 1

○Product structure : Silicon monolithic chip ○This chip is not designed for protection against ratio active rays.

Typical Application Circuit 2
（TOP VIEW）

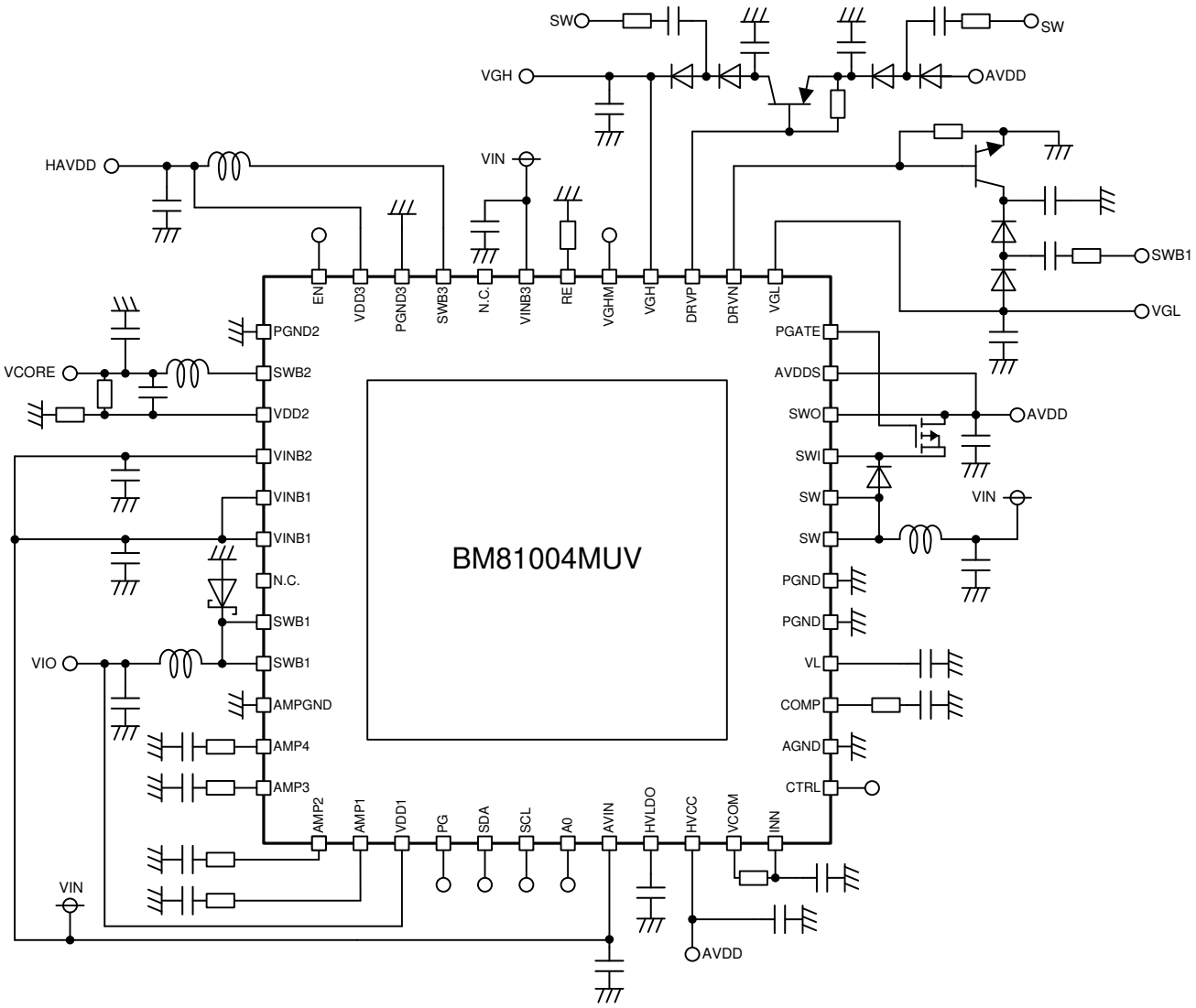

Figure 2. Application Circuit 2

Contents

Pin Configuration
(TOP VIEW)

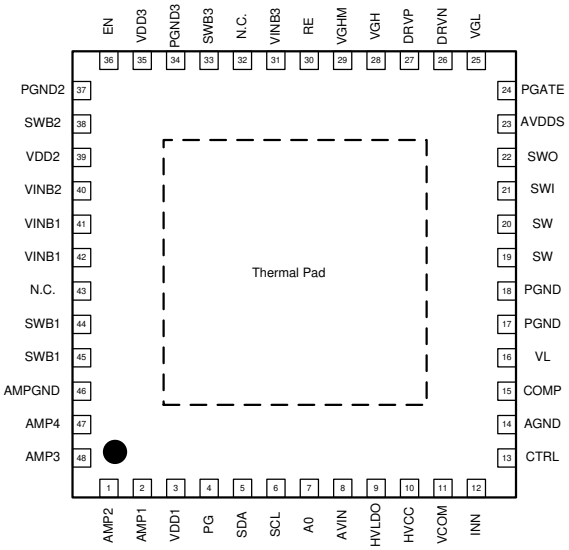

Figure 3. Pin Configuration

Pin Description

PIN No.	SYMBOL	FUNCTION	PIN No.	SYMBOL	FUNCTION
1	AMP2	Gamma amplifier output pin 2	25	VGL	Negative charge pump output pin
2	AMP1	Gamma amplifier output pin 1	26	DRVN	Negative charge pump drive pin
3	VDD1	Step-down DC/DC output pin 1	27	DRVP	Positive charge pump drive pin
4	PG	Power GOOD signal output pin	28	VGH	Positive charge pump output pin
5	SDA	Serial data input pin	29	VGHM	GPM output pin
6	SCL	Serial clock input pin	30	RE	GPM Slope adjustment pin
7	A0	I2C address selected pin	31	VINB3	Power supply pin for Step-down DC/DC 3
8	AVIN	Power supply input pin	32	N.C.	—
9	HVLDO	High Voltage LDO output pin	33	SWB3	Step-down DC/DC switching pin 3
10	HVCC	VCOM and Gamma power supply pin	34	PGND3	Step-down DC/DC GND pin 3
11	VCOM	VCOM amplifier output pin	35	VDD3	Step-down DC/DC output pin 3
12	INN	VCOM amplifier feedback pin	36	EN	Enable pin
13	CTRL	GPM control pin	37	PGND2	Step-down DC/DC GND pin 2
14	AGND	Analog GND pin	38	SWB2	Step-down DC/DC switching pin 2
15	COMP	Error amplifier output pin	39	VDD2	Step-down DC/DC output pin 2
16	VL	Internal REG output pin	40	VINB2	Power supply pin for Step-down DC/DC 2
17	PGND	Step-up DC/DC GND pin	41	VINB1	Power supply pin for Step-down DC/DC 1
18	PGND	Step-up DC/DC GND pin	42	VINB1	Power supply pin for Step-down DC/DC 1
19	SW	Step-up DC/DC switching pin	43	N.C.	—
20	SW	Step-up DC/DC switching pin	44	SWB1	Step-down DC/DC switching pin 1
21	SWI	Load switch input pin	45	SWB1	Step-down DC/DC switching pin 1
22	SWO	Load switch output pin	46	AMPGND	Gamma amplifier GND pin
23	AVDDS	Step-up DC/DC feedback pin	47	AMP4	Gamma amplifier output pin 4
24	PGATE	Load switch gate drive pin	48	AMP3	Gamma amplifier output pin 3

Block Diagram

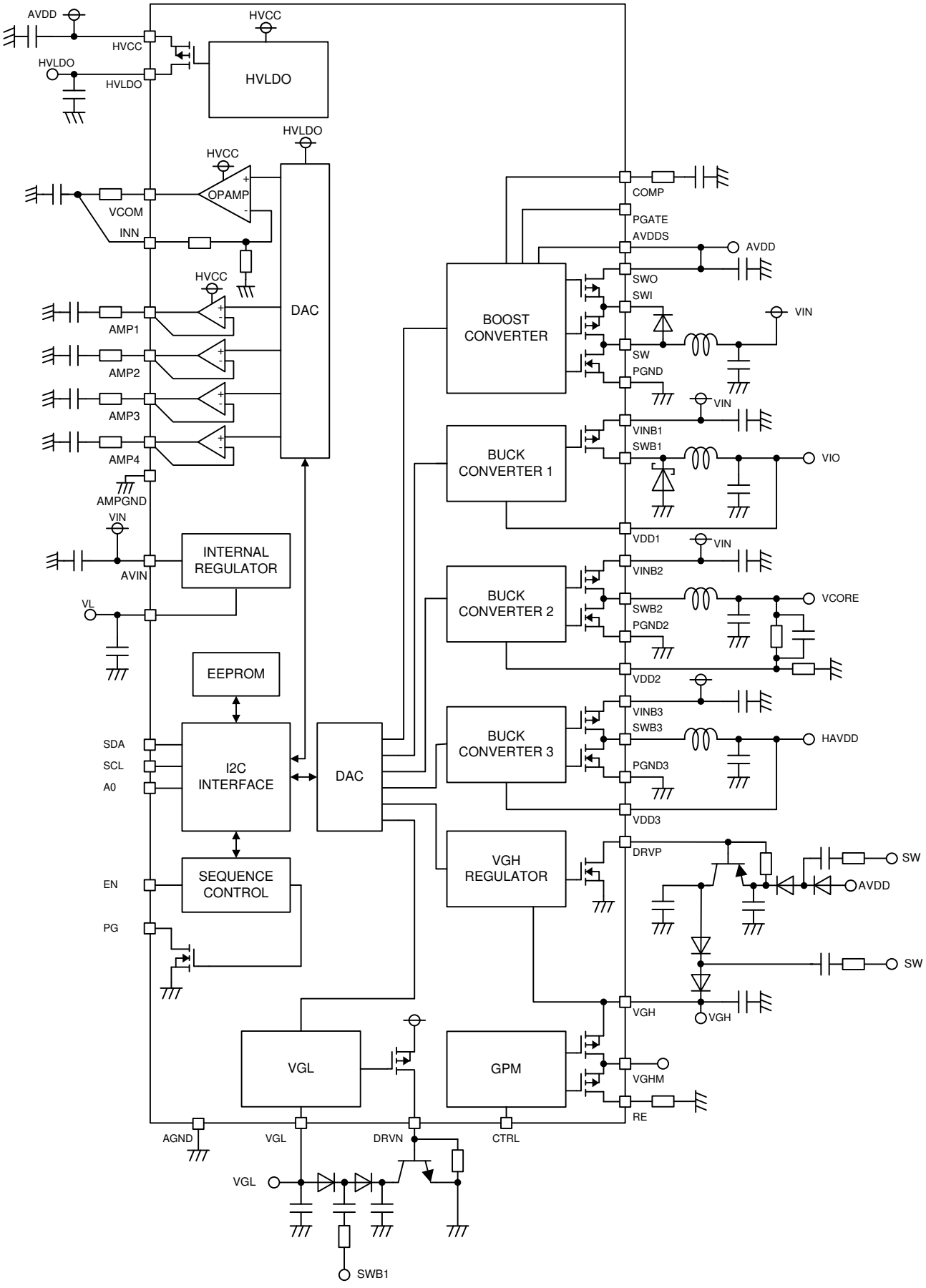

Figure 4. Block Diagram

Description of each Block

① BUCK CONVERTER BLOCK 2
This block generates VCORE (VDD2) voltage from Power supply voltage.
After releasing UVLO of VIN, VL starts activating. After Auto Read is operated to EEPROM, VCORE will be activated.
During operations, it is possible to prevent destruction of IC by OVP, UVP and OCP protection function.

② BUCK CONVERTER BLOCK 1
This block generates VIO (VDD1) voltage from Power supply voltage of VIO.
After completing VCORE start-up, VIO starts activating.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by OVP, UVP and OCP protection function.

③ VGL REGULATOR BLOCK
This block generates VGL voltage.
After completing VCORE start-up, VGL starts activating.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by UVP and OCP protection function.

④ BOOST CONVERTER BLOCK
This block generates AVDD (SWO) voltage from Power supply voltage.
It activates when EN=H, and under condition where VIO and VGL are activating.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by OVP, UVP and OCP protection function.

⑤ BUCK CONVERTER BLOCK 3
This block generates HAVDD (VDD3) voltage from Power supply voltage.
HAVDD starts up following AVDD output voltage.
The setting voltage range of the HAVDD voltage depends on the AVDD setting voltage, and the lower limit level of the HAVDD voltage is limited in AVDD × 0.4.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by OVP, UVP and OCP protection function.

⑥ HIGH VOLTAGE LDO BLOCK
This block generates HVLDO voltage from Power supply voltage of AVDD (HVCC).
HVLDO starts up following AVDD output voltage.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by UVP and OCP protection function.

⑦ VCOM AMPLIFIER BLOCK
This block generates VCOM voltage from Power supply voltage of AVDD (HVCC). VCOM calibrator function is built-in.
VCOM starts up following AVDD output voltage.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.

⑧ GAMMA AMPLIFIER BLOCK
This block generates AMP1 to 4 voltages from Power supply voltage of AVDD (HVCC).
AMP1 to 4 startup following AVDD output voltage.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.

⑨ VGH REGULATOR BLOCK
This block generates VGH voltage from AVDD voltage.
After completing AVDD start-up, VGH starts activating.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by OVP, UVP and OCP protection function.

⑩ GPM BLOCK
This is a switching circuit to drive a gate voltage for TFT that consist of PMOS FET.
VGHM output synchronizes with CTRL input and outputs High voltage = VGH at CTRL=H.
GPM Falling Limit voltage can be controlled by EEPROM.

※ Caution
・EN Input tolerant function is built in this IC. No need to be always EN < VIN.
・When PG pin is not used, PG pin must be connected to GND, or it should be open.

Absolute Maximum Ratings

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Supply Voltage	AVIN, VINB1, VINB2, VINB3	-0.3	-	24	V
	HVCC	-0.3	-	20	V
Input Voltage	SDA, SCL, A0, EN, CTRL	-0.3	-	7	V
Output Voltage	VL	-0.3	-	6.5	V
	COMP, PG	-0.3	-	7	V
	SW, SWI, SWO, PGATE, AVDDS, VDD1, SWB1, VDD2, SWB2, VDD3, SWB3	-0.3	-	24	V
	HVLDO, VCOM, INN AMP1, AMP2, AMP3, AMP4	-0.3	-	20	V
	VGL, DRVN	-15	-	7	V
	DRVP, VGH, VGHM, RE	-0.3	-	48	V
Operating Ambient Temperature Range	Ta	-40	-	105	℃
Storage Temperature Range	Tstg	-55	-	150	℃
Maximum Continuous Junction Temperature	Tjmax (*1)	-	-	150	℃
Power Dissipation (*2)	Pd	5.08			W
	Θja	24.6			degC/W

*1 It shows junction temperature when stores.
*2 Derate by 40.6mW/℃ at Ta>25℃(on 4-layer 76.2mm × 114.3mm × 1.6mm glass epoxy board).

Recommended Operating Ranges
(Ta=-40℃～105℃)

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Supply Voltage	AVIN	8.6	-	14	V
Functional pin voltage	EN, A0, CTRL	-0.1	-	5.5	V
2 wire serial pin voltage	SDA, SCL	-0.1	-	5.5	V
2 wire serial frequency	FCLK	-	-	400	kHz

Electrical Characteristics

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 GENERAL 】						
VIN Under Voltage Lockout Threshold	VIN_ UVLO	8.0	8.3	8.6	V	VIN rising
		7.25	7.55	7.85	V	VIN falling
Thermal shutdown	TSD	155	175	195	℃	Design guarantee
Internal Oscillator Frequency 1	FOSC1	600	750	900	kHz	AVDD, VIO, 0 < Ta < 50℃
Internal Oscillator Frequency 2	FOSC2	800	1000	1200	kHz	VCORE, HAVDD, 0 < Ta < 50℃
VL Voltage	VL	4.9	5	5.1	V	
Consumption Current	ICC	-	5.4	-	mA	Not Switching
【 LOGIC SIGNALS SDA, SCL, EN, A0, CTRL 】						
High Level Input Voltage	VIH	2	-	-	V	
Low Level Input Voltage	VIL	-	-	0.5	V	
Minimum Output Voltage	VSDA	-	-	0.4	V	SDA, ISDA=3mA
Pull-Down Resistance	RLOGIC	140	200	260	kΩ	EN, A0, CTRL
【 BOOST CONVERTER (AVDD) 】						
Output Voltage Range	AVDD	11.7	-	18.0	V	0.1V step
Regulation Voltage	AVDD_R	15.444	15.6	15.756	V	27h, 1%, 0 < Ta < 50℃
Hi-Side Leakage Current	ILK_SWH	-	0	10	uA	SWI=18V, SW=0V
Hi-Side SW ON-Resistance	RON_SWH	-	100	200	mΩ	ISW=-500mA
Lo-Side SW Leakage Current	ILK_SWL	-	0	10	uA	SW=18V
Lo-Side SW ON-Resistance	RON_SWL	-	100	200	mΩ	ISW=500mA
Load SW ON-Resistance	RON_LS	-	100	200	mΩ	ILS=500mA
SW Current Limit	ILIM_SW	4.25	5	5.75	A	5.0A – Offset(0.0A) setting L=6.8uH, 0 < Ta < 50℃
SW Current Limit Offset	ILIM_SET	0	-	2.8	A	0.4A step
Over-Voltage Protection Rise	VOVP_AVD D_RISE	18	19.5	21	V	
Over-Voltage Protection Fall	VOVP_AVD D_FALL	-	18	-	V	
AVDD UVP Detecting Voltage	VUVP_ AVDD	-	AVDD x 0.8	-	V	
Soft Start Time	TSS_ AVDD	10	-	20	msec	
Load Switch Current Limit	ILIM_LSW	-	7	-	A	
External Load Switch Current Limit	ILIM_EXT	450	540	630	mV	
PGATE Drive Capability	PGATE_ DRV	-	10	-	uA	

Electrical Characteristics

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 BUCK CONVERTER 1 (VIO) 】						
Output Voltage Range	VIO	2.2	-	3.7	V	0.1V step
Regulation Voltage	VIO_R	3.234	3.3	3.366	V	0Bh, 2%, 0 < Ta < 50℃
Hi-Side SWB1 Leak Current	ILK_ SWB1H	-	0	10	uA	VINB1=18V, SWB1=0V
Hi-Side SWB1 ON-Resistance	RON_ SWB1H	-	200	300	mΩ	SWB1=-500mA
SWB1 Current Limit	ILIM_ SWB1	2.8	3.5	4.2	A	L=6.8uH, 0 < Ta < 50℃
VIO Over-Voltage Protection	VOVP_ VIO	VIO x 1.03	VIO x 1.1	VIO x 1.17	V	
VIO UVP Detecting Voltage	VUVP_ VIO	-	VIO x 0.8	-	V	Frequency 1/4
Soft Start Time	TSS_VIO	-	3.3	-	msec	VIO=3.3V
【 BUCK CONVERTER 2 (VCORE) 】						
VCORE Reference Voltage	VCORE_ REF	0.396	0.400	0.404	V	1%, Ta=25℃
		0.394	0.400	0.406	V	1.5%, 0 < Ta < 50℃
Hi-Side SWB2 Leak Current	ILK_ SWB2H	-	0	10	uA	VINB2=18V, SWB2=0V
Hi-Side SWB2 ON-Resistance	RON_ SWB2H	-	175	300	mΩ	SWB2=-500mA
Lo-Side SWB2 Leak Current	ILK_ SWB2L	-	0	10	uA	SWB2=18V
Lo-Side SWB2 ON-Resistance	RON_ SWB2L	-	175	300	mΩ	SWB2=500mA
SWB2 Current Limit	ILIM_ SWB2	2.4	3.0	3.6	A	L=6.8uH, 0 < Ta < 50℃
VCORE Over-Voltage Protection	VOVP_ VCORE	VCORE x 1.03	VCORE x 1.1	VCORE x 1.17	V	
VCORE UVP Detecting Voltage	VUVP_ VCORE	-	VCORE x 0.8	-	V	Frequency 1/4
Soft Start Time	TSS_ VCORE	-	3	-	msec	
【 BUCK CONVERTER 3 (HAVDD) 】						
Output Voltage Range	HAVDD	4.8	-	11.1	V	0.1V step
Regulation Voltage	HAVDD_R	7.68	7.8	7.92	V	1Eh, 1.5%, 0 < Ta < 50℃
Hi-Side SWB3 Leak Current	ILK_ SWB3H	-	0	10	uA	VINB3=18V, SWB3=0V
Hi-Side SWB3 ON-Resistance	RON_ SWB3H	-	300	500	mΩ	SWB3=-500mA
Lo-Side SWB3 Leak Current	ILK_ SWB3L	-	0	10	uA	SWB3=18V
Lo-Side SWB3 ON-Resistance	RON_ SWB3L	-	300	500	mΩ	SWB3=500mA
SWB3 Current Limit	ILIM_ SWB3	1.2	1.8	2.4	A	L=6.8uH, 0 < Ta < 50℃
HAVDD Over-Voltage Protection	VOVP_ HAVDD	HAVDD x 1.03	HAVDD x 1.1	HAVDD x 1.17	V	
HAVDD UVP Detecting Voltage	VUVP_ HAVDD	-	HAVDD x 0.8	-	V	Frequency 1/4

Electrical Characteristics

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 VGH REGULATOR 】						
Output Voltage Range	VGH	25	-	40.5	V	0.5V step
Regulation Voltage	VGH_R	34.47	35	35.53	V	14h, 1.5%, 0 < Ta < 50℃ Io=5mA
Over-Current Protection	ILIM_ DRVP	5	-	-	mA	
VGH Over-Voltage Protection	VOVP_ VGH	42	45	48	V	
VGH UVP Detecting Voltage	VUVP_ VGH	-	VGH x 0.8	-	V	
Soft Start Time	TSS_VGH	-	7	-	msec	VGH=35V
【 VGL REGULATOR 】						
Output Voltage Range	VGL	-10.2	-	-4.0	V	0.2V step
Regulation Voltage	VGL_R	-6.09	-6	-5.91	V	0Ah, 1.5%, Ta=25℃ Io=5mA
		-6.12	-6	-5.88	V	0Ah, 2.0%, 0 < Ta < 50℃ Io=5mA
Over-Current Protection	ILIM_ DRVN	5	-	-	mA	
VGL UVP Detecting Voltage	VUVP_ VGL	-	VGL×0.8	-	V	
Delay Time	TDLY_VGL	-	2.5	-	msec	
【 GATE PULSE MODULATION (GPM) 】						
VGH-VGHM ON-Resistance	RGHH	-	3	5	Ω	
RE-VGHM ON-Resistance	RGHL	-	3	-	Ω	
Propagation Delay	TGPM	150	250	350	nsec	

Electrical Characteristics

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 HIGH VOLTAGE LDO 】						
Output Voltage Range	LDO	11.7	—	18.0	V	0.1V step
Regulation Voltage	LDO_R	15.12	15.2	15.28	V	23h, 0.5%
	LDO_R	15.09	15.2	15.31	V	23h, 0.7%, 0 < Ta < 50℃
Over-Current Protection	ILIM_ LDO	-	100	-	mA	
HVLDO UVP Detecting Voltage	LDO_UVP	-	LDOx0.8	-	V	
【 VCOM AMPLIFIER 】						
Output Voltage Range	VCOM_R	HVLDO X0.36	—	HVLDO X0.54	V	
Slew Rate	SR	-	30	-	V/usec	No external components
Output Current Capability	I_VCOM	-	±200	-	mA	C2h
Load Stability	ΔVO1	-	±15	-	mV	Io=-50mA～50mA
DAC Resolution	RES1		8		Bit	
DAC Integral Non-linearity Error (INL)	LE1	-1	-	+1	LSB	02～FD is the allowable margin of error against the ideal linear.
DAC Differential Non-linearity Error (DNL)	DLE1	-1	-	+1	LSB	02～FD is the allowable margin of error against the ideal increase of 1LSB.
【 GAMMA AMPLIFIER 】						
Output Current Capability	I_AMP	30	-	-	mA	
Load Stability	ΔVO2	-	±15	-	mV	Io=-5mA～5mA
DAC Resolution	RES2		10		Bit	
DAC Integral Non-linearity Error (INL)	LE2	-2	-	+2	LSB	00F ～ 3F0 is the allowable margin of error against the ideal linear.
DAC Differential Non-linearity Error (DNL)	DLE2	-2	-	+2	LSB	00F ～ 3F0 is the allowable margin of error against the ideal increase of 1LSB.

○This product has no designed for protection against radioactive rays.

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

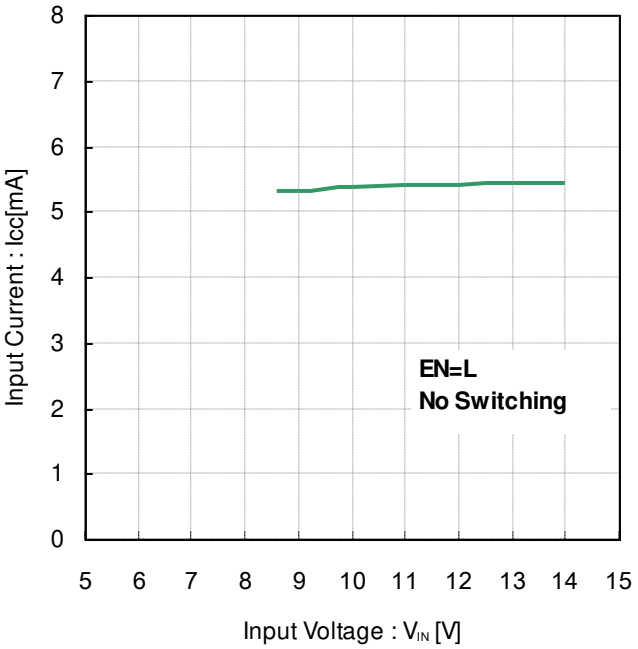

Figure 5. Input Current vs Input Voltage (EN=L, no switching)

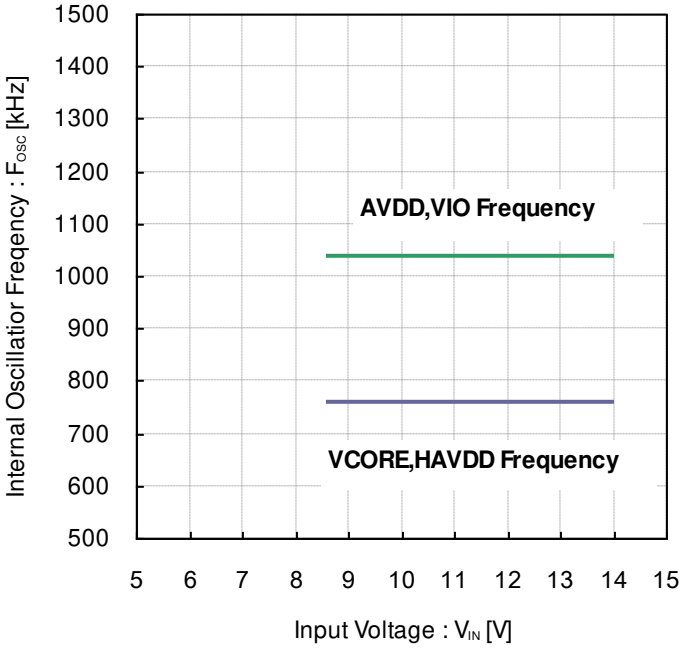

Figure 6. Internal Oscillator Frequency vs Input Voltage

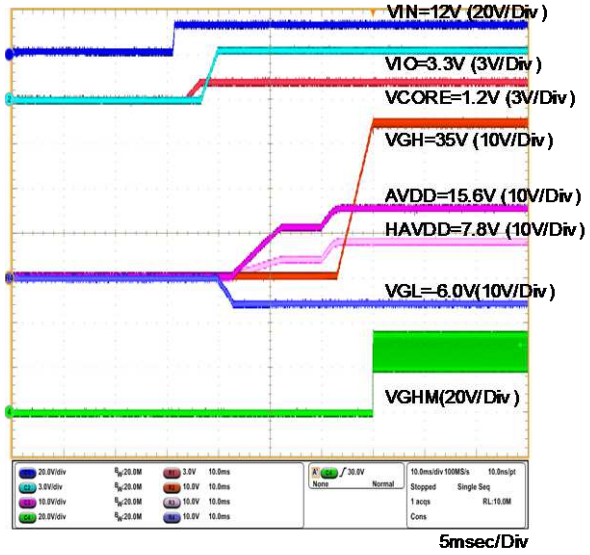

Figure 7. Power-on (till AVDD and VGH on)

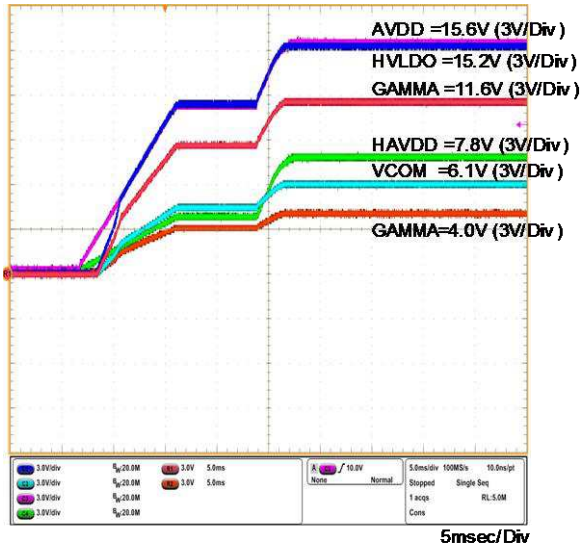

Figure 8. Power-on (after AVDD on)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

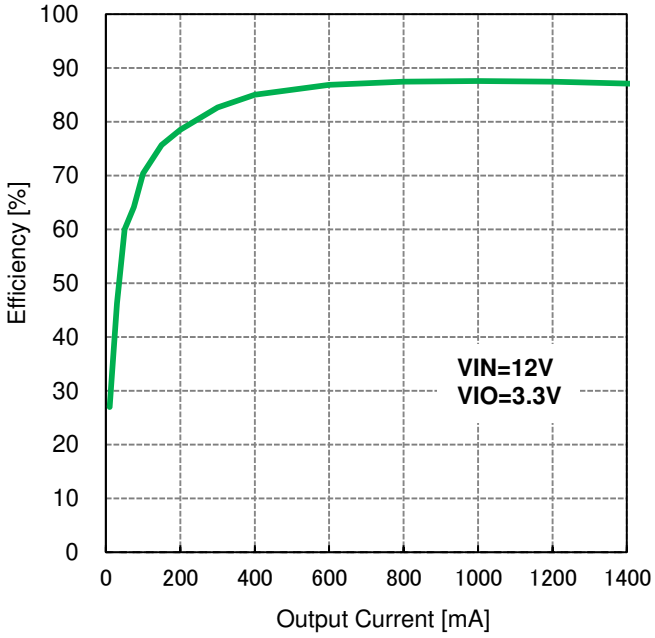

Figure 9. VIO Efficiency vs Output Current

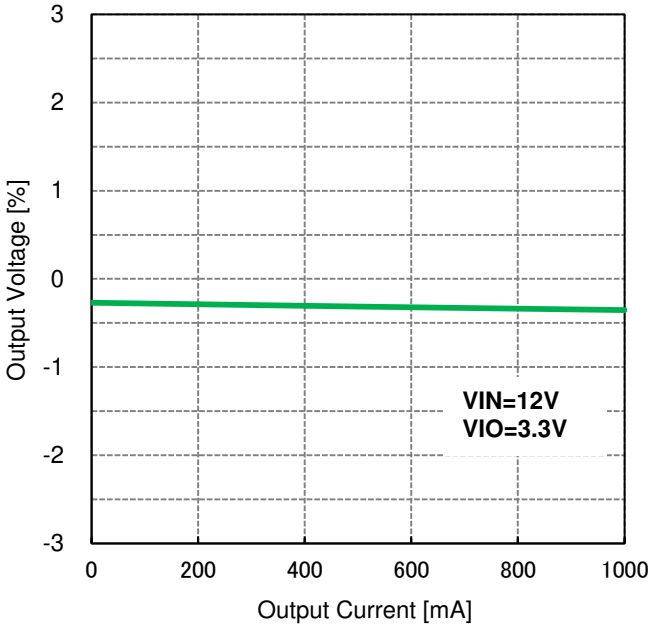

Figure 10. VIO Output Voltage vs Output Current

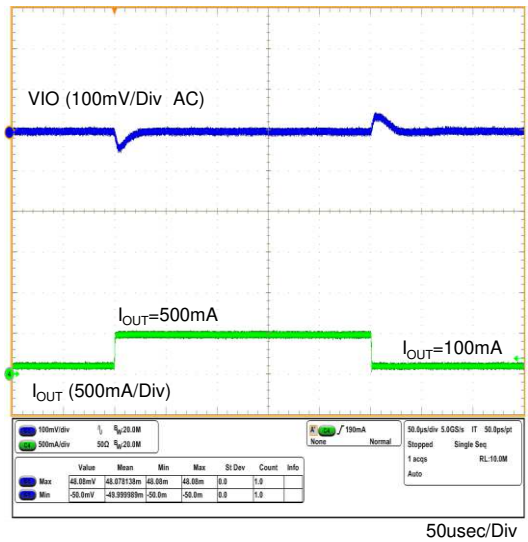

Figure 11. VIO Load Transient

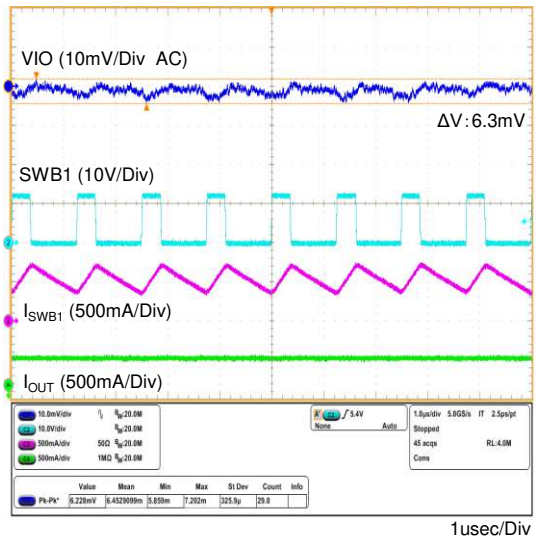

Figure 12. VIO Switching
(Output Current=500mA)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

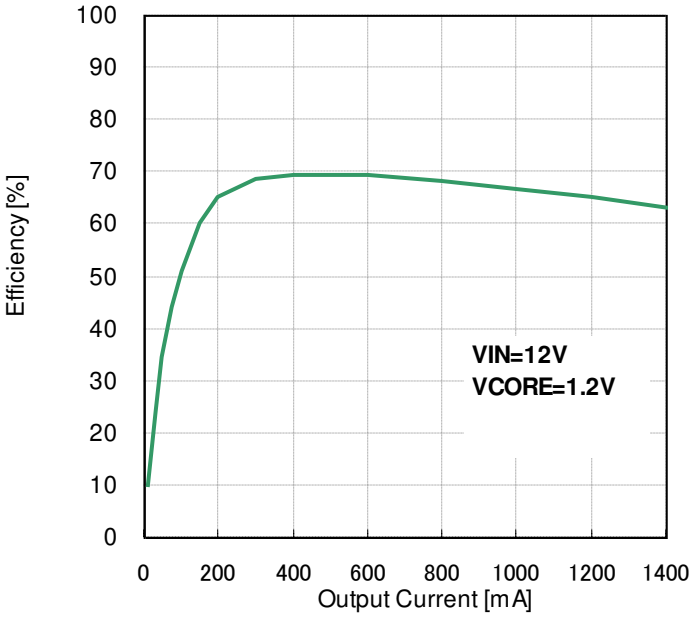

Figure 13. VCORE Efficiency vs Output Current

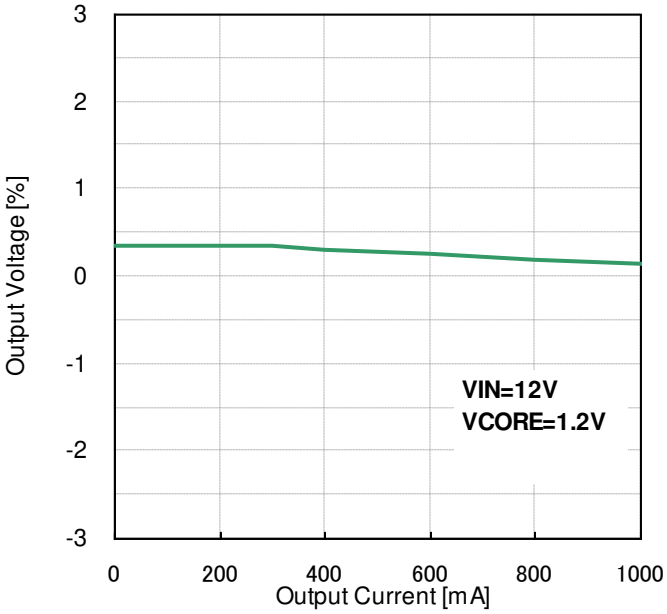

Figure 14. VCORE Output Voltage vs Output Current

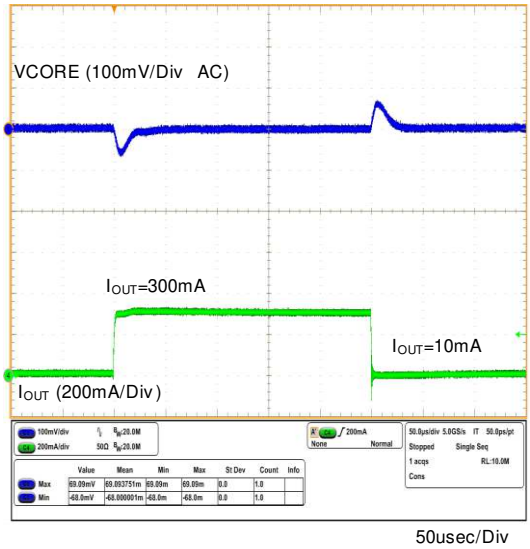

Figure 15. VCORE Load Transient

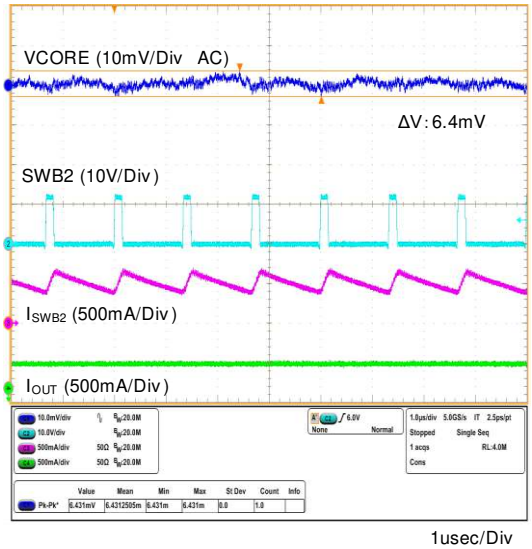

Figure 16. VCORE Switching (Output Current=500mA)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

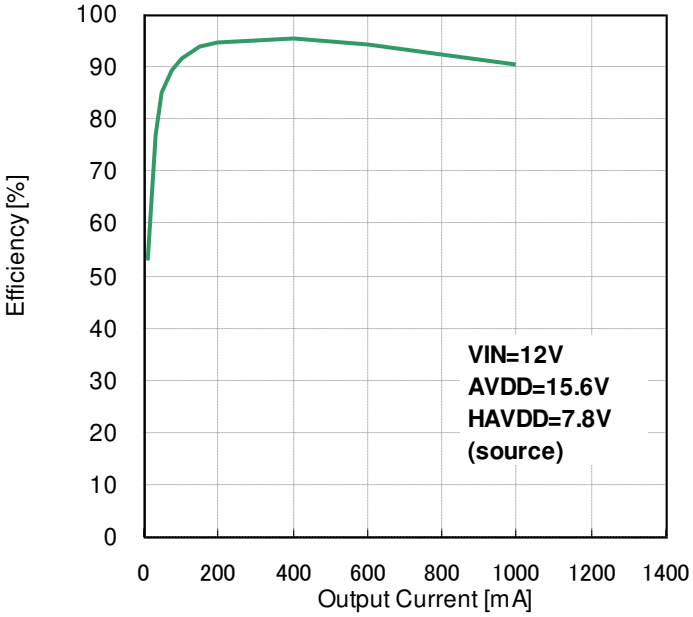

Figure 17. HAVDD Efficiency vs Output Current (source)

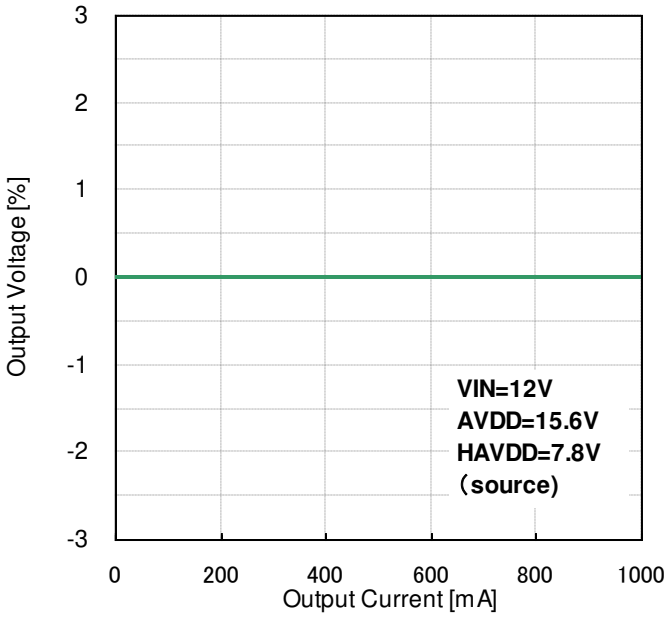

Figure 18. HAVDD Output Voltage vs Output Current (source)

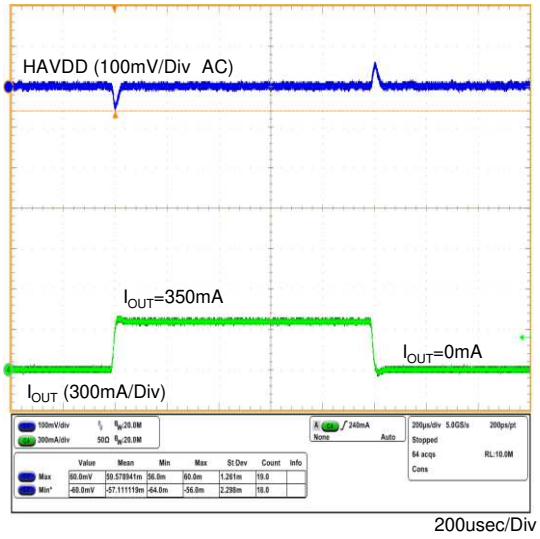

Figure 19. HAVDD Load Transient (source)

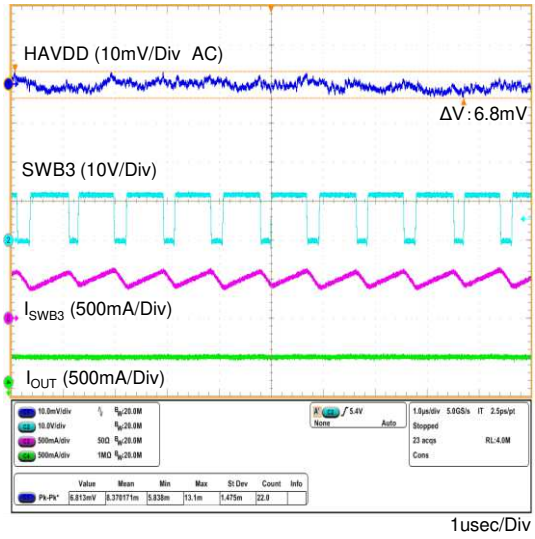

Figure 20. HAVDD Switching (source)
(Output Current=500mA)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

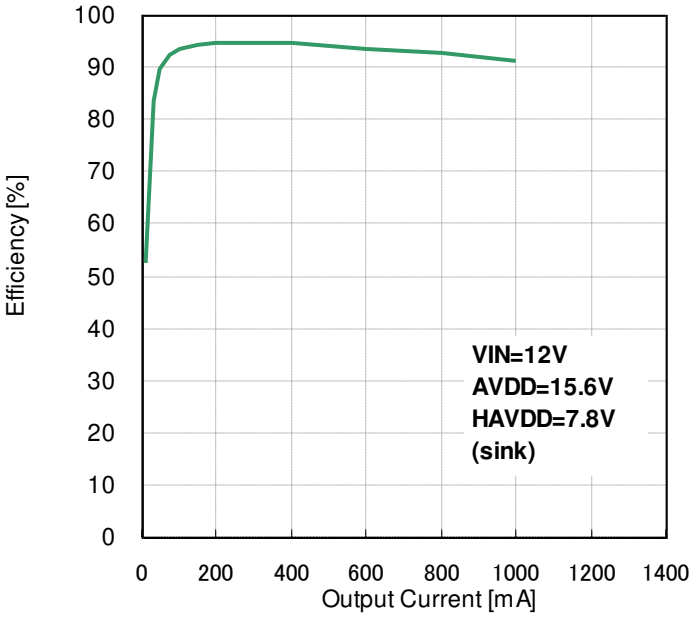

Figure 21. HAVDD Efficiency vs Output Current (sink)

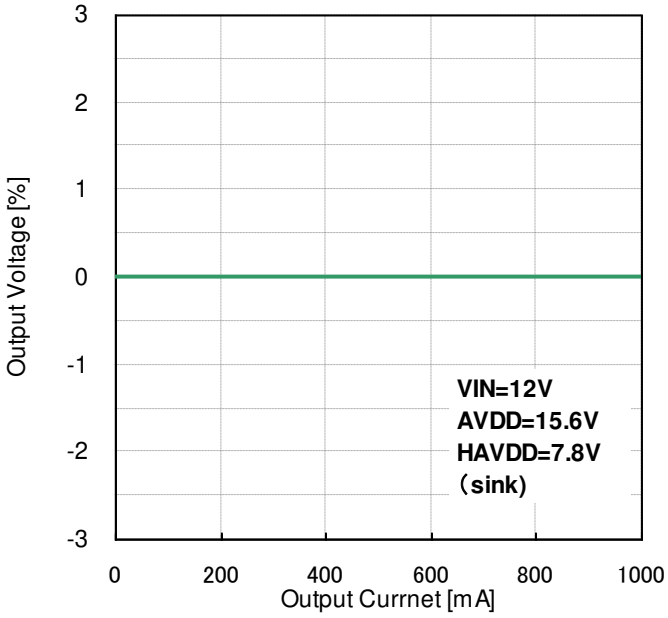

Figure 22. HAVDD Output Voltage vs Output Current (sink)

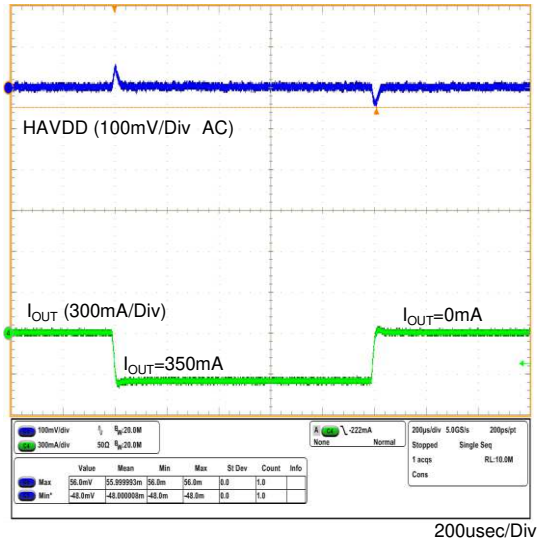

Figure 23. HAVDD Load Transient (sink)

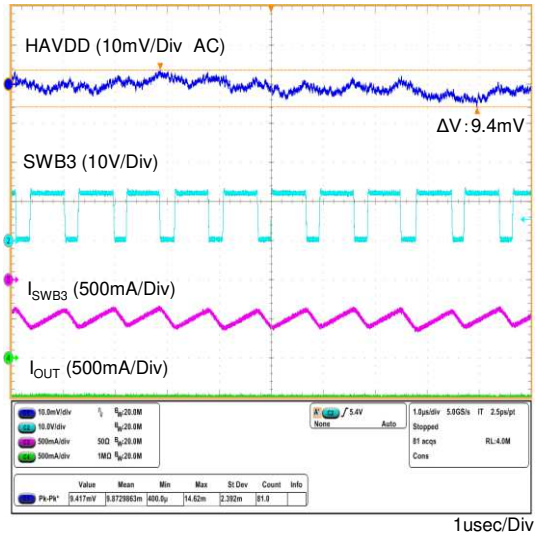

Figure 24. HAVDD Switching (sink)
(Output Current=500mA)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

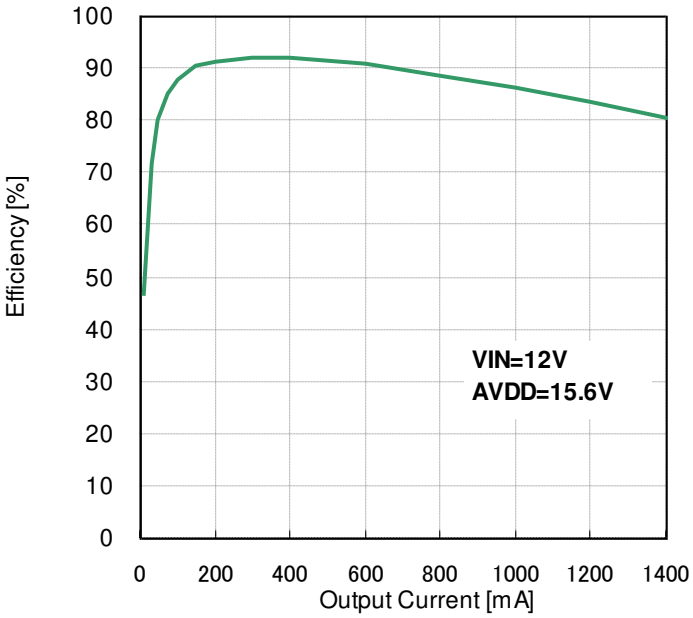

Figure 25. AVDD Efficiency vs Output Current

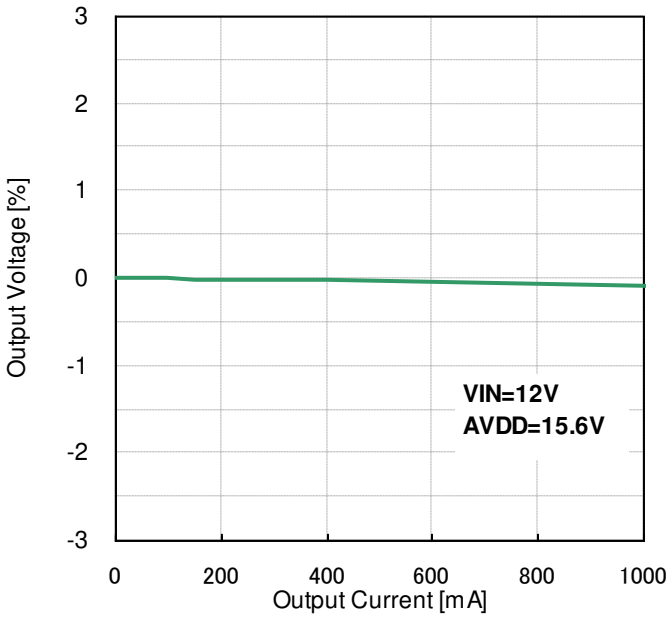

Figure 26. AVDD Output Voltage vs Output Current

Figure 27. AVDD Load Transient

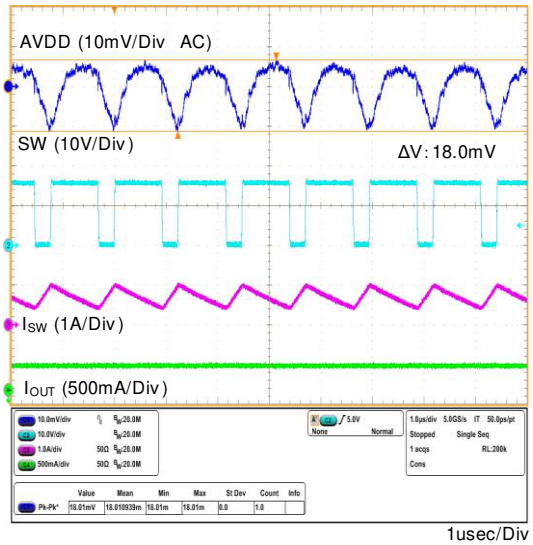

Figure 28. AVDD Switching (Output Current=500mA)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

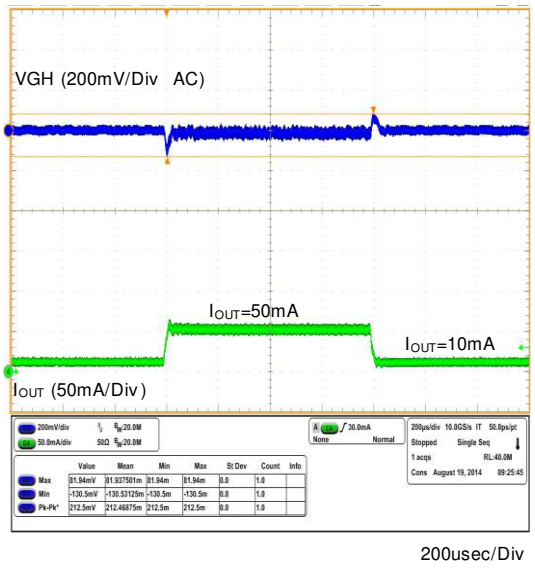

Figure 29. VGH Load Transient

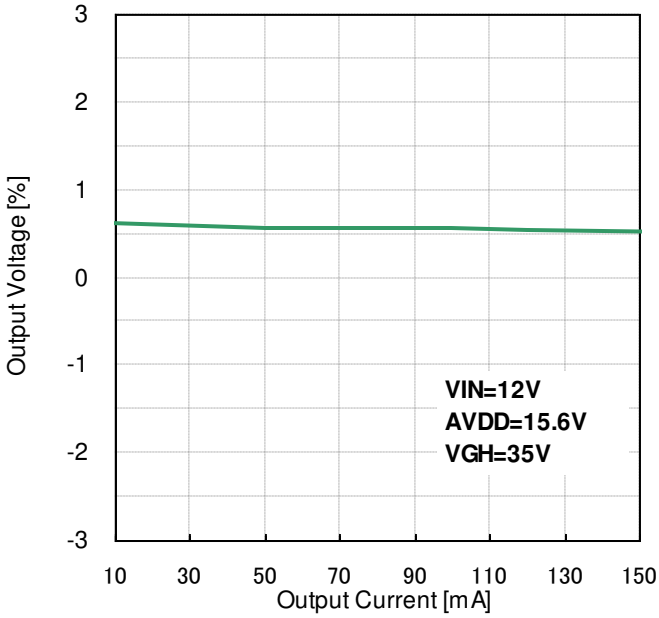

Figure 30. VGH Output Voltage vs Output Current

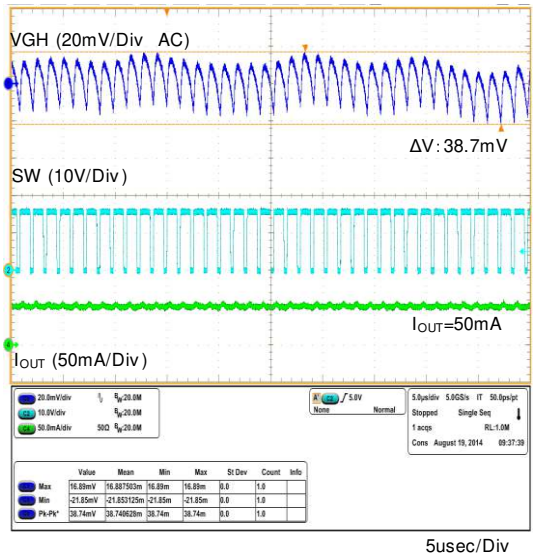

Figure 31. VGH Ripple Voltage

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

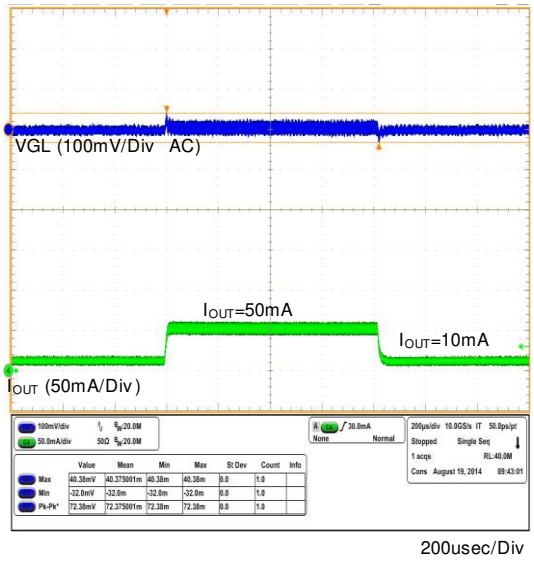

Figure 32. VGL Load Transient

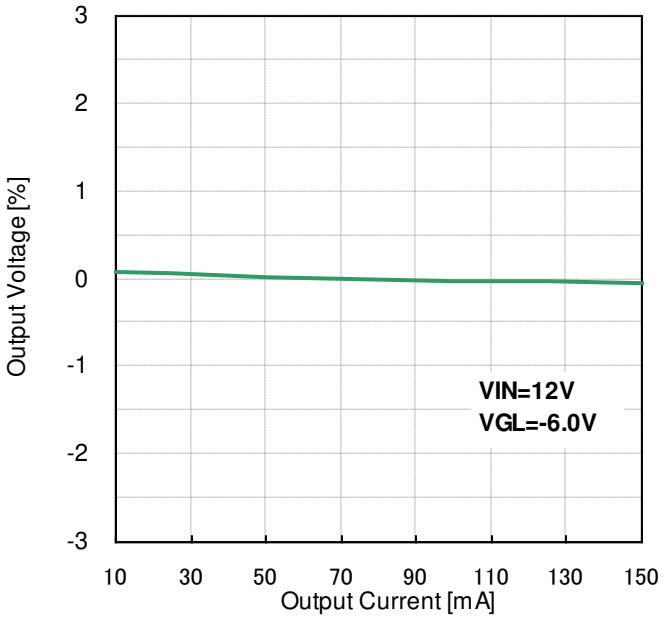

Figure 33. VGL Output Voltage vs Output Current

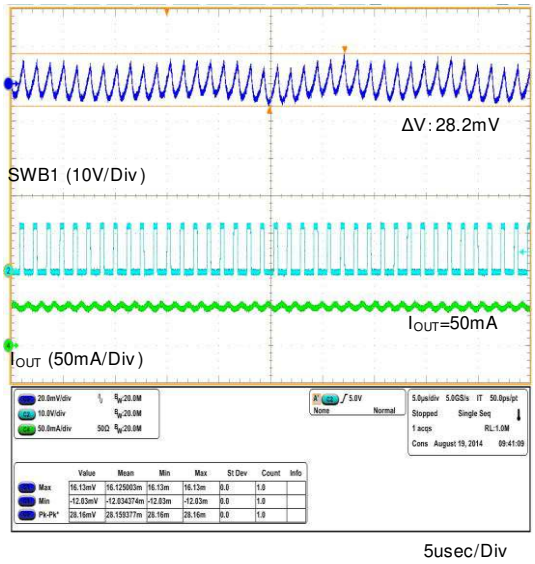

Figure 34. VGL Ripple Voltage

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

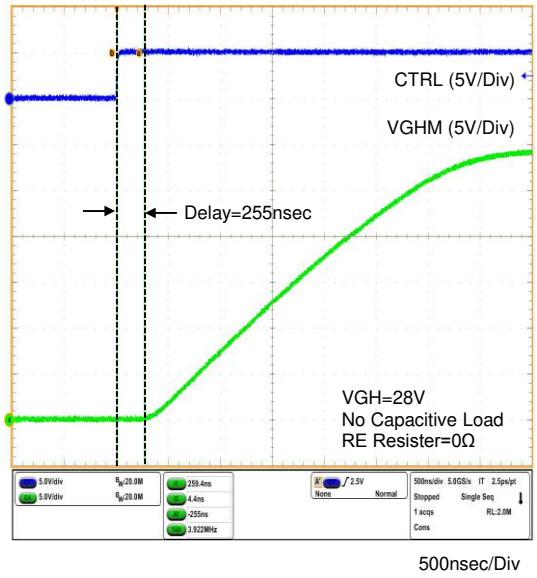

Figure 35. GPM Propagation Delay (rise)

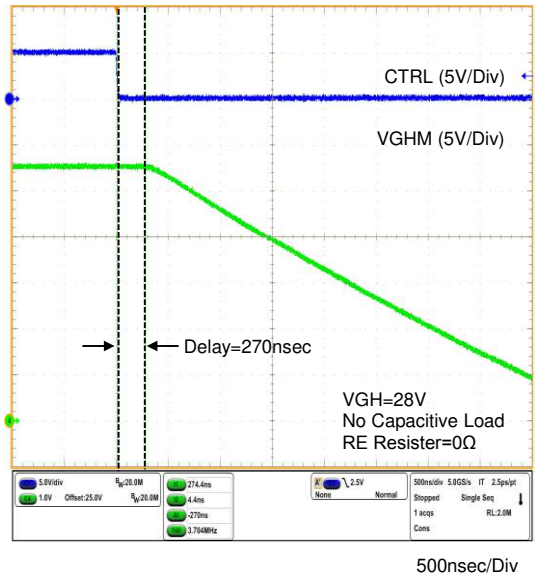

Figure 36. GPM Propagation Delay (fall)

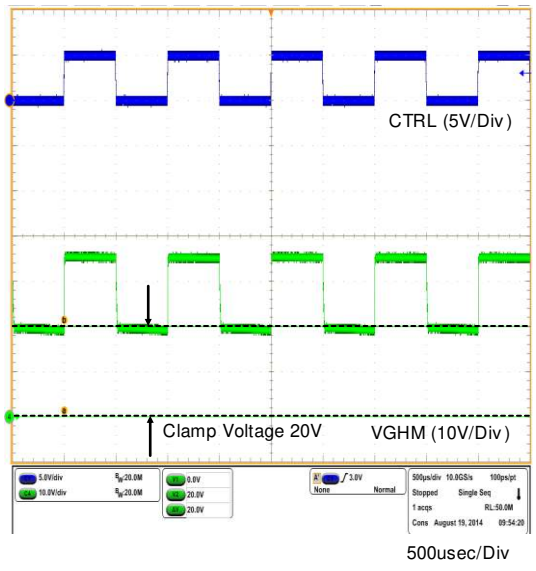

Figure 37. GPM Clamp Voltage (20V Clamp)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

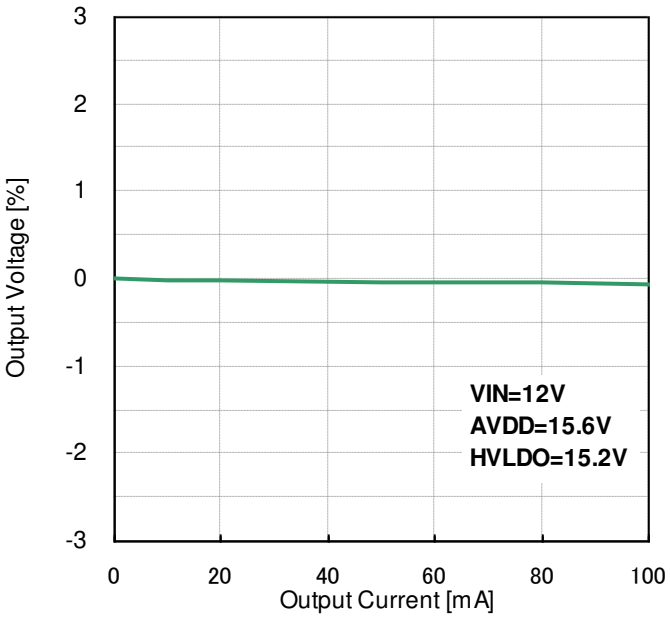

Figure 38. HVLDO Output Voltage vs Output Current

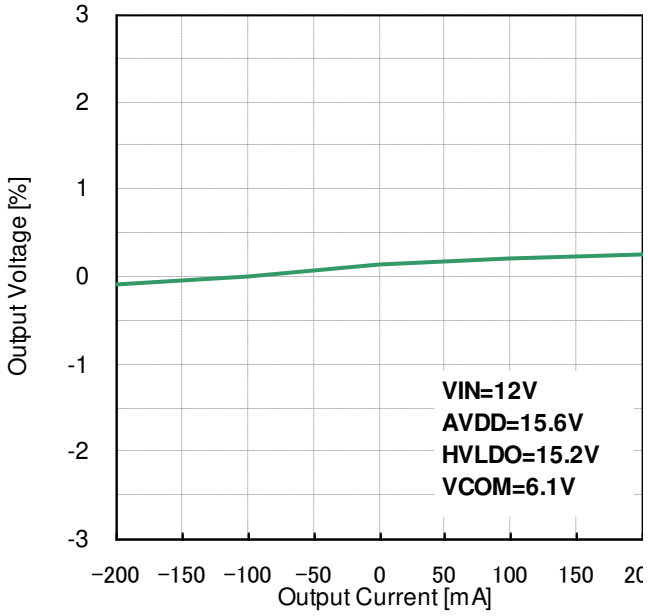

Figure 39. VCOM Output Voltage vs Output Current

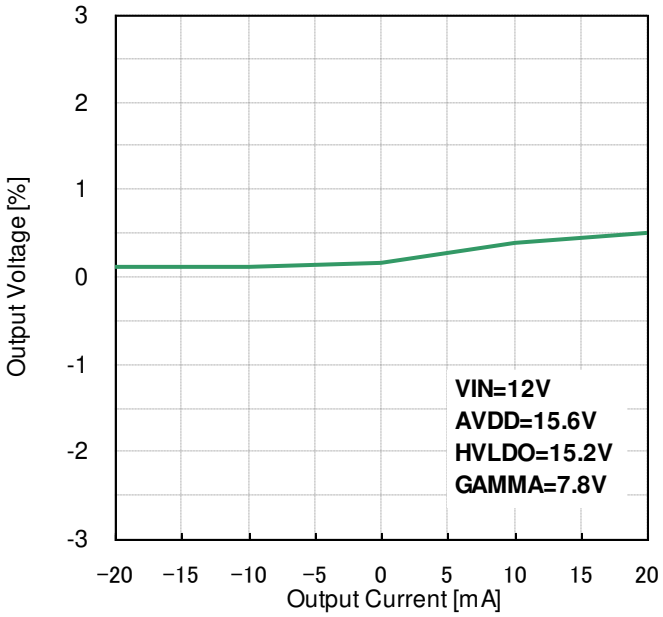

Figure 40. GAMMA Output Voltage vs Output Current

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

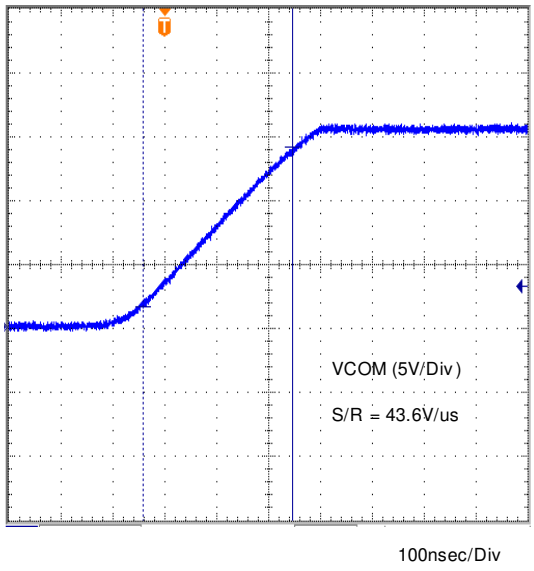

Figure 41. VCOM Slew Rate（Rise）

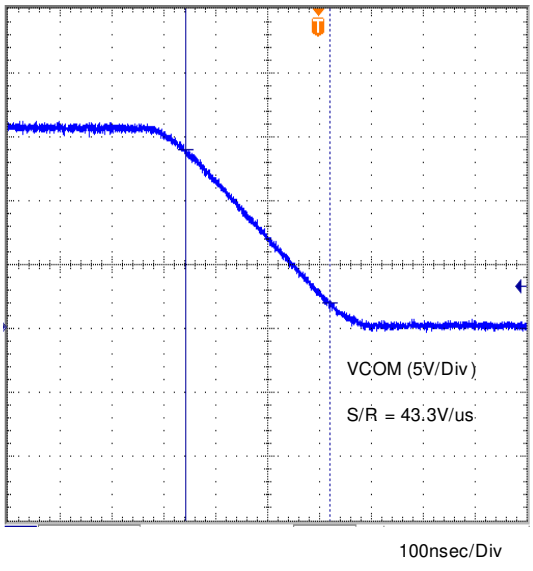

Figure 42. VCOM Slew Rate（Fall）

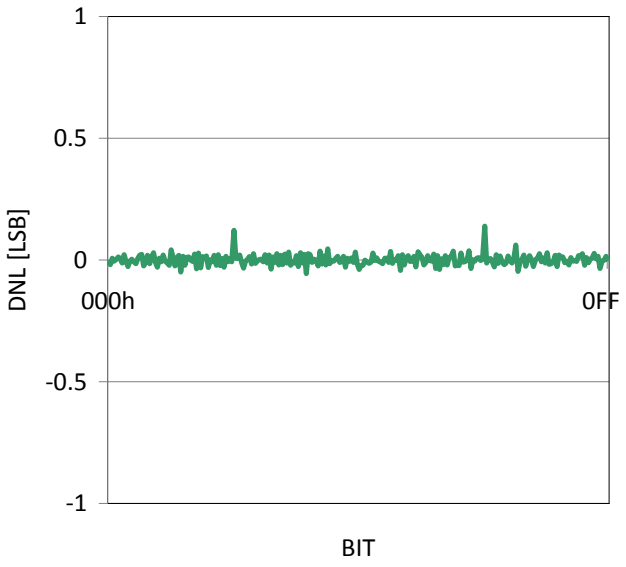

Figure 43. VCOM DNL vs BIT

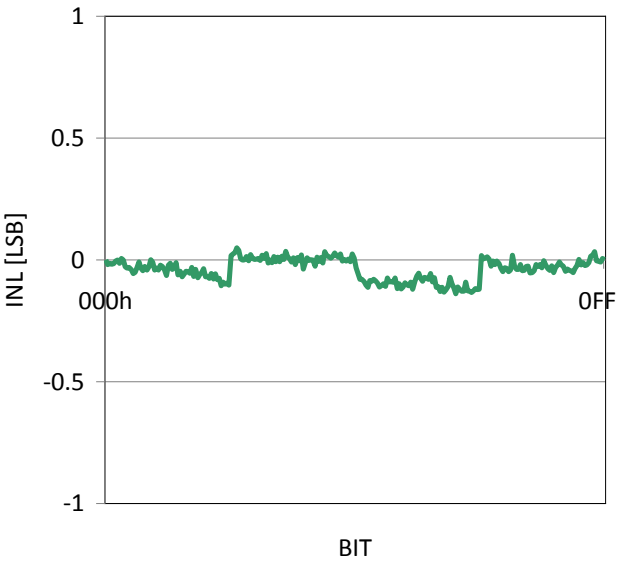

Figure 44. VCOM INL vs BIT

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

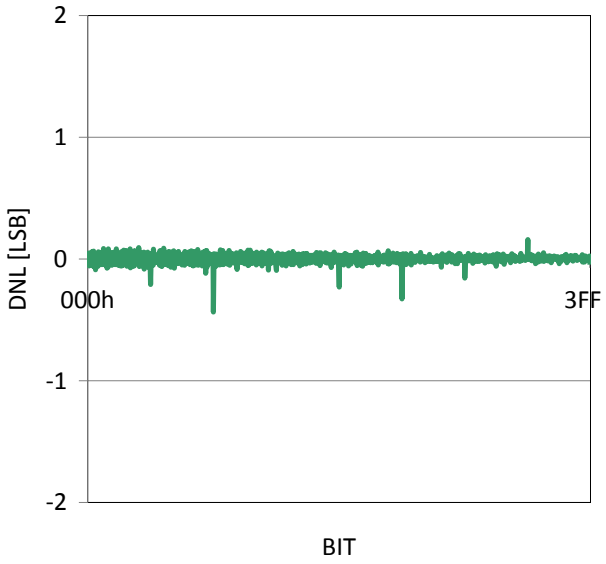

Figure 45. GAMMA DNL vs BIT

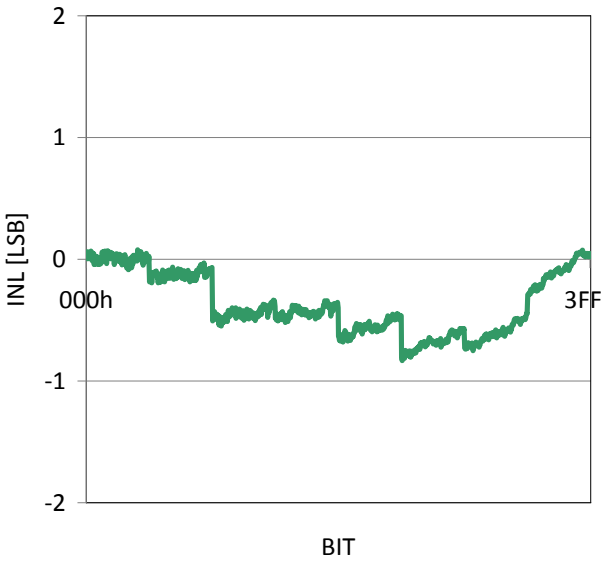

Figure 46. GAMMA INL vs BIT

Timing Chart

ON and OFF Sequence of this IC are shown below.

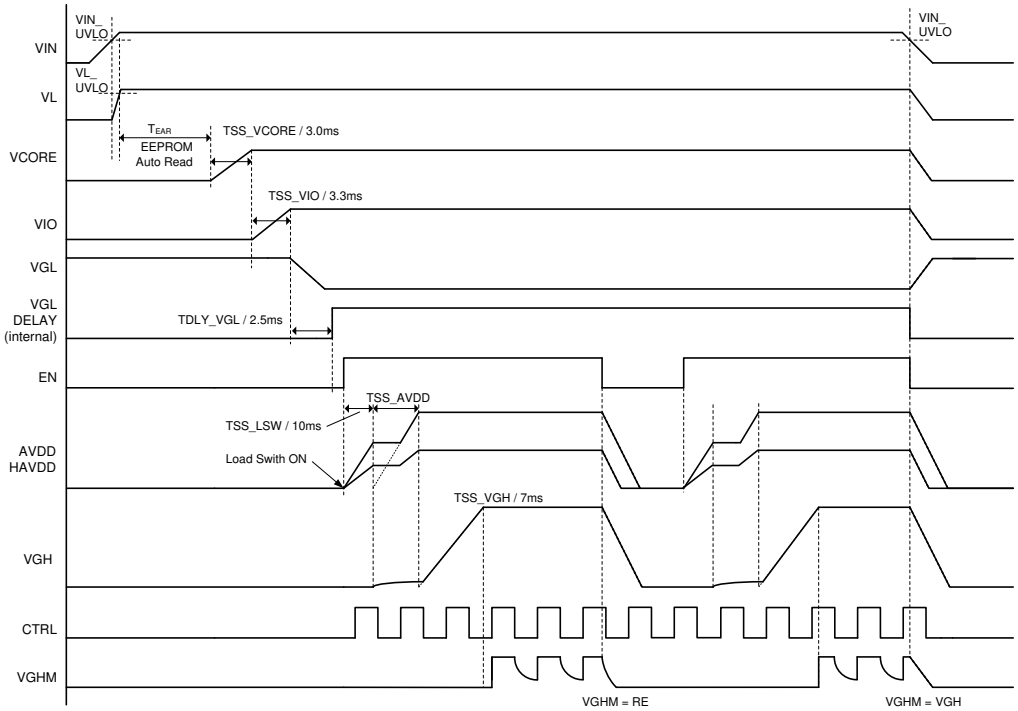

Figure 47. Timing Chart

VL activates with UVLO release of VIN.
It reads EEPROM data by Auto Read operation after VL finish its activation. (T_{EAR}=2msec)
After Auto Read completion, VCORE activates. The Soft Start time of VCORE is 3msec.
After VCORE soft-start completion, VIO activates. The Soft Start time of VIO is 3.3msec if the setting is 3.3V.
After VIO soft-start completion, PG becomes high and VGL activates. (If SWB1 is used)
The Soft Start time of VGL depends on output voltage setting, external capacitor etc.
2.5msec after VIO soft-start completion, Load SW turns ON (10msec) because of EN=High and AVDD activates.
The Soft Start time of AVDD can be changed by register setting. (10msec or 20msec)
After AVDD started, VGH activates. The Soft Start time of VGH is 7msec if the setting is 35V.
After VGH started, CTRL rising or falling will be a trigger to activate GPM operation.

When VGHM voltage at CTRL =L reaches the GPM clamp voltage, VGHM output is high impedance.
GPM, VGH, AVDD, HAVDD shuts down when EN=Low. GPM output (VGHM) will be the same potential with RE.
All output shuts down when UVLO of VIN is detected. VGHM will be the same potential with VGH.

HVLDO, HAVDD and VCOM starts up followed by AVDD output voltage. AMP 1 to 4 startup followed by HVLDO output voltage.

When EN=low, AVDD and HAVDD output become high impedance. HVLDO, VCOM and AMP1 to 4 output shut down followed by AVDD till AVDD is below a certain level.

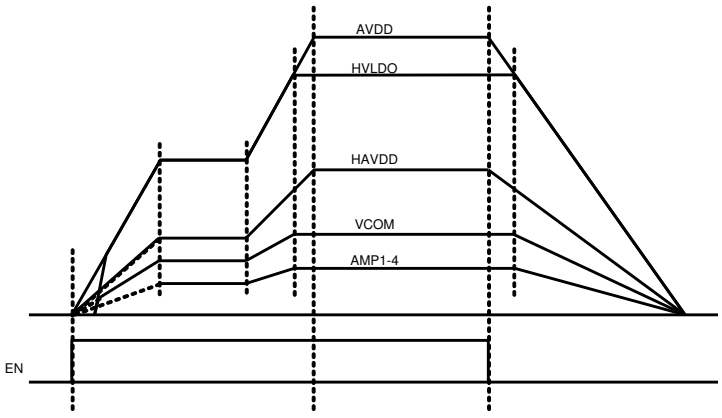

Figure 48. Timing Chart 2

Example Application
（TOP VIEW）

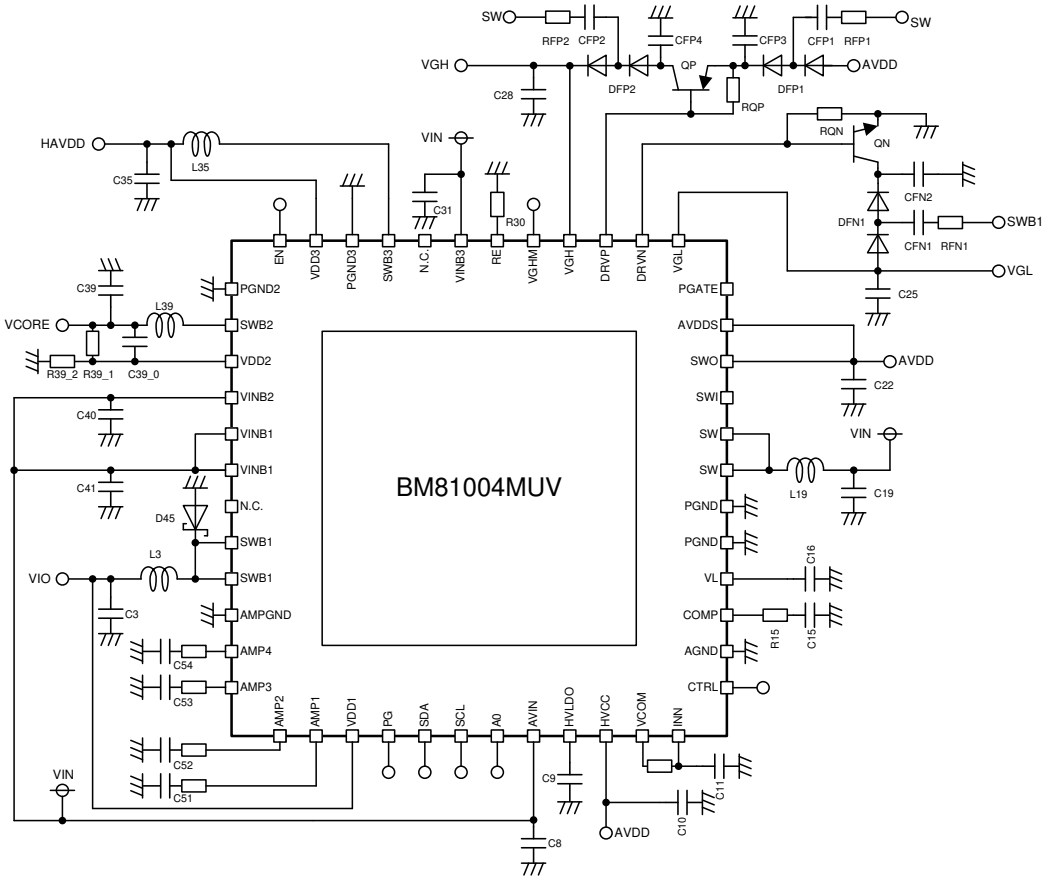

Figure 49. Example Application

Application circuit components list

Parts name	Value	Company	Parts Number	Parts name	Value	Company	Parts Number
C3	4x 10 [uF]	MURATA	GRM21BB31A106KE18	C40	10 [uF]	MURATA	GRM31CB31E106KA75
C8	1 [uF]	MURATA	GRM188B31E105KA75	C41	2x 10 [uF]	MURATA	GRM31CB31E106KA75
C9	10 [uF]	MURATA	GRM31CB31E106KA75	C51-54	0.1 [uF]	MURATA	GRM188B31H104KA92
C10	10 [uF]	MURATA	GRM31CB31E106KA75	R15	2.7 [kΩ]	ROHM	MCR03
C11	10 [uF]	MURATA	GRM31CB31E106KA75	R30	300 [Ω]	ROHM	MCR25
C15	6.8 [nF]	MURATA	GRM188B11E682KA01	R39_1	330 [Ω]	ROHM	MCR03
C16	1 [uF]	MURATA	GRM188CB31E105KA75	R39_2	120 [Ω]	ROHM	MCR03
C19	2x 10 [uF]	MURATA	GRM31CB31E106KA75	RFN1	2.2 [Ω]	ROHM	MCR25
C22	4x 10 [uF]	MURATA	GRM31CB31E106KA75	RFP1-2	2.2 [Ω]	ROHM	MCR25
C25	4.7 [uF]	MURATA	GRM219B31C475KE15	RQN	100 [kΩ]	ROHM	MCR03
CFN1	0.1 [uF]	MURATA	GRM188B31H104KA92	RQP	100 [kΩ]	ROHM	MCR03
CFN2	470 [pF]	MURATA	GRM188B11H471KA01	L19	6.8 [uH]	TAIYO YUDEN	NS10165T6R8N
CFP1	0.1 [uF]	MURATA	GRM188B31H104KA92	L3	6.8 [uH]	TAIYO YUDEN	NRS8040T6R8M
CPF2	0.1 [uF]	MURATA	GRM188B31H104KA92	L35	6.8 [uH]	TAIYO YUDEN	NRS8040T6R8M
CPF3	1 [uF]	MURATA	GRM21BB31H105KA12	L39	6.8 [uH]	TAIYO YUDEN	NRS8040T6R8M
CFP4	2.2 [nF]	MURATA	GRM188B11H222KA01	D45	-	ROHM	RSX301L-30
C28	10 [uF]	MURATA	GRM31CB31H106KA12	DFN1	-	ROHM	RB558W
C31	10 [uF]	MURATA	GRM31CB31E106KA75	DFP1	-	ROHM	RB558W
C35	2x 10 [uF]	MURATA	GRM31CB31E106KA75	DFP2	-	ROHM	RB558W
C39	4x 10 [uF]	MURATA	GRM21BB31A106KE18	QN	PNP	ROHM	2SCR513P
C39_0	22 [nF]	MURATA	GRM188B31H104KA92	QP	NPN	ROHM	2SAR513P