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Power supply IC series for TFT-LCD panels

12V Input Multi-Channel System Power Supply IC

BM81110MUW

General Description

BM81110MUW is a system power supply for TFT-LCD panels used for liquid crystal TVs. This IC is incorporated with Negative and Positive charge pump controllers and Gate Pulse Modulation (GPM) function. It also features built-in EEPROM to contain each setting voltage, soft start time, etc.

Features

- Step-up DC/DC converter (AVDD) (Synchronous rectification, built-in load switch)
- Step-down DC/DC converter 1 (VIO) (Non-synchronous rectification)
- Step-down DC/DC converter 2 (VCORE) (Synchronous rectification)
- Step-down DC/DC converter 3 (HAVDD) (Synchronous rectification)
- Positive charge pump controller (VGH)
- Negative charge pump controller (VGL)
- Gate Pulse Modulation (GPM) function
- Output voltage control by I2C
- Built-in EEPROM
- Switching Frequency 750kHz (AVDD, VIO)
- Switching Frequency 1MHz (VCORE, HAVDD)

Applications

- TFT-LCD panel

Key Specifications

- Input voltage range : 8.6V to 14.7V
- AVDD Output voltage range : 13.5V to 19.8V
- VIO Output voltage range : 2.2V to 3.7V
- VCORE Output voltage range : 0.8V to 3.3V
- HAVDD Output voltage range : 4.8V to 11.1V
- VGH Output voltage range : 20V to 35V
- VGL Output voltage range : -14.5V to -5.5V
- Switching Frequency : 750kHz(Typ) 1MHz(Typ)
- Operating temperature range : -40℃ to +85℃

Package

	W(Typ) x D(Typ) x H(Max)
VQFN40W6060A	6.00mm x 6.00mm x 0.8mm

Typical Application Circuit（TOP VIEW）

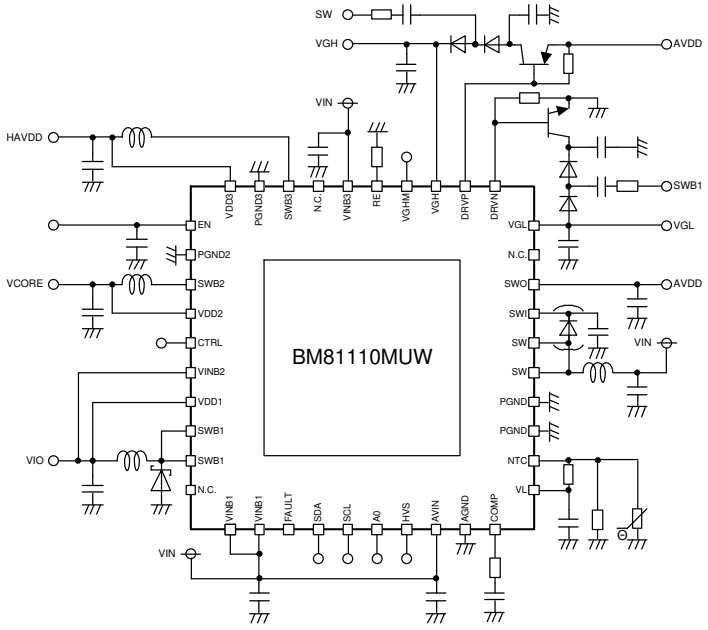


Figure1. Application Circuit

Contents

Pin Configuration (TOP View)

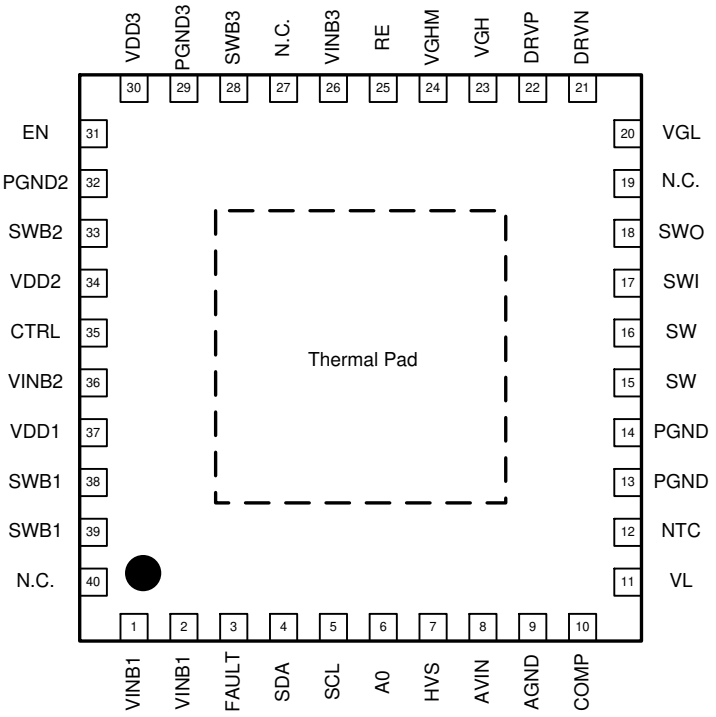


Figure 2. Pin Configuration

Pin Description

PIN No.	SYMBOL	FUNCTION	PIN No.	SYMBOL	FUNCTION
1	VINB1	Step-down DC/DC power supply input 1	21	DRVN	Negative charge pump drive pin
2	VINB1	Step-down DC/DC power supply input 1	22	DRVP	Positive charge pump drive pin
3	FAULT	FAULT signal output	23	VGH	Positive charge pump output
4	SDA	Serial data input	24	VGHM	GPM output
5	SCL	Serial clock input	25	RE	GPM Slope adjustment pin
6	A0	I2C address select pin	26	VINB3	Step-down DC/DC power supply input 3
7	HVS	HVS mode select pin	27	N.C.	—
8	AVIN	Power supply input	28	SWB3	Step-down DC/DC switching pin 3
9	AGND	Analog ground	29	PGND3	Step-down DC/DC ground 3
10	COMP	Error amplifier output	30	VDD3	Step-down DC/DC output 3
11	VL	Internal REG output	31	EN	Enable input
12	NTC	Thermistor connecting pin	32	PGND2	Step-down DC/DC ground 2
13	PGND	Step-up DC/DC ground	33	SWB2	Step-down DC/DC switching pin 2
14	PGND	Step-up DC/DC ground	34	VDD2	Step-down DC/DC output 2
15	SW	Step-up DC/DC switching pin	35	CTRL	GPM control pin
16	SW	Step-up DC/DC switching pin	36	VINB2	Step-down DC/DC power supply input 2
17	SWI	Load switch input	37	VDD1	Step-down DC/DC output 1
18	SWO	Load switch output	38	SWB1	Step-down DC/DC switching pin 1
19	N.C.	—	39	SWB1	Step-down DC/DC switching pin 1
20	VGL	Negative charge pump output	40	N.C.	—

Block Diagram (VGH Doubler)

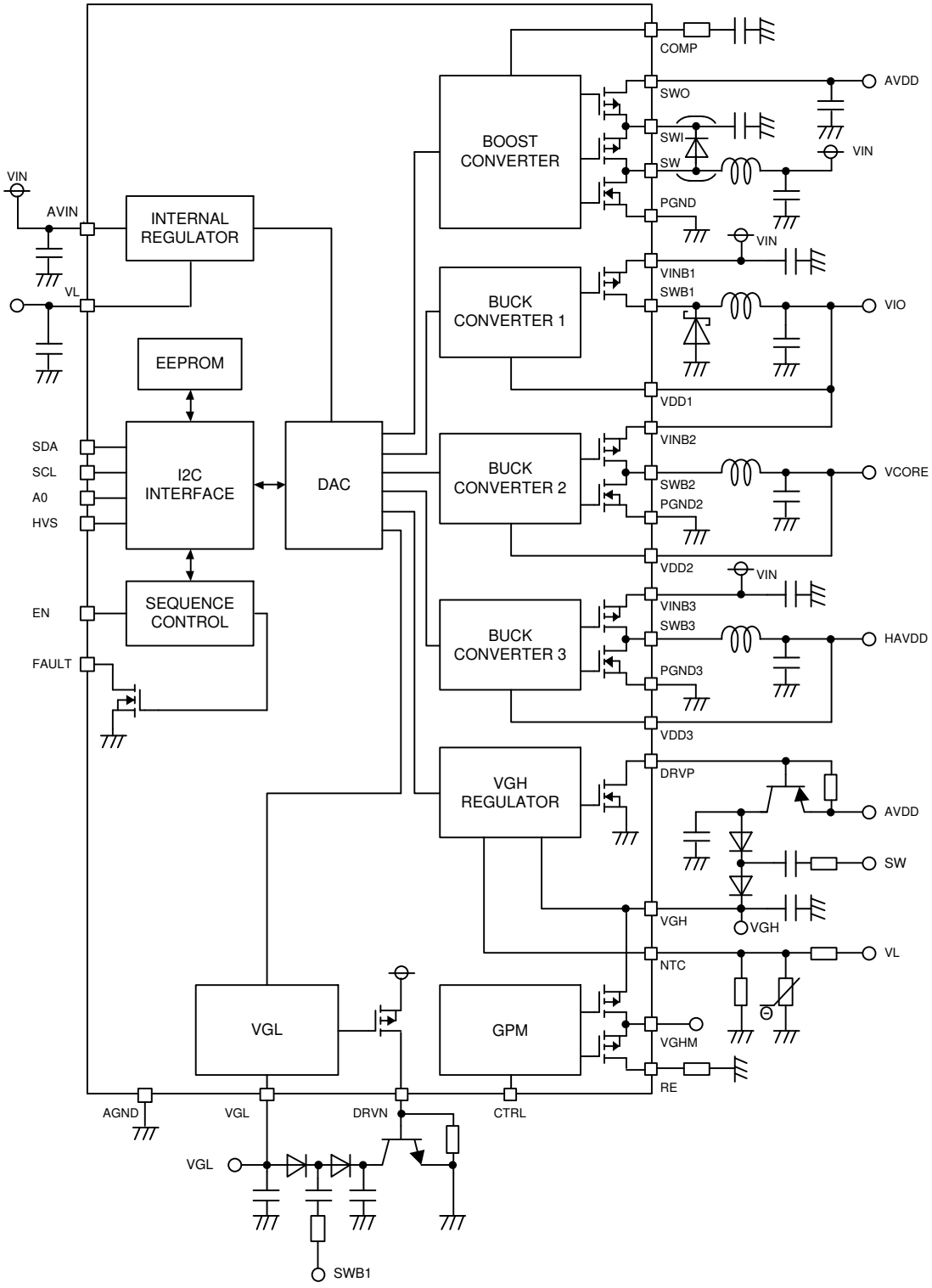


Figure 3. Block Diagram (VGH Doubler)

Block Diagram (VGH Trippler)

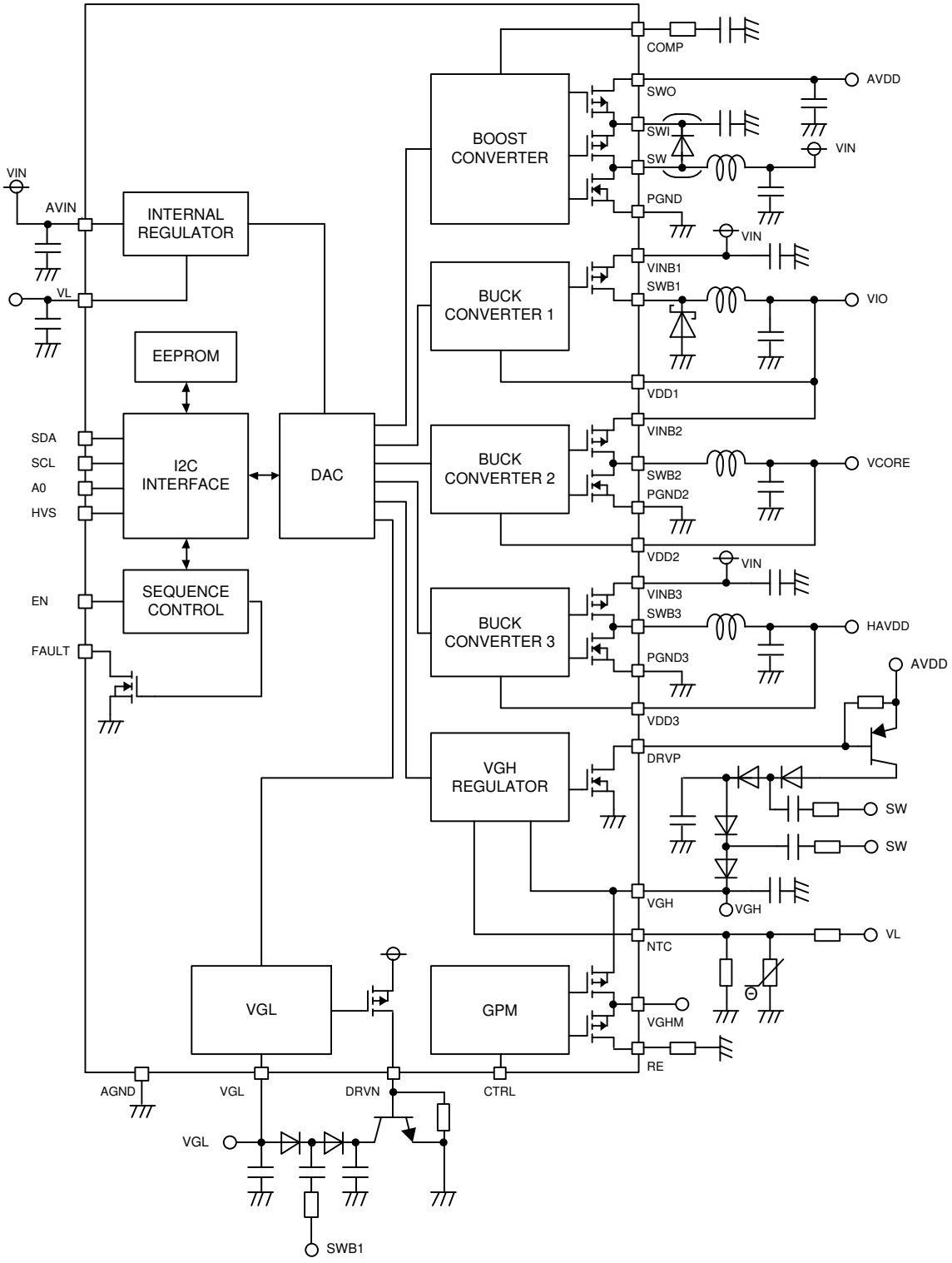


Figure 4. Block Diagram (VGH Trippler)

Description of each Block

① BUCK CONVERTER BLOCK 1
This block generates VIO (VDD1) voltage from Power supply voltage.
After releasing UVLO of VIN, VL starts activating. After Auto Read is operated to EEPROM, VIO will be activated.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by OVP, UVP and OCP protection functions.

② BUCK CONVERTER BLOCK 2
This block generates VCORE (VDD2) voltage from Power supply voltage of VIO.
After completing VIO start-up, VCORE starts activating.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by OVP, UVP and OCP protection functions.

③ VGL REGULATOR BLOCK
This block generates VGL voltage.
After completing VCORE start-up, VGL starts activating.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by UVP and OCP protection functions.

④ BOOST CONVERTER BLOCK
This block generates AVDD (SWO) voltage from Power supply voltage.
It activates when EN=H, and under condition where VIO and VGL are active.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by OVP, UVP and OCP protection functions.

⑤ BUCK CONVERTER BLOCK 3
This block generates HAVDD (VDD3) voltage from Power supply voltage.
HAVDD starts up following AVDD output voltage.
The setting voltage range of the HAVDD voltage depends on the AVDD setting voltage, and the lower limit level of the HAVDD voltage is limited to AVDD × 0.4.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by OVP, UVP and OCP protection functions.

⑥ VGH REGULATOR BLOCK
This block generates VGH voltage from AVDD voltage.
After completing AVDD star-up, VGH starts activating.
Power on Reset works at the time of VIN startup and the setting written to EEPROM will be reflected in Register.
During operation, it is possible to prevent destruction of IC by OVP, UVP and OCP protection functions.

⑦ GPM BLOCK
This is a switching circuit to drive a gate voltage for TFT consisted of PMOS FET.
VGHM output synchronizes with CTRL input and outputs High voltage = VGH at CTRL=H.
GPM Falling Limit voltage can be controlled by EEPROM.

※ Caution
・EN Input tolerant function is built-in. No need to be always EN < VIN.
・When FAULT pin is not used, FAULT pin must be connected to GND, or it should be open.
・When NTC pin is not used, NTC pin must be connected to GND.
・When HVS pin is not used, HVS pin must be connected to GND.

Absolute Maximum Ratings

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Supply Voltage	AVIN, VINB1, VINB3	-0.3	-	24	V
	VINB2	-0.3	-	7	V
Input Voltage	SDA, SCL, A0, HVS, NTC, EN, CTRL	-0.3	-	7	V
Output Voltage	VL	-0.3	-	6.5	V
	COMP, FAULT VDD2, SWB2	-0.3	-	7	V
	SW, SWI, SWO, VDD1, SWB1, VDD3, SWB3	-0.3	-	24	V
	VGL, DRVN	-15	-	7	V
	DRVP, VGH, VGHM, RE	-0.3	-	40	V
Operating Ambient Temperature Range	Ta	-40	-	85	℃
Storage Temperature Range	Tstg	-55	-	150	℃
Maximum Continuous Junction Temperature	Tjmax (*1)	-	-	150	℃
Power Dissipation (*2)	Pd	3.20			W
	θ ja	39.1			degC/W

*1 It shows junction temperature when stores.
*2 Derate by 25.6mW/℃ at Ta>25℃ when mounted on 4-layer 114.3mm × 74.2mm × 1.6mm glass epoxy board.

Recommended Operating Conditions (Ta=-40℃～85℃)

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Supply Voltage	AVIN	8.6	-	14.7	V
Functional pin voltage	EN, A0, HVS, CTRL	-0.1	-	5.5	V
2 wire serial pin voltage	SDA, SCL	-0.1	-	5.5	V
2 wire serial frequency	FCLK	-	-	400	kHz

Electrical Characteristics (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 GENERAL 】						
VIN Under Voltage Lockout Threshold	VIN_ UVLO	8.0	8.3	8.6	V	VIN rising
		7.25	7.55	7.85	V	VIN falling
Thermal shutdown	TSD	-	175	-	℃	
Internal Oscillator Frequency 1	FOSC1	600	750	900	kHz	AVDD, VIO
Internal Oscillator Frequency 2	FOSC2	800	1000	1200	kHz	VCORE, HAVDD
VL Voltage	VL	4.9	5	5.1	V	
Consumption Current	ICC	-	5.0	-	mA	No switching
【 LOGIC SIGNALS SDA, SCL, EN, A0, CTRL, HVS 】						
High Level Input Voltage	VIH	2	-	-	V	
Low Level Input Voltage	VIL	-	-	0.5	V	
Minimum Output Voltage	VSDA	-	-	0.4	V	SDA, ISDA=3mA
Pull-Down Resistance	RLOGIC	140	200	260	kΩ	EN, A0, CTRL, HVS
【 BOOST CONVERTER (AVDD) 】						
Output Voltage Range	AVDD	13.5	-	19.8	V	0.1V step
HVS Mode Offset Voltage	VHVS	0	-	3	V	0.2V step
Regulation Voltage	AVDD_R	14.85	15.0	15.15	V	Data：0Fh
Hi-Side Leakage Current	ILK_SWH	-	0	10	uA	SW=0V
Hi-Side SW ON-Resistance	RON_SWH	-	100	200	mΩ	ISW=-500mA
Lo-Side SW Leakage Current	ILK_SWL	-	0	10	uA	SW=24V
Lo-Side SW ON-Resistance	RON_SWL	-	100	200	mΩ	ISW=500mA
Load SW ON-Resistance	RON_LS	-	100	200	mΩ	ILS=500mA
SW Current Limit	ILIM_SW	4.25	5	5.75	A	L=10uH
SW Current Limit Offset	ILIM_SET	0	-	2.8	A	0.4A step
Over-Voltage Protection Rise	VOVP_AVDD_RISE	20.5	21.5	22.5	V	
Over-Voltage Protection Fall	VOVP_AVDD_FALL	20	-	-	V	
AVDD UVP Detecting Voltage	VUVP_ AVDD	-	AVDD x 0.8	-	V	
Soft Start Time	TSS_ AVDD	10	-	20	msec	
Load Switch Current Limit	ILIM_LSW	-	7	-	A	

Electrical Characteristics (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 BUCK CONVERTER 1 (VIO) 】						
Output Voltage Range	VIO	2.2	-	3.7	V	0.1V step
Regulation Voltage	VIO_R	2.45	2.5	2.55	V	Data：03h
Hi-Side SWB1 Leak Current	ILK_SWB1H	-	0	10	uA	SWB1=0V
Hi-Side SWB1 ON-Resistance	RON_SWB1H	-	200	300	mΩ	SWB1=-500mA
SWB1 Current Limit	ILIM_SWB1	2.8	3.5	4.2	A	L=10uH
VIO Over-Voltage Protection	VOVP_VIO	-	VIO x 1.1	-	V	
VIO UVP Detecting Voltage	VUVP_VIO	-	VIO x 0.8	-	V	Frequency 1/4
Soft Start Time	TSS_VIO	-	3	-	msec	VIO=3.0V
【 BUCK CONVERTER 2 (VCORE) 】						
Output Voltage Range	VCORE	0.8	-	3.3	V	0.1V step
Regulation Voltage	VCORE_R	0.98	1.0	1.02	V	Data：02h
Hi-Side SWB2 Leak Current	ILK_SWB2H	-	0	10	uA	SWB2=0V
Hi-Side SWB2 ON-Resistance	RON_SWB2H	-	175	300	mΩ	SWB2=-500mA
Lo-Side SWB2 Leak Current	ILK_SWB2L	-	0	10	uA	SWB2=7V
Lo-Side SWB2 ON-Resistance	RON_SWB2L	-	175	300	mΩ	SWB2=500mA
SWB2 Current Limit	ILIM_SWB2	2.0	3.0	4.0	A	L=10uH
VCORE Over-Voltage Protection	VOVP_VCORE	-	VCORE x 1.1	-	V	
VCORE UVP Detecting Voltage	VUVP_VCORE	-	VCORE x 0.8	-	V	Frequency 1/4
Soft Start Time	TSS_VCORE	-	4	-	msec	VCORE=2.0V
【 BUCK CONVERTER 3 (HAVDD) 】						
Output Voltage Range	HAVDD	4.8	-	11.1	V	0.1V step
Regulation Voltage	HAVDD_R	7.3875	7.5	7.6125	V	Data：1Bh
Hi-Side SWB3 Leak Current	ILK_SWB3H	-	0	10	uA	SWB3=0V
Hi-Side SWB3 ON-Resistance	RON_SWB3H	-	300	500	mΩ	SWB3=-500mA
Lo-Side SWB3 Leak Current	ILK_SWB3L	-	0	10	uA	SWB3=24V
Lo-Side SWB3 ON-Resistance	RON_SWB3L	-	300	500	mΩ	SWB3=500mA
SWB3 Current Limit	ILIM_SWB3	1.0	1.5	2.0	A	L=10uH
HAVDD Over-Voltage Protection	VOVP_HAVDD	-	HAVDD x 1.1	-	V	
HAVDD UVP Detecting Voltage	VUVP_HAVDD	-	HAVDD x 0.8	-	V	Frequency 1/4

Electrical Characteristics (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 VGH REGULATOR 】						
Output Voltage Range	VGH	20	-	35	V	1V step
Regulation Voltage	VGH_R	26.6	28	29.4	V	Data : 08h Io=5mA
VGH_H Offset Voltage	VGHH_O	0	-	15	V	
Over-Current Protection	ILIM_DRVP	5	-	-	mA	
VGH UVP Detecting Voltage	VUVP_VGH	-	VGH x 0.8	-	V	
VGH Over-Voltage Protection	VOVP_VGH	36	38	40	V	
Soft Start Time	TSS_VGH	-	7	-	msec	VGH=28V
【 VGL REGULATOR 】						
Output Voltage Range	VGL	-14.5	-	-5.5	V	0.6V step
Regulation Voltage	VGL_R	-8.0975	-7.9	-7.7025	V	Data : 04h Io=5mA
Over-Current Protection	ILIM_DRVN	5	-	-	mA	
VGL UVP Detecting Voltage	VUVP_VGL	-	VGL×0.8	-	V	
Delay Time	TDLY_VGL	-	2.5	-	msec	
DRVN Internal Register	R_DRVN	-	100	-	kΩ	
【 GATE PULSE MODULATION (GPM) 】						
VGH-VGHM ON-Resistance	RGHH	-	3	5	Ω	
RE-VGHM ON-Resistance	RGHL	-	3	-	Ω	
Propagation Delay	TGPM	150	250	350	nsec	

○This product has no designed protection against radioactive rays.

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

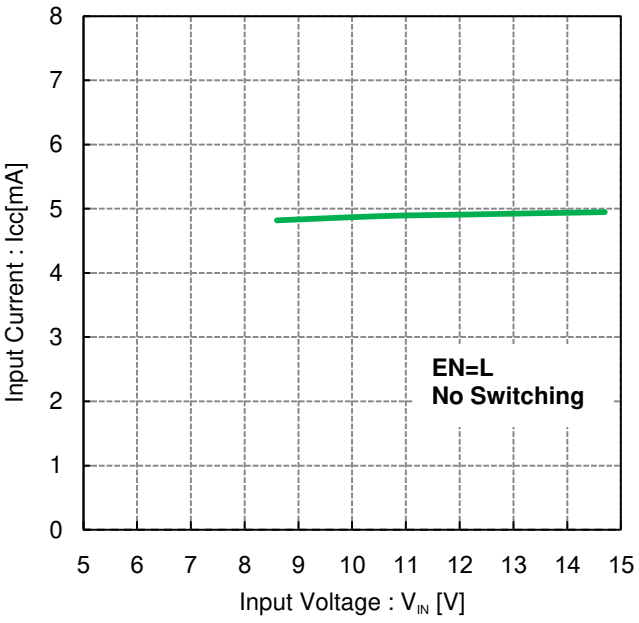


Figure 5. Input Current vs Input Voltage
(EN=L, no switching)

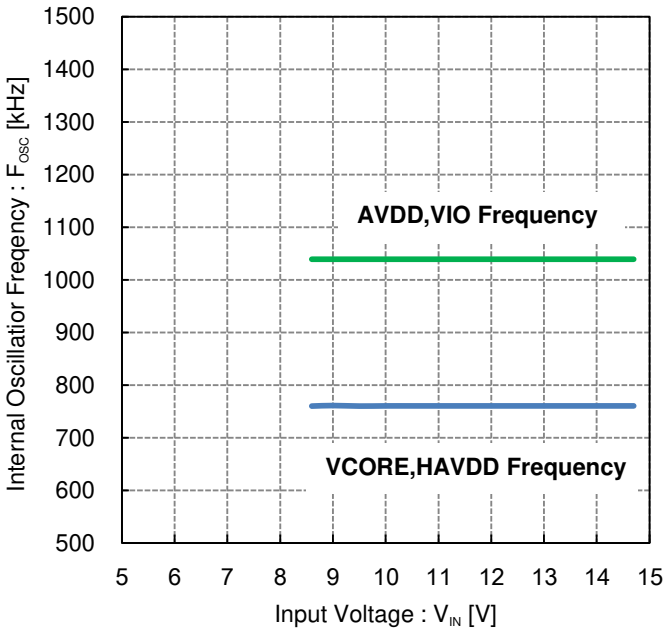


Figure 6. Internal Oscillator Frequency vs Input Voltage

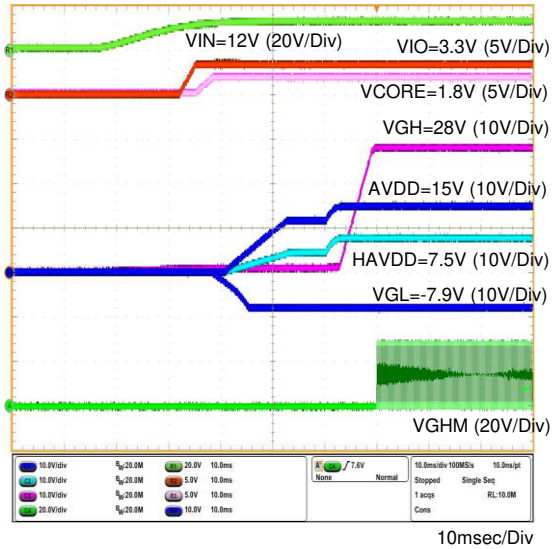


Figure 7. Power-on 1
(VGL driven by VIO switch node)

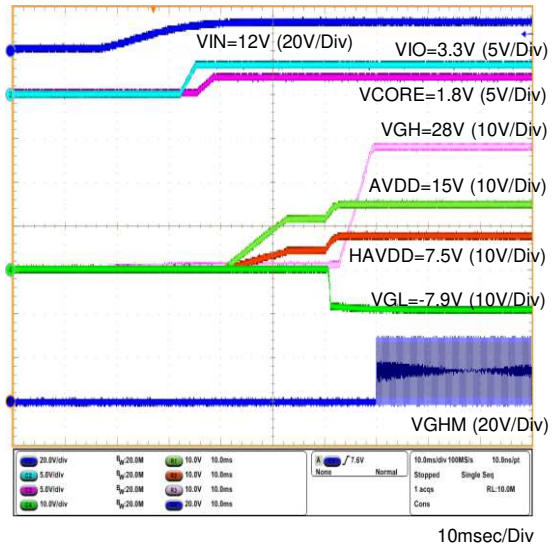


Figure 8. Power-on 2
(VGL driven AVDD switch node)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

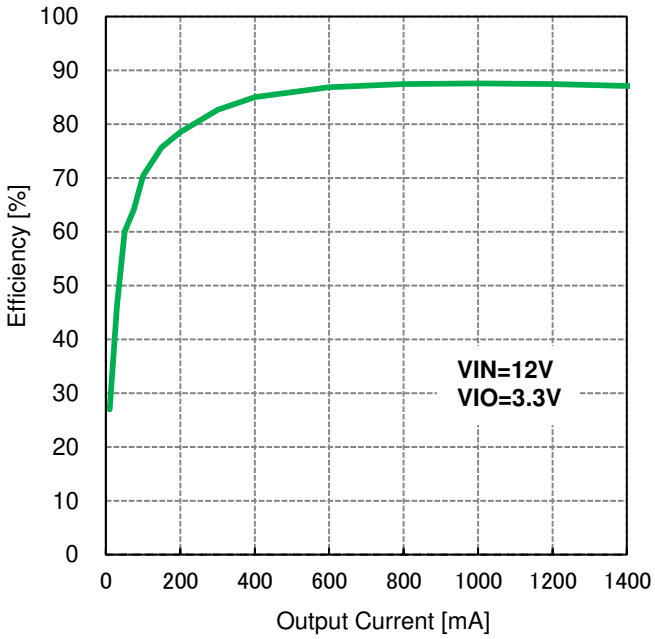


Figure 9. VIO Efficiency vs Output Current

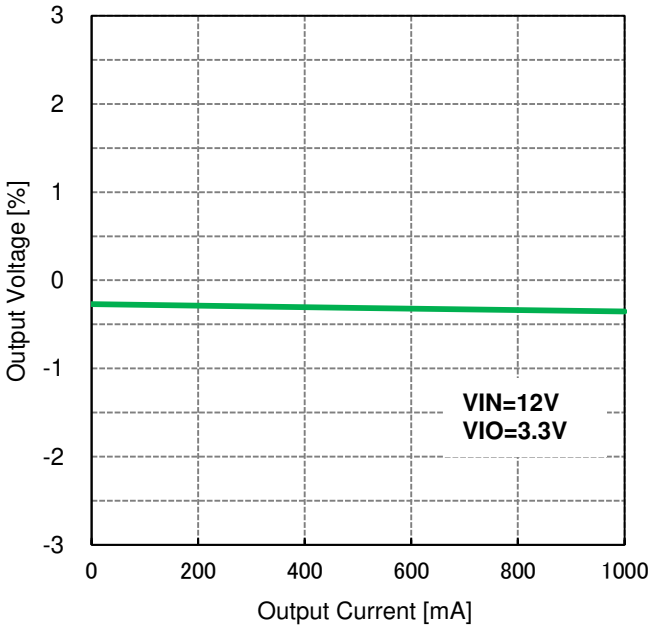


Figure 10. VIO Output Voltage vs Output Current

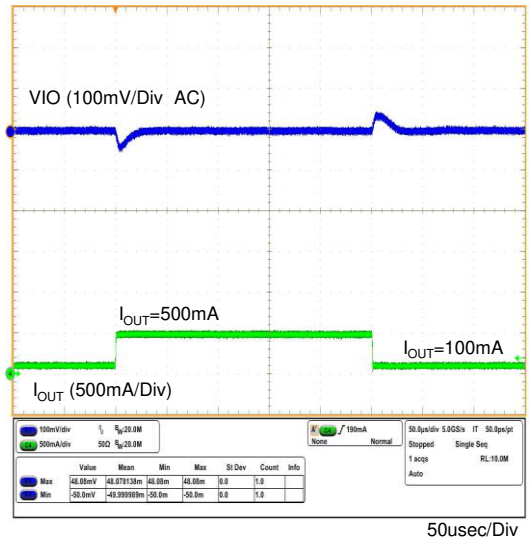


Figure 11. VIO Load Transient

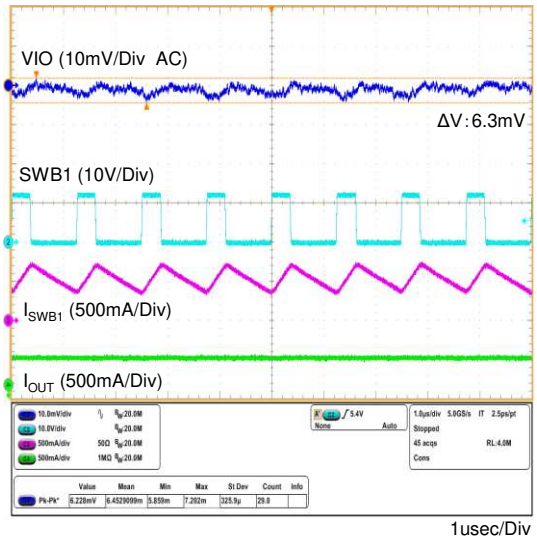


Figure 12. VIO Switching
(Output Current=500mA)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

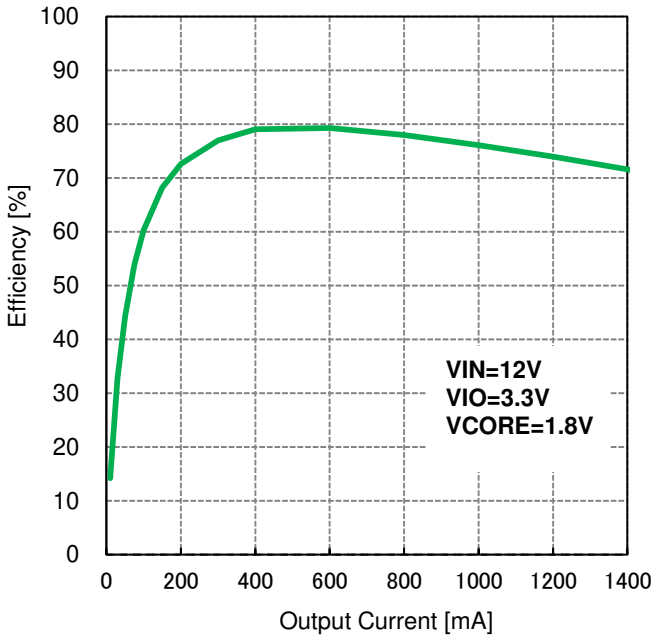


Figure 13. VCORE Efficiency vs Output Current

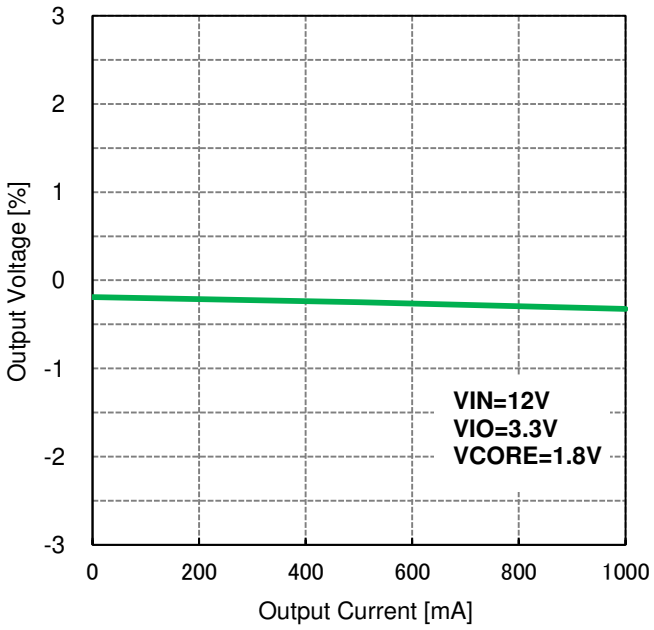


Figure 14. VCORE Output Voltage vs Output Current

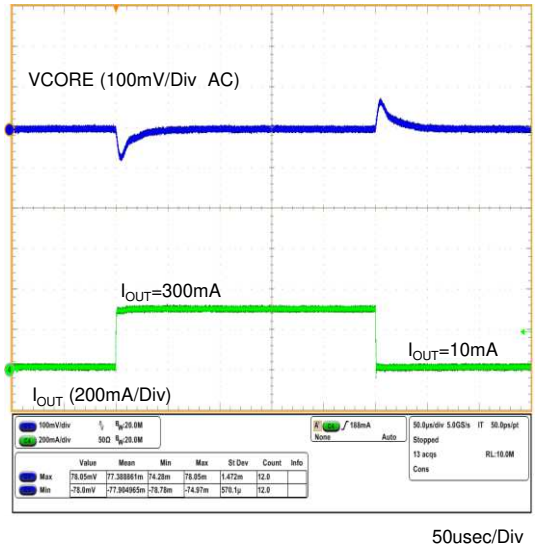


Figure 15. VCORE Load Transient

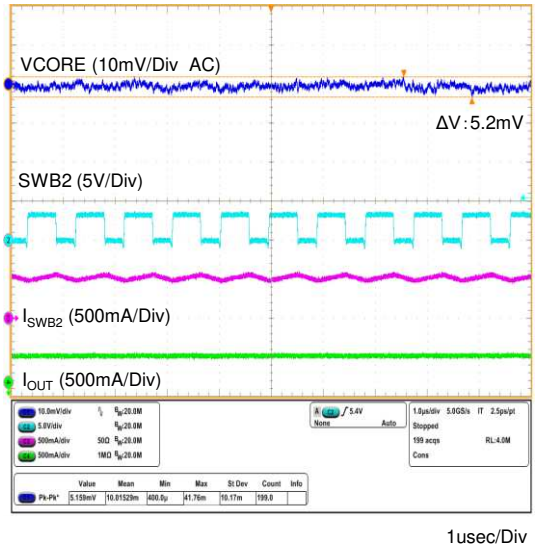


Figure 16. VCORE Switching (Output Current=500mA)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

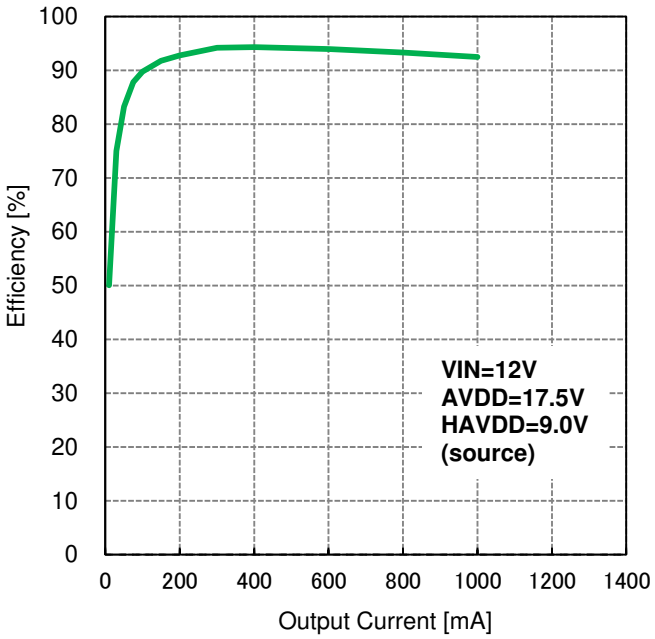


Figure 17. HAVDD Efficiency vs Output Current (source)

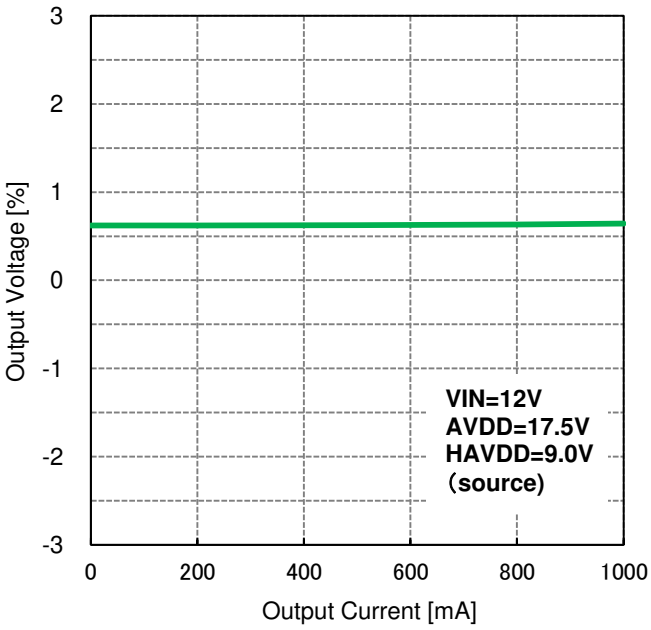


Figure 18. HAVDD Output Voltage vs Output Current (source)

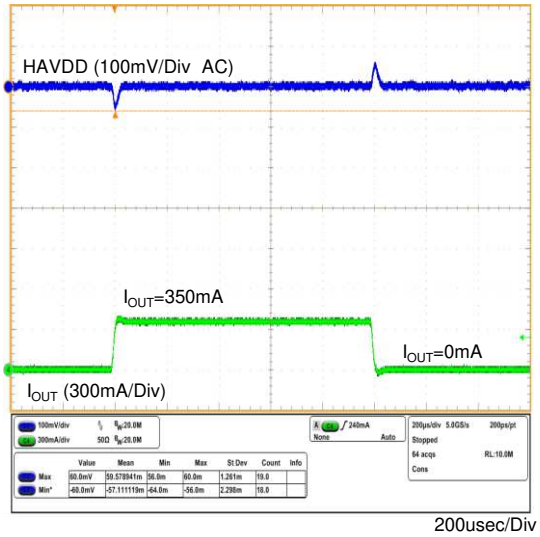


Figure 19. HAVDD Load Transient (source)

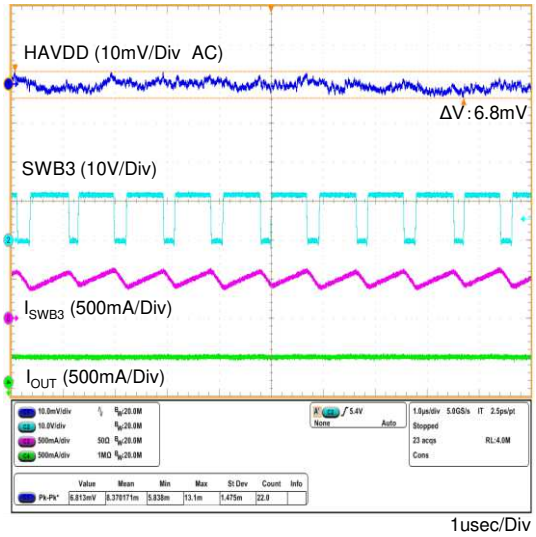


Figure 20. HAVDD Switching (source)
(Output Current=500mA)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

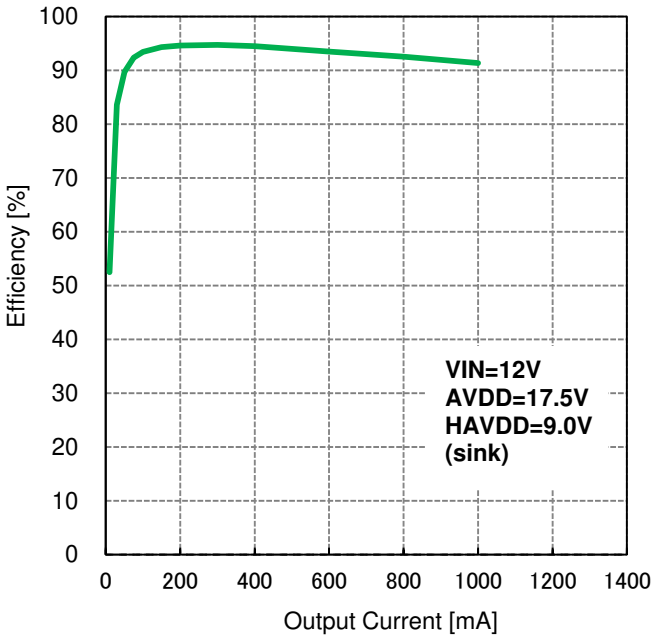


Figure 21. HAVDD Efficiency vs Output Current (sink)

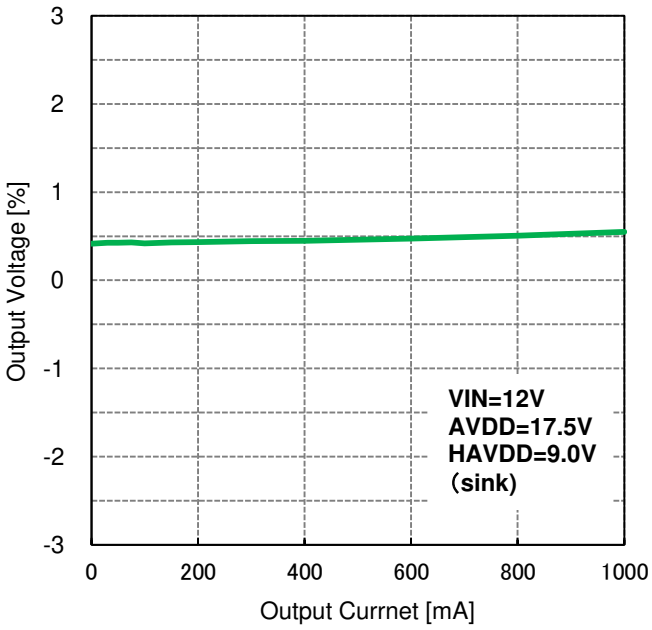


Figure 22. HAVDD Output Voltage vs Output Current (sink)

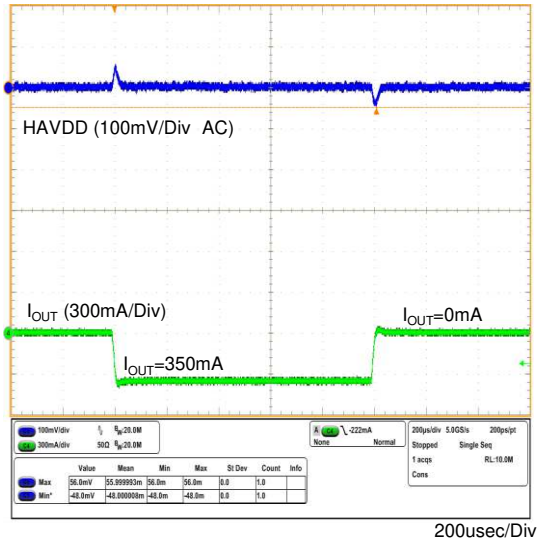


Figure 23. HAVDD Load Transient (sink)

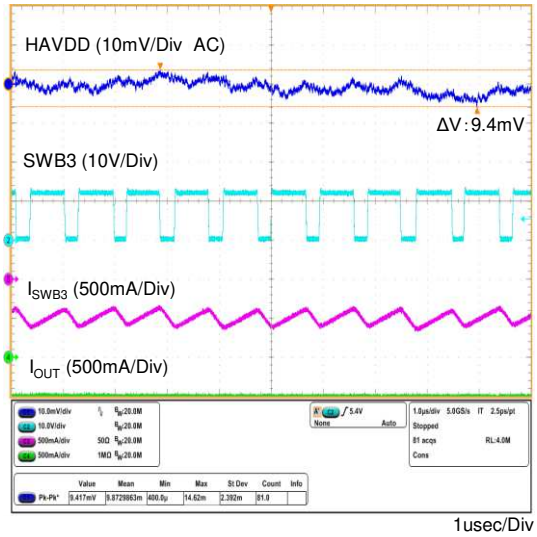


Figure 24. HAVDD Switching (sink)
(Output Current=500mA)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

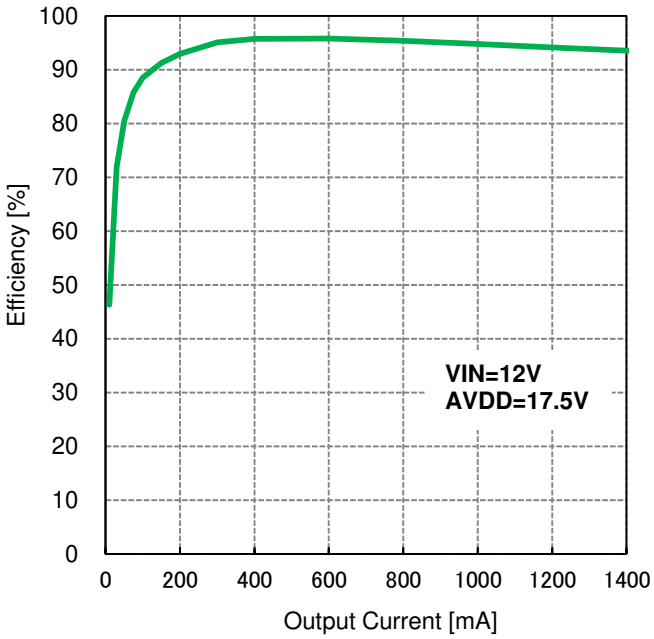


Figure 25. AVDD Efficiency vs Output Current

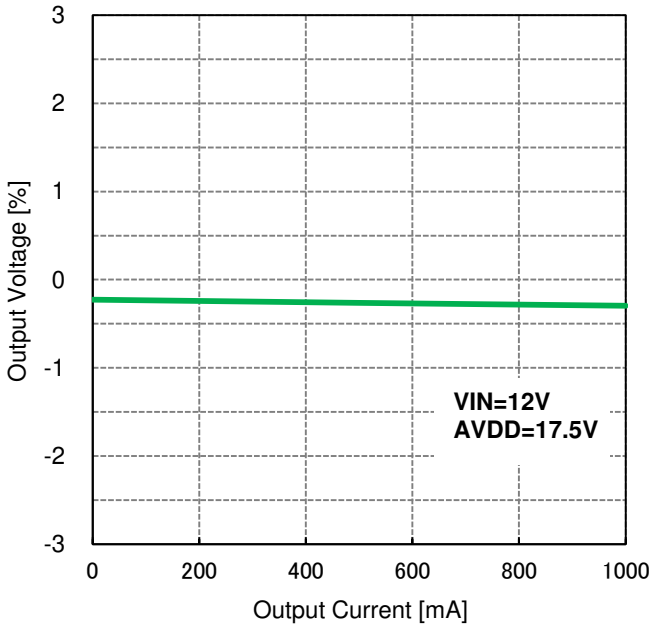


Figure 26. AVDD Output Voltage vs Output Current

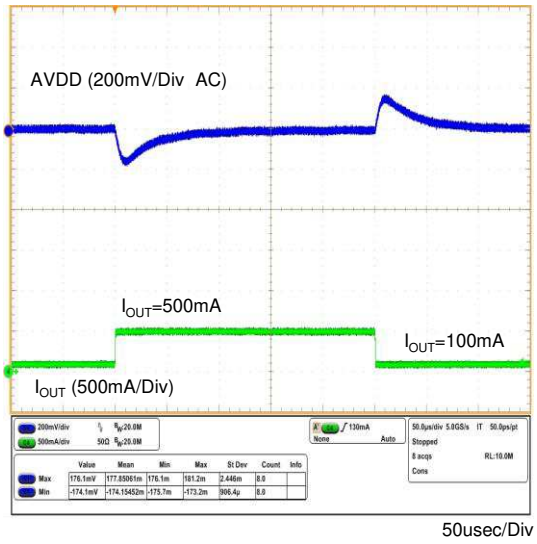


Figure 27. AVDD Load Transient

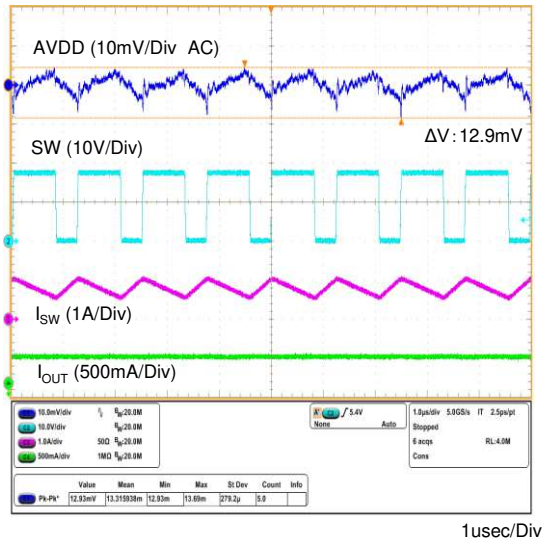


Figure 28. AVDD Switching (Output Current=500mA)

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

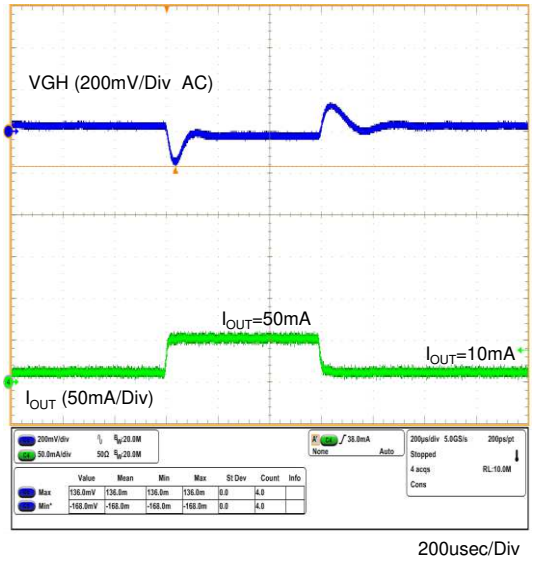


Figure 29. VGH Load Transient

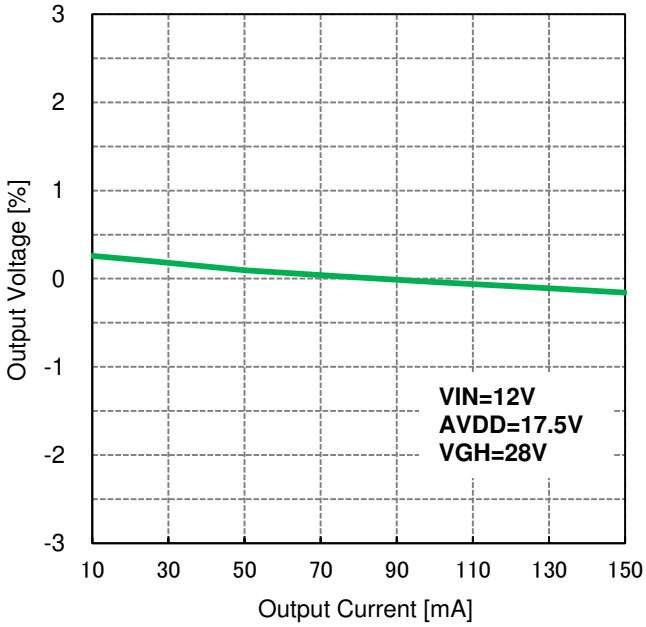


Figure 30. VGH Output Voltage vs Output Current

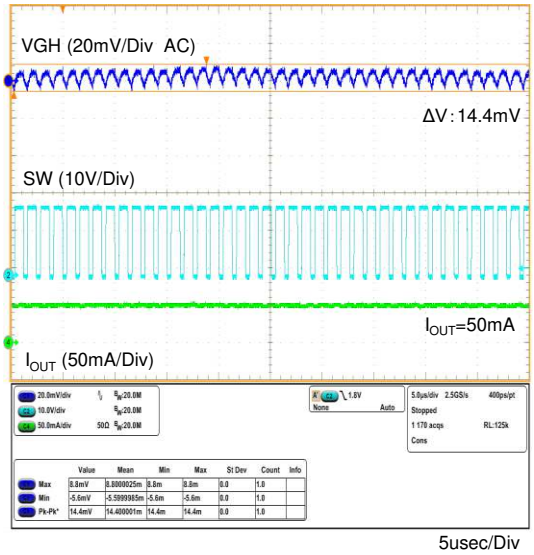


Figure 31. VGH Ripple Voltage

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

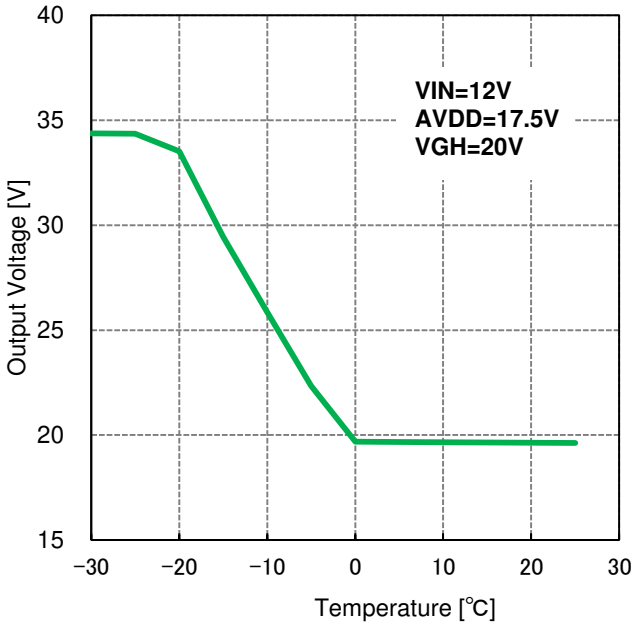
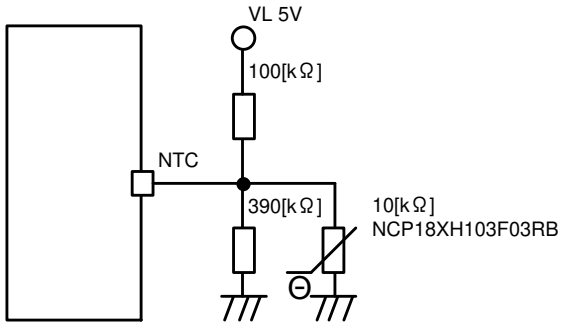


Figure 32. VGH Voltage vs Ta



Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

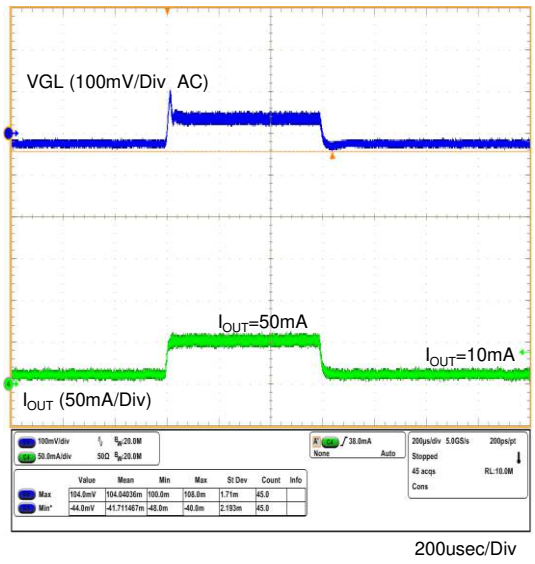


Figure 33. VGL Load Transient

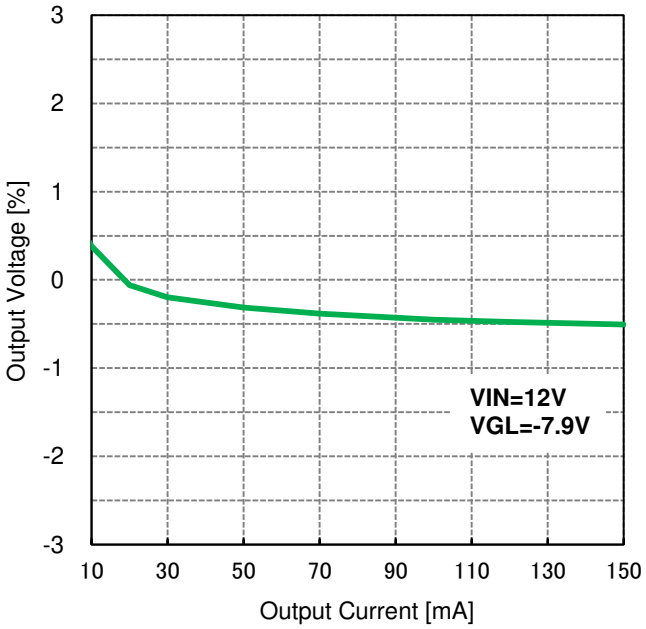


Figure 34. VGL Output Voltage vs Output Current

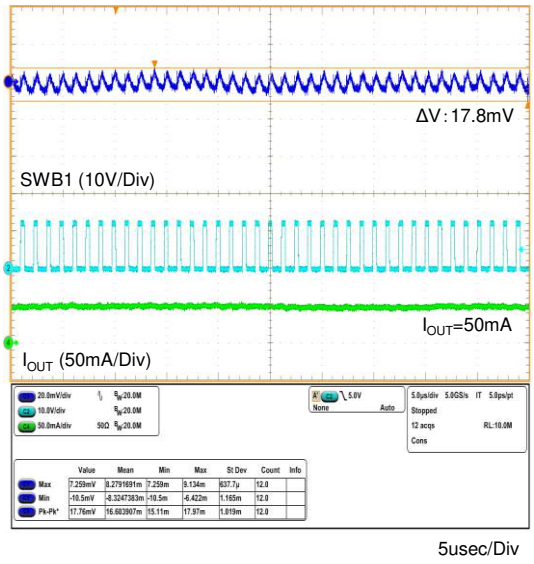


Figure 35. VGL Ripple Voltage

Typical Performance Curves (Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB3=12V, VINB2=3.3V, VIO=3.3V, VCORE=1.8V, AVDD=17.5V, HAVDD=9.0V, VGH=28V, VGL=-7.9V, RL=no load)

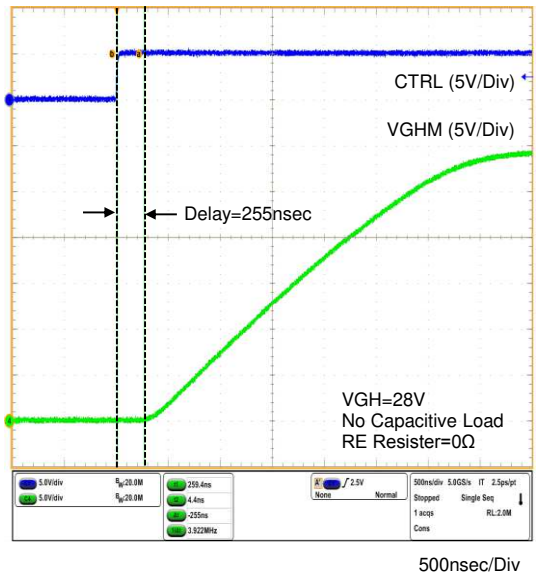


Figure 36. GPM Propagation Delay (rise)

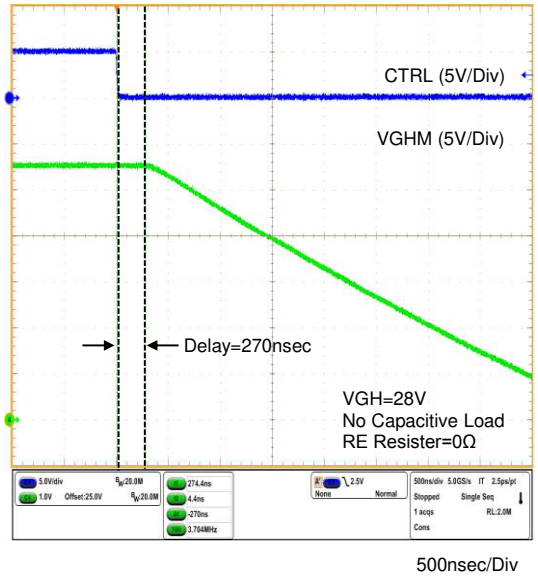


Figure 37. GPM Propagation Delay (fall)

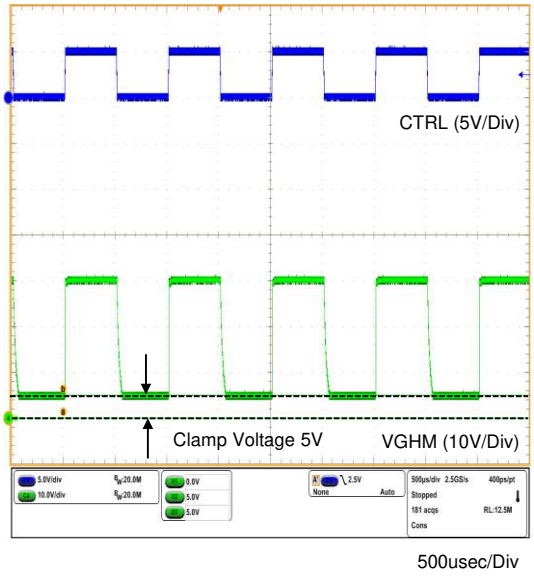


Figure 38. GPM Clamp Voltage (5V Clamp)

Timing Chart

ON and OFF Sequence of this IC are shown below.

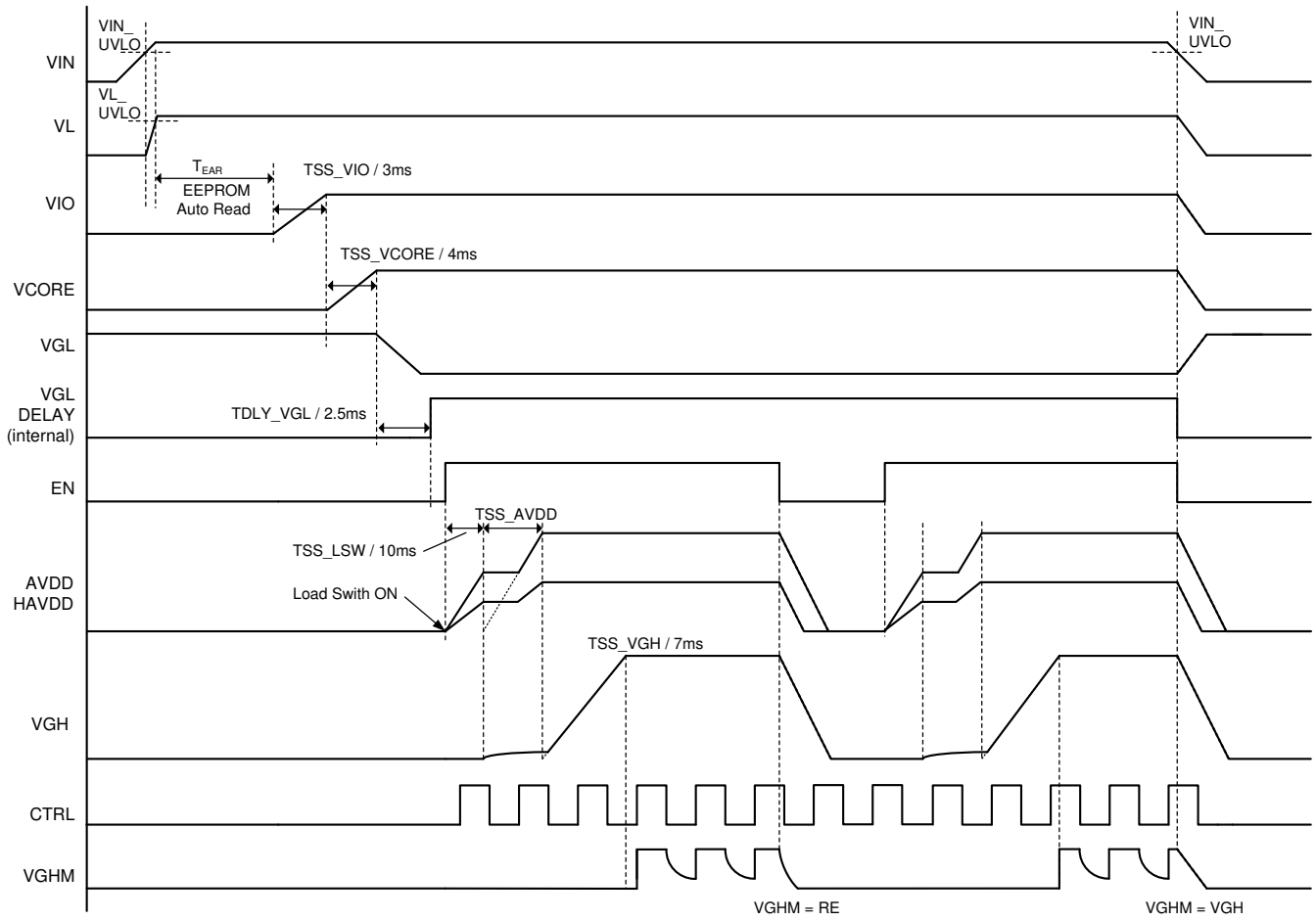


Figure 39. Timing Chart

VL activates with UVLO release of VIN.
It reads EEPROM data by Auto Read operation upon VL activation. (T_{EAR}=2msec)
After Auto Read completion, VIO activates. The Soft Start time of VIO is 3msec if the setting is 3.0V.
After VIO soft-start completion, VCORE activates. The Soft Start time of VCORE is 4msec if the setting is 2.0V.
After VCORE soft-start completion, VGL activates. The Soft Start time of VGL depends on output voltage setting, external capacitor, etc.
2.5msec after VCORE soft-start completion, Load SW turns ON (10msec) when EN=High then AVDD activates.
The Soft Start time of AVDD can be changed by register setting (10msec or 20msec).
After AVDD started, VGH activates. The Soft Start time of VGH is 7msec if the setting is 28V.
While VGH is active, CTRL rising or falling will be a trigger to activate GPM operation.
When VGHM voltage at CTRL=L reaches the GPM clamp voltage, VGHM output is high impedance.
GPM, VGH, AVDD, and HAVDD shut down when EN=Low. GPM output (VGHM) will be the same potential with RE.
All outputs shut down when a drop in VIN of UVLO is detected. VGHM will be the same potential with VGH.

Example Application（TOP VIEW, VGH Doubler）

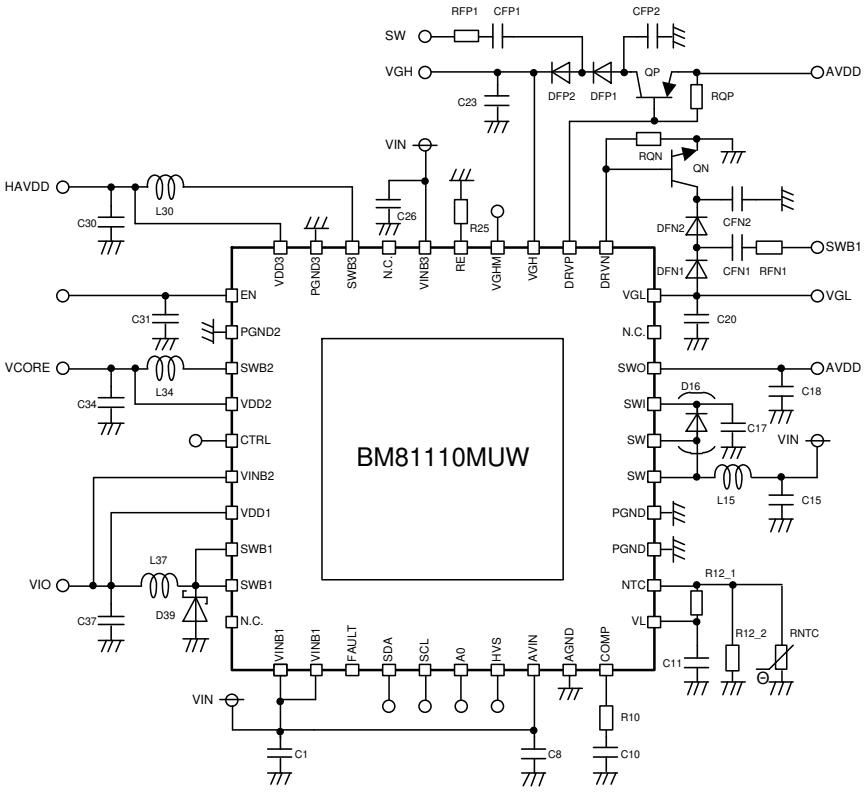


Figure 40. Example Application

Application circuit components list

Parts name	Value	Company	Parts Number	Parts name	Value	Company	Parts Number
C1	10 [uF]×2	MURATA	GRM31CB31E106KA75	RQN	100 [kΩ]	ROHM	MCR03
C8	1 [uF]	MURATA	GRM188B31E105KA75	RQP	100 [kΩ]	ROHM	MCR03
R10	75 [kΩ]	ROHM	MCR03	QP	-	ROHM	2SAR513P
C10	470 [pF]	MURATA	GRM188B11H471KA01	CFP2	470 [pF]	MURATA	GRM188B11H471KA01
C11	1 [uF]	MURATA	GRM188B31E105KA75	DFP1	-	ROHM	RB558W
R12_1	100 [kΩ]	ROHM	MCR03	DFP2			
R12_2	390 [kΩ]	ROHM	MCR03	CFP1	0.47 [uF]	MURATA	GRM188B31E474KA75
RNTC	10 [kΩ]	MURATA	NCP18XH103F03RB	RFP1	2.2 [Ω]	ROHM	MCR15
L15	10 [uH]	TAIYO YUDEN	NS10165T100MNA	C23	4.7 [uF]×2	MURATA	GRM31CB31H475KA12
C15	10 [uF]×2	MURATA	GRM31CB31E106KA75	R25	300 [Ω]	ROHM	MCR03
D16	-	ROHM	RB080L-30TE25	C26	10 [uF]	MURATA	GRM31CB31E106KA75
C17	10 [uF]×2	MURATA	GRM31CB31E106KA75	L30	10[uH]	TAIYO YUDEN	NRS8040T100M
C18	10 [uF]×4	MURATA	GRM31CB31E106KA75	C30	10 [uF]×2	MURATA	GRM31CB31E106KA75
C20	4.7 [uF]×2	MURATA	GRM219B31C475KE15	C31	0.1 [uF]	MURATA	GRM152B30J104KE19
DFN1	-	ROHM	RB558W	L34	10[uH]	TAIYO YUDEN	NRS8040T100M
DFN2				C34	10 [uF]×2	MURATA	GRM21BB31A106KE18
CFN1	0.47 [uF]	MURATA	GRM188B31E474KA75	L37	10[uH]	TAIYO YUDEN	NRS8040T100M
RFN1	2.2 [Ω]	ROHM	MCR15	C37	10 [uF]×3	MURATA	GRM21BB31A106KE18
CFN2	0.22 [uF]	MURATA	GRM188B31E224KA87	D39	-	ROHM	RSX301L-30
QN	-	ROHM	2SCR513P				

Example Application（TOP VIEW, VGH Trippler）

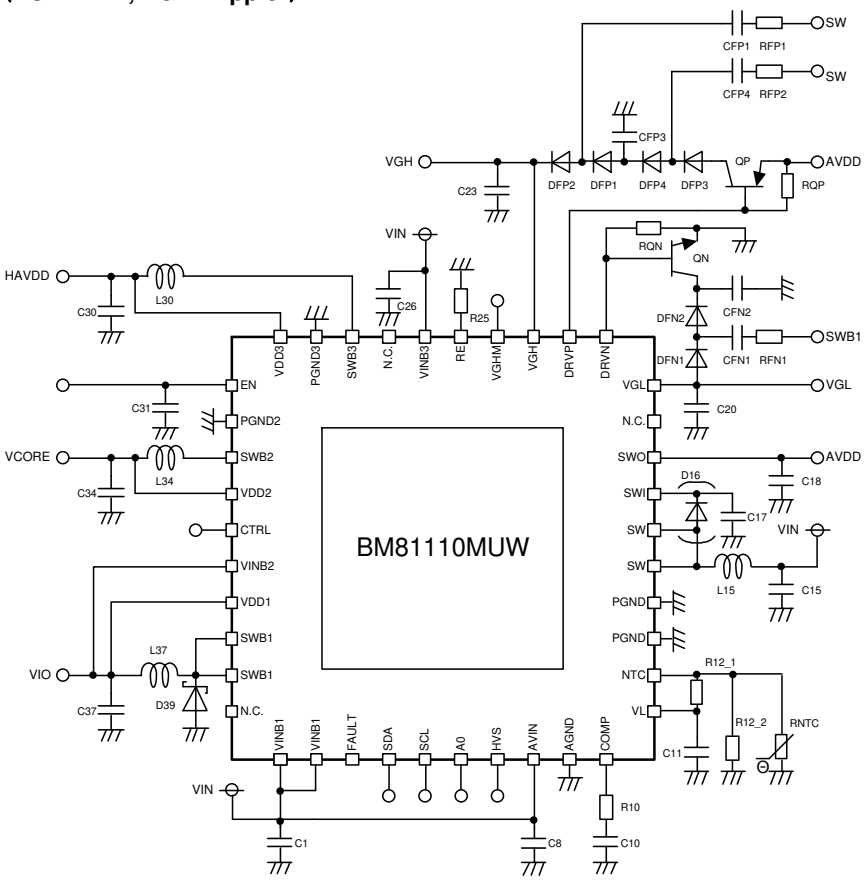


Figure 41. Example Application

Application circuit components list

Parts name	Value	Company	Parts Number	Parts name	Value	Company	Parts Number
C1	10 [uF]×2	MURATA	GRM31CB31E106KA75	QP	-	ROHM	2SAR513P
C8	1 [uF]	MURATA	GRM188B31E105KA75	CFP1	0.1 [uF]	MURATA	GRM188B31E104KA75
R10	75 [kΩ]	ROHM	MCR03	RFP1	2.2 [Ω]	ROHM	MCR15
C10	470 [pF]	MURATA	GRM188B11H471KA01	DFP1	-	ROHM	RB558W
C11	1 [uF]	MURATA	GRM188B31E105KA75	DFP2			
R12_1	100 [kΩ]	ROHM	MCR03	DFP3	-	ROHM	RB558W
R12_2	390 [kΩ]	ROHM	MCR03	DFP4			
RNTC	10 [kΩ]	MURATA	NCP18XH103F03RB	CFP3	1[uF]	MURATA	GRM21BB31H105KA12
L15	10 [uH]	TAIYO YUDEN	NS10165T100MNA	RFP2	2.2 [Ω]	ROHM	MCR15
C15	10 [uF]×2	MURATA	GRM31CB31E106KA75	CFP4	0.1 [uF]	MURATA	GRM188B31E104KA75
D16	-	ROHM	RB080L-30TE25	C23	4.7 [uF]×2	MURATA	GRM31CB31H475KA12
C17	10 [uF]×2	MURATA	GRM31CB31E106KA75	R25	300 [Ω]	ROHM	MCR03
C18	10 [uF]×4	MURATA	GRM31CB31E106KA75	C26	10 [uF]	MURATA	GRM31CB31E106KA75
C20	4.7 [uF]×2	MURATA	GRM219B31C475KE15	L30	10[uH]	TAIYO YUDEN	NRS8040T100M
DFN1	-	ROHM	RB558W	C30	10 [uF]×2	MURATA	GRM31CB31E106KA75
DFN2				C31	0.1 [uF]	MURATA	GRM152B30J104KE19
CFN1	0.47 [uF]	MURATA	GRM188B31E474KA75	L34	10[uH]	TAIYO YUDEN	NRS8040T100M
RFN1	2.2 [Ω]	ROHM	MCR15	C34	10 [uF]×2	MURATA	GRM21BB31A106KE18
CFN2	0.22 [uF]	MURATA	GRM188B31E224KA87	L37	10[uH]	TAIYO YUDEN	NRS8040T100M
QN	-	ROHM	2SCR513P	C37	10 [uF]×3	MURATA	GRM21BB31A106KE18
RQN	100 [kΩ]	ROHM	MCR03	D39	-	ROHM	RSX301L-30
RQP	100 [kΩ]	ROHM	MCR03				

Protection function explanation of each block

1. BUCK CONVERTER BLOCK 1 (VIO)

1-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or other components from malfunctioning due to rising VIO voltage.
Voltage inputted to VDD1 pin is monitored and if VIO voltage reaches VIO>110%(Typ), it is judged as unusual condition thus OVP function is operated. If OVP is detected, switching is stopped until OVP release voltage (100%, Typ) falls to VIO voltage. After OVP is released, switching is re-started.

1-2. Over Current Protection (OCP)

If excessive load current (SWB1 peak current>3.5A, Typ) is present, it limits current to flow to built–in Power MOS by controlling Switching.

1-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built-in.
When the unusual condition (VIO<80%) is detected, SWB1 frequency is divided into 1/4 and UVP timer starts.
If the unusual condition continues up to 10msec (Typ), all output will be latched in shutdown state. Power reset is needed to remove the latch state and to re-start.

2. BUCK CONVERTER BLOCK 2 (VCORE)

2-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or others components from malfunctioning due to rising VCORE voltage.
Voltage inputted to VDD2 pin is monitored and if VCORE voltage reaches VCORE>110%(Typ), it is judged as unusual condition thus OVP function is operated. If OVP is detected, switching is stopped until OVP release voltage (100%, Typ) falls to VCORE voltage. After OVP is released, switching is re-started.

2-2. Over Current Protection (OCP)

If excessive load current (SWB2 peak current>3.0A, Typ) is present, it limits current to flow to built–in Power MOS by controlling Switching.

2-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built-in.
When the unusual condition (VCORE<80%) is detected, SWB2 frequency is divided into 1/4 and UVP timer starts.
If the unusual condition continues upto 10msec (Typ), all output will be latched in shutdown state. Power reset is needed to remove the latch state and to re-start.

3. VGL REGULATOR BLOCK

3-1. Over Current Protection (OCP)

If excessive load current (I_DRVN>5mA, min.) is present, It controls source current (Base current of NPN Tr) of DRVN.

3-2. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built-in.
When unusual condition is detected (VGL>80%), the UVP time counter starts. If the unusual condition continues up to 10msec (Typ), all output is latched in shut-down condition. Power reset is needed to cancel the latch state and to re-start.

4. BOOST CONVERTER BLOCK (AVDD)

4-1. Over Voltage Protection (OVP)

OVP function is built in to prevent IC or other components from malfunctioning due to excessive rise in AVDD voltage.
The voltage inputted to SWO pin is being monitored. If the SWO pin voltage becomes 21.5V(Typ), OVP is detected. Once OVP is detected, switching is stopped. After AVDD voltage falls below OVP detection release voltage 20V(min.), switching is restarted.

4-2. Over Current Protection (OCP)

If excessive load current over 5A (Typ) of SW peak current is present, OCP limits current to rush to built-in Power MOS by controlling its output switching.

4-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built in.
When an unusual condition is detected (AVDD<80%), UVP timer starts. If the unusual condition continues up to 10msec(Typ), all output is latched in shut-down condition. Power reset is needed to remove the latch state and to re-start.

4-4. Load Switch Over Current Protection (LSW_OCP)

If excessive load current (7A, Typ) is present, It controls current of load switch.

5. BUCK CONVERTER BLOCK 3 (HAVDD)

5-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or other components from malfunctioning due to rising HAVDD voltage.
Voltage inputted to VDD3 pin is being monitored and if HAVDD voltage reaches HAVDD>110% (Typ), it is judged as unusual condition thus OVP function is operated. If OVP is detected, switching is stopped until OVP release voltage (100%, Typ) falls to HAVDD voltage. After OVP release, switching is re-started.

5-2. Over Current Protection (OCP)

If excessive load current (SWB3 peak current>1.5A, typ.) is present, it limits current to flow to built–in Power MOS by controlling Switching.

5-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built in.
When the unusual condition (HAVDD<80%) is detected, SWB3 frequency is divided into 1/4 and UVP timer starts.
If the unusual condition continues up to 10msec(Typ), all output will be latched in shutdown state. Power reset is needed to remove the latch state and to re-start.

6. VGH REGULATOR BLOCK

6-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or other components from malfunctioning due to VGH voltage rising.
Voltage inputted to VGH pin is being monitored and if VGH voltage reaches VGH>38V(Typ), it is judged as unusual condition so that OVP function is operated. If OVP is detected, limit DRVP current until OVP release voltage (35V, Typ) falls to VGH voltage. After OVP release, the current limiting of the DRVP pin is canceled.

6-2. Over Current Protection (OCP)

If excessive load current (I_DRVP>5mA, min.) is present, it controls sink current (Base current of PNP Tr) of DRVP.

6-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built in.
When an unusual condition is detected (VGH<80%), UVP timer starts. If the unusual condition continues up to 10msec (Typ), all output is latched in shut-down condition. Power reset is needed to remove the latch state and to re-start.

7. GENERAL

7-1. Thermal shutdown

All outputs will shut down when the IC temperature exceeds 175℃(typ.). After the temperature falls below 150℃(Typ), the operation re-starts.

7-2. VIN Under Voltage Lock Out

VIN Under Voltage Lock Out prevents the circuit malfunction below the UVLO voltage. If VIN voltage is below the UVLO voltage (8.3V / 7.55V), it enters the standby state.