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USB Type-C Power Delivery Controller

BM92A56MWV-Z

General Description

BM92A56MWV-Z is a full function USB Type-C Power Delivery (PD) controller that supports USB Power Delivery using baseband communication.
BM92A56MWV-Z includes support for the PD policy engine and communicates with an Embedded Controller or the SoC via host interface. It supports SOP, SOP' and SOP'' signaling, allowing it to communicate with cable marker ICs, support alternate modes.

Features

- USB Type-C Specification Compatible
- USB PD Specification Compatible (BMC-PHY)
- Two Power Path Control using N-ch MOSFET Drivers with Back Flow Prevention
- Type-C Cable Orientation Detection
- Built-in VCONN Switch and VCONN Controller
- Direct VBUS Powered Operation
- Supports DFP/UFP/DRP mode
- Supports Dead Battery Operation
- SMBus Interface for Host Communication
- EC-less Operation (Auto mode)

Key Specifications

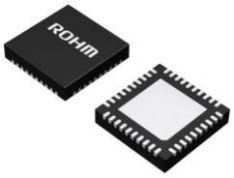
- VBUS Voltage Range: 4.75 V to 20 V
- Power Consumption at Sleep Power: 0.4 mW (Typ)
- Operating Temperature Range: -30 °C to +105 °C

Applications

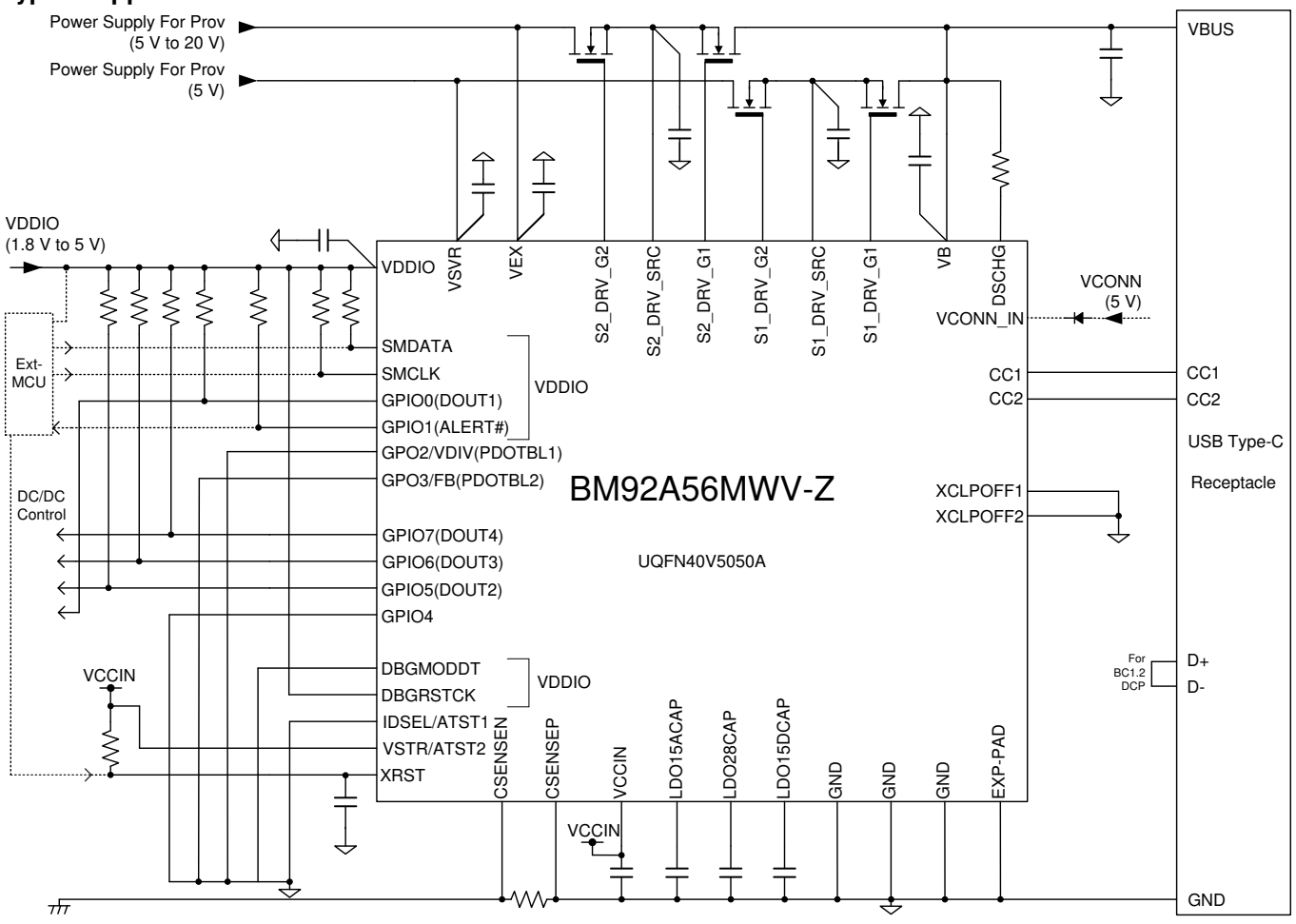
- Consumer Applications:
  Monitors, Docking Stations, TVs, STBs
  Powerbank, USB Charger

Package

Package	W(Typ) x D(Typ) x H(Max)
UQFN40V5050A	5.00 mm x 5.00 mm x 1.00 mm



Typical Application Circuit



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

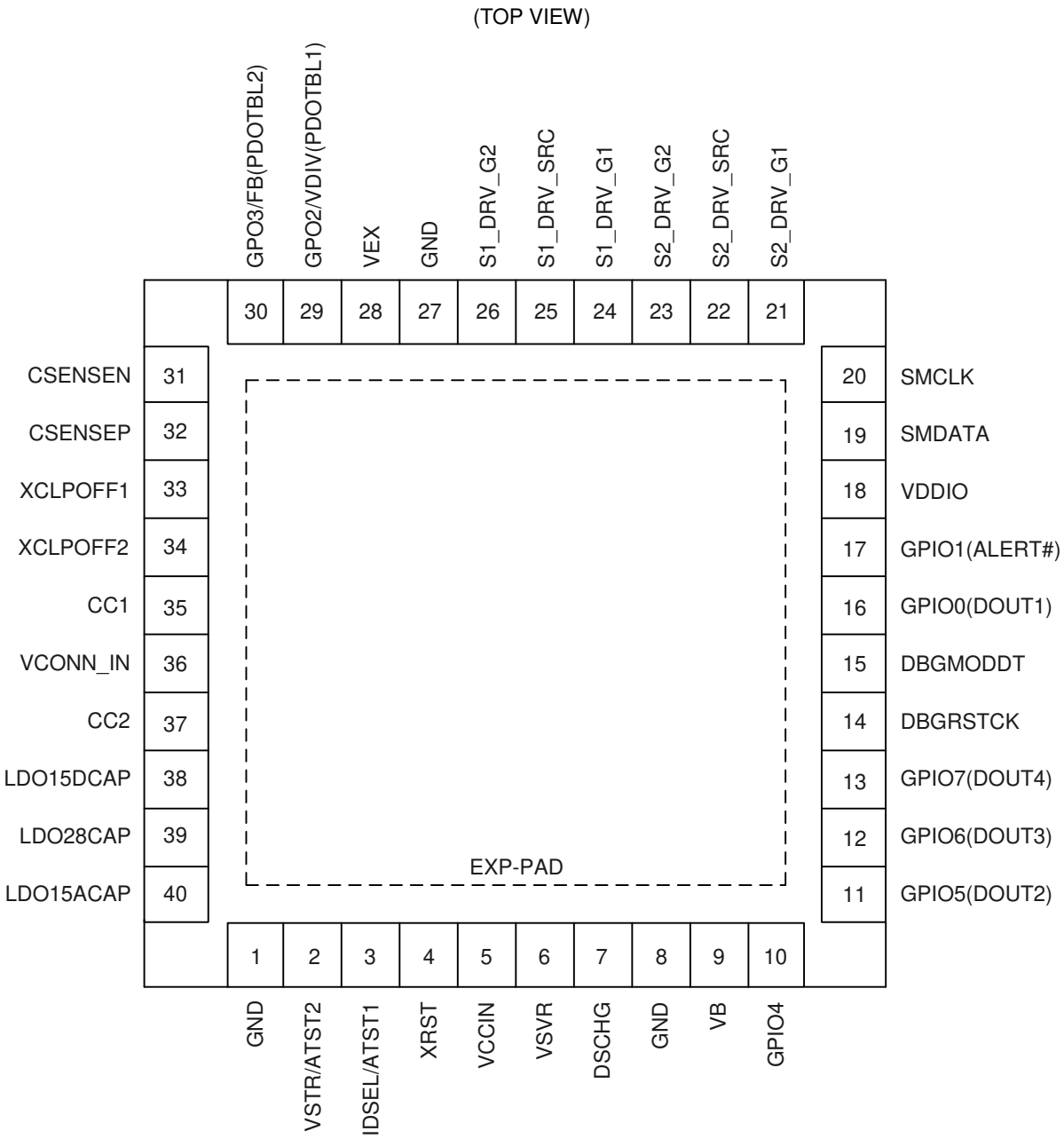
Notation

Category	Notation	Description
Unit	V	Volt (Unit of voltage)
	A	Ampere (Unit of current)
	Ω, Ohm	Ohm (Unit of resistance)
	F	Farad (Unit of capacitance)
	deg., degree	degree Celsius (Unit of temperature)
	Hz	Hertz (Unit of frequency)
	s (lower case)	second (Unit of time)
	min	minute (Unit of time)
	b, bit	bit (Unit of digital data)
	B, byte	1 byte=8 bits
Unit prefix	M, mega-, mebi-	2^{20}=1,048,576 (used with “bit” or “byte”)
	M, mega-, million-	10^{6}=1,000,000 (used with “Ω” or “Hz”)
	K, kilo-, kibi-	2^{10}=1,024 (used with “bit” or “byte”)
	k, kilo-	10^{3}=1,000 (used with “Ω” or “Hz”)
	m, milli-	10^{-3}
	µ, micro-	10^{-6}
	n, nano-	10^{-9}
	p, pico-	10^{-12}
Numeric value	xx h, xx H	Hexadecimal number. “x”: any alphanumeric of 0 to 9 or A to F.
	xx b	Binary number; “b” may be omitted. “x”: a number, 0 or 1 “_” is used as a nibble (4 bit) delimiter. (eg. “0011_0101b”=“35 h”)
Address	#xx h	Address in a hexadecimal number. “x”: any alphanumeric of 0 to 9 or A to F.
Data	bit[n]	n-th single bit in the multi-bit data.
	bit[n:m]	Bit range from bit[n] to bit[m].
Signal level	“H”, High	High level (over V_{IH} or V_{OH}) of logic signal.
	“L”, Low	Low level (under V_{IL} or V_{OL}) of logic signal.
	“Z”, “Hi-Z”	High impedance state of 3-state signal.

Reference

Name	Reference Document	Release Date	Publisher
USB Type-C	“USB Type-C Specification Release 1.1”	3.Apr.2015	USB.org
USB PD	“Power Delivery Specification Revision 2.0 Version 1.1”	7.May.2015	USB.org
SMBus	“System Management Bus (SMBus) Specification Version 2.0”	3.Aug.2000	System Management Implementers Forum

Pin Configuration



Pin Descriptions

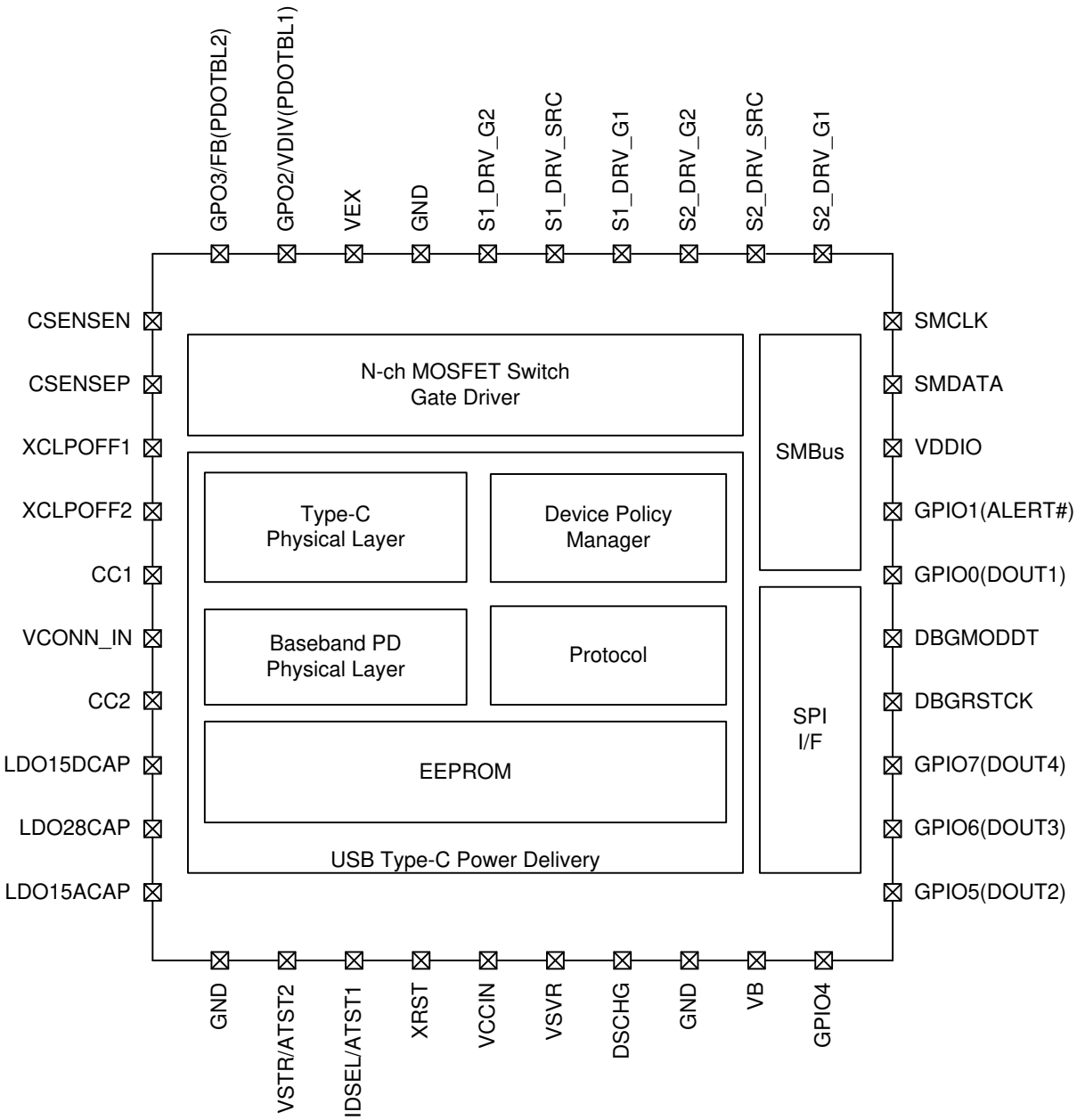
Pin No.	Pin Name	I/O	Type	Digital I/O Level	Description
1	GND	I	GND	-	Ground
2	VSTR/ATST2	IO	Analog	-	Analog test/Debug pin
3	IDSEL/ATST1	I	Analog/ Digital	VCCIN	SMBus ID (device address) selection “H”: 1A h, “L”: 18 h/Debug pin
4	XRST	I	Digital	VCCIN	Digital block reset
5	VCCIN	O	Analog	-	Internal power supply (Need capacitor)
6	VSVR	I	Power	-	Power supply from SVR (5 V)
7	DSCHG	IO	Analog	-	Discharge N-ch MOSFET drain
8	GND	I	GND	-	Ground
9	VB	I	Power	-	Power supply from VBUS
10	GPIO4	I	Digital	-	Mode fixation (Fix: L)
11	GPIO5(DOUT2)	O	Digital	-	DOUT2 signal
12	GPIO6(DOUT3)	O	Digital	-	DOUT3 signal
13	GPIO7(DOUT4)	O	Digital	-	DOUT4 signal
14	DBGRSTCK	IO	Digital	VDDIO	Test for logic
15	DBGMODDT	IO	Digital	VDDIO	Test for logic
16	GPIO0(DOUT1)	O	Digital	VDDIO	DOUT1 signal
17	GPIO1(ALERT#)	O*(Note 1)*	Digital	VDDIO	Alert signal
18	VDDIO	I	Power	-	Interface voltage
19	SMDATA	IO	Digital	VDDIO	SMBus data
20	SMCLK	I	Digital	VDDIO	SMBus clock
21	S2_DRV_G1	O	Analog	-	Power path N-ch MOSFET gate control
22	S2_DRV_SRC	I	Analog	-	Power path N-ch MOSFET BG/source
23	S2_DRV_G2	O	Analog	-	Power path N-ch MOSFET gate control
24	S1_DRV_G1	O	Analog	-	Power path N-ch MOSFET gate control
25	S1_DRV_SRC	I	Analog	-	Power path N-ch MOSFET BG/source
26	S1_DRV_G2	O	Analog	-	Power path N-ch MOSFET gate control
27	GND	I	GND	-	Ground
28	VEX	I	Power	-	Extension power input
29	GPO2/VDIV(PDOTBL1)	I	Digital	VCCIN	Select source PDO table
30	GPO3/FB(PDOTBL2)	I	Digital	VCCIN	Select source PDO table
31	CSENSEN	I	Analog	VCCIN	Current sense voltage input negative
32	CSENSEP	I	Analog	VCCIN	Current sense voltage input positive
33	XCLPOFF1	I	Analog	VCCIN	Disable clamper of CC1 (Fix: L)
34	XCLPOFF2	I	Analog	VCCIN	Disable clamper of CC2 (Fix: L)
35	CC1	IO	Analog	-	Configuration channel 1 for Type-C
36	VCONN_IN	I	Analog	-	Input power for VCONN
37	CC2	IO	Analog	-	Configuration channel 2 for Type-C
38	LDO15DCAP	O	Analog	-	Internal LDO 1.5 V for Digital (Need capacitor)
39	LDO28CAP	O	Analog	-	Internal LDO 2.8 V for Analog (Need capacitor)
40	LDO15ACAP	O	Analog	-	Internal LDO 1.5 V for Analog (Need capacitor)
-	EXP-PAD	-	-	-	The EXP-PAD connect to GND.

(Note 1) N-ch Open Drain

Block Diagram

BM92A56MWV-Z is a full function USB Type-C PD controller that supports USB Power Delivery using baseband communication. It is compatible with USB Type-C Specification and USB Power Delivery Specification.

BM92A56MWV-Z includes the following functional blocks: Type-C Physical Layer (baseband PHY), BMC encoder/decoder, USB PD Protocol engine, two N-ch MOSFET switch drivers to control each, OVP, Discharge FET and SMBus interface for communicating with the host controller. It requires an external embedded controller that includes Device Policy Manager and GPIOs for USB Type-C PD operation. BM92A56MWV-Z is able to operate independently in a dead battery condition where the embedded controller is not operational. BM92A56MWV-Z includes an EEPROM, enabling code updates via the SMBus interface during prototyping phase.



Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Supply Voltage1 (VB, VEX, DSCHG, S2_DRV_G1, S2_DRV_G2, S2_DRV_SRC, S1_DRV_G1, S1_DRV_SRC, S1_DRV_G2)	V_{IN1}	-0.3 to +28	V	*(Note 2)*
Maximum Supply Voltage2 (VDDIO, VSVR, DBGRSTCK, DBGMODDT, GPIO0, GPIO1, SMDATA, SMCLK, XRST, VCONN_IN, VSTR/ATST2, IDSEL/ATST1, VCCIN, GPIO4, GPIO5, GPIO6, GPIO7, GPO2/VDIV, GPO3/FB, CSENSEN, CSENSEP, XCLPOFF1, XCLPOFF2, CC1, CC2, LDO28CAP)	V_{IN2}	-0.3 to +6.5	V	-
Maximum Supply Voltage3 (LDO15DCAP, LDO15ACAP)	V_{IN3}	-0.3 to +2.1	V	-
Maximum Different Voltage (S2_DRV_G1 - S2_DRV_SRC, S2_DRV_G2 - S2_DRV_SRC, S1_DRV_G1 - S1_DRV_SRC, S1_DRV_G2 - S1_DRV_SRC)	V_{DIFF}	-0.3 to +6.5	V	-
Maximum Junction Temperature	Tjmax	150	°C	-
Storage Temperature Range	Tstg	-55 to +125	°C	-

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 2) The DSCHG pin connects more than 1 kΩ for current limiting.

Thermal Resistance*(Note 3)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 5)*	2s2p*(Note 6)*	
UQFN40V5050A				
Junction to Ambient	θ_{JA}	125.0	43.0	°C/W
Junction to Top Characterization Parameter*(Note 4)*	Ψ_{JT}	21	14	°C/W

(Note 3) Based on JESD51-2A(Still-Air).

(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 5) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

(Note 6) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 7)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 7) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VB, VEX Voltage	V_B, V_{EX}	4.75	-	20	V	USB VBUS voltage
VSVR Voltage	V_{SVR}	3.1	-	5.5	V	-
VDDIO Voltage	V_{DDIO}	1.7	-	5.5	V	-
VCONN_IN Input Voltage	V_{CONN}	4.75	5.0	5.5	V	-
Operating Temperature	Topr	-30	+25	+105	°C	-

Electrical Characteristics

1. Internal Memory Cell Characteristics

(V_B=V_{EX}=4.75 V to 20 V, V_{SVR}=3.1 V to 5.5 V)

Item	Limit			Unit	Conditions
	Min	Typ	Max		
Data Rewriting Number*(Note 8)*	1000	-	-	time	Ta≤25 °C
	100	-	-	time	Ta≤105 °C
Data Retention Life*(Note 8)*	20	-	-	year	Ta≤25 °C
	10	-	-	year	Ta≤105 °C

Caution : *Customer is permitted to rewrite EEPROM on BM92A56MWV-Z only in case of being provided technical support from ROHM.*
(Note 8) Not 100% tested.

2. Circuit Power Characteristics

(Ta=25 °C, V_{SVR}=V_{DDIO}=3.3 V, VB=VEX=Open)

Item	Limit			Unit	Conditions
	Min	Typ	Max		
Sleep Power	-	0.4	-	mW	*(Note 9)*
Standby Power	-	3.5	-	mW	*(Note10)*

(Note 9) Sleep power: Power consumption at unattached plug.
(Note 10) Standby power: Power consumption at attached plug.

Electrical Characteristics - continued

3. Digital Pin DC Characteristics

(Ta=25 °C, V_{SVR}=V_{DDIO}=3.3 V, VCCIN=VSVR, VB=VEX=Open)

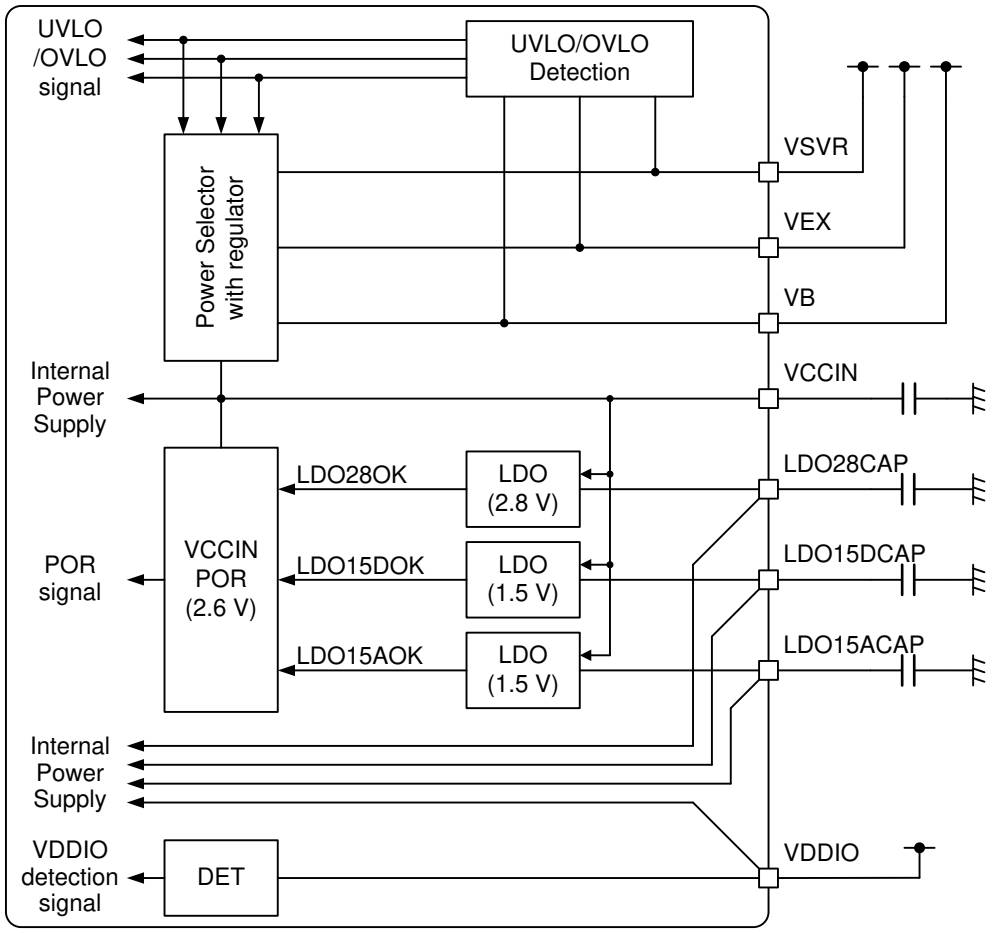
Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
VDDIO Power Pin: GPIO0, GPIO1, SMDATA, SMCLK						
Input "H" Level	V_{IH1}	0.8× V_{DDIO}	-	V_{DDIO}+ 0.3	V	-
Input "L" Level	V_{IL1}	-0.3	-	0.2× V_{DDIO}	V	-
Input Leak Current	I_{IC1}	-5	0	+5	µA	Power: VDDIO
Output Voltage when “H”	V_{OH1}	0.7× V_{DDIO}	-	-	V	Source=1 mA
SMDATA Pin "L" Level Voltage (SMDATA)	V_{OL_SMDATA}	-	-	0.4	V	Sink=350 µA Max.
Output Voltage when “L” (GPIO0, GPIO1)	V_{OL1}	-	-	0.3	V	Sink=1 mA
VCCIN Power Pin: XRST, GPO2, GPO3, GPIO4, GPIO5, GPIO6, GPIO7						
Input "H" Level	V_{IH2}	0.8× V_{CCIN}	-	V_{CCIN}+ 0.3	V	-
Input "L" Level	V_{IL2}	-0.3	-	0.2× V_{CCIN}	V	-
Input Leak Current	I_{IC2}	-5	0	+5	µA	Power: VCCIN
Output Voltage when “H” (GPIOs)	V_{OH2}	0.7× V_{CCIN}	-	-	V	Source=1 mA
Output Voltage when “L” (GPIOs)	V_{OL2}	-	-	0.3	V	Sink=1 mA

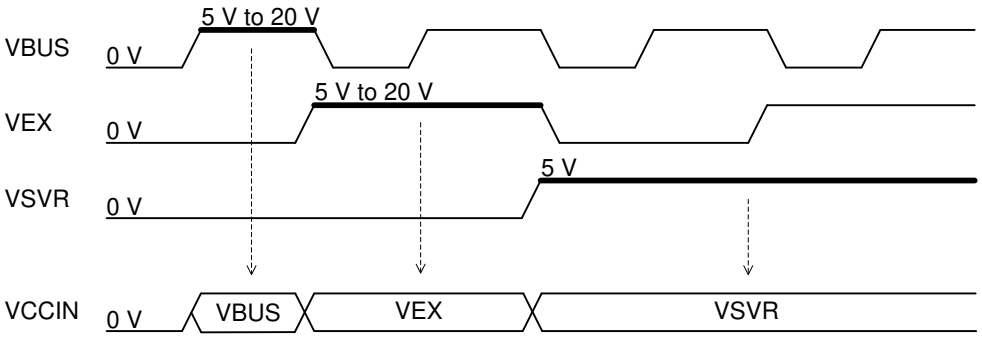
Electrical Characteristics - continued

4. Power Supply Management

BM92A56MWV-Z has a power selector. It selects the lowest power supply voltage from the VSVR, VEX or VB pins for low power consumption. Internal Power Supply (the VCCIN pin) gives priority in order of the VSVR, VEX and VB pins. The VCCIN pin supplied from the power selector is used to BM92A56MWV-Z main power source. LDOs (for internal only) are supplied from the VCCIN pin, and output each internal supply voltage.

Each power supply input has UVLO and OVLO. And POR (power on reset) signal is generated from detection of LDO28OK, LDO15DOK and LDO15AOK signals, and the VCCIN pin.





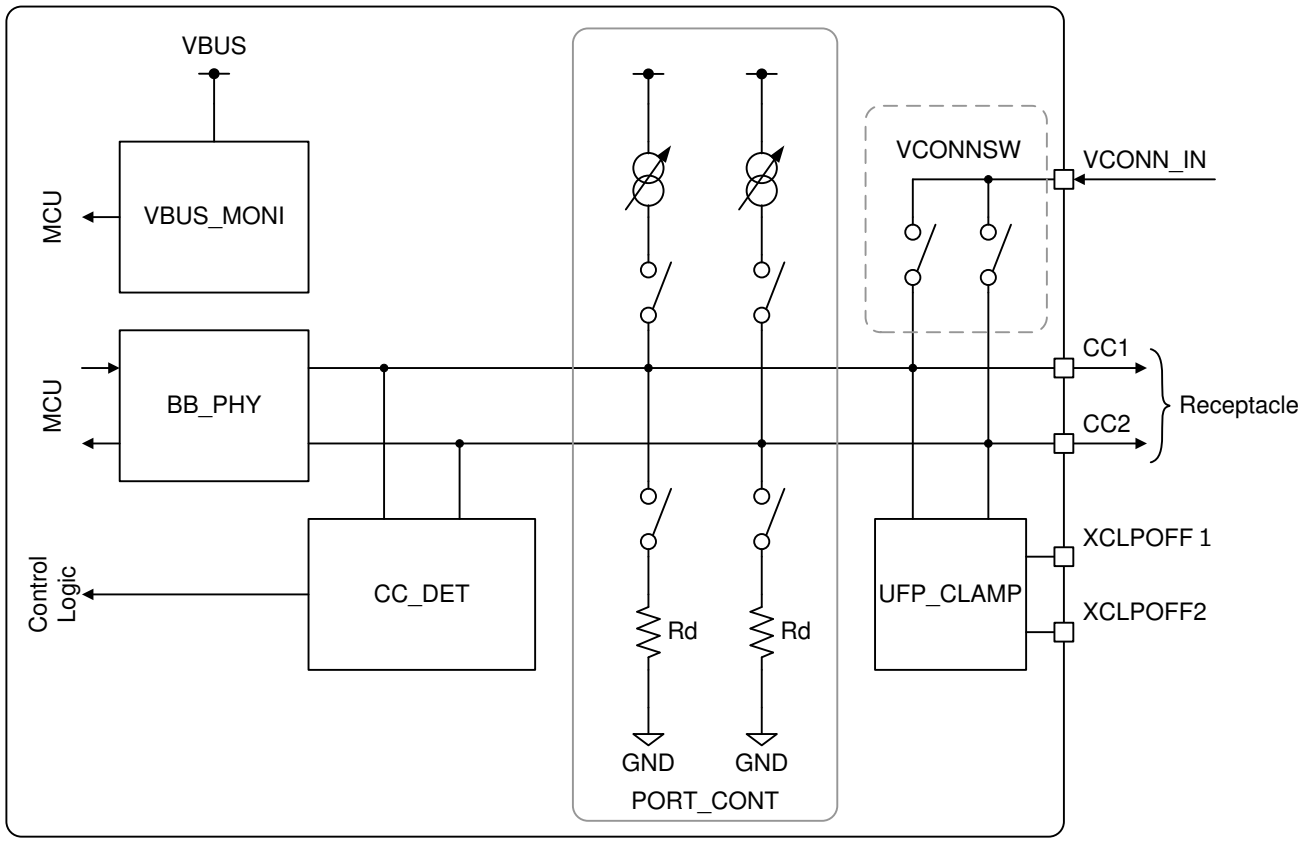
4. Power Supply Management - continued

Item	Limit			Unit	Comment
	Min	Typ	Max		
Unless otherwise specified Ta=25 °C, V_{GND}=0 V, C_{VCCIN}=4.7 µF (Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1 µF (Ceramic) Input Analog Pins: VSVR, VEX, VB					
UVLO Rising Threshold Voltage 1	-	2.8	-	V	VSVR
UVLO Rising Threshold Voltage 2	-	3.5	-	V	VEX, VB
UVLO Falling Threshold Voltage	-	2.7	-	V	VSVR, VEX, VB
OVLO Rising Threshold Voltage	-	6.4	-	V	VSVR
OVLO Rising Threshold Voltage	-	28	-	V	VEX, VB
OVLO Hysteresis Voltage 1	-	240	-	mV	VSVR
OVLO Hysteresis Voltage 2	-	920	-	mV	VEX, VB
Power ON Reset Threshold Voltage	-	2.6	-	V	VCCIN
VDDIO Detection Voltage	1.7	-	-	V	For dead battery operation
LDO28CAP Output Voltage	-	2.8	-	V	No Load, V_{SVR}=5 V
LDO15DCAP Output Voltage	-	1.5	-	V	No Load, V_{SVR}=5 V
LDO15ACAP Output Voltage	-	1.5	-	V	No Load, V_{SVR}=5 V

Electrical Characteristics - continued

5. CC_PHY

CC_PHY has below functions of USB Type-C (Refer to USB Type-C Specification):
- Defining Port Mode: DFP/UFP/DRP
- DFP-to-UFP Attach/Detach Detection
- Plug Orientation/Cable Twist Detection
- USB Type-C VBUS Voltage Detection and Usage
- VCONN (Supply for SOP') Control
- Baseband Power Delivery Communication (BBPD Communication)



PORT_CONT

This block chose the port mode according to the setting from MCU.
- DFP mode: Variable current source is connected to the CC1 and CC2 pin. These currents of each mode are Default Current, Medium Current and High Current.
- UFP mode: Pull-down resistor is connected to the CC1 and CC2 pin.
- DRP mode: Changing DFP and UFP is repeated frequently.

CC_DET

CC_DET has functions of "Attach/Detach Detection", "Plug Orientation/Cable Twist Detection", "Discovery and detect extension mode" and "USB Type-C VBUS Current Detection".

Attach/Detach is detected with monitoring voltage of the CC1 and CC2 pin. When the voltage of the CC1 and CC2 pin become under a threshold voltage at DFP, attach is detected. Oppositely, when the voltage of the CC1 and CC2 pin become over a threshold voltage, detach is detected. When the voltage of the CC1 and CC2 pin become over a threshold voltage at UFP, attach is detected.

5. CC_PHY - continued

Plug orientation and cable twist is detected from the relationship of the CC1 and CC2 pins.
UFP can detect the maximum current of the power source by monitoring the voltage of the CC1 and CC2 pin.

UFP_CLAMP

Clamp is used for UFP emulation at dead-battery condition.

VBUS_MONI

UFP detect Attach/Detach by existence of VBUS voltage. VBUSDET detects Attach when VBUS voltage over the threshold voltage. And it detects Detach when VBUS under the threshold voltage.

VCONNSW

VCONNSW is the power switch for VCONN source. It has OCP function.

BB_PHY

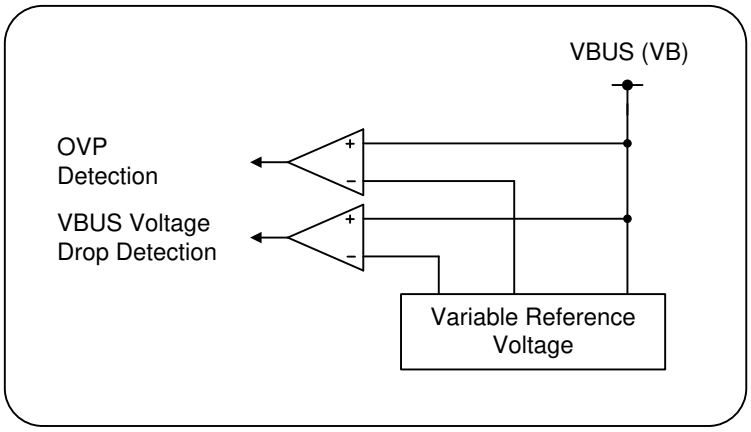
If Type-C controller supports BBPD, the CC1 and CC2 pin can output BBPD communication signal.

Item	Limit			Unit	Comment
	Min	Typ	Max		
[PORT_CONT Characteristics] Unless otherwise specified Ta=25 °C, V_{SVR}=V_B=V_{CONN_IN}=5 V, V_{DDIO}=3.3 V, V_{GND}=0 V, C_{VCCIN}=4.7 µF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1 µF(Ceramic) Input Analog Pins: CC1, CC2					
Default Current	64	80	96	µA	-
Medium Current	166	180	194	µA	-
High Current	304	330	356	µA	-
Pull Down Resistor	4.6	5.1	5.6	kΩ	-
[UFP_CLAMP Characteristics] Unless otherwise specified Ta=25 °C, V_{SVR} =V_B =V_{CONN_IN}=5 V, V_{DDIO}=3.3 V, V_{GND}=0 V, C_{VCCIN}=4.7 µF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1 µF(Ceramic) Input Analog Pins: CC1, CC2					
CCx Pin Input Impedance	126	-	-	kΩ	-
CCx Clamp Voltage	0.7	-	1.3	V	Pull up=64 µA to 356 µA
[VBUS_MONI] Unless otherwise specified Ta=25 °C, V_{SVR}=V_{CONN_IN}=5 V, V_{DDIO}=3.3 V, V_{GND}=0 V, C_{VCCIN}=4.7 µF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1 µF(Ceramic) Input Analog Pin: VB					
VBUS Presence Detection Level	-	3.42	-	V	-
[VCONNSW] Unless otherwise specified Ta=25 °C, V_{SVR}=V_B=V_{CONN_IN}=5 V, V_{DDIO}=3.3 V, V_{GND}=0 V, C_{VCCIN}=4.7 µF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1 µF(Ceramic) Input Analog Pins: CC1, CC2, VCONN_IN					
VCONN_IN to CCx Resistance	-	-	500	mΩ	-
Overcurrent Protection Level	1.1	-	-	A	-

Electrical Characteristics - continued

6. Voltage Detection

VDET Block detects the voltage level of VB. It can detect follow conditions:
OVP (Over Voltage Protection) Detection
VBUS Voltage Drop Detection

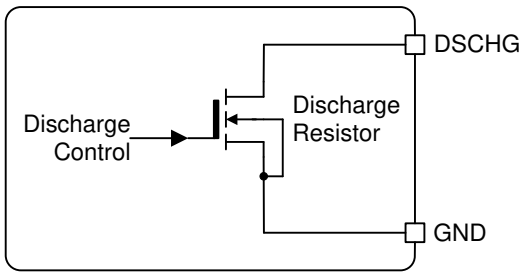


Item	Limit			Unit	Comment
	Min	Typ	Max		
Unless otherwise specified Ta=25 °C, V_{SVR}=V_{CONN_IN}=5 V, V_{DDIO}=3.3 V, V_{GND}=0 V, C_{VCCIN}=4.7 µF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1 µF(Ceramic) Input Analog Pin: VB					
Over Voltage Protection Detection Rate	+15	+20	+25	%	*(Note 11)*
VBUS Voltage Drop Detection Rate	-30	-25	-20	%	*(Note 11)*

(Note 11) Reference value is USB PD negotiation voltage.

7. VBUS Discharge

FET switch is prepared for VBUS discharging.

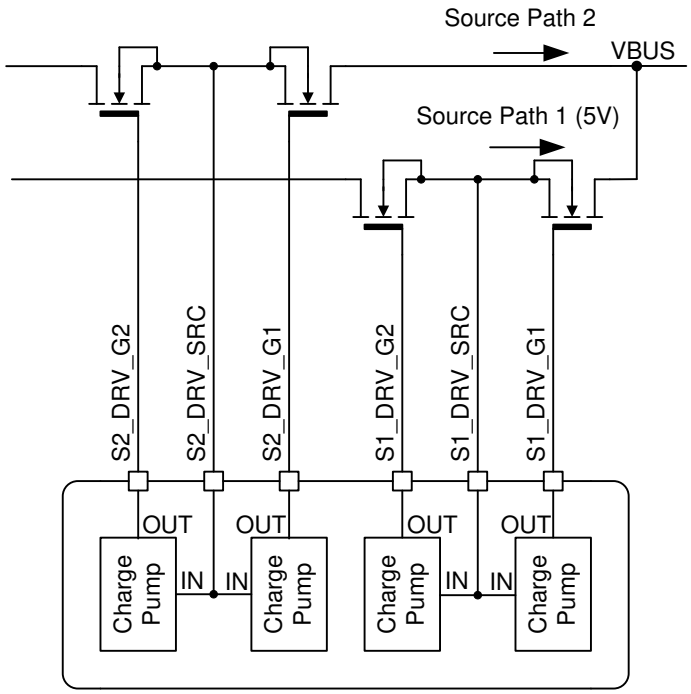


Item	Limit			Unit	Comment
	Min	Typ	Max		
Unless otherwise specified Ta=25 °C, V_{SVR}=V_B=V_{CONN_IN}=5 V, V_{DDIO}=3.3 V, V_{GND}=0 V, C_{VCCIN}=4.7 µF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1 µF(Ceramic) Input Analog Pin: DSCHG					
FET Switch ON Resistance	-	25	-	Ω	-

Electrical Characteristics - continued

8. Power FET Gate Driver

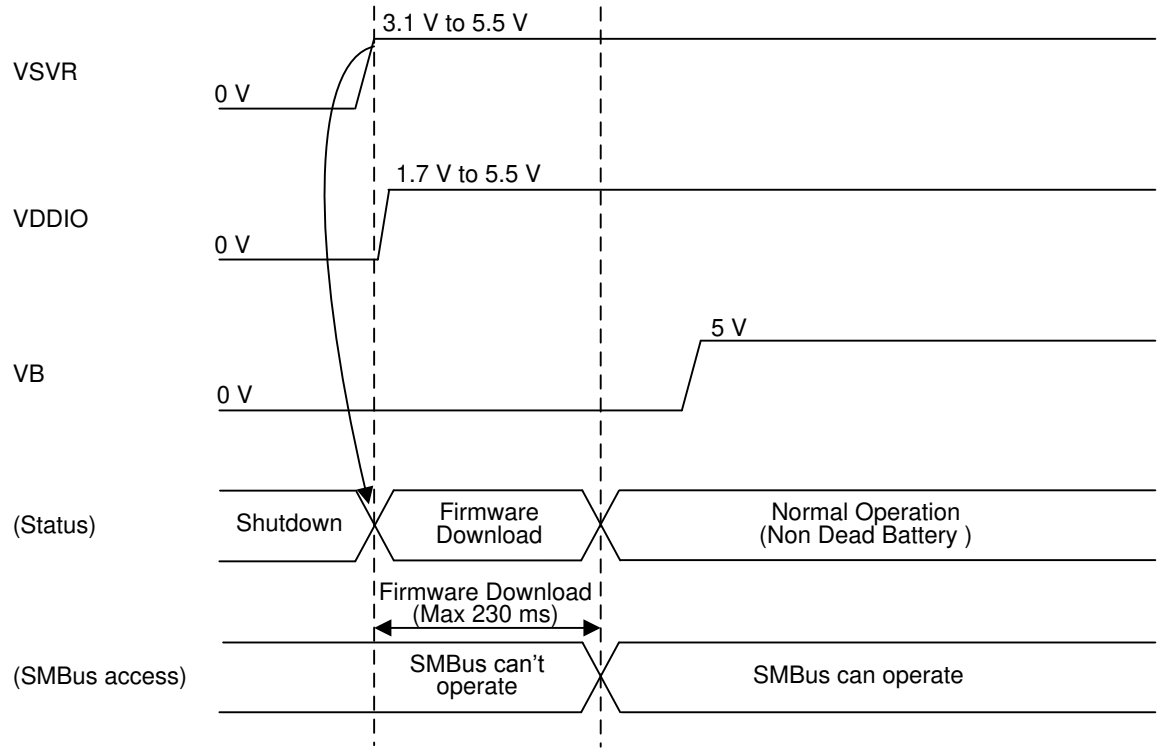
FET Gate Driver is the external N-ch MOSFET switch driver for power line switch.



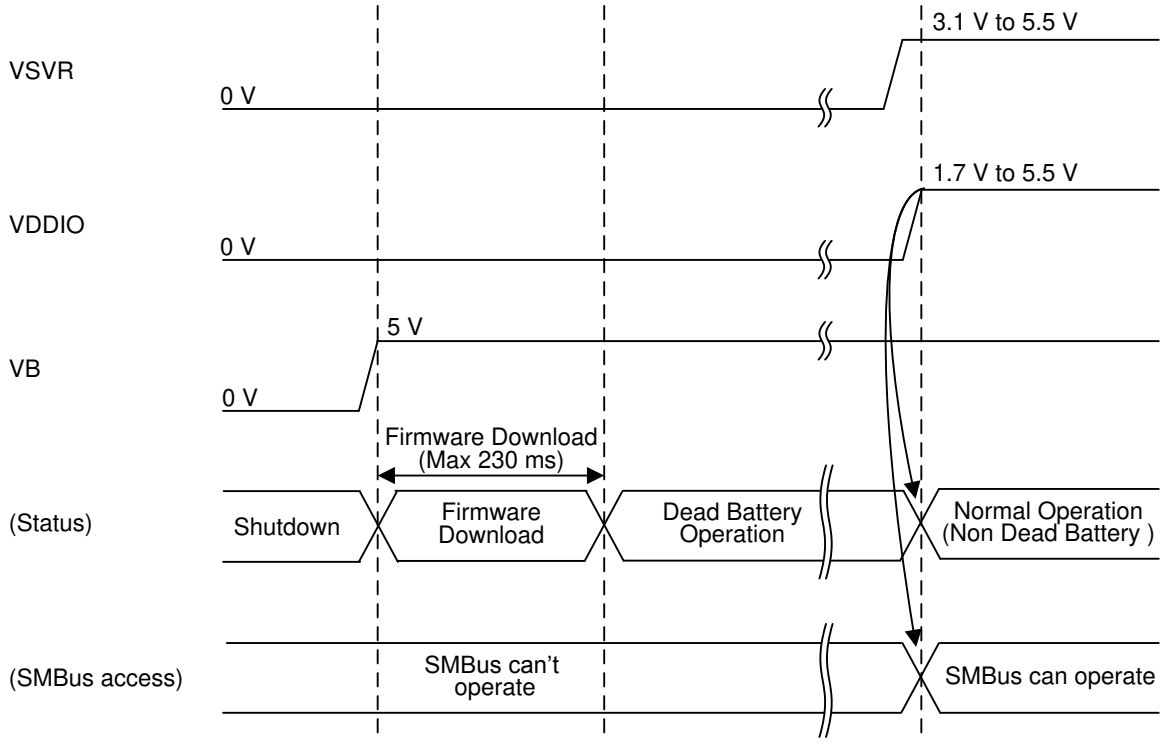
Item	Limit			Unit	Comment
	Min	Typ	Max		
Unless otherwise specified Ta=25 °C, V_{SVR}=V_B=V_{CONN_IN}=5 V, V_{DDIO}=3.3 V, V_{GND}=0 V, C_{VCCIN}=4.7 µF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1 µF(Ceramic) Input Analog Pins: S1_DRV_SRC=S2_DRV_SRC=0 V Output Analog Pins: S1_DRV_G1, S1_DRV_G2, S2_DRV_G1, S2_DRV_G2					
N-ch MOSFET Control Voltage Between Gate and Source	-	6.0	-	V	S1_DRV_G1 - S1_DRV_SRC S1_DRV_G2 - S1_DRV_SRC S2_DRV_G1 - S2_DRV_SRC S2_DRV_G2 - S2_DRV_SRC

Timing Chart

1. Power On Sequence (Non Dead Battery Operation)

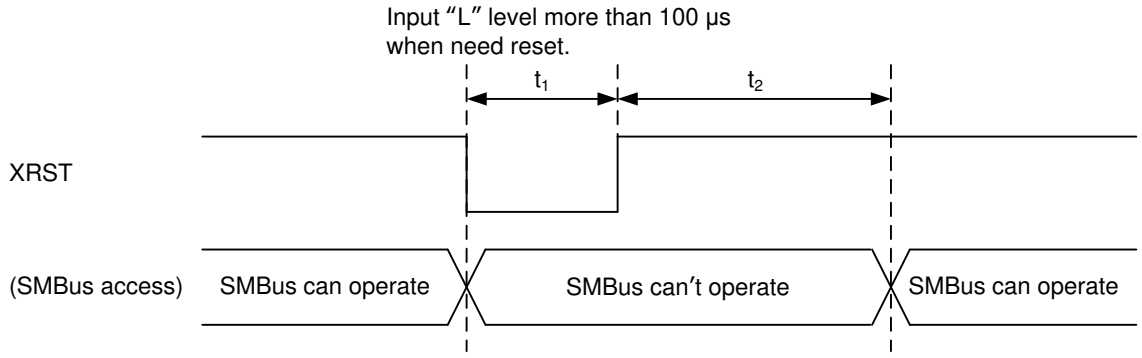


2. Power On Sequence (Dead Battery Operation)



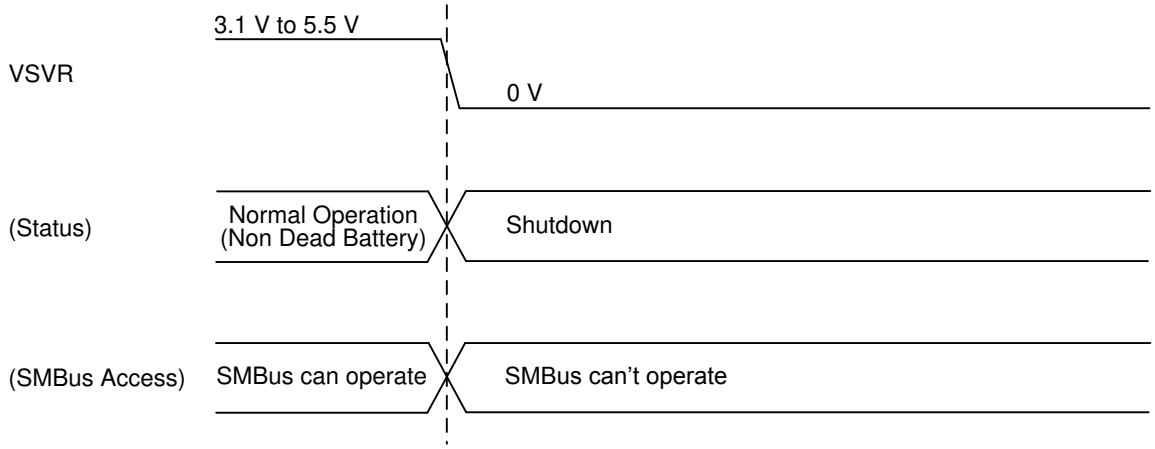
Timing Chart - continued

3. Reset Timing

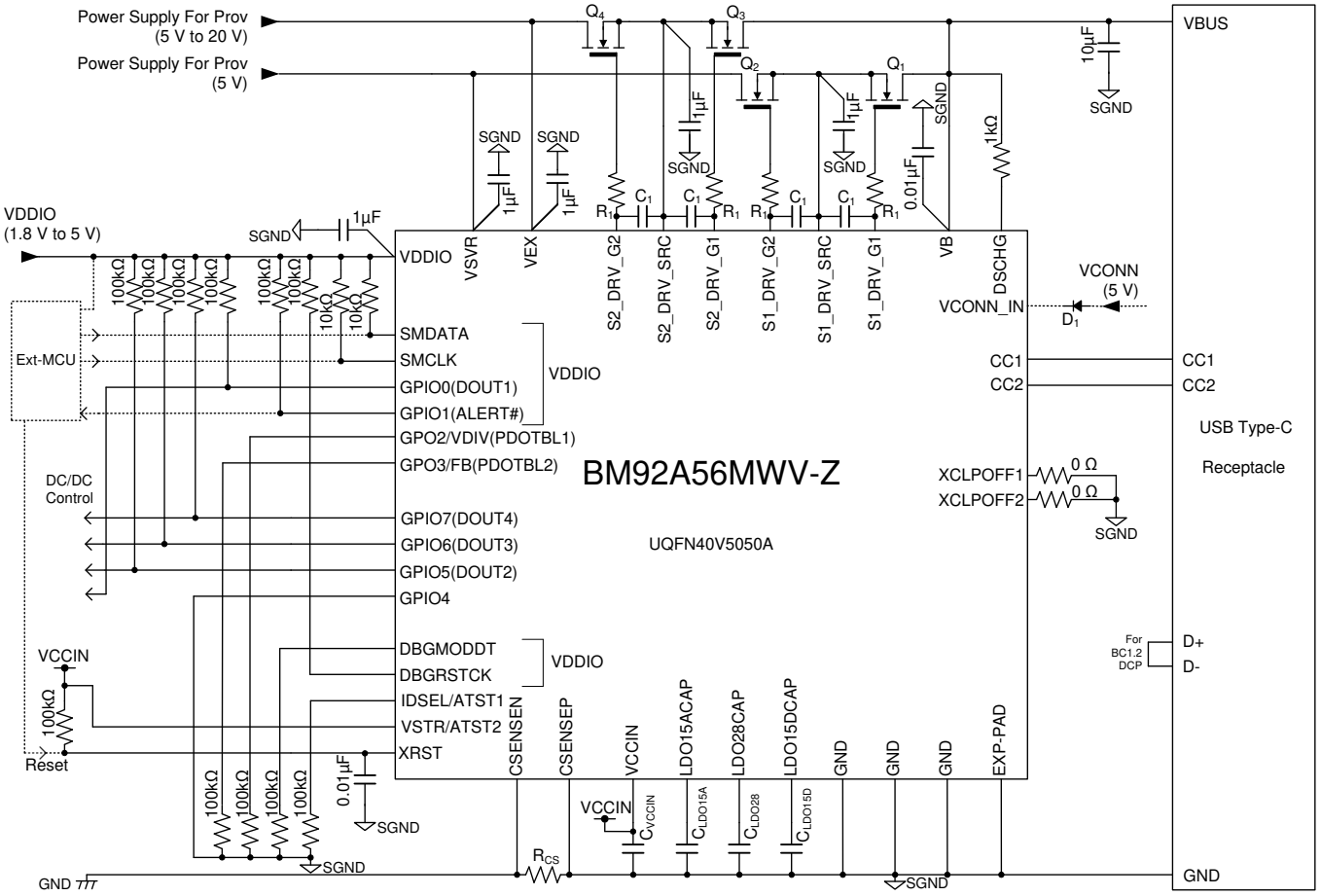


Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
XRST Minimum "L" Level Pulse	t_1	100	-	-	µs	-
SMBus Access Start After XRST Release	t_2	230	-	-	ms	-

4. Power Off Sequence



Application Example

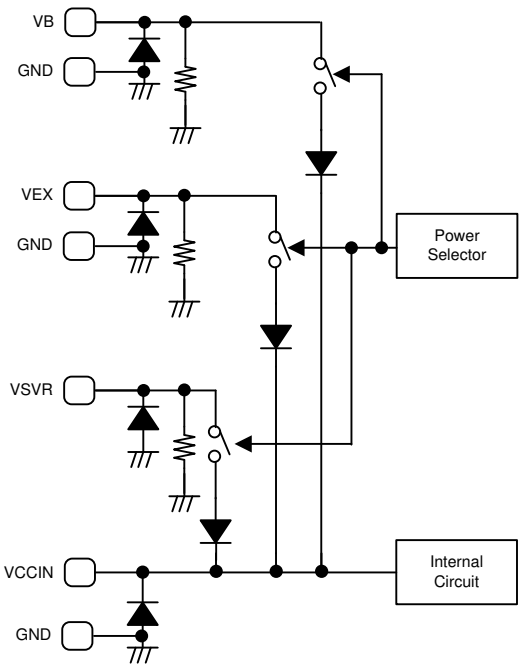
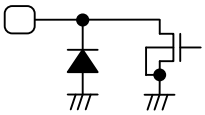
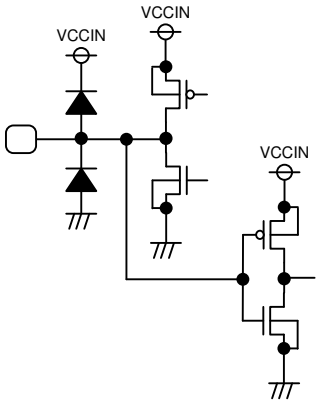
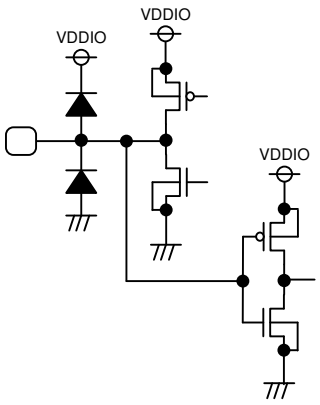


Selection of Components Externally Connected

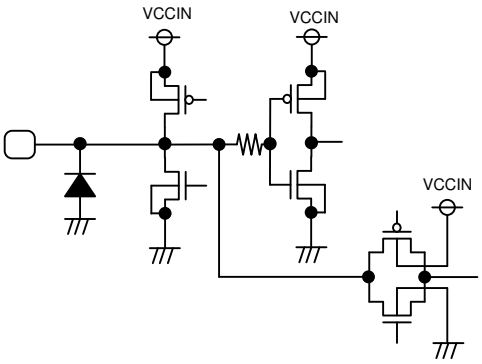
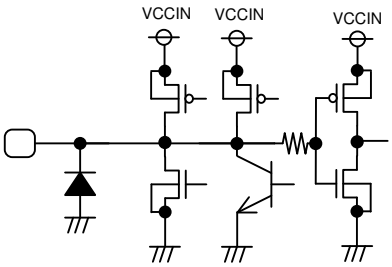
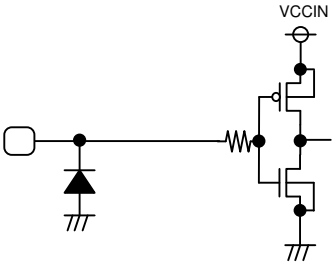
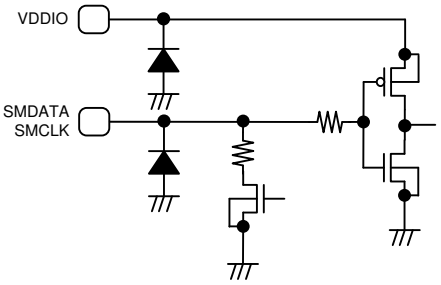
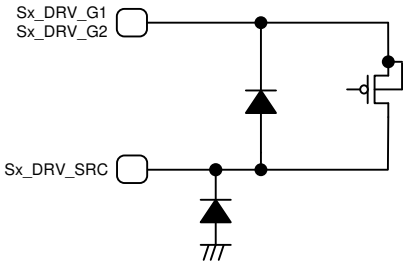
Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
VCCIN Capacitance	C_{VCCIN}	0.60	4.7	10	µF	*(Note 12)*
LDO15ACAP Capacitance	C_{LDO15A}	0.47	1.0	2.2	µF	*(Note 12)*
LDO15DCAP Capacitance	C_{LDO15D}	0.47	1.0	2.2	µF	*(Note 12)*
LDO28CAP Capacitance	C_{LDO28}	0.47	1.0	2.2	µF	*(Note 12)*
Q_1, Q_2, Q_3, Q_4 Gate-Source Capacitance	C_{Qx_gs}	470 p	-	0.5 µ	F	-
Phase Compensation Capacitance	C_1	470 p	-	0.5 µ	F	*(Note 12)* In the case of not R_1=0 Ω, C_1 is this range.
	C_1+C_{Qx_gs}	470 p	-	0.5 µ	F	*(Note 12)* In the case of R_1=0 Ω, C_1+C_{Qx_gs} is this range.
Resistance for the VBUS Setup Timing	R_1	-	-	-	Ω	-
Current Sensing Resistor for OCP	R_{CS}	-	10	-	mΩ	-

(Note 12) Use the ceramic capacitor which capacitance value to decrease by temperature characteristics and DC bias is larger than the minimum limit.

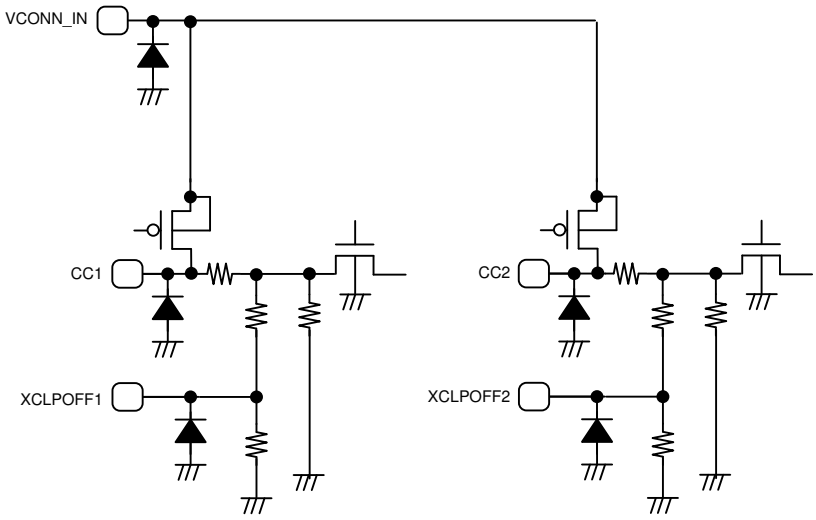
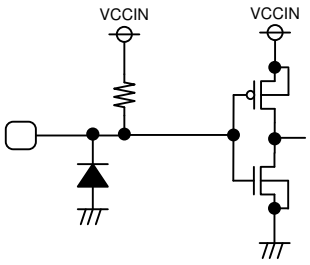
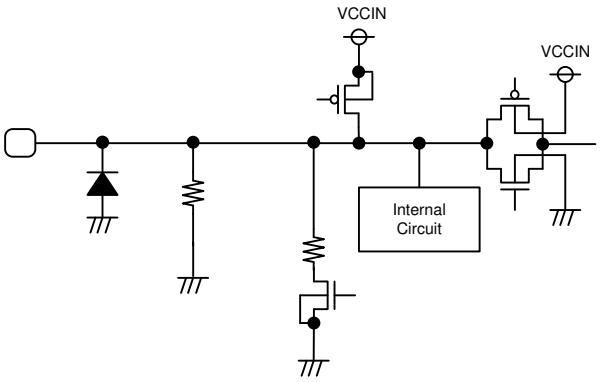
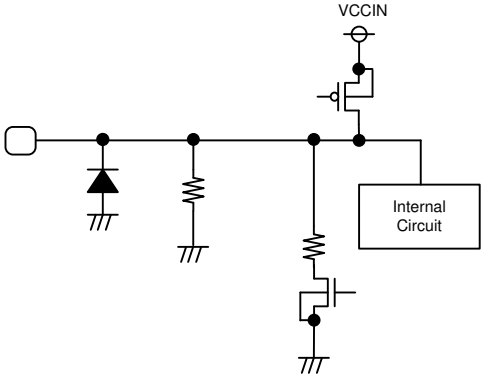
I/O Equivalence Circuit

Pin No.	Pin Name	Equivalent Circuit Diagram
1 5 6 8 9 27 28	GND VCCIN VSVR GND VB GND VEX	
7	DSCHG	
10 11 12 13	GPIO4 GPIO5(DOUT2) GPIO6(DOUT3) GPIO7(DOUT4)	
14 15 16 17	DBGRSTCK DBGMODDT GPIO0(DOUT1) GPIO1(ALERT#)	

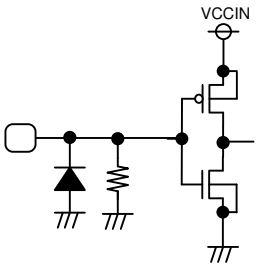
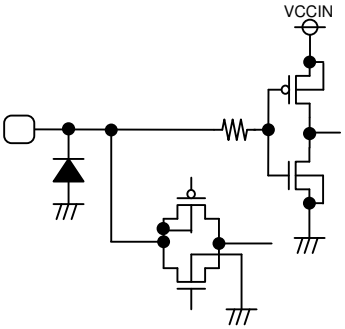
I/O Equivalence Circuit - continued

Pin No.	Pin Name	Equivalent Circuit Diagram
29	GPO2/VDIV(PDOTBL1)	
30	GPO3/FB(PDOTBL2)	
31 32	CSENSEN CSENSEP	
18 19 20	VDDIO SMDATA SMCLK	
21 22 23 24 25 26	S2_DRV_G1 S2_DRV_SRC S2_DRV_G2 S1_DRV_G1 S1_DRV_SRC S1_DRV_G2	

I/O Equivalence Circuit - continued

Pin No.	Pin Name	Equivalent Circuit Diagram
33 34 35 36 37	XCLPOFF1 XCLPOFF2 CC1 VCONN_IN CC2	
4	XRST	
38 40	LDO15DCAP LDO15ACAP	
39	LDO28CAP	

I/O Equivalence Circuit - continued

Pin No.	Pin Name	Equivalent Circuit Diagram
2	VSTR/ATST2	
3	IDSEL/ATST1	

Register Initial Values of BM92A56MWV-Z

Firmware Information

Code	Command	Protocols	Data Size	Initial Values
4B h	Firmware Type (Vendor Specific)	Read Word	2	0605 h
4C h	Firmware Revision (Vendor Specific)	Read Word	2	15AA h

PDO Settings

PDOTBL1	PDOTBL2	PDO1	PDO2	PDO3	PDO4	PDO5	PDO6	PDO7	Watt
L	L	5 V 3 A	9 V 3 A	12 V 3 A	15 V 3 A	20 V 3 A	-	-	60 W
L	H	5 V 3 A	9 V 3 A	12 V 3 A	15 V 3 A	20 V 2.25 A	-	-	45 W
H	L	5 V 3 A	9 V 3 A	12 V 2.25 A	15 V 1.8 A	20 V 1.35 A	-	-	27 W
H	H	5 V 3 A	9 V 2 A	12 V 1.5 A	15 V 1.2 A	20 V 0.9 A	-	-	18 W

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes - continued

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. Unused Input Pins

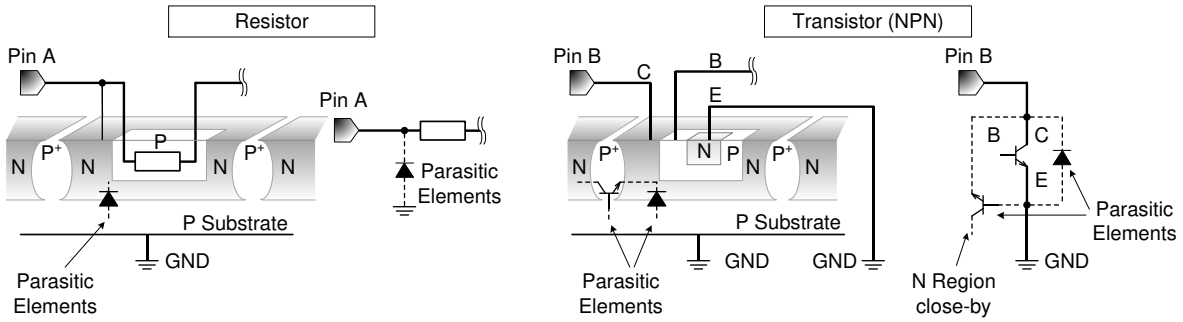
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

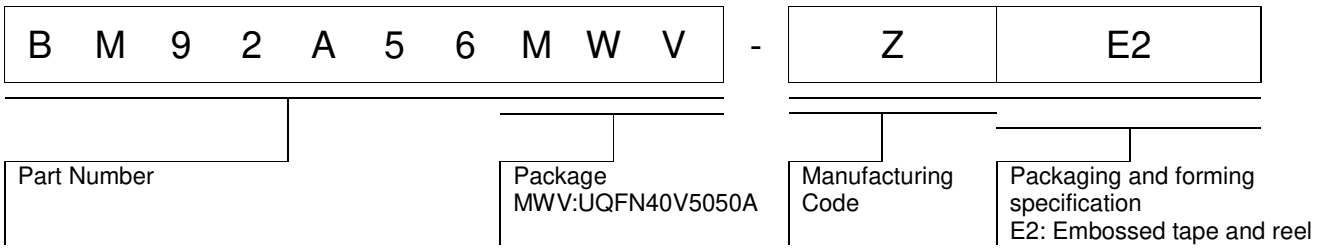
13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information



Marking Diagrams