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Type-C USB Power Delivery Controller

BM92T20MWV

General Description

BM92T20 is a full function Type-C USB-PD controller that supports USB Power Delivery using base-band communication. It is compatible with USB Type-C specification rev1.1 and USB Power Delivery specification rev2.0.

BM92T20 includes support for the PD policy engine and communicates with an Embedded Controller or the SoC via host interface. It supports SOP, SOP', SOP'' and SOP''' signaling, allowing it to communicate with cable marker ICs, support alternate modes and protocol adapters.

Features

- USB Type-C Spec 1.1 compatible
- USB PD Spec 2.0 compatible (BMC-PHY)
- Two channel power path control using N-channel MOSFET drivers with back flow prevention
- Type C cable orientation detection
- Direct VBUS powered operation
- Supports DFP mode.
- SMBus Interface for Host Communication
- EC-less Operation (Auto mode)

Applications

- Consumer Applications
  - AC Adaptors

Key Specifications

- VBUS Voltage Range: 4.75V to 20V
- Power Sink Voltage Range: 4.75V to 20V
- Power Source Voltage Range: 4.75V to 20V
- Power Consumption at Low Power: 0.4m W (Typ)
- Operating Temperature Range: -30°C to +105°C

Package

	W (Typ) x D (Typ) x H (Max)
UQFN40V5050A	5.00mm x 5.00mm x 1.00mm

Typical Application Circuit(s)

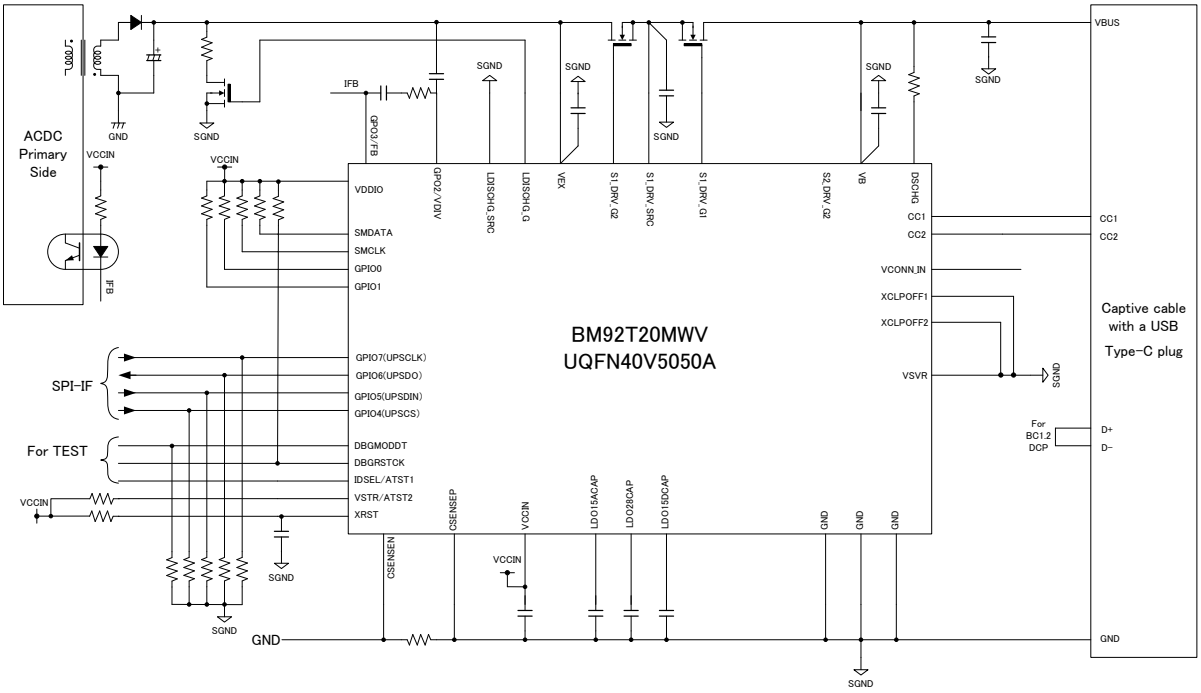


Figure A. Typical Application Circuit

Contents

Notation

Category	Notation	Description
Unit	V	Volt (Unit of voltage)
	A	Ampere (Unit of current)
	Ω, Ohm	Ohm (Unit of resistance)
	F	Farad (Unit of capacitance)
	deg., degree	degree Celsius (Unit of Temperature)
	Hz	Hertz (Unit of frequency)
	s (lower case)	second (Unit of time)
	min	minute (Unit of time)
	b, bit	bit (Unit of digital data)
	B, byte	1 byte = 8 bits
Unit prefix	M, mega-, mebi-	2^{20} = 1,048,576 (used with “bit” or “byte”)
	M, mega-, million-	10^{6} = 1,000,000 (used with “Ω” or “Hz”)
	K, kilo-, kibi-	2^{10} = 1,024 (used with “bit” or “byte”)
	k, kilo-	10^{3} = 1,000 (used with “Ω” or “Hz”)
	m, milli-	10^{-3}
	μ, micro-	10^{-6}
	n, nano-	10^{-9}
	p, pico-	10^{-12}
Numeric value	xxh, xxH	Hexadecimal number. “x”: any alphanumeric of 0 to 9 or A to F.
	xxb	Binary number; “b” may be omitted. “x”: a number, 0 or 1 “_” is used as a nibble (4-bit) delimiter. (eg. “0011_0101b” = “35h”)
Address	#xxh	Address in a hexadecimal number. “x”: any alphanumeric of 0 to 9 or A to F.
Data	bit[n]	n-th single bit in the multi-bit data.
	bit[n:m]	Bit range from bit[n] to bit[m].
Signal level	“H”, High	High level (over V_{IH} or V_{OH}) of logic signal.
	“L”, Low	Low level (under V_{IL} or V_{OL}) of logic signal.
	“Z”, “Hi-Z”	High impedance state of 3-state signal.

Reference

Name	Reference Document	Release Date	Publisher
USB Type-C	“USB Type-C Specification Release 1.1”	Apr. 3, 2015	USB.org
USB PD	“Power Delivery Specification Revision2.0 Version1.0”	Aug. 11, 2014	USB.org
SMBus	“System Management Bus (SMBus) Specification Version 2.0”	Aug. 3, 2000	System Management Implementers Forum

1 Introduction

BM92T20 is a full function Type-C USB-PD controller that supports USB Power Delivery using base-band communication. It is compatible with USB Type-C specification rev1.1 and USB Power Delivery specification rev2.0

BM92T20 includes the following functional blocks: Type-C Physical Layer (base-band PHY), BMC encoder / decoder, USB-PD Protocol engine, two N-ch MOSFET switch drivers to control two MOSFETS each, OVP FET and SMBus interface for communicating with the host controller. It requires an external embedded controller that includes Device Policy Manager and GPIOs for Type-C USB-PD operation. BM92T20 is able to operate independently in an AC adapter or in a dead battery condition where the embedded controller is not operational. BM92T20 includes an EEPROM, enabling code updates via the SPI interface during prototyping phase.
BM92T20 controller comes in four variations depending on Technical Note for their circuit design. Please refer for additional details

Figure 1-1 shows the block diagram.

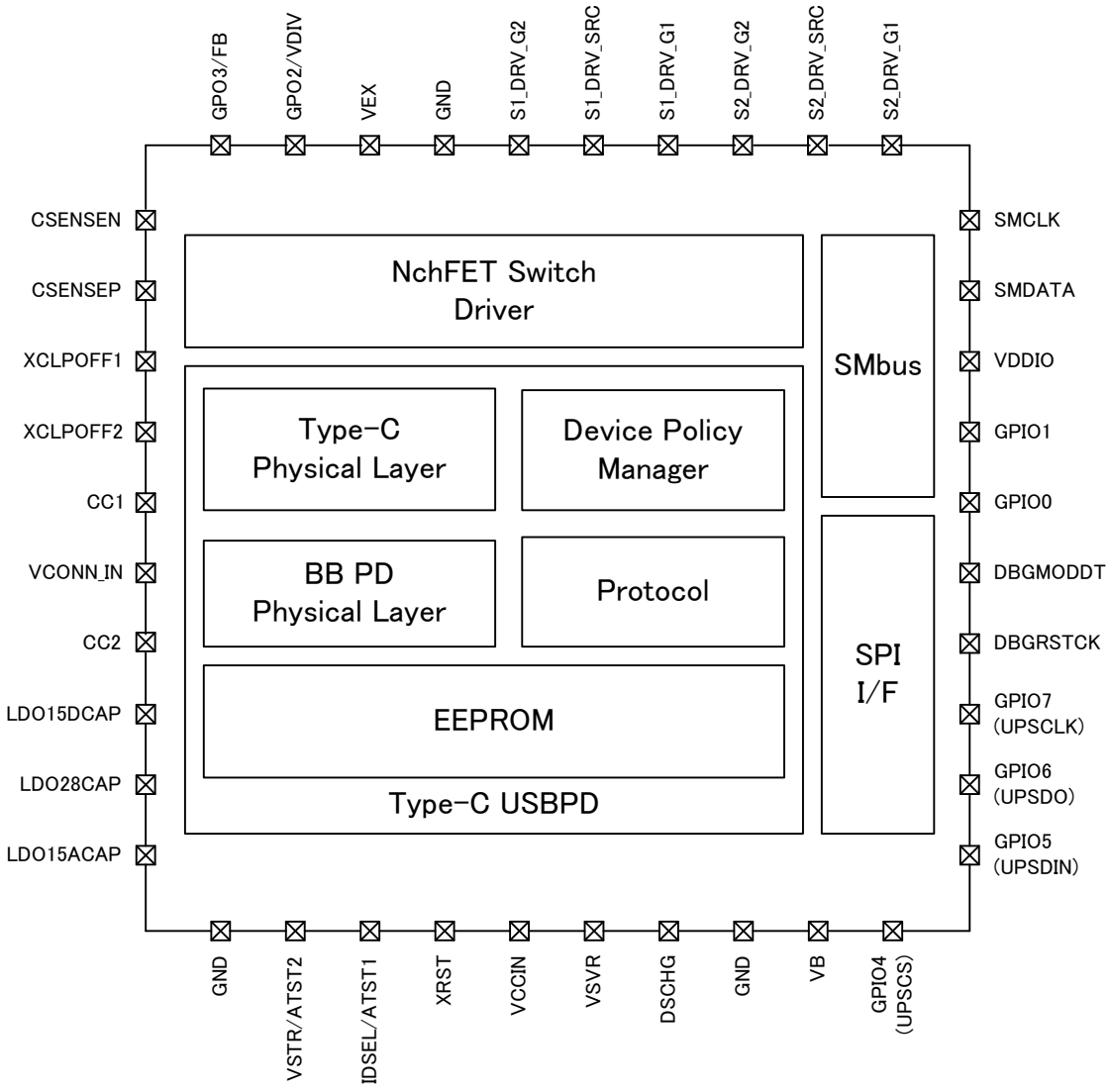


Figure 1-1. Block Diagram

2 Pin Description

Table 2-1. Pin Description

PKG PIN #	Pin Name	BLOCK	I/O	Type	Power System	Description	Note
1	GND	GND	I	GND		Ground	
2	VSTR/ATST2	TEST/Debug	IO	Analog		Analog TEST/ Debug Pin2	
3	IDSEL/ATST1	TEST/Debug	I	Analog		SMBus ID (device address) selection “H”:1Ah, “L”:18h /Debug Pin1	
4	XRST	Interface	I	Digital	VCCIN	Digital block Reset	
5	VCCIN	USB-PD	O	Analog		Internal Power supply (For internal use, need to connect capacitor to GND	
6	VSVR	POWER	I	Power		5V SVR INPUT and SPDSRC_FET_SRC voltage	
7	DSCHG	Interface	IO	Analog		Discharge NMOS Drain	
8	GND	GND	I	GND		Ground	
9	VB	POWER	I	Power		Power Source from VBUS	
10	GPIO4 (Ext mode: UPSCS)	Interface	I/O (O)	Digital	VCCIN	General purpose I/O port 4 /(Ext mode: SPI Chip Select)	Refer to Technical Note
11	GPIO5 (Ext mode: UPSDIN)	Interface	I/O (I)	Digital	VCCIN	General purpose I/O port 5 /(Ext mode: SPI DATA IN)	Refer to Technical Note
12	GPIO6 (Ext mode: UPSDO)	Interface	I/O (O)	Digital	VCCIN	General purpose I/O port 6 /(Ext mode: SPI DATA OUT)	Refer to Technical Note
13	GPIO7 (Ext mode: UPSCLK)	Interface	I/O (IO)	Digital	VCCIN	General purpose I/O port 7 /(Ext mode: SPI CLK INPUT)	Refer to Technical Note
14	DBGRSTCK	TEST	IO	Digital	VDDIO	Test for logic	
15	DBGMODDT	TEST	IO	Digital	VDDIO	Test for logic	
16	GPIO0	Interface	IO	Digital	VDDIO	General purpose I/O port 0 Don’t used	Refer to Technical Note
17	GPIO1	Interface	IO	Digital	VDDIO	General purpose I/O port 1 Don’t used	Refer to Technical Note
18	VDDIO	POWER	I	Power		Interface Voltage (3.3V)	
19	SMDATA	Interface	IO	Digital	VDDIO	SMBus Data	
20	SMCLK	Interface	I	Digital	VDDIO	SMBus Clock	

PKG PIN #	Pin Name	BLOCK	I/O	Type	Power System	Description	Note
21	S2_DRV_G1	FET Gate Control	O	Analog		Power Path FET Gate Control LDISCHG_G1	Refer to Technical Note
22	S2_DRV_SRC	FET Gate Control	I	Analog		Power Path FET BG/SRC Voltage LDISCHG_SRC	Refer to Technical Note
23	S2_DRV_G2	FET Gate Control	O	Analog		Power Path FET Gate Control Not used	Refer to Technical Note
24	S1_DRV_G1	FET Gate Control	O	Analog		Power Path FET Gate Control SPDSRC_G1	Refer to Technical Note
25	S1_DRV_SRC	FET Gate Control	I	Analog		Power Path FET BG/SRC Voltage SPDSRC_SRC	Refer to Technical Note
26	S1_DRV_G2	FET Gate Control	O	Analog		Power Path FET Gate Control SPDSRC_G2	Refer to Technical Note
27	GND	GND	I	GND		Ground	
28	VEX	POWER	I	Power		Extension Power Input	
29	GPO2/VDIV	Interface	O /IO	Digital /Analog	VCCIN	General purpose Output port 2 VDIV	
30	GPO3/FB	Interface	O /IO	Digital /Analog	VCCIN	General purpose Output port 3 FB	
31	CSENSEN	CDET	I	Analog	VCCIN	Current Sense Voltage Input Negative / Pin 29,30 Configuration *(Pin31,Pin32)=(H,H):GPO mode, other case: Current Sense mode.	
32	CSENSEP	CDET	I	Analog	VCCIN	Current Sense Voltage Input Positive / Pin 29,30 Configuration *(Pin31,Pin32)=(H,H):GPO mode, other case: Current Sense mode.	
33	XCLPOFF1	CCPHY	I	Analog	VCCIN	Disable Clamper of CC1 L:Dead-battery not support Open: Dead-battery support	
34	XCLPOFF2	CCPHY	I	Analog	VCCIN	Disable Clamper of CC2 L:Dead-battery not support Open: Dead-battery support	
35	CC1	CCPHY	IO	Analog		Configuration channel 1 for Type-C	
36	VCONN_IN	CCPHY	I	Analog		Input power for VCONN	
37	CC2	CCPHY	IO	Analog		Configuration channel 2 for Type-C	
38	LDO15DCAP	POWER	O	Analog		Internal LDO 1.5V for Digital Need Capacitor	
39	LDO28CAP	POWER	O	Analog		Internal LDO 2.8V for Analog Need Capacitor	
40	LDO15ACAP	POWER	O	Analog		Internal LDO 1.5V for Analog Need Capacitor	

3 Pin Configuration

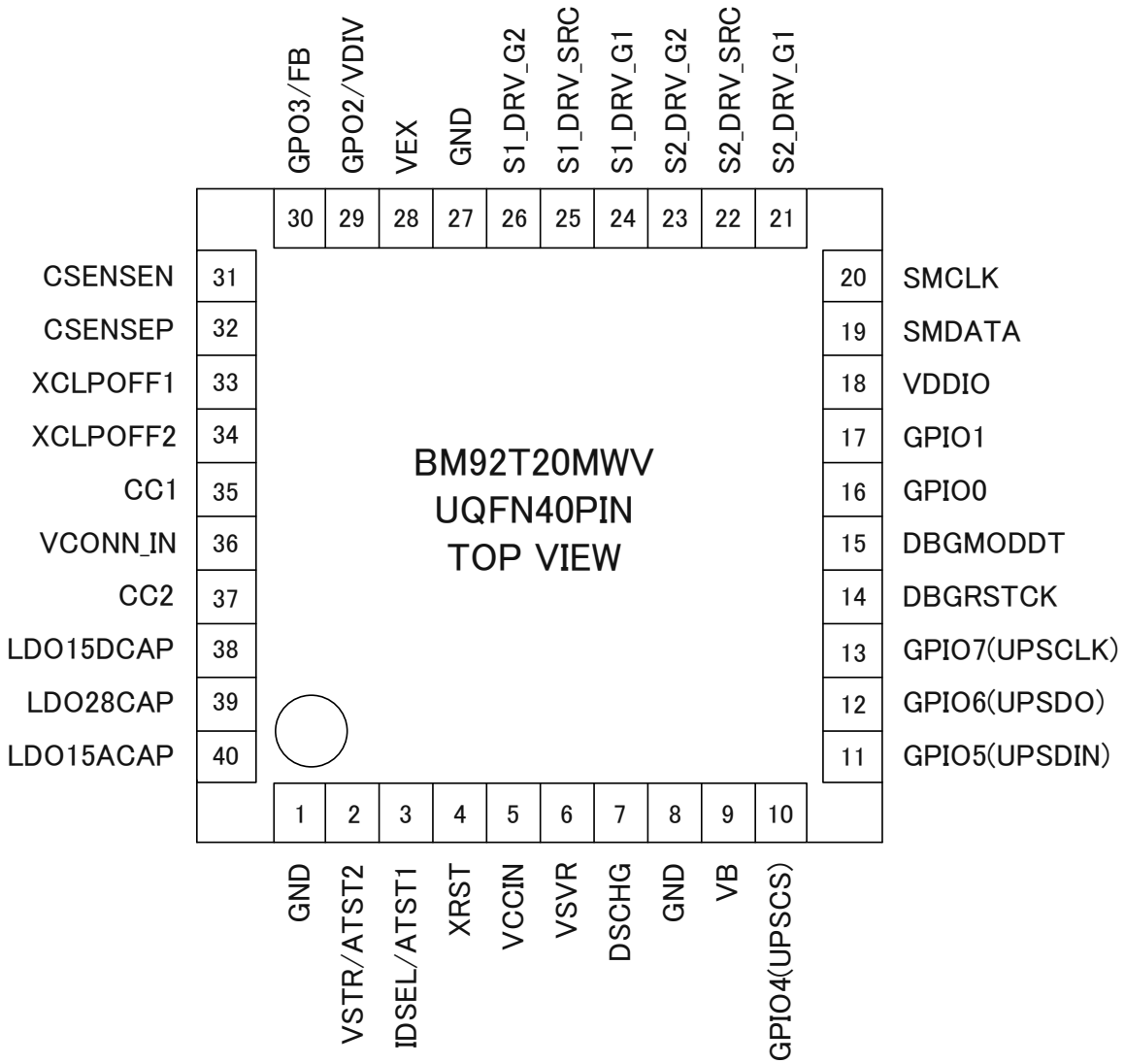


Figure 3-1. Pin configuration

4 Package Dimensions

Ordering Information

B	M	9	2	T	2	0	M	W	V	-	E 2

Part Number

Package
MWV:UQFN40V5050A

Packaging and forming specification
E2: Embossed tape and reel

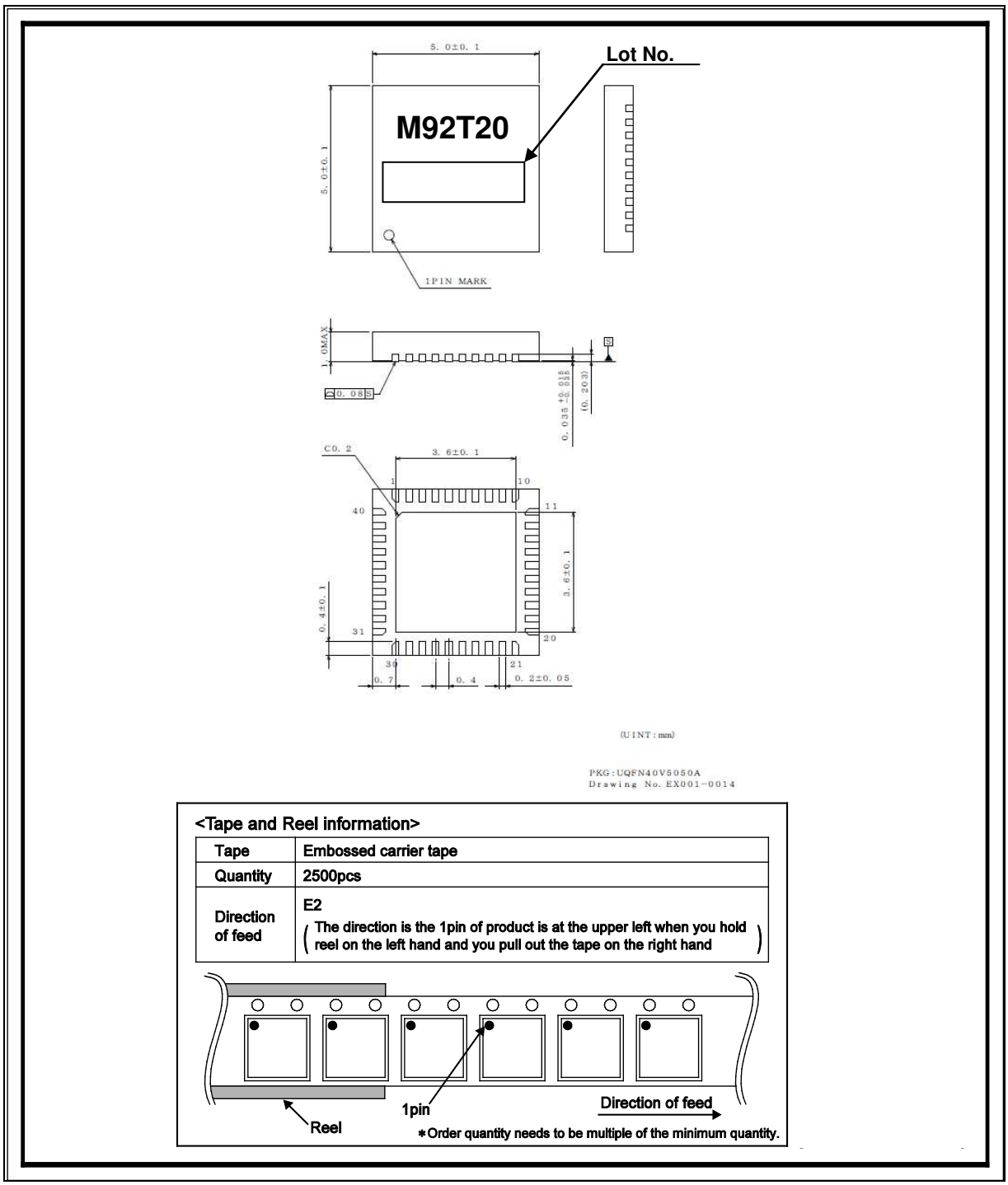


Figure 4-1. UQFN40V5050A Package Dimensions

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1. Absolute Maximum Ratings

（Ta=25℃）

Parameter	Symbol	Rating	Unit	Conditions
Maximum Supply Voltage1 (VB, VEX, DSCHG, S2_DRV_G1, S2_DRV_G2,S2_DRV_SRC, S1_DRV_G1,S1_DRV_SRC, S1_DRV_G2)	VIN1	-0.3 to +28	V	*1 *2
Maximum Supply Voltage2 (VDDIO)	VIN2	-0.3 to +6.0	V	
Maximum Supply Voltage3 (VSVR, DBGRSTCK, DBGMODDT, GPIO0, GPIO1, SMDATA, SMCLK, VCONN_IN)	VIN3	-1.0 to+6.0	V	
Maximum Supply Voltage4 (VSTR/ATST2, IDSEL/ATST1, XRST, VCCIN, GPIO4, GPIO5,GPIO6,GPIO7, GPO2/VDIV, GPO3/FB, CSENSEN, CSENSEP, XCLPOFF1, XCLPOFF2, CC1, CC2, LDO15DCAP, LDO28CAP, LDO15ACAP,)	VIN4	-0.3 to +6.0	V	
Maximum different Voltage (S2_DRV_G1-S2_DRV_SRC, S2_DRV_G2-S2_DRV_SRC, S1_DRV_G1-S1_DRV_SRC, S1_DRV_G2-S1_DRV_SRC)	Vdiff	-0.3 to +6.0	V	
Power Dissipation	Pd	2.61	W	*3
Operating Temperature Range	Topr	-30 to +105	degree	*4
Storage Temperature Range	Tstg	-55 to +125	degree	

*1 When the DSCHG pin is applied voltage should by way of resistance more than 120Ω (4W).
*2 The different voltage between S*DRV_G* and S*DRV_SRC is defined “Symbol Vdiff”. S*_DRV_G*=S*_DRV_SRC+5.8V (typ.)
*3 This value is the permissible loss using a ROHM specification board (74.2 x 74.2 x 1.6tmm, 4 layered board mounting).
At the time of PCB mounting the permissible loss varies with the size and material of board.
When using more than at Ta=25℃, it is reduced 26.1 mW per 1℃.（Caution）Use in excess of this value may result in damage to the device. Moreover, normal operation is not protected.
*4 Target spec.

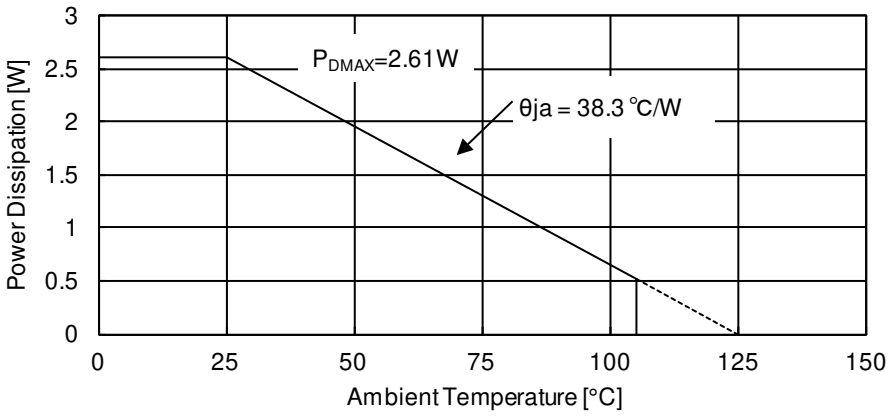


Figure 5-1. Power Dissipation

5.2 Recommended Operating Conditions

Table 5-2. Recommended Operating Conditions

(Ta=25°C)

Item	Symbol	Range	Unit	Conditions
VB, VEX Voltage	VB, VEX	4.75 ～ 20	V	
VSVR Voltage	VSVR	3.1 ～ 5.5	V	*2
VDDIO Voltage	VDDIO	1.7 ～ 5.5	V	*2
VCONN_IN Input Voltage	VCONN	4.75 ～ 5.5	V	

*2 target design

5.3 Circuit Current Characteristics

Table 5-3. Common Characteristics

Electrical Characteristics (Ta=25°C, VSVR=3.3V, VB=open, VEX=open, VDDIO=3.3V)

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Circuit Current]						
Unattached current	Idd_unatt		0.4		mW	@VSVR=3.3V
Attached current	Idd_att		3.5		mW	@VSVR=3.3V

5.4 Digital Pin DC Characteristics

Table5-4. Digital Pin DC Characteristics

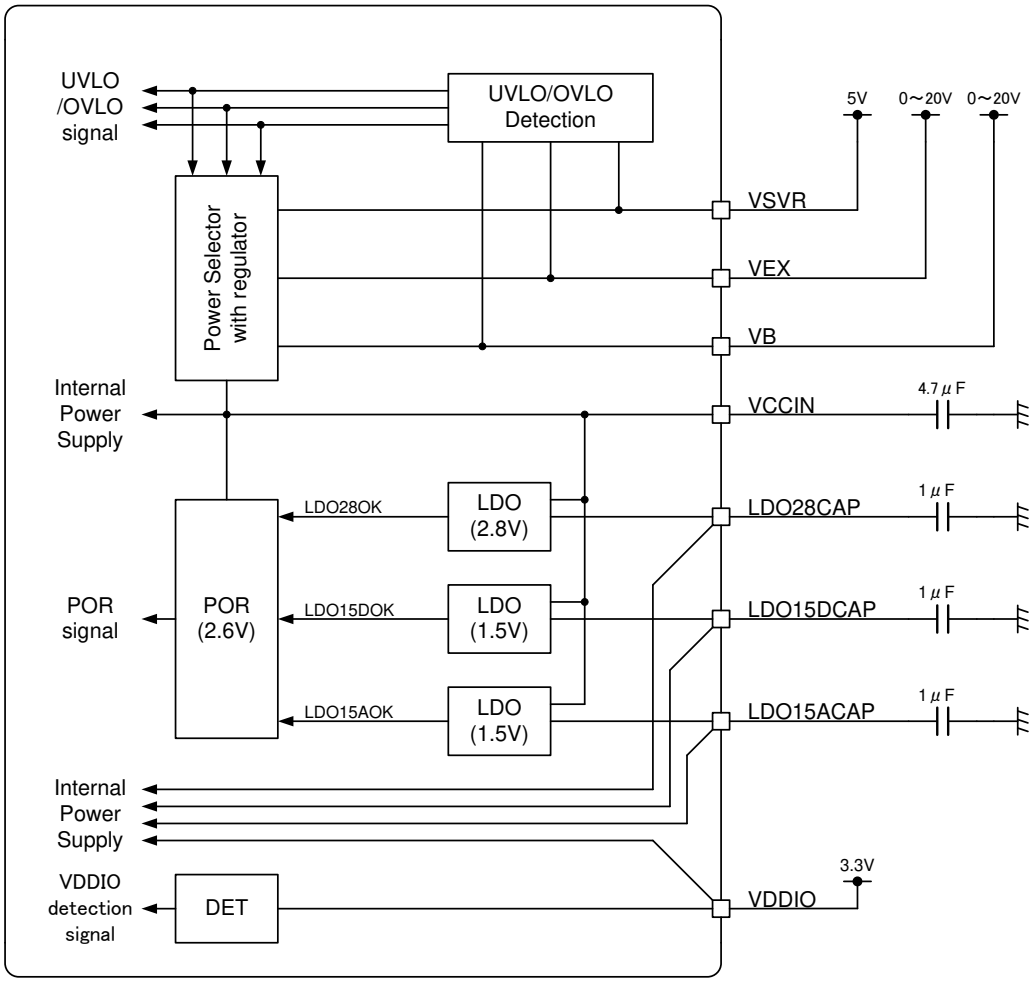
Electrical Characteristics (Ta=25°C, VSVR=3.3V, VB=open, VEX=open, VDDIO=3.3V, VCCIN=VSVR)

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[Digital characteristics Power: VDDIO] (Input Digital Pins: SMCLK, DBGRSTCK) (Input/ Output Pins: GPIO0, GPIO1, SMDATA, DBGMODDT)						
Input "H" level (SMCLK, SMDATA)	VIH1	0.8×VDDIO	-	VDDIO+0.3	V	
Input "L" level (SMCLK, SMDATA)	VIL1	-0.3	-	0.2×VDDIO	V	
Input leak current (SMCLK, SMDATA)	IIC1	-5	0	5	μA	Power: VDDIO
Input "H" level (other Digital input)	VIH2	0.8×VDDIO	-	VDDIO+0.3	V	
Input "L" level (other Digital input)	VIL2	-0.3	-	0.2×VDDIO	V	
Input leak current (other Digital input)	IIC2	-1	0	1	μA	Power: VDDIO
SMDATA pin "L" level voltage	VOL SMDATA	-	-	0.4	V	IOL=350uA Max
Output Voltage when “L” (other Digital output)	VOL1	-	-	0.3	V	Source=1mA
OFF Leakage Current (other Digital output)	IIOFF1	-3	-	3	μA	VIN=VDDIO
[Digital characteristics Power: VCCIN] (Input Digital Pins: XRST) (Input/ Output Pins:GPIO4, GPIO5, GPIO6, GPIO7) (Output Pins: GPO2/VDIV, GPO3/FB)						
Input "H" level (XRST,GPIOs)	VIH3	0.8×VCCIN	-	VCCIN+0.3	V	
Input "H" level(XRST,GPIOs)	VIH3	0.8×VCCIN	-	VCCIN+0.3	V	
Input "L" level (XRST,GPIOs)	VIL3	-0.3	-	0.2×VDDIO	V	
Input leak current (XRST,GPIOs)	IIC3	-5	0	5	μA	Power: VCCIN
Input "H" level (other Digital input)	VIH4	0.8×VDDIO	-	VDDIO+0.3	V	
Input "L" level (other Digital input)	VIL4	-0.3	-	0.2×VDDIO	V	Power: VCCIN
Input leak current (other Digital input)	IIC4	-1	0	1	μA	
Output Voltage when “L” (other Digital output)	VOL2	-	-	0.3	V	Source=1mA
OFF Leakage Current (other Digital output)	IIOFF2	-3	-	3	μA	VIN=VCCIN CSENSEP=CSENSEN=VCCIN

5.5 Power supply management

5.5.1 Outline

This LSI has a power selector. It select the lowest power supply voltage from VSVR, VEX, or VB for low power consumption. Internal Power Supply (VCCIN) gives priority in order of VSVR, VEX, and VB. VCCIN supplied from the power selector is used to LSI main power source. LDOs (for internal only) are supplied from VCCIN, and output each internal supply voltage.
Each power supply input have UVLO (2.8Vtyp) and OVLO (VSVR: 6.4Vtyp, VEX/VB: 6.4/15.0/28.0Vtyp).And POR (power on reset) signal is generated from detection of LDO28OK, LDO15DOK, LDO15AOK, and VCCIN.



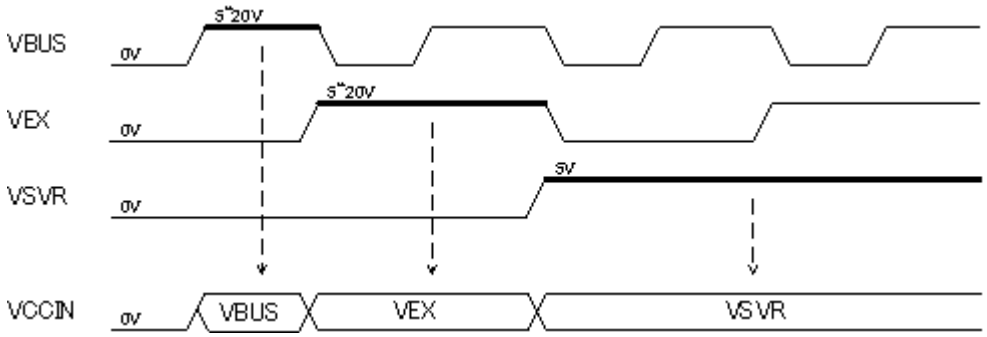


Figure 5-2. Power Supply Management Block Diagram and Timing Chart

5.5.2 Electrical Characteristics

Table 5-5. Power Supply Management Characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[Analog characteristics] Unless otherwise specified Ta=25°C, GND=0V, Bypass Capacitor(VCCIN)=4.7µF, Bypass Capacitors(LDO28CAP, LDO15DCAP, LDO15ACAP) =1µF Input Analog Pins: VSVR, VEX, VB						
UVLO release voltage	UVLO1H	-	2.8	-	V	VSVR, VEX, VB=up
UVLO detect voltage	UVLO1L	-	2.7	-	V	VSVR, VEX, VB=down
OVLO detect voltage (5V mode)	OVLO5	-	6.4	-	V	VSVR, VEX, VB=up
OVLO detect voltage (12V mode)	OVLO12	-	15	-	V	VEX, VB=up
OVLO detect voltage (20V mode)	OVLO20	-	28	-	V	VEX, VB=up
OVLO hysteresis voltage (5V mode)	OVLO5hys	-	240	-	mV	OVLO5-release voltage
OVLO hysteresis voltage (12V mode)	OVLO12hys	-	580	-	mV	OVLO12-release voltage
OVLO hysteresis voltage (20V mode)	OVLO20hys	-	580	-	mV	OVLO20-release voltage
Power ON reset threshold voltage	POR	-	2.6	-	V	VCCIN=up
LDO28CAP output voltage	V28	-	2.8	-	V	No Load, VSVR=5V
LDO15DCAP output voltage	V15D	-	1.5	-	V	No Load, VSVR=5V
LDO15ACAP output voltage	V15D	-	1.5	-	V	No Load, VSVR=5V

5.6 CC_PHY

5.6.1 Outline

CC_PHY has below functions of USB Type-C. (Refer to USB Type-C Spec)
- Defining Port Mode
  - > DFP Mode Condition
  - > UFP Mode Condition
  - > DRP Mode Condition
- DFP-to-UFP Attach / Detach Detection
- Plug Orientation / Cable Twist Detection
- USB Type-C VBUS Current Detection and Usage
- VCONN (Supply for SOP') Control
- Base-Band Power Delivery Communication (BBPD communication)
- Discovery and Configuration of Functional Extensions

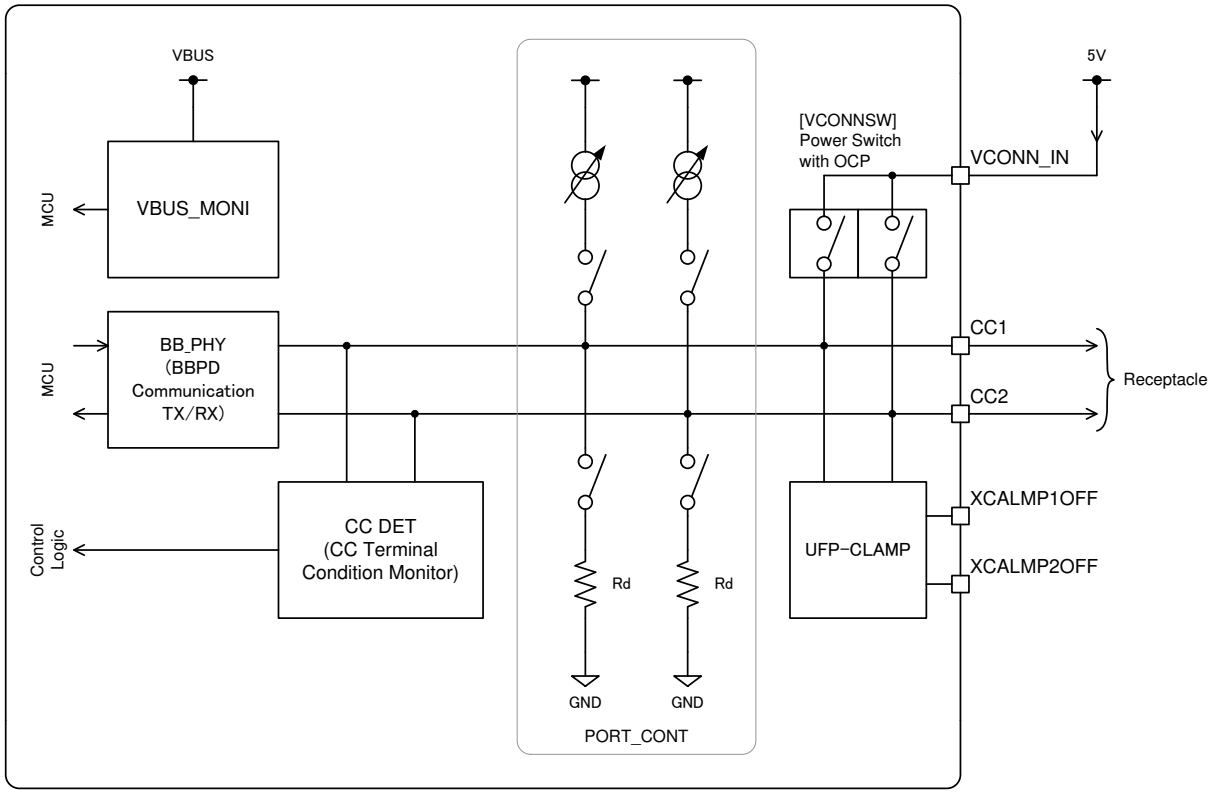


Figure 5-3. CC_PHY Block Diagram

[PORT_CONT]

This block chose the port mode according to the setting from MCU.

(DFP)
Variable current source is connected to CC terminal. These currents of each mode are 80μA±20%: Default Current, 180μA±8%: Medium Current and 330μA±8%: High Current.

(UFP)
Pull-down resistor (Rd=5.1kΩ±10%) is connected to CC terminal.

(DRP)
Changing DFP and UFP is repeated frequently.

[CC_DET]
CC_DET has functions of "Attach / Detach Detection", "Plug Orientation / Cable Twist Detection", "Discovery and detect extension mode" and "USB Type-C VBUS Current Detection".

Attach / Detach is detected with monitoring voltage of CC terminal. When the voltage of CC terminal become under a threshold voltage at DFP, attach is detected. Oppositely, when the voltage of CC terminal become over a threshold voltage, detach is detected. When the voltage of CC terminal become over a threshold voltage at UFP, attach is detected.

Plug orientation and cable twist is detected from the relationship of two CC terminals. Because only one wire is connected to Rd, the difference between two CC terminals is generated.

UFP can detect the maximum current of the power source by monitoring the voltage of CC terminal.

It is possible to detect extension mode because DFP can detect Ra at Attach / Detach detection.

[UFP_CLAMP]
1.1V Clamp is used for UFP emulation at dead-battery condition.

[VBUS_MONI]
UFP detect Attach / Detach by existence of VBUS voltage. VBUSDET detects Attach when VBUS voltage over the threshold voltage. And it detects Detach when VBUS under the threshold voltage.

[VCONNSW]
VCONNSW is the power switch for VCONN source. It has OCP (1.3Atyp) function.

[BB_PHY]
If Type-C controller supports BBPD, CC terminal can output BBPD communication signal. (Refer to BB_PHY)

5.6.2 Electrical Characteristics

Table 5-6. CC_PHY Characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[PORT_CONT characteristics] Unless otherwise specified Ta=25°C, VSVR=VEX=VB=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, Bypass Capacitor(VCCIN)=4.7µF, Bypass Capacitors(LDO28CAP, LDO15DCAP, LDO15ACAP) =1µF Input Analog Pins: CC1, CC2, VCONN_IN						
Pull up current 1	CCPUP1	64	80	96	µA	Ta=-30～105°C
Pull up current 2	CCPUP2	166	180	194	µA	Ta=-30～105°C
Pull up current 3	CCPUP3	304	330	356	µA	Ta=-30～105°C
Pull down resistor	CCPDN	4.6	5.1	5.6	kΩ	Ta=-30～105°C
[UFP_CLAMP characteristics] Unless otherwise specified Ta=25°C, VSVR=VEX=VB=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, Bypass Capacitor(VCCIN)=4.7µF, Bypass Capacitors(LDO28CAP, LDO15DCAP, LDO15ACAP) =1µF Input Analog Pins: CC1, CC2, VCONN_IN						
CCx terminal input impedance	CCZin	126	-	-	kΩ	
CCx clamp voltage	CCCLP	0.7	-	1.3	V	Iin=80 to 330µA
[VBUS MONI] Unless otherwise specified Ta=25°C, VSVR=VEX=VB=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, Bypass Capacitor(VCCIN)=4.7µF, Bypass Capacitors(LDO28CAP, LDO15DCAP, LDO15ACAP) =1µF Input Analog Pins: CC1, CC2, VCONN_IN						
VBUS presence detection level	CCVBDET	-	3.42	-	V	
[VCONNSW] Unless otherwise specified Ta=25°C, VSVR=VEX=VB=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, Bypass Capacitor(VCCIN)=4.7µF, Bypass Capacitors(LDO28CAP, LDO15DCAP, LDO15ACAP) =1µF Input Analog Pins: CC1, CC2, VCONN_IN						
VCONN_IN to CCx resistance	CCVCR	-	-	500	mΩ	
Overcurrent protection level	CCVCOCP	1.1	-	-	A	
[BB_PHY] Unless otherwise specified Ta=25°C, VSVR=VEX=VB=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, Bypass Capacitor(VCCIN)=4.7µF, Bypass Capacitors(LDO28CAP, LDO15DCAP, LDO15ACAP) =1µF Input Analog Pins: CC1, CC2, VCONN_IN						
TX BCM frequency	fBBTX		300		kHz	
TX voltage output H level	BBVOH	1.05	-	1.2	V	
TX voltage output L level	BBVOL	0	-	75	mV	
RX voltage input H level	BBVIH	-	0.6	0.65	V	
RX voltage input L level	BBVIL	0.45	0.5	-	V	

5.7 Voltage detection

5.7.1 Outline

VDET Block detects the voltage level of VBUS or VEX. It can detect follow conditions; (1) the voltage over the protection level, (2) the voltage over the setting range and (3) the voltage under the setting range.
-VBUS or VEX voltage Detection for PDO of USB-PD spec.
-OVP (over voltage protection) Detection: Vnom +20%typ
-OVR (over voltage range) Detection: Vnom +5%typ
-UVR (under voltage range) Detection: Vnom -5%typ

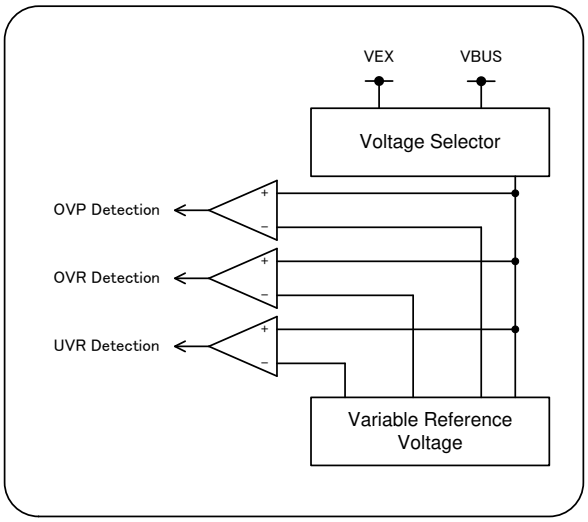


Figure 5-4. Voltage Detection Block Diagram

5.7.2 Electrical Characteristics

Table 5-7. Voltage Detection characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[VDET characteristics] Unless otherwise specified Ta=25°C, VSVR=VEX=VB=5V, VCONN_IN=VCCIN, VDDIO=3.3V, GND=0V, Bypass Capacitor(VCCIN)=4.7µF, Bypass Capacitors(LDO28CAP, LDO15DCAP, LDO15ACAP) =1µF, Vnom=5V Input Analog Pins: VEX, VB						
Over voltage protection detection rate	OVP	17	20	23	%	Standard voltage=Vnom
Over voltage range detection rate	OVR	3	5	7	%	Standard voltage=Vnom
Under voltage range detection rate	UVR	-7	-5	-3	%	Standard voltage=Vnom

5.8 VBUS Discharge

5.8.1 Outline

NMOS switch is prepared for VBUS discharging.

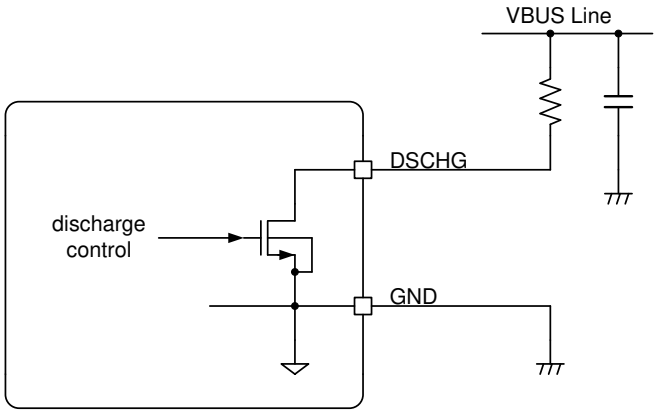


Figure 5-5. VBUS Discharge Block Diagram

5.8.2 Electrical Characteristics

Table 5-8. VBUS Discharge Characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[Discharge characteristics] Unless otherwise specified Ta=25°C, VSVR=VEX=VB=5V, VCONN_IN=VCCIN, VDDIO=3.3V, GND=0V, Bypass Capacitor(VCCIN)=4.7µF, Bypass Capacitors(LDO28CAP, LDO15DCAP, LDO15ACAP) =1µF Input Analog Pins: DSCHG						
Discharge Resistor	RDSCHG	-	25	-	Ω	

5.9 Power FET Gate Driver (SINK & SOURCE)

5.9.1 Outline

FET Gate Driver is the NMOS switch driver for power line switch.
- External Nch-FET gate control: S1, S2
- One of two DC input selection

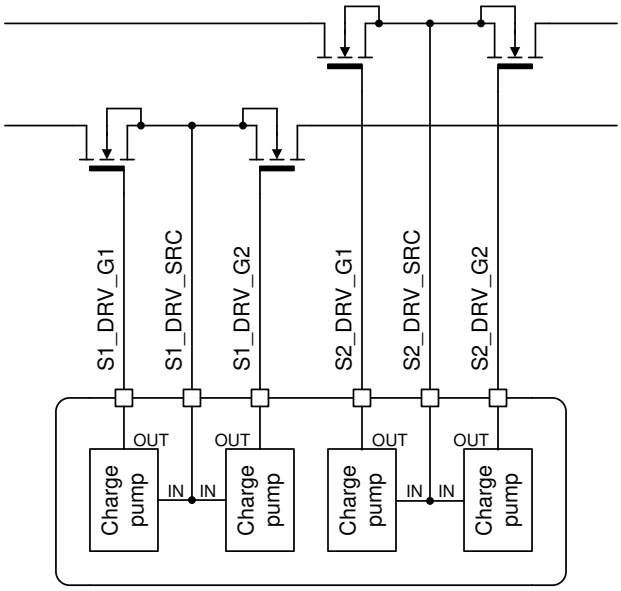


Figure 5-6. Power FET Gate Driver Block Diagram

5.9.2 Electrical Characteristics

Table 5-9. Power FET Gate Driver Characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[Discharge characteristics] Unless otherwise specified Ta=25°C, VSVR=VEX=VB=5V, VCONN_IN=VCCIN, VDDIO=3.3V, GND=0V, Bypass Capacitor(VCCIN)=4.7µF, Bypass Capacitors(LDO28CAP, LDO15DCAP, LDO15ACAP) =1µF Input Analog Pins: S1_DRV_SRC, S2_DRV_SRC Output Analog Pins: S1_DRV_G1, S1_DRV_G2, S2_DRV_G1, S2_DRV_G2						
FET control voltage between gate and source	VGS	-	6.0	-	V	S1_DRV_G1 – S1_DRV_SRC S1_DRV_G2 – S1_DRV_SRC S2_DRV_G1 – S2_DRV_SRC S2_DRV_G2 – S2_DRV_SRC

5.10 ACDC Bridge

5.10.1 Outline

BRIDGE Block is ACDC Bridge function block. It has an error amplifier and current sensing comparator.
-Error Amplifier for ACDC (for Fly-back DCDC Secondary side): 0 to 25.6V / 50mV step (from PDO)
-Current sensing: 0 to 10.24A / 10mA step (from PDO)

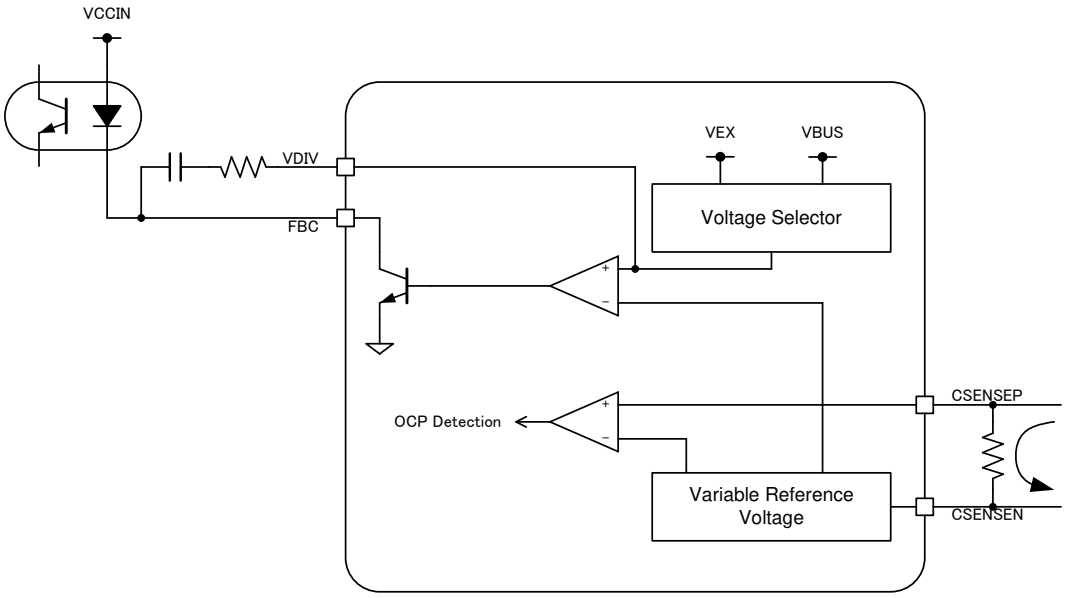


Figure 5-7. ACDC Bridge Block Diagram

5.10.2 Electrical Characteristics

Table 5-10. ACDC Bridge Characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[Discharge characteristics] Unless otherwise specified Ta=25°C, VSVR=VEX=VB=5V, VCONN_IN=VCCIN, VDDIO=3.3V, GND=0V, Bypass Capacitor(VCCIN)=4.7µF, Bypass Capacitors(LDO28CAP, LDO15DCAP, LDO15ACAP) =1µF Input Analog Pins: VEX, VB, CSENSEP, CSENSEN Output Analog Pins: FBC, VDIV						
PDO voltage setting range	BRDVR	5	-	20	V	
PDO voltage setting step	BRDVS	-	50	-	mV	
Feedback current threshold voltage (PDO=Vnom)	BRDVTH	Vnom -2%	Vnom	Vnom +2%	V	VEX= up
Trans conductance	BRDTC	-	1	-	S	ΔIFB/ΔVEX
Maximum feedback current	BRDImax	2	-	-	mA	Ta=-30 to 105°C
PDO current setting range	BRDIR	0	-	5	A	
PDO current setting step	BRDIS	-	10	-	mA	
Current sense detecting rate(*1) (PDO=Inom)	BRDCCS	-	Inom X1.2	-	A	

(*1)Minimum BRDCCS value is 1.2A.
For example, when PDO is 0.5A, BRDCCS value is not 0.5A × 1.2, BRDCCS value is 1.2A.

5.11 Power On Sequence

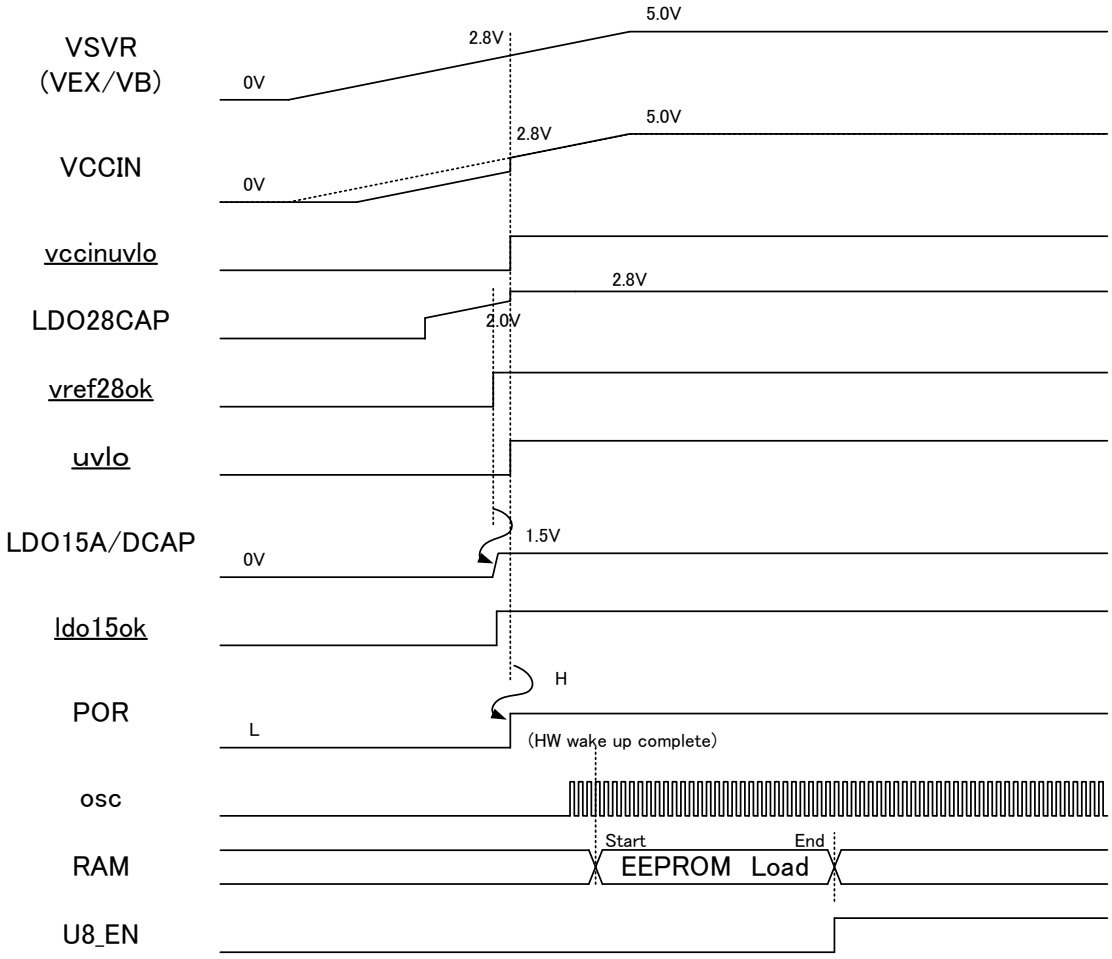


Figure 5-8. Power On Sequence

5.12 Power Off Sequence

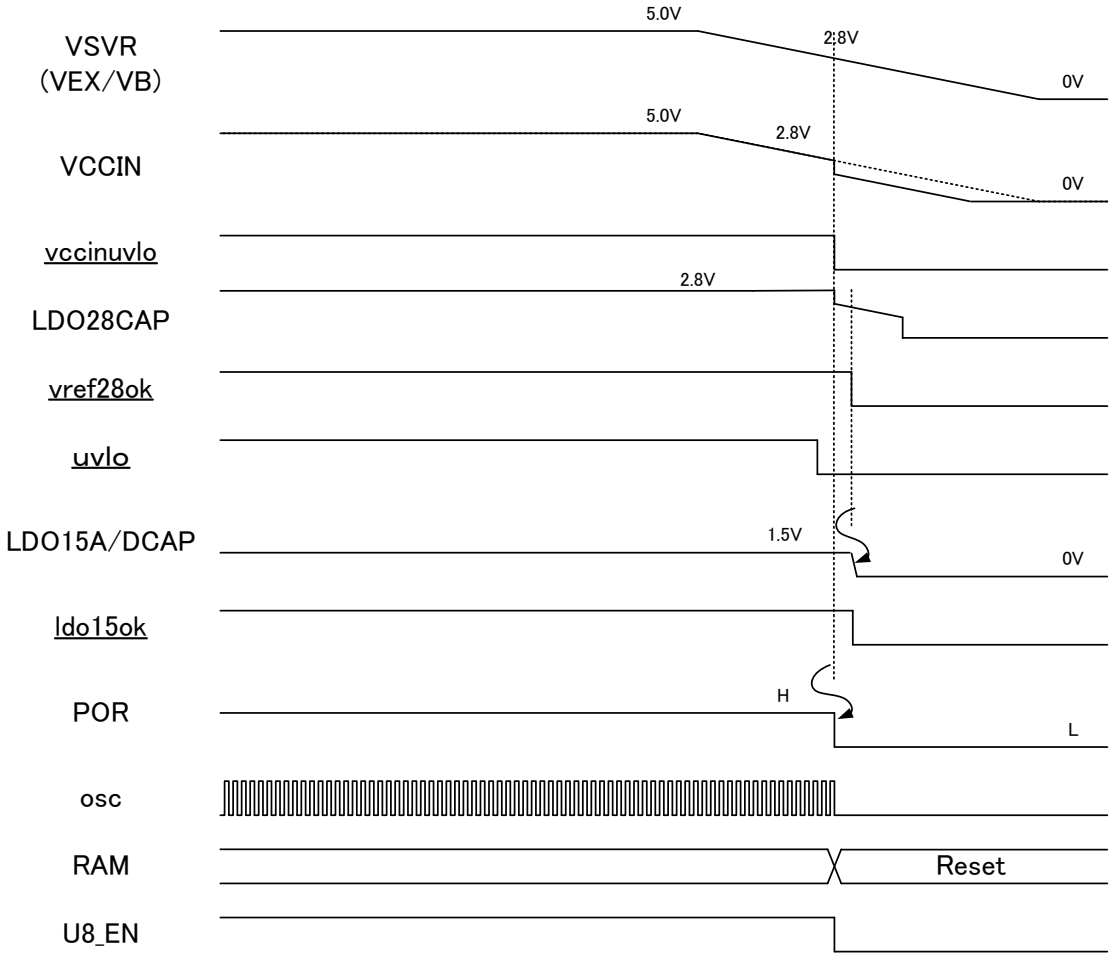
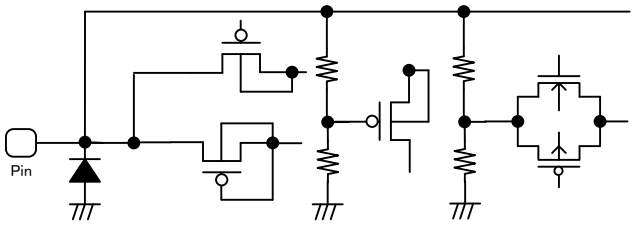
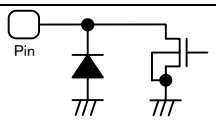
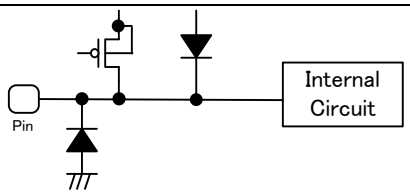
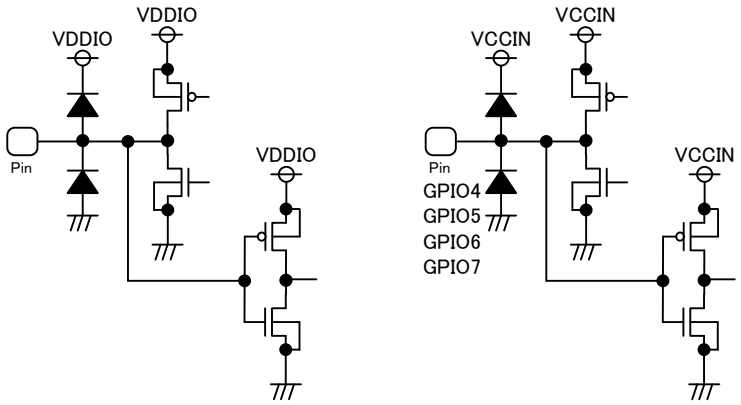
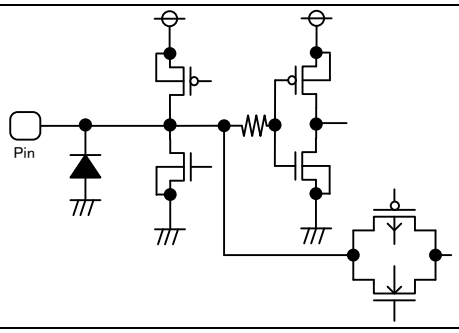
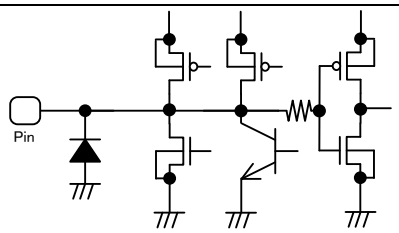
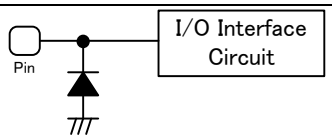
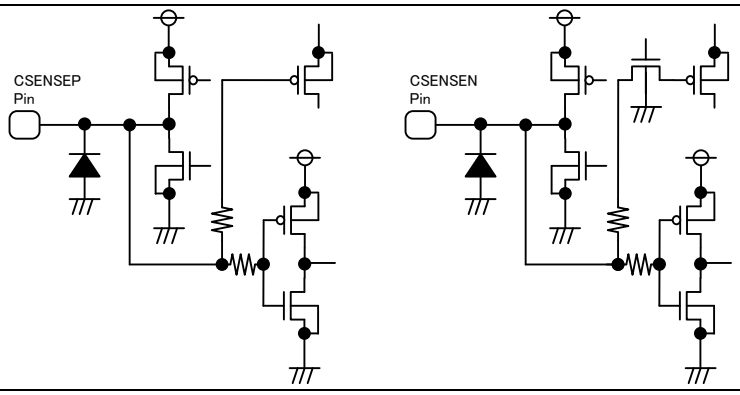
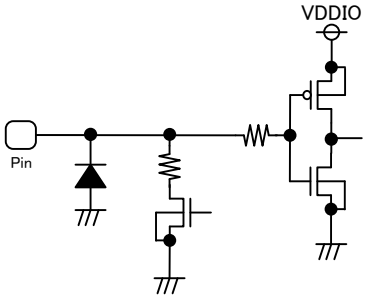
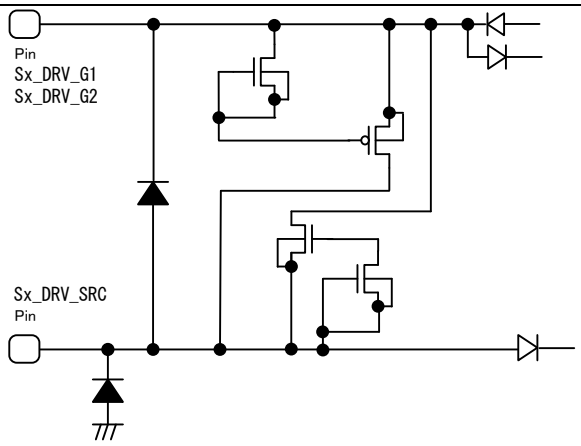
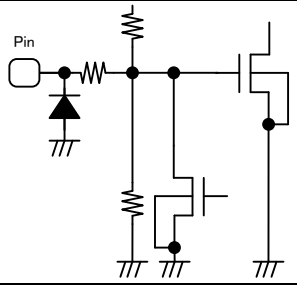
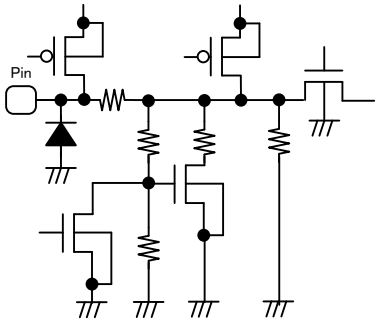
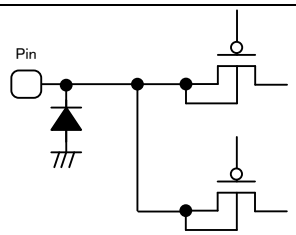
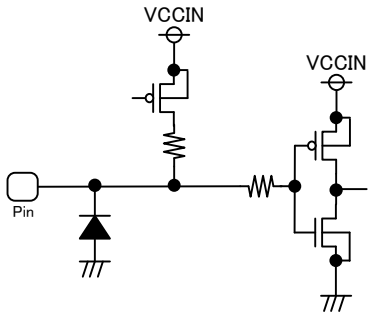
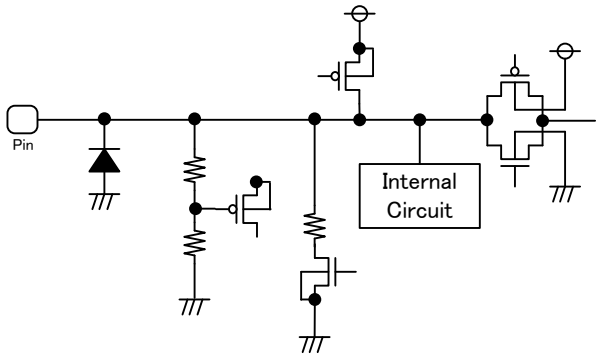
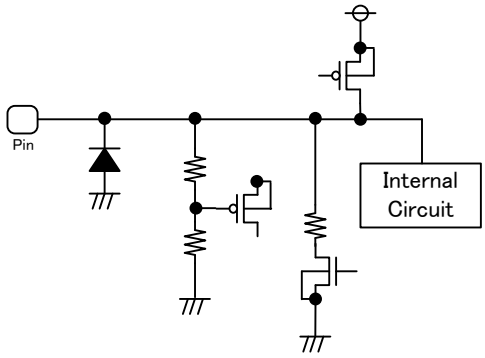
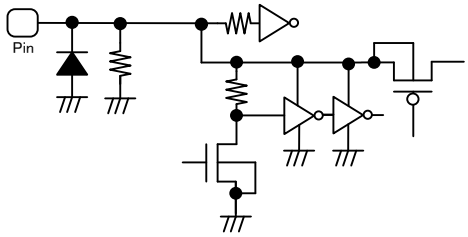


Figure 5-9. Power Off Sequence

5.13 I/O Equivalence Circuit

PIN No.	PIN Name	Equivalent circuit diagram
6 9 28	VSVR VB VEX	
7	DSCHG	
5	VCCIN	
16 17 15 14 10 11 12 13	GPIO0(VIN_EN) GPIO1(ALERT#) DBGMODDT DBGRSTCK GPIO4(UPSCS) GPIO5(UPSDIN) GPIO6(UPSDO) GPIO7(UPSCLK)	
29	GPO2_VDIV	
30	GPO3_FB	
18	VDDIO	

32 31	CSENSEP CSENSEN	
19 21	SMDATA SMCLK	
32 22 23 24 25 26	S2_DRV_G1 S2_DRV_SRC S2_DRV_G2 S1_DRV_G1 S1_DRV_SRC S1_DRV_G2	
33 34	XCLPOFF1 XCLPOFF2	
35 37	CC1 CC2	

36	VCONN_IN	
4	XRST	
38 40	LDO15DCAP LDO15ACAP	
39	LDO28CAP	
2	VSTR/ATST2	
3	IDSEL/ATST1