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Preliminary data sheet

BMA223
Digital, triaxial acceleration sensor

Bosch Sensortec

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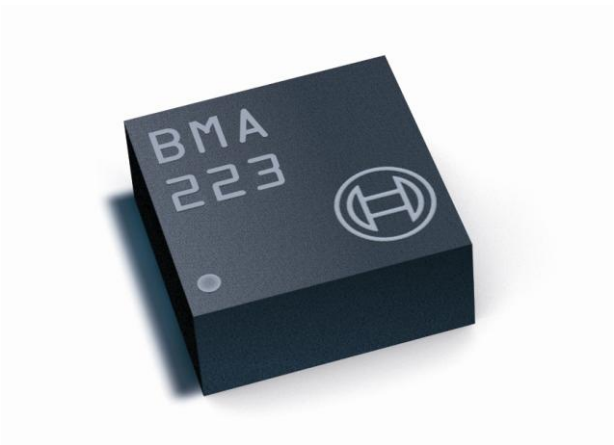

BMA223: Preliminary data sheet

Document revision	0.7
Document release date	04 April 2013
Document number	BST-BMA223-DS000-00
Technical reference code(s)	0 273 141 188
Notes	Data in this document are preliminary and subject to change without notice. Product photos and pictures are for illustration purposes only and may differ from the real product's appearance. **Confidential and under NDA**

BMA223

8 BIT, DIGITAL, TRIAXIAL ACCELERATION SENSOR WITH INTELLIGENT ON-CHIP MOTION-TRIGGERED INTERRUPT CONTROLLER

Key features

- Ultra-Small package — LGA package (12 pins), footprint 2mm x 2mm, height 0.95mm
- Digital interface — SPI (4-wire, 3-wire), I²C, 2 interrupt pins; V_{DDIO} voltage range: 1.2V to 3.6V
- Programmable functionality — Acceleration ranges ±2g/±4g/±8g/±16g; Low-pass filter bandwidths 1kHz - <8Hz
- On-chip FIFO — Integrated FIFO with a depth of 32 frames
- On-chip interrupt controller — Motion-triggered interrupt-signal generation for
  - new data
  - any-motion (slope) detection
  - tap sensing (single tap / double tap)
  - orientation recognition
  - flat detection
  - low-g/high-g detection
  - no-motion / inactivity detection
- Ultra-low power — Low current consumption, short wake-up time, advanced features for system power management
- Temperature sensor
- RoHS compliant, halogen-free

Typical applications

- Display profile switching
- Menu scrolling, tap / double tap sensing
- Gaming
- Pedometer / step counting
- Free-fall detection
- E-compass tilt compensation
- Drop detection for warranty logging
- Advanced system power management for mobile applications

General description

The BMA223 is a triaxial, low-g acceleration sensor with digital output for consumer applications. It allows measurements of acceleration in three perpendicular axes. An evaluation circuitry (ASIC) converts the output of a micromechanical acceleration-sensing structure (MEMS) that works according to the differential capacitance principle.

Package and interfaces of the BMA223 have been defined to match a multitude of hardware requirements. Since the sensor features an ultra-small footprint and a flat package it is ingeniously suited for mobile applications.

The BMA223 offers a variable V_{DDIO} voltage range from 1.2V to 3.6V and can be programmed to optimize functionality, performance and power consumption in customer specific applications.

In addition it features an on-chip interrupt controller enabling motion-based applications without use of a microcontroller.

The BMA223 senses tilt, motion, inactivity and shock vibration in cell phones, handhelds, computer peripherals, man-machine interfaces, virtual reality features and game controllers.

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1. Specification

Unless stated otherwise, the given values are over lifetime, operating temperature and voltage ranges. Minimum/maximum values are ±3σ.

Table 1: Parameter specification

OPERATING CONDITIONS						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Units**
Acceleration Range	g_{FS2g}	Selectable via serial digital interface		±2		g
	g_{FS4g}			±4		g
	g_{FS8g}			±8		g
	g_{FS16g}			±16		g
Supply Voltage Internal Domains	V_{DD}		1.62	2.4	3.6	V
Supply Voltage I/O Domain	V_{DDIO}		1.2	2.4	3.6	V
Voltage Input Low Level	V_{IL}	SPI & I²C			$0.3V_{DDIO}$	-
Voltage Input High Level	V_{IH}	SPI & I²C	$0.7V_{DDIO}$			-
Voltage Output Low Level	V_{OL}	I_{OL} = 3mA, SPI & I²C			$0.2V_{DDIO}$	-
Voltage Output High Level	V_{OH}	I_{OH} = 3mA, SPI	$0.8V_{DDIO}$			-
Total Supply Current in Normal Mode	I_{DD}	T_A=25°C, bw = 1kHz		130		µA
Total Supply Current in Suspend Mode	I_{DDsum}	T_A=25°C		2.1		µA
Total Supply Current in Deep Suspend Mode	I_{DDdsum}	T_A=25°C		1		µA
Total Supply Current in Low-power Mode 1	I_{DDlp1}	T_A=25°C, bw = 1kHz sleep duration = 25ms		6.5		µA
Total Supply Current in Low-power Mode 2	I_{DDlp2}	T_A=25°C, bw = 1kHz sleep duration = 25ms		45		µA

Total Supply Current in Standby Mode	I_{DDsbm}	T_A=25°C		42		µA
Wake-Up Time 1	$t_{w,up1}$	from Low-power Mode 1 or Suspend Mode or Deep Suspend Mode bw = 1kHz		1.3	1.8	ms
Wake-Up Time 2	$t_{w,up2}$	from Low-power Mode 2 or Stand-by Mode bw = 1kHz		1	1.2	ms
Start-Up Time	$t_{s,up}$	POR, bw = 1kHz			3	ms
Non-volatile memory (NVM) write-cycles	n_{NVM}				15	cycles
Operating Temperature	T_A		-40		+85	°C
OUTPUT SIGNAL						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Units**
Sensitivity	S_{2g}	g_{FS2g}, T_A=25°C		64		LSB/g
	S_{4g}	g_{FS4g}, T_A=25°C		32		LSB/g
	S_{8g}	g_{FS8g}, T_A=25°C		16		LSB/g
	S_{16g}	g_{FS16g}, T_A=25°C		8		LSB/g
Sensitivity Temperature Drift	TCS	g_{FS2g}, Nominal V_{DD} supplies		±0.02		%/K
Zero-g Offset	Off	g_{FS2g}, T_A=25°C, nominal V_{DD} supplies, over life-time		±100		mg
Zero-g Offset Temperature Drift	TCO	g_{FS2g}, Nominal V_{DD} supplies		±1.5		mg/K
Bandwidth	bw_8	2nd order filter, bandwidth programmable		8		Hz
	bw_{16}			16		Hz
	bw_{31}			31		Hz
	bw_{63}			63		Hz
	bw_{125}			125		Hz
	bw_{250}			250		Hz
	bw_{500}			500		Hz
	bw_{1000}			1,000		Hz
Nonlinearity	NL	best fit straight line, g_{FS2g}		±0.5		%FS
Output Noise Density	n_{rms}	g_{FS2g}, T_A=25°C Nominal V_{DD} supplies Normal mode		1000		µg/√Hz

Temperature Sensor Measurement Range	T_S		-40		85	°C
Temperature Sensor Slope	dT_S			0.5		K/LSB
Temperature Sensor Offset	OT_S			±2		K

MECHANICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Units
Cross Axis Sensitivity	S	relative contribution between any two of the three axes		1		%
Alignment Error	E_A	relative to package outline		±0.5		°

2. Absolute maximum ratings

Table 2: Absolute maximum ratings

Parameter	Condition	Min	Max	Units
Voltage at Supply Pin	V_{DD} Pin	-0.3	4.25	V
	V_{DDIO} Pin	-0.3	4.25	V
Voltage at any Logic Pin	Non-Supply Pin	-0.3	V_{DDIO}+0.3	V
Passive Storage Temp. Range	≤ 65% rel. H.	-50	+150	°C
None-volatile memory (NVM) Data Retention	T = 85°C, after 15 cycles	10		y
Mechanical Shock	Duration ≤ 200µs		10,000	g
	Duration ≤ 1.0ms		2,000	g
	Free fall onto hard surfaces		1.8	m
ESD	HBM, at any Pin		2	kV
	CDM		500	V
	MM		200	V

Note:
Stress above these limits may cause damage to the device. Exceeding the specified electrical limits may affect the device reliability or cause malfunction.

3. Block diagram

Figure 1 shows the basic building blocks of the BMA223:

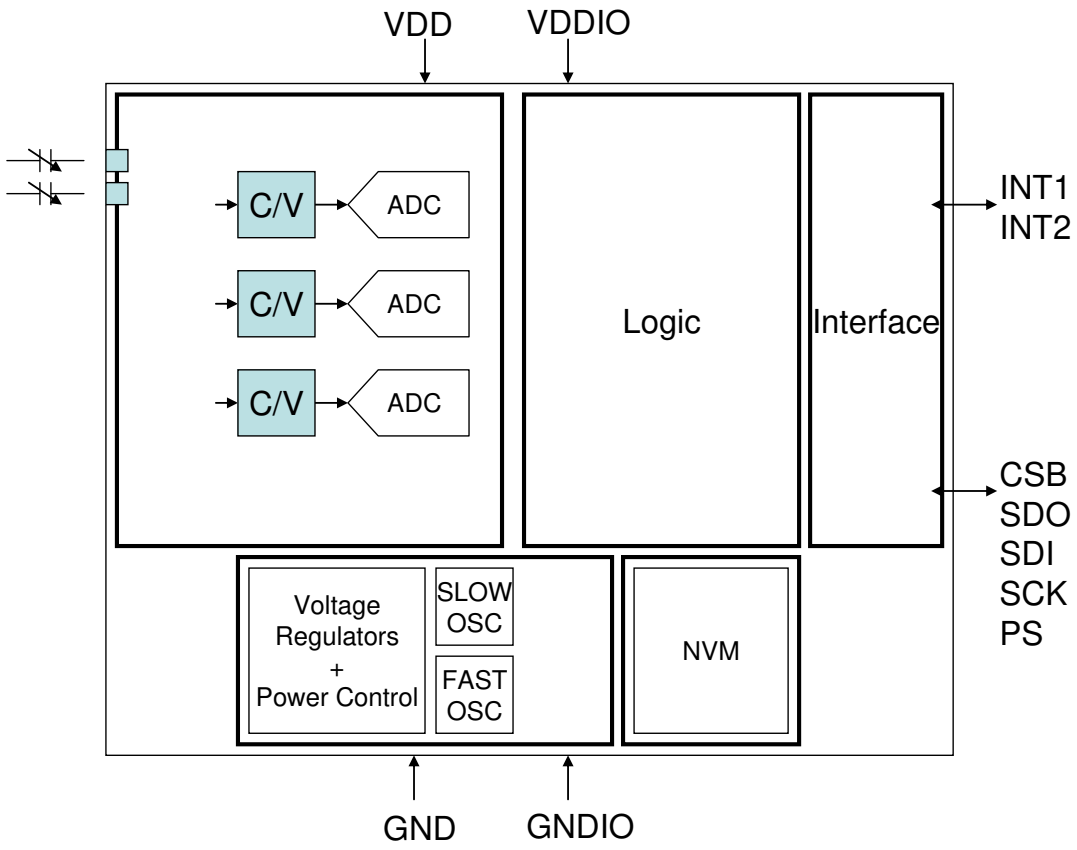

Figure 1: Block diagram of BMA223

4. Functional description

Note: Default values for registers can be found in chapter 6.

4.1 Supply voltage and power management

The BMA223 has two distinct power supply pins:

- V_{DD} is the main power supply for the internal blocks
- V_{DDIO} is a separate power supply pin used for supplying power for the interface

There are no limitations on the voltage levels of both pins relative to each other, as long as each of them lies within its operating range. Furthermore, the device can be completely switched off (V_{DD} = 0V) while keeping the V_{DDIO} supply on (V_{DDIO} > 0V) or vice versa.

When the V_{DDIO} supply is switched off, all interface pins (CSB, SDI, SCK, PS) must be kept close to GND_{IO} potential.

The device contains a power-on reset (POR) generator. It resets the logic part and the register values after powering-on V_{DD} and V_{DDIO}. Please note, that all application specific settings which are not equal to the default settings (refer to 6.2 register map), must be re-set to its designated values after POR.

There are no constraints on the switching sequence of both supply voltages. In case the I²C interface shall be used, a direct electrical connection between V_{DDIO} supply and the PS pin is needed in order to ensure reliable protocol selection. For SPI interface mode the PS pin must be directly connected to GND_{IO}.

4.2 Power modes

The BMA223 has six different power modes. Besides normal mode, which represents the fully operational state of the device, there are five energy saving modes: deep-suspend mode, suspend mode, standby mode, low-power mode 1 and low-power mode 2.

The possible transitions between the power modes are illustrated in figure 2:

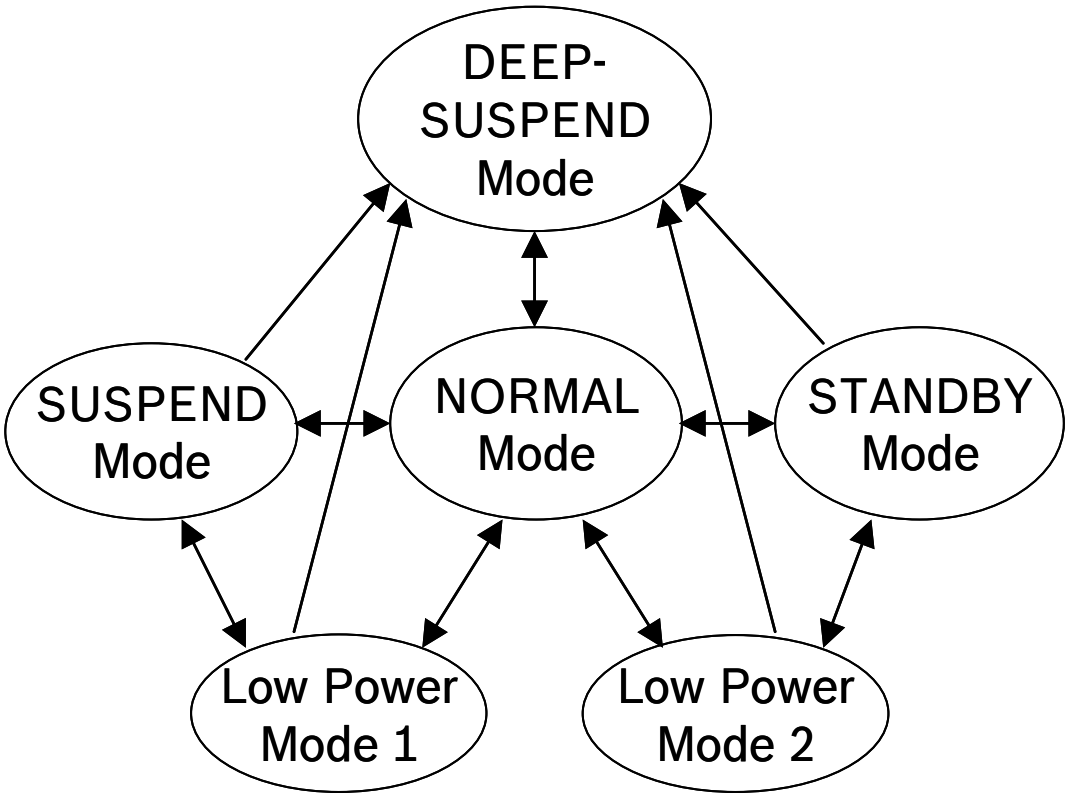

Figure 2: Power mode transition diagram

After power-up BMA223 is in normal mode so that all parts of the device are held powered-up and data acquisition is performed continuously.

In **deep-suspend** mode the device reaches the lowest possible power consumption. Only the interface section is kept alive. No data acquisition is performed and the content of the configuration registers is lost. Deep suspend mode is entered (left) by writing '1' ('0') to the *(0x11) deep_suspend* bit while *(0x11) suspend* bit is set to '0'. The I^2C watchdog timer remains functional. The *(0x11) deep_ suspend* bit, the *(0x34) spi3* bit, *(0x34) i2c_wdt_en* bit and the *(0x34) i2c_wdt_sel* bit are functional in deep-suspend mode. Equally the interrupt level and driver configuration registers *(0x20) int1_lvl*, *(0x20) int1_od*, *(0x20) int2_lvl*, and *(0x20) int2_od* are accessible. Still it is possible to enter normal mode by performing a softreset as described in chapter 4.8. Please note, that all application specific settings which are not equal to the default settings (refer to 6.2 register map), must be re-set to its designated values after leaving deep-suspend mode.

In **suspend mode** the whole analog part is powered down. No data acquisition is performed. While in suspend mode the latest acceleration data and the content of all configuration registers are kept. Writing to and reading from registers is supported except from the *(0x3F) fifo_data* register. It is possible to enter normal mode by performing a softreset as described in chapter 4.8.

Suspend mode is entered (left) by writing ´1´ (´0´) to the *(0x11) suspend* bit after bit *(0x12) lowpower_mode* has been set to '0'. Although write access to registers is supported at the full interface clock speed (SCL or SCK), a waiting period must be inserted between two consecutive write cycles (please refer also to section 7.2.1).

In **standby mode** the analog part is powered down, while the digital part remains largely operational. No data acquisition is performed. Reading and writing registers is supported without any restrictions. The latest acceleration data and the content of all configuration registers are kept. Standby mode is entered (left) by writing ´1´ (´0´) to the *(0x11) suspend* bit after bit *(0x12) lowpower_mode* has been set to '1'. It is also possible to enter normal mode by performing a softreset as described in chapter 4.8.

In **low-power mode 1**, the device is periodically switching between a sleep phase and a wake-up phase. The wake-up phase essentially corresponds to operation in normal mode with complete power-up of the circuitry. The sleep phase essentially corresponds to operation in suspend mode. Low-power mode is entered (left) by writing ´1´ (´0´) to the *(0x11) lowpower_en* bit with bit *(0x12) lowpower_mode* set to '0'. Read access to registers is possible except from the *(0x3F) fifo_data* register. However, unless the register access is synchronised with the wake-up phase, the restrictions of the suspend mode apply.

Low-power mode 2 is very similar to low-power mode 1, but register access is possible at any time without restrictions. It consumes more power than low-power mode 1. In low-power mode 2 the device is periodically switching between a sleep phase and a wake-up phase. The wake-up phase essentially corresponds to operation in normal mode with complete power-up of the circuitry. The sleep phase essentially corresponds to operation in standby mode. Low-power mode is entered (left) by writing ´1´ (´0´) to the *(0x11) lowpower_en* bit with bit *(0x12) lowpower_mode* set to '1'.

The timing behaviour of the low-power modes 1 and 2 depends on the setting of the *(0x12) sleeptimer_en* bit. When *(0x12) sleeptimer_en* is set to '0', the event-driven time-base mode (EDT) is selected. In EDT the duration of the wake-up phase depends on the number of samples required by the enabled interrupt engines. If an interrupt is detected, the device stays in the wake-up phase as long as the interrupt condition endures (non-latched interrupt), or until the latch time expires (temporary interrupt), or until the interrupt is reset (latched interrupt). If no interrupt is detected, the device enters the sleep phase immediately after the required number of acceleration samples have been taken and an active interface access cycle has ended. The EDT mode is recommended for power-critical applications which do not use the FIFO. Also, EDT mode is compatible with legacy BST sensors. Figure 3 shows the timing diagram for low-power modes 1 and 2 when EDT is selected.

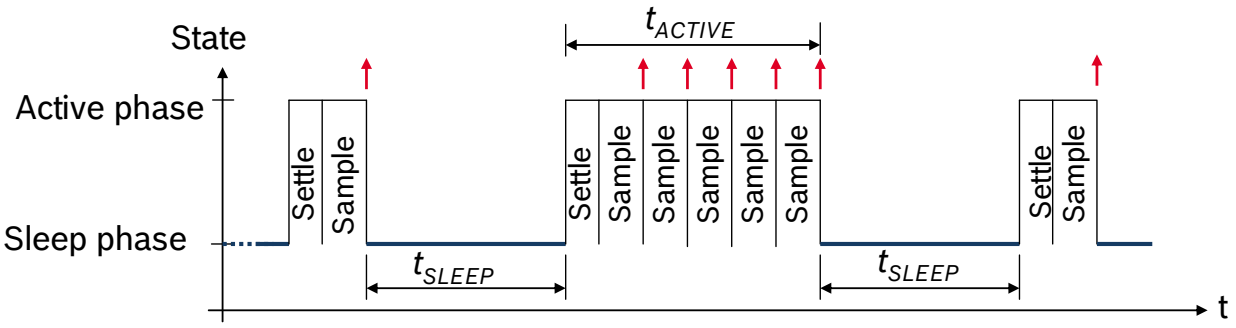

Figure 3: Timing Diagram for low-power mode 1/2, EDT

When *(0x12) sleeptimer_en* is set to '1', the equidistant-sampling mode (EST) is selected. The use of the EST mode is recommended when the FIFO is used since it ensures that equidistant samples are sampled into the FIFO regardless of whether the active phase is extended by active interrupt engines or interface activity. In EST mode the sleep time t_{SLEEP} is defined as shown in Figure 4. The FIFO sampling time t_{SAMPLE} is the sum of the sleep time t_{SLEEP} and the sensor data sampling time t_{SSMP}. Since interrupt engines can extend the active phase to exceed the sleep time t_{SLEEP}, equidistant sampling is only guaranteed if the bandwidth has been chosen such that $1/(2 * bw) = n * t_{SLEEP}$ where n is an integer. If this condition is infringed, equidistant sampling is not possible. Once the sleep time has elapsed the device will store the next available sample in the FIFO. This set-up condition is not recommended as it may result in timing jitter.

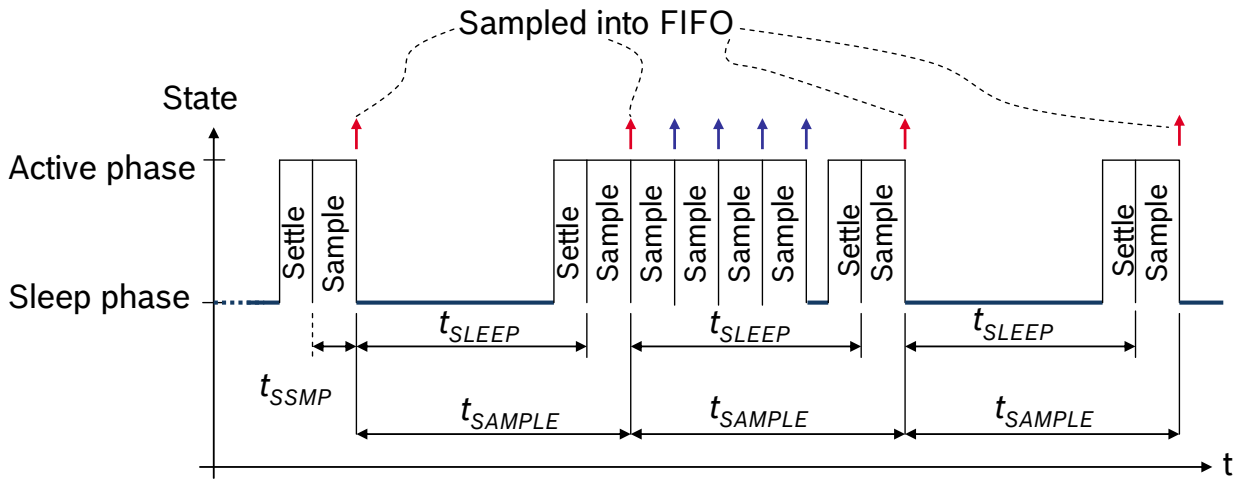

Figure 4: Timing Diagram for low-power mode 1/2, EST

The sleep time for lower-power mode 1 and 2 is set by the *(0x11) sleep_dur* bits as shown in the following table:

Table 3: Sleep phase duration settings

(0x11) sleep_dur	Sleep Phase Duration t_{sleep}
0000b	0.5ms
0001b	0.5ms
0010b	0.5ms
0011b	0.5ms
0100b	0.5ms
0101b	0.5ms
0110b	1ms
0111b	2ms
1000b	4ms
1001b	6ms
1010b	10ms
1011b	25ms
1100b	50ms
1101b	100ms
1110b	500ms
1111b	1s

The current consumption of the BMA223 in low-power mode 1 (I_{DDlp1}) and low-power mode 2 (I_{DDlp2}) can be estimated with the following formulae:

$$I_{DDlp1} \approx \frac{t_{sleep} \cdot I_{DDsum} + t_{active} \cdot I_{DD}}{t_{sleep} + t_{active}}.$$

$$I_{DDlp2} \approx \frac{t_{sleep} \cdot I_{DDsbm} + t_{active} \cdot I_{DD}}{t_{sleep} + t_{active}}$$

When estimating the length of the wake-up phase t_{active}, the corresponding typical wake-up time, $t_{w,up1}$ or $t_{w,up2}$ and t_{ut} (given in Table 4) have to be considered:

If bandwidth is >=31.25 Hz:
$t_{active} = t_{ut} + t_{w,up1} - 0.9$ ms (or $t_{active} = t_{ut} + t_{w,up2} - 0.9$ ms)
else:
$t_{active} = 4\ t_{ut} + t_{w,up1} - 0.9$ ms (or $t_{active} = 4\ t_{ut} + t_{w,up2} - 0.9$ ms)

During the wake-up phase all analog modules are held powered-up, while during the sleep phase most analog modules are powered down. Consequently, a wake-up time of more than $t_{w,up1}$ ($t_{w,up2}$) is needed to settle the analog modules so that reliable acceleration data are generated.

4.3 Sensor data

4.3.1 Acceleration data

The width of acceleration data is 8 bits given in two´s complement representation. The 8 bit data word for each axis is contained the MSB of the acceleration data output registers 0x03, 0x05, 0x07. The LSB of the acceleration data output registers contain a (0x02, 0x04, 0x06) new_data flag. Reading the acceleration data registers shall always start with the LSB part. In order to ensure the integrity of the acceleration data, the content of an MSB register is locked by reading the corresponding LSB register (shadowing procedure). When shadowing is enabled, the MSB must always be read in order to remove the data lock. The shadowing procedure can be disabled (enabled) by writing ´1´ (´0´) to the bit *shadow_dis*. With shadowing disabled, the content of both MSB and LSB registers is updated by a new value immediately. Unused bits of the LSB registers may have any value and should be ignored. The *(0x02, 0x04, 0x06) new_data* flag of each LSB register is set if the data registers have been updated. The flag is reset if either the corresponding MSB or LSB part is read.

Two different streams of acceleration data are available, unfiltered and filtered. The unfiltered data is sampled with 2kHz. The sampling rate of the filtered data depends on the selected filter bandwidth and is always twice the selected bandwidth (BW = ODR/2). Which kind of data is stored in the acceleration data registers depends on bit *(0x13) data_high_bw*. If *(0x13) data_high_bw* is ´0´ (´1´), then filtered (unfiltered) data is stored in the registers. Both data streams are offset-compensated.

The bandwidth of filtered acceleration data is determined by setting the *(0x10) bw* bit as followed:

Table 4: Bandwidth configuration

bw	Bandwidth	Update Time t_{ut}
00xxx	*)	-
01000	7.81Hz	64ms
01001	15.63Hz	32ms
01010	31.25Hz	16ms
01011	62.5Hz	8ms
01100	125Hz	4ms
01101	250Hz	2ms
01110	500Hz	1ms
01111	1000Hz	0.5ms
1xxxx	*)	-

*) Note: Settings 00xxx result in a bandwidth of 7.81 Hz; settings 1xxxx result in a bandwidth of 1000 Hz. It is recommended to actively set an application specific and an appropriate bandwidth and to use the range from ´01000b´ to ´01111b´ only in order to be compatible with future products.

The BMA223 supports four different acceleration measurement ranges. A measurement range is selected by setting the *(0x0F)* range bits as follows:

Table 5: Range selection

Range	Acceleration measurement range	Resolution
0011	±2g	15.63 mg/LSB
0101	±4g	31.25 mg/LSB
1000	±8g	62.5 mg/LSB
1100	±16g	125 mg/LSB
others	reserved	-

4.3.2 Temperature sensor

The width of temperature data is 8 bits given in two´s complement representation. Temperature values are available in the *(0x08) temp* register.

The slope of the temperature sensor is 0.5K/LSB, its center temperature is 23°C [*(0x08) temp* = 0x00].

4.4 Self-test

This feature permits to check the sensor functionality by applying electrostatic forces to the sensor core instead of external accelerations. By actually deflecting the seismic mass, the entire signal path of the sensor can be tested. Activating the self-test results in a static offset of the acceleration data; any external acceleration or gravitational force applied to the sensor during active self-test will be observed in the output as a superposition of both acceleration and self-test signal.

Before the self-test is enabled the g-range should be set to 8 g.The self-test is activated individually for each axis by writing the proper value to the *(0x32) self_test_axis* bits (´01b´ for x-axis, ´10b´ for y-axis, ´11b´ for z-axis, ´00b´ to deactivate self-test). It is possible to control the direction of the deflection through bit *(0x32) self_test_sign*. The excitation occurs in negative (positive) direction if *(0x32) self_test_sign* = ´0b´ (´1b´). The amplitude of the deflection has to be set high by writing *(0x32) self_test_amp*=´1b´. After the self-test is enabled, the user should wait 50ms before interpreting the acceleration data.

In order to ensure a proper interpretation of the self-test signal it is recommended to perform the self-test for both (positive and negative) directions and then to calculate the difference of the resulting acceleration values. Table 6 shows the minimum differences for each axis. The actually measured signal differences can be significantly larger.

Table 6: Self-test difference values

	x-axis signal	y-axis signal	z-axis signal
resulting minimum difference signal	800 mg	800 mg	400 mg

It is recommended to perform a reset of the device after a self-test has been performed. If the reset cannot be performed, the following sequence must be kept to prevent unwanted interrupt generation: disable interrupts, change parameters of interrupts, wait for at least 50ms, enable desired interrupts.

4.5 Offset compensation

Offsets in measured signals can have several causes but they are always unwanted and disturbing in many cases. Therefore, the BMA223 offers an advanced set of four digital offset compensation methods which are closely matched to each other. These are slow, fast, and manual compensation as well as inline calibration.

The compensation is performed with unfiltered data, and is then applied to both, unfiltered and filtered data. If necessary the result of this computation is saturated to prevent any overflow errors (the smallest or biggest possible value is set, depending on the sign). However, the registers used to read and write compensation values have only a width of 8 bits.

An overview of the offset compensation principle is given in figure 5:

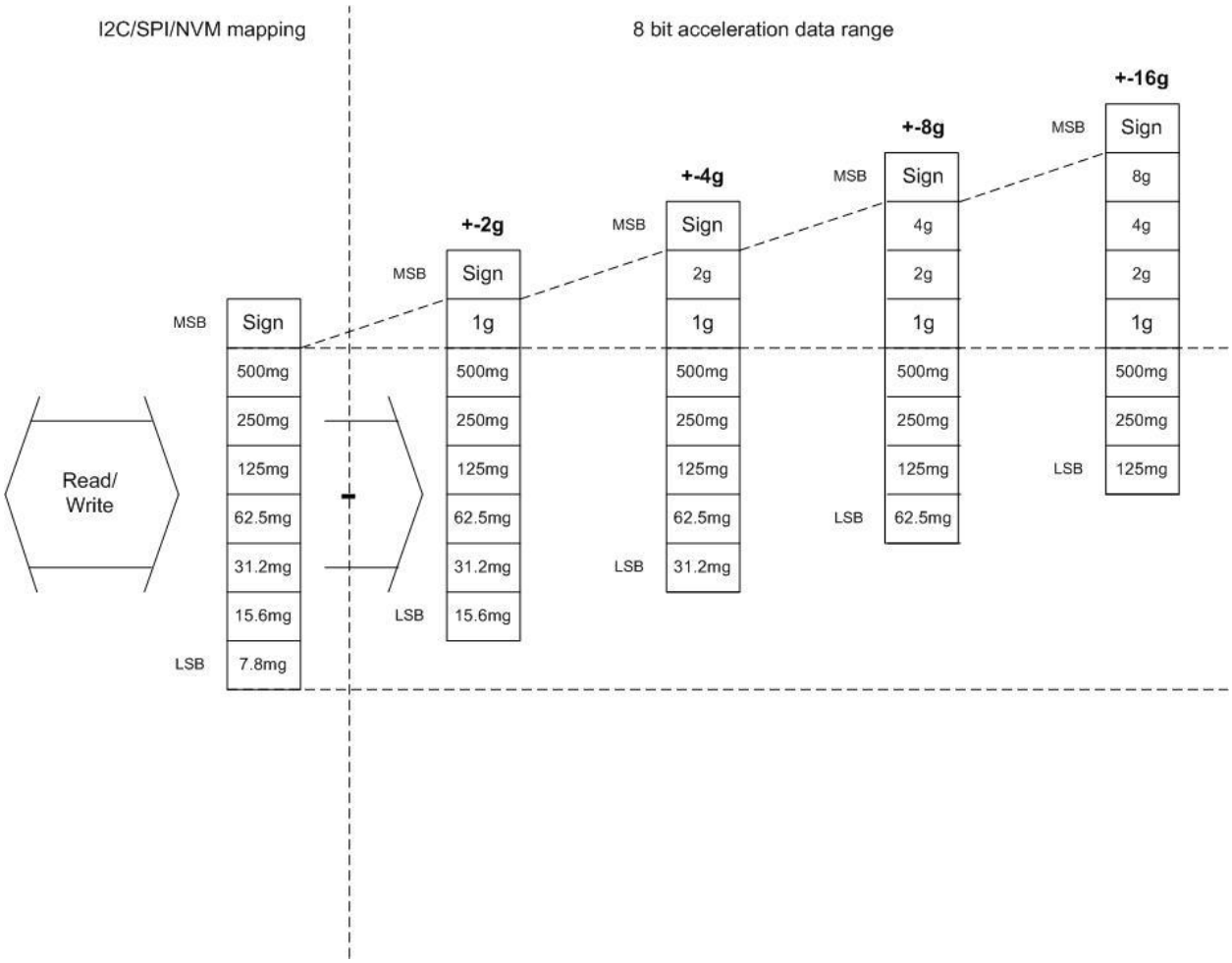

Figure 5: Principle of offset compensation

The public offset compensation registers *(0x38) offset_x*, *(0x39) offset_y*, *(0x3A) offset_z* are images of the corresponding registers in the NVM. With each image update (see section 4.6 Non-volatile memory for details) the contents of the NVM registers are written to the public registers. The public registers can be over-written by the user at any time.

Figure 5 illustrates how the offset compensation value scales with the range setting. The scaled offset compensation value is subsequently subtracted from the raw acceleration value.

By writing ´1´ to the *(0x36) offset_reset* bit, all offset compensation registers are reset to zero.

4.5.1 Slow compensation

Slow compensation is based on a 1st order high-pass filter, which continuously drives the average value of the output data stream of each axis to zero. The bandwidth of the high-pass filter is configured with bit *(0x37) cut_off* according to Table 7.

Table 7: Compensation period settings

(0x37) cut_off	high-pass filter bandwidth
0b	1
1b	10 Hz

The slow compensation can be enabled (disabled) for each axis independently by setting the bits *(0x36) hp_x_en, hp_y_en, hp_z_en* to ´1´ (´0´), respectively.

Slow compensation should not be used in combination with low-power mode. In low-power mode the conditions (availability of necessary data) for proper function of slow compensation are not fulfilled.

4.5.2 Fast compensation

Fast compensation is a one-shot process by which the compensation value is set in such a way that when added to the raw acceleration, the resulting acceleration value of each axis approaches the target value. This is best suited for “end-of-line trimming” with the customer’s device positioned in a well-defined orientation. For fast compensation the g-range has to be switched to 2g.

The algorithm in detail: An average of 16 consecutive acceleration values is computed and the difference between target value and computed value is written to *(0x38, 0x39, 0x3A) offset_filt_x/y/z*. The public registers *(0x38, 0x39, 0x3A) offset_filt_x/y/z* are updated with the contents of the internal registers (using saturation if necessary) and can be read by the user.

Fast compensation is triggered for each axis individually by setting the *(0x36) cal_trigger* bits as shown in Table 8:

Table 8: Fast compensation axis selection

(0x36) cal_trigger	Selected Axis
00b	none
01b	x
10b	y
11b	z

Register *(0x36) cal_trigger* is a write-only register. Once triggered, the status of the fast correction process is reflected in the status bit *(0x36) cal_rdy*. Bit *(0x36) cal_rdy* is ‘0’ while the correction is in progress. Otherwise it is ‘1’. Bit *(0x36) cal_rdy* is ´0´ when *(0x36) cal_trigger* is not ´00´.

For the fast offset compensation, the compensation target can be chosen by setting the bits *(0x37) offset_target_x*, *(0x37) offset_target_y*, and *(0x37) offset_target_z* according to Table 9:

Table 9: Offset target settings

(0x37) offset_target_x/y/z	Target value
00b	0g
01b	+1g
10b	-1g
11b	0g

Fast compensation should not be used in combination with any of the low-power modes. In low-power mode the conditions (availability of necessary data) for proper function of fast compensation are not fulfilled.

4.5.3 Manual compensation

The contents of the public compensation registers *(0x38, 0x39, 0x3A) offset_filt_x/y/z* can be set manually via the digital interface. It is recommended to write into these registers directly after a new data interrupt has occurred in order not to disturb running offset computations.

Writing to the offset compensation registers is not allowed while the fast compensation procedure is running.

4.5.4 Inline calibration

For certain applications, it is often desirable to calibrate the offset once and to store the compensation values permanently. This can be achieved by using one of the aforementioned offset compensation methods to determine the proper compensation values and then storing these values permanently in the NVM. See section 4.6 Non-volatile memory for details of the storing procedure.

Each time the device is reset, the compensation values are loaded from the non-volatile memory into the image registers and used for offset compensation until they are possibly overwritten using one of the other compensation methods.

4.6 Non-volatile memory

The entire memory of the BMA223 consists of three different kinds of registers: hard-wired, volatile, and non-volatile. Part of it can be both read and written by the user. Access to non-volatile memory is only possible through (volatile) image registers.

Altogether, there are eight registers (octets) with NVM backup which are accessible by the user. The addresses of the image registers range from 0x38 to 0x3C. While the addresses up to 0x3A are used for offset compensation (see 4.4 Offset Compensation), addresses 0x3B and 0x3C are general purpose registers not linked to any sensor-specific functionality.

The content of the NVM is loaded to the image registers after a reset (either POR or softreset) or after a user request which is performed by writing ´1´ to the write-only bit *(0x33) nvm_load*. As long as the image update is in progress, bit *(0x33) nvm_rdy* is ´0´, otherwise it is ´1´.

The image registers can be read and written like any other register.

Writing to the NVM is a three-step procedure:

1. Write the new contents to the image registers.
2. Write ´1´ to bit *(0x33) nvm_prog_mode* in order to unlock the NVM.
3. Write ´1´ to bit *(0x33) nvm_prog_trig* and keep ´1´ in bit *(0x33) nvm_prog_mode* in order to trigger the write process.

Writing to the NVM always renews the entire NVM contents. It is possible to check the write status by reading bit *(0x33) nvm_rdy*. While *(0x33) nvm_rdy* = ´0´, the write process is still in progress; if *(0x33) nvm_rdy* = ´1´, then writing is completed. As long as the write process is ongoing, no change of power mode and image registers is allowed. Also, the NVM write cycle must not be initiated while image registers are updated, in low-power mode, and in suspend mode.

Please note that the number of permitted NVM write-cycles is limited as specified in Table 1. The number of remaining write-cycles can be obtained by reading bits *(0x33) nvm_remain*.