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3950 Fairview Industrial Dr.
Salem, Oregon 97302
866-6-RIGADO ◆ modules@rigado.com
www.rigado.com/modules

# BMD-340 Module for Bluetooth 5 and 802.15.4

The **BMD-340** is an advanced, highly flexible, ultra-low power multiprotocol SoM that enables **Bluetooth 5** (BLE) and **IEEE 802.15.4** (Thread and Zigbee) connectivity for portable, extremely low power embedded systems. With an ARM® Cortex™-M4F CPU, integrated 2.4GHz transceiver, and an integrated antenna, the **BMD-340** provides a complete RF solution allowing faster time to market with reduced development costs. Providing full use of the **Nordic nRF52840**'s capabilities and peripherals, the **BMD-340** can power the most demanding applications, all while simplifying designs and reducing BOM costs. The **BMD-340** is an ideal solution for designs that require the latest **Bluetooth 5** features or 802.15.4 based networking for Thread. Increased integration with built in USB and 5.5V compatible DC/DC supply reduces design complexity and BOM cost, while expanding possible applications. **BMD-340** designs are footprint compatible with the **BMD-300/301/BMD-330**, providing low-cost flexibility for tiered product lineups.


## 1. Features

- Based on the Nordic nRF52840 SoC
- Bluetooth 5 Long Range, 2Mbs, and Advertising Extension support
- IEEE 802.15.4 with Thread and Zigbee support
- Complete RF solution with integrated antenna
- Integrated DC-DC converter
- No external components required
- ARM® Cortex™-M4F 32-bit processor
- ARM® TrustZone® Cryptocell 310 security
- True Random Number Generator
- Serial Wire Debug (SWD)
- Nordic SoftDevice ready
- 1MB embedded flash memory
- 256kB RAM
- 48 General Purpose I/O Pins
- -40C to +85C Temperature Range
- FCC: **2AA9B10**
- 12-bit/200KSPS ADC
- One Full-Speed USB (12Mbps)
- Four SPI Master/Slave (8 Mbps)
- Quad SPI with Execute in Place (XIP)
- Low power comparator
- Temperature sensor
- Two 2-wire Master/Slave (I2C compatible)
- I2S audio interface
- Two UARTs (w/ CTS/RTS and DMA)
- 20 channel CPU independent Programmable Peripheral Interconnect (PPI)
- Quadrature Demodulator (QDEC)
- 128-bit AES HW encryption
- 5 x 32bit, 3 x 24bit Real Timer Counters (RTC)
- NFC-A tag interface for OOB pairing
- Dimensions: 15.0 x 10.2 x 1.9mm
- IC: **12208A-10**

## 2. Applications

- Climate Control
- Lighting Products
- Safety and Security
- Home Appliances
- Access Control
- Internet of Things
- Home Health Care
- Advanced Remote Controls
- Smart Energy Management
- Low-Power Sensor Networks
- Interactive Entertainment Devices
- Environmental Monitoring
- Hotel Automation
- Office Automation

# 3. Ordering Information

Email modules@rigado.com for quotes and ordering or visit www.rigado.com/BMD-340

| Part Number | Description |
|---|---|
| BMD-340-A-R | BMD-340 module, Rev A, nRF52840-QIAA, Tape & Reel, 1000 piece multiples |
| BMD-340-A-EVK | BMD-340-A Evaluation Kit with Segger J-Link programmer |
| BMD-340-EVK | BMD-340-A Evaluation Kit with Segger J-Link programmer |

*Table 1 – Ordering Part Numbers*

# 4. Block Diagram

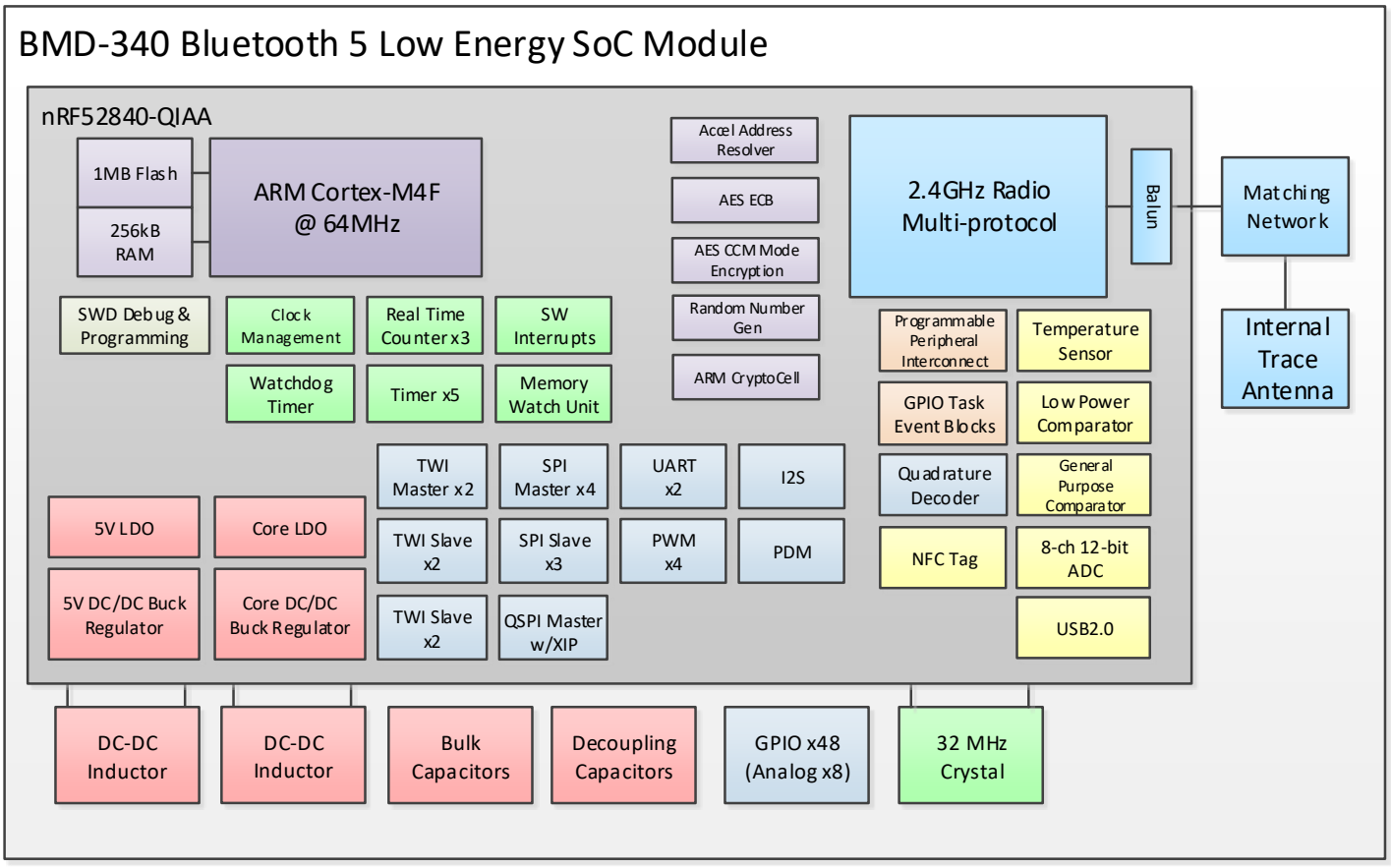


*Figure 1 – Block Diagram*

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# 5. Quick Specifications

| | | |
|---|---|---|
| **Bluetooth** | | |
| Version | 5.0 (*Bluetooth* Low Energy) Concurrent Central & Peripheral (S140) | |
| Security | AES-128 | |
| LE connections | Up to 20 as Central, 1 as Peripheral, Observer, Broadcaster (S140) | |
| **IEEE 802.15.4** | | |
| Thread Stack | OpenThread, Thread 1.1 certified | |
| Thread Security | AES-128, ARM® Cryptocell accelerated | |
| Zigbee Stack | Zigbee 3.0 | |
| **Radio** | | |
| Frequency | 2.360GHz to 2.500GHz | |
| Modulations | GFSK at 1 Mbps and 2Mbps, QPSK at 250kbps | |
| Transmit power | +8 dBm | |
| Receiver sensitivity | -93dBm (2Mbps), -96 dBm (1Mbps), -103 (125ksps BLE), -100 dBm (IEEE 802.15.4) | |
| Antenna | Integrated | |
| **Current Consumption** | | |
| TX only @ +8 dBm, 0 dBm @ 3V, DCDC enabled | 14.8 mA, 4.8 mA | |
| TX only @ +8 dBm, 0 dBm | 32.7 mA, 10.6 mA | |
| RX only @ 1 Mbps @ 3V, DCDC enabled | 4.6 mA | |
| RX only @ 1 Mbps | 9.9 mA | |
| CPU @ 64MHz from flash, from RAM | 6.3 mA, 5.2mA | |
| CPU @ 64MHz from flash, from RAM @ 3V, DCDC enabled | 3.3 mA, 2.8mA | |
| System Off, On (Supply on VDD), no RAM retention | 0.4 µA, 0.97 µA | |
| System Off, On (Supply on VDD), full 256kB RAM retention | 1.86 µA, 2.35µA | |
| **Dimensions** | | |
| BMD-340 | Length<br>Width<br>Height | 15.0 mm ± 0.3 mm<br>10.2 mm ± 0.3 mm<br>1.9 mm ± 0.1 mm |
| **Hardware** | | |
| Interfaces | SPI Master/Slave x4<br>Quad SPI x1<br>UART x2<br>Two-Wire Master/Slave (I2C) x2<br>GPIO x48 | I2S x1<br>PWM x12<br>PDM x1<br>USB 2.0 x1<br>Analog input x8 |
| Power supply | VDD: 1.7V to 3.6V, 1.75V required to start DCDC<br>VDDH: 2.5V to 5.5V<br>VBUS: 4.35V to 5.5V (For USB operation) | |
| Temperature Range | -40 to +85°C | |
| **Certifications** | | |
| FCC | FCC part 15 modular certification<br>BMD-340 FCC ID: **2AA9B10** | |
| IC | Industry Canada RSS-210 modular certification<br>BMD-340 IC: **12208A-10** | |
| CE | EN 60950-1: 2011-01<br>EN 301 489-1 V2.1.1&<br>EN 301 489-17 V3.1.1<br>EN 300 328 V2.1.1 | 3.1 (a): Health and Safety of the User<br>3.1 (b): Electromagnetic Compatibility<br><br>3.2: Effective use of spectrum allocated |
| Australia / New Zealand | AS/NZS 4268 :2012+AMDT 1:2013, Radio equipment and systems – Short range devices | |
| Bluetooth | BMD-340 RF-PHY Component (Tested) – DID: D040773; QDID: 95452 | |

*Table 2 – Quick Specifications*

# 6. Pin Descriptions

## 6.1 BMD-340

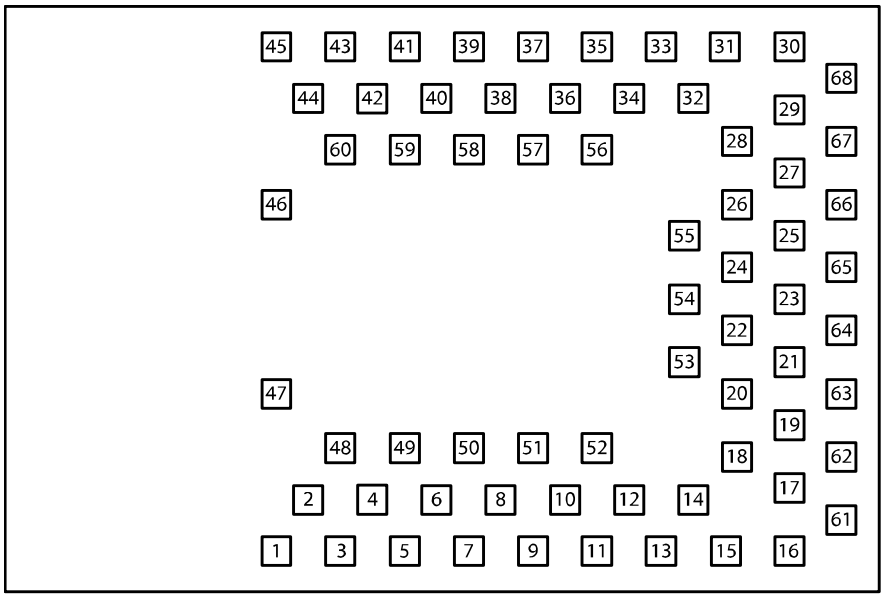



*Figure 2 – BMD-340 Pin out (Top View)*

**Pin description**

| Pin | Name | Direction | Description |
|---|---|---|---|
| 6 | P0.25 | In/Out | GPIO |
| 7 | P0.26 | In/Out | GPIO |
| 8 | P0.27 | In/Out | GPIO |
| 9 | P0.28 | In/Out | GPIO/AIN4[2] |
| 10 | P0.29 | In/Out | GPIO/AIN5[2] |
| 11 | P0.30 | In/Out | GPIO/AIN6[2] |
| 12 | P0.31 | In/Out | GPIO/AIN7[2] |
| 13 | P0.00 | In/Out | GPIO/XTAL1 (32.768kHz) |
| 14 | P0.01 | In/Out | GPIO/XTAL2 (32.768kHz) |
| 15 | P0.02 | In/Out | GPIO/AIN0[2] |
| 19 | P0.03 | In/Out | GPIO/AIN1[2] |
| 20 | P0.04 | In/Out | GPIO/AIN2 |
| 21 | P0.05 | In/Out | GPIO/AIN3 |
| 22 | P0.06 | In/Out | GPIO |
| 23 | P0.07 | In/Out | GPIO/TRACECLK |
| 24 | P0.08 | In/Out | GPIO |
| 25 | P0.09 | In/Out | GPIO/NFC1[2] |
| 26 | P0.10 | In/Out | GPIO/NFC2[2] |
| 27 | P0.11 | In/Out | GPIO/TRACEDATA[2] |
| 28 | P0.12 | In/Out | GPIO/TRACEDATA[1] |
| 31 | P0.13 | In/Out | GPIO |

| Pin | Name | Direction | Description |
|---|---|---|---|
| 32 | P0.14 | In/Out | GPIO |
| 33 | P0.15 | In/Out | GPIO |
| 34 | P0.16 | In/Out | GPIO |
| 35 | P0.17 | In/Out | GPIO |
| 36 | P0.21 | In/Out | GPIO |
| 37 | P0.19 | In/Out | GPIO |
| 38 | P0.20 | In/Out | GPIO |
| 39 | P0.18 | In/Out | GPIO/$\overline{\text{RESET}}$ |
| 40 | P0.22 | In/Out | GPIO |
| 41 | P0.23 | In/Out | GPIO |
| 42 | P0.24 | In/Out | GPIO |
| 43 | SWCLK | In | SWD Clock |
| 44 | SWDIO | In/Out | SWD IO |
| 48 | P1.05 | In/Out | GPIO[2] |
| 49 | P1.06 | In/Out | GPIO[2] |
| 50 | P1.07 | In/Out | GPIO[2] |
| 51 | P1.08 | In/Out | GPIO |
| 52 | P1.09 | In/Out | GPIO/TRACEDATA[3] |
| 53 | P1.10 | In/Out | GPIO[2] |
| 54 | P1.11 | In/Out | GPIO[2] |
| 56 | P1.00 | In/Out | GPIO/TRACEDATA[0]/SWO |
| 57 | P1.01 | In/Out | GPIO[2] |
| 58 | P1.02 | In/Out | GPIO[2] |
| 59 | P1.03 | In/Out | GPIO[2] |
| 60 | P1.04 | In/Out | GPIO[2] |
| 61 | P1.12 | In/Out | GPIO[2] |
| 62 | P1.13 | In/Out | GPIO[2] |
| 63 | P1.14 | In/Out | GPIO[2] |
| 64 | P1.15 | In/Out | GPIO[2] |
| 67 | USB-D- | In/Out | USB Data - |
| 68 | USB-D+ | In/Out | USB Data + |
| 66 | VBUS | Power | USB PHY supply: 4.35V to 5.5V in<br>Connect to USB Host device 5V supply |
| 17 | VCC[1] | Power In/Out | LV Mode: 1.7V to 3.6V in<br>HV Mode: 1.8V to 3.3V supply out[3] |
| 65 | VCCH[1] | Power | LV Mode: Connect to VCC<br>HV Mode: 2.5V to 5.5V in |
| 1, 2, 3, 4, 5, 16, 18, 29, 30, 45, 46, 47, 55 | GND | Power | Electrical Ground |

Note 1: An internal 4.7µF bulk capacitor is included on the module. However, it is good design practice to add additional bulk capacitance as required for your application, i.e. those with heavy GPIO usage and/or current draw.

Note 2: These pins are in close proximity to the nRF52 radio power supply and antenna pins. Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current on these pins. Nordic recommends using only low frequency, low-drive functions when possible.

Note 3: In HV mode, VCC acts as a regulated supply that can power other external devices. The voltage output of VCC can be configured in software but is limited to no more than VCCH-0.3V. In System Off mode VCC can supply no more than 1mA.

*Table 3 – BMD-340 Pin Descriptions*

## 6.2 Peripheral Pins

The BMD-340 features a pin muxing system that allows most internal peripherals, such as UART and SPI, to be used on any GPIO pin. This freedom in pin choice enables better optimization of designs and PCB layout. Note that only one peripheral signal can be muxed to a GPIO pin at a time. Some functions are restricted to certain pins due to additional internal circuitry required by the interface. These include: Trace signals, analog inputs, XTAL signals, USB signals, SWD interface, and reset. See Table 4 below for details:

| Peripheral | Signal | Pin Options |
|---|---|---|
| UART0, UART1 | All | P0.00-P0.31, P1.00-P1.15 |
| I2C0, I2C1 | | |
| SPI0, SPI1, SPI2, SPI3 | | |
| I2S0 | | |
| QSPI0 | | |
| PWM0, PWM1, PWM2, PWM3 | | |
| PDN0 | | |
| ADC, COMP, LPCOMP | All | P0.02-P0.05, P0.28-P0.31 (AIN0-AIN7) |
| NFC | NFC1 | P0.09 |
| | NFC2 | P0.10 |
| Reset | $\overline{\text{RESET}}$ | P0.18 |
| Trace | TRACECLK | P0.07 |
| | SWO/TRACEDATA[0] | P1.00 |
| | TRACEDATA[1] | P0.12 |
| | TRACEDATA[2] | P0.11 |
| | TRACEDATA[3] | P1.09 |
| SWD | SWD Clock | SWCLK |
| | SWD IO | SWDIO |
| 32.768kHz Crystal | XTAL1 | P0.00 |
| | XTAL2 | P0.01 |
| USB | USB Data + | USB-D+ |
| | USB Data - | USB-D- |

*Table 4 – Peripheral Pin Options*

**Note:** Some peripherals on the BMD-340 share the same memory location for their registers. This means that only one of these peripherals can be used at a time. It is possible to switch between peripherals that share the same register location by clearing and reinitializing the associated configuration registers. See the Nordic Semiconductor nRF52840 Product Specification for details.

| Peripheral ID | Base Address | Shared Peripherals | |
|---|---|---|---|
| 3 | 0x40003000 | SPI0 | I2C0 |
| 4 | 0x40004000 | SPI1 | I2C1 |

*Table 5 – Peripherals with Shared Registers*

## 6.3 BMD-300 Series Footprint Compatibility and Migration

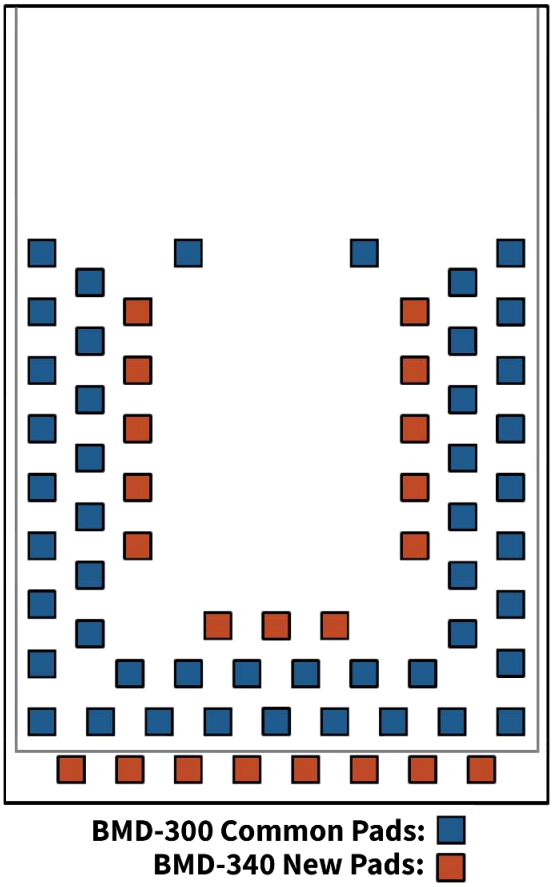



*Figure 3 – BMD-340 and BMD-300/301/330 Footprint Comparison*

The BMD-340 footprint has been designed to allow for backwards compatibility with the BMD-300, BMD-301, and BMD-330 modules with pins 1 through 47 of the BMD-340 directly mapping to the same pin numbers on the BMD-300/301/330. This allows BMD-300, BMD-301, and BMD-330 modules to be placed directly onto the BMD-340 footprint for easy migration and enabling tiered product design. Generally, all pin names and functions remain the same, except for some differences noted below. Pins 48 through 68 of the BMD-340 footprint are new pads used for new features that are not present on the BMD-300/301/330 modules, such as USB interface and additional GPIO and power connections.

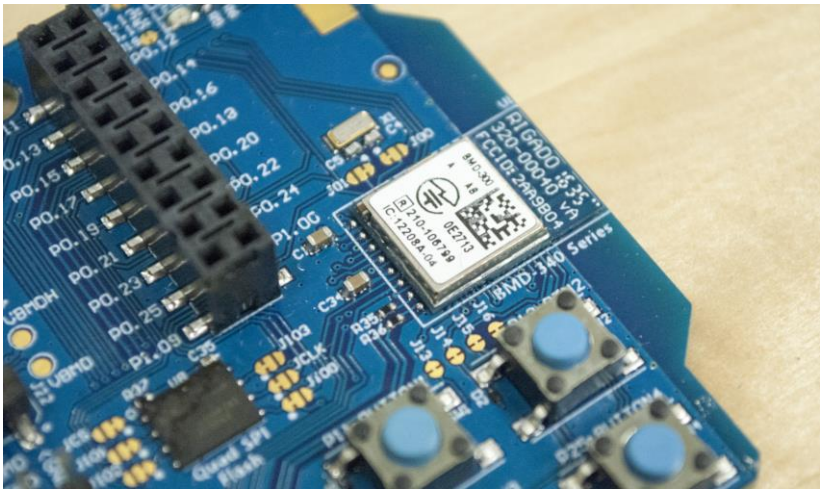


*Figure 4 – BMD-300 Module Soldered to BMD-340 Footprint*

### 6.3.1 BMD-300/301/330 to BMD-340 Pad Differences

Due to changes in the nRF52840 SoC used by the BMD-340, not all functions (such as SWO/TRACE signals) are found on the same pins as on the BMD-300/301/330. Particularly of note is the reset pin function which on the BMD-340 is now available on P0.18 instead of P0.21 as on the BMD-300/301. To maintain pin for pin compatibility of the reset signal, P0.18 and P0.21 have swapped pad locations on the BMD-340 footprint. These differences are detailed in Table 6 below:

| Pin | BMD-300/301 Name | BMD-300/301 Function | BMD-340 Name | BMD-340 Function |
|---|---|---|---|---|
| 39 | **P0.21** | GPIO/$\overline{\text{RESET}}$ | **P0.18** | GPIO/$\overline{\text{RESET}}$ |
| 38 | P0.20 | GPIO/**TRACECLK** | P0.20 | GPIO |
| 36 | **P0.18** | GPIO/**TRACEDATA[0]/SWO** | **P0.21** | GPIO |
| 34 | P0.16 | GPIO/**TRACEDATA[1]** | P0.16 | GPIO |
| 33 | P0.15 | GPIO/**TRACEDATA[2]** | P0.15 | GPIO |
| 32 | P0.14 | GPIO/**TRACEDATA[3]** | P0.14 | GPIO |
| 23 | P0.07 | GPIO | P0.07 | GPIO/**TRACECLK** |
| 56 | N/A | N/A | P1.00 | GPIO/**TRACEDATA[0]/SWO** |
| 28 | P0.12 | GPIO | P0.12 | GPIO/**TRACEDATA[1]** |
| 27 | P0.11 | GPIO | P0.11 | GPIO/**TRACEDATA[2]** |
| 52 | N/A | N/A | P1.09 | GPIO/**TRACEDATA[3]** |

*Table 6 – BMD-300/301/330 to BMD-340 Pad Differences*

### 6.3.2 BMD-300/301/330 to BMD-340 Design Migration

Existing designs incorporating the BMD-300, BMD-301, or BMD-330 module can be migrated over to the BMD-340 with the addition of a single footprint pad for VCCH (pin 65). This migration option is only suitable for applications that do not require the new USB interface, additional GPIO, or higher supply voltage functionality. The VCCH pad must be present and electrically connected to the same supply as VCC in order for the module to operate correctly. Vias underneath the BMD-340 should be tented to avoid shorts to unused module pads. Firmware written for the BMD-300/301/330 can generally be ported to the BMD-340 with minimal effort. See the Nordic Semiconductor SDK documentation for details.

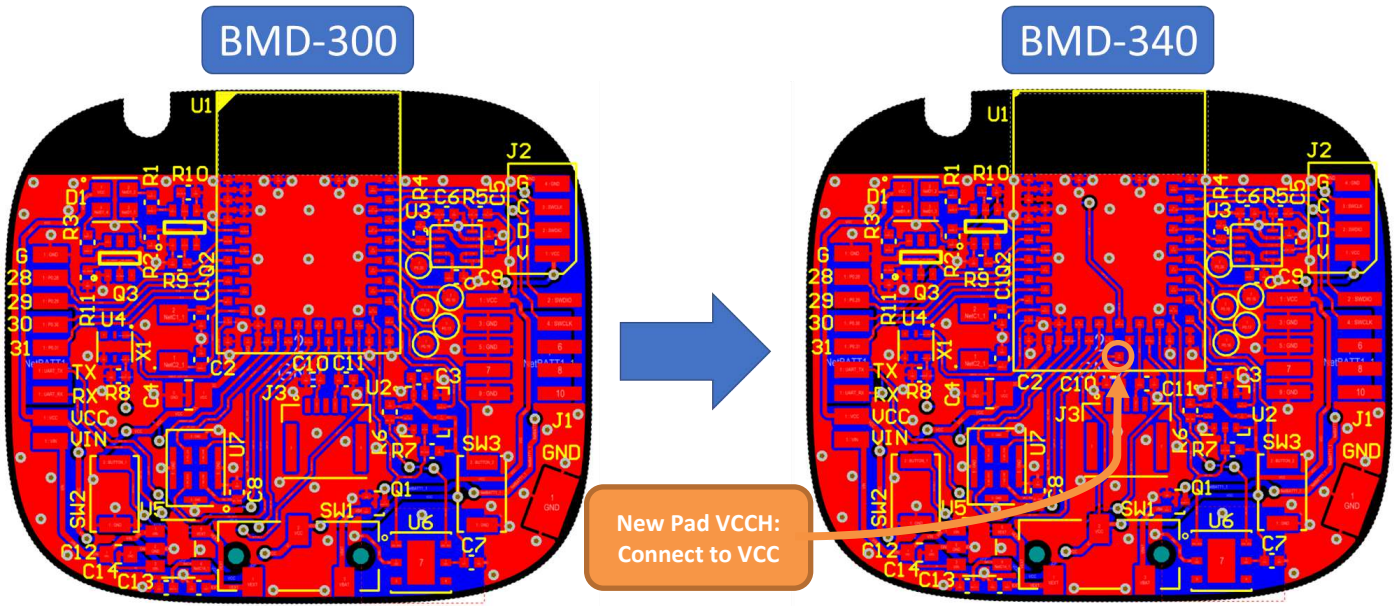



*Figure 5 – BMD-300 to BMD-340 Migration Example*

Using the BMD-340 minimal footprint, with only the additional VCCH pad added, allows BMD-300 designs to gain the following BMD-340 features with typically minor layout re-work:

- Bluetooth 5 long range modes
- IEEE 802.15.4 (Thread and Zigbee) connectivity
- Doubled Flash memory (1MB vs. 512kB)
- Quadrupled RAM (256kB vs. 64kb)
- ARM® TrustZone® Cryptocell 310 security co-processor

To take advantage of new hardware features, such as the additional UART and Quad SPI interface, the full BMD-340 footprint should be used. Designs that require the 5V DCDC converter, trace interface, USB interface, or the additional GPIO (P1.00-P1.15) must use the full BMD-340 footprint.

**Note:** Since the BMD-300/330 can be soldered to the full BMD-340 footprint, it is highly recommended that all new BMD-300 and BMD-340 projects use the full BMD-340 footprint. When migrating designs, the full BMD-340 footprint should be used whenever possible as it is better suited for use with mass production SMT processing.

## 6.4 BMD-340 Fanout Example

The following figure is a BMD-340 fanout example on a simple 2-layer PCB. This example is powered via VCCH from a USB connection. See Section 7.3 for details on power and DCDC operation.

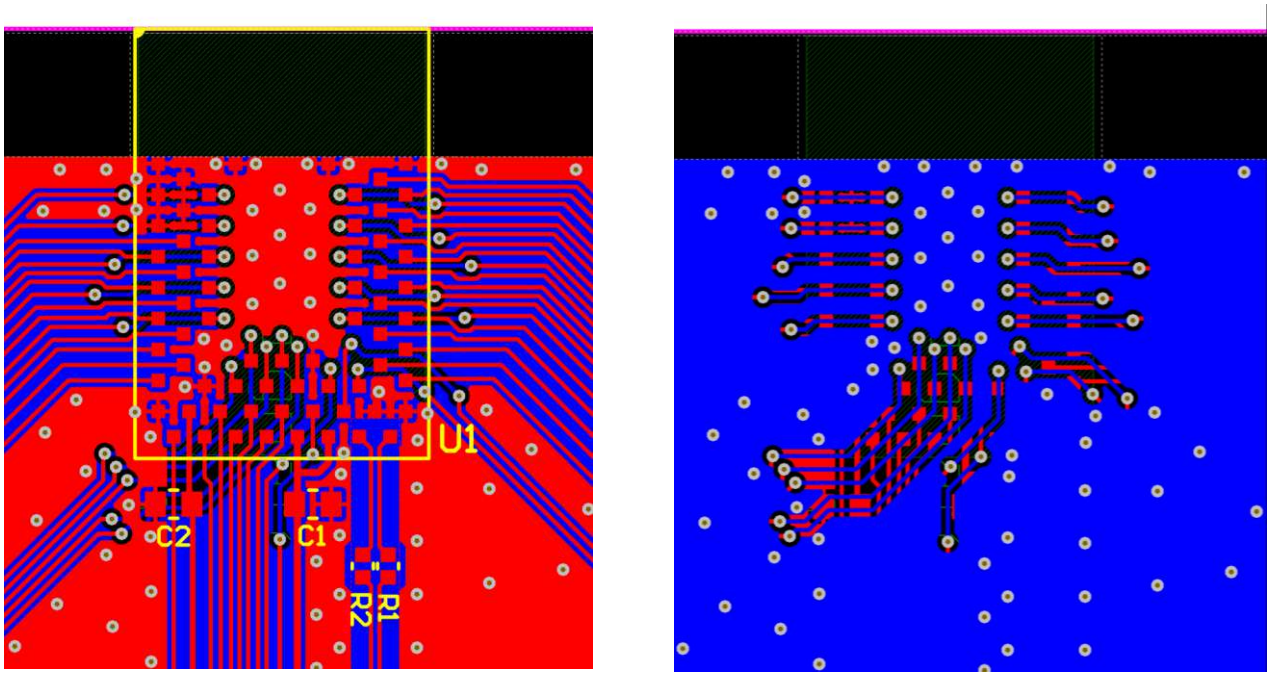



*Figure 6 – BMD-340 2 Layer Fanout Example*

# 7. Electrical Specifications

## 7.1 Absolute Maximum Ratings

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC\_MAX}$ | Voltage on VCC supply pin | -0.3 | 3.9 | V |
| $V_{CCH\_MAX}$ | Voltage on VCCH supply pin | -0.3 | 5.8 | V |
| $V_{BUS\_MAX}$ | Voltage on VBUS Supply pin | -0.3 | 5.8 | V |
| $V_{IO\_MAX}$ | Voltage on GPIO pins ($V_{CC}$ > 3.6V) | -0.3 | 3.9 | V |
| $V_{IO\_MAX}$ | Voltage on GPIO pins ($V_{CC}$ ≤ 3.6V) | -0.3 | $V_{CC}$ + 0.3V | V |
| $T_S$ | Storage Temperature Range | -40 | 125 | °C |

*Table 7 – Absolute Maximum Ratings*

## 7.2 Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC\_IN}$ | VCC operating supply voltage in | 1.7 | 3.0 | 3.6 | V |
| $V_{CC\_START}$ | VCC DCDC starting voltage | 1.75 | - | - | V |
| $V_{CCH\_HV}$ | VCCH operating supply voltage in | 2.5 | 5.0 | 5.5 | V |
| $V_{BUS\_IN}$ | VBUS operating supply voltage in | 4.35 | 5.0 | 5.5 | V |
| $T_{R\_VCC}$ | VCC Supply rise time (0V to 1.7V) | - | - | 60 | ms |
| $T_{R\_VCCH}$ | VCCH Supply rise time (0V to 3.7V)[1] | - | - | 1 | ms |
| $T_A$ | Operating Ambient Temperature Range | -40 | 25 | 85 | °C |

Note 1: Applies when module is configured to use HV mode. When using LV mode $T_{R\_VCC}$ applies. See Nordic nRF52840 Rev 1 errata [202] for details on $T_{R\_VCCH}$ requirement.

*Table 8 – Operating Conditions*

## 7.3 Power and DCDC Configuration

**Important Note Regarding REG0:** Initial mass production silicon (Nordic Rev 1) for the nRF52840 includes some errata that affect the REG0 regulator. The REG0 DC-DC converter mode cannot be used reliably. The LDO mode of REG0 can be used in High Voltage mode but when applying power the input voltage must have a rise time of 1ms or less. Due to the rise time constraint and higher current consumption of LDO mode compared to DCDC, High Voltage mode should be considered non-functional for most applications and should not be used on ES2 and Revision A BMD-340 modules. See Nordic nRF52840 errata 197 and 202 for more details. These errata are expected to be corrected in future production silicon releases and subsequent revisions of the BMD-340 module. Contact Rigado for timing and details.

The BMD-340 has two internal regulator stages that each contain an LDO and DCDC regulator. The first regulator, REG0, is fed by the VCCH pin and can accept a source voltage of 2.5V to 5.5V. The output of REG0 is connected to the VCC pin and the input of the second regulator stage REG1. REG1 supplies power to the module core and can accept an input source voltage of 1.7V to 3.6V. Depending on how the VCC and VCCH pins are connected, the module will operate in one of two modes: Normal/Low Voltage (LV) or High Voltage (HV). The voltage present on the VCC pin is always the GPIO high logic level voltage, regardless of power mode.

To enter LV Mode, the same source voltage is applied to both the VCC and VCCH pins causing REG0 to automatically shut down leaving only the REG1 stage active. To enter HV, the source voltage is only applied to VCCH causing the VCC pin to become an output source supplied by REG0.

| Mode | Pin | Name | Connection |
|---|---|---|---|
| Normal (LV) | 17 | VCC | 1.7V to 3.6V source in |
| | 65 | VCCH | Same source as VCC |
| High Voltage (HV) | 17 | VCC | 1.8V to 3.3V supply out |
| | 65 | VCCH | 2.5V to 5.5V source in |

*Table 9 – Power Mode Pin Connections*

**Important:** in both LV and HV mode, the GPIO logic level voltage is determined by the VCC pin. In HV mode, all external devices that are connected to the BMD-340's GPIO must either be powered by the module (from VCC) or use level translation.

REG0 can supply a maximum current of ~50mA for the module and external circuits in System On Mode and 1mA in System Off Mode. External circuits powered from VCC in HV mode should be limited to no more than 20mA to ensure stability.

### 7.3.1 USB Power

The USB interface on the BMD-340 can be used when the module is in either Normal (LV) or High Voltage (HV) mode. The BMD-340 USB PHY is powered by a dedicated, internal LDO regulator that is fed by the VBUS pin (66). This means that applying power to only the VBUS pin will not power the rest of the module. In order for the USB PHY to operate, VBUS must be externally powered.

## 7.3.2 Normal (LV) Power Mode Examples

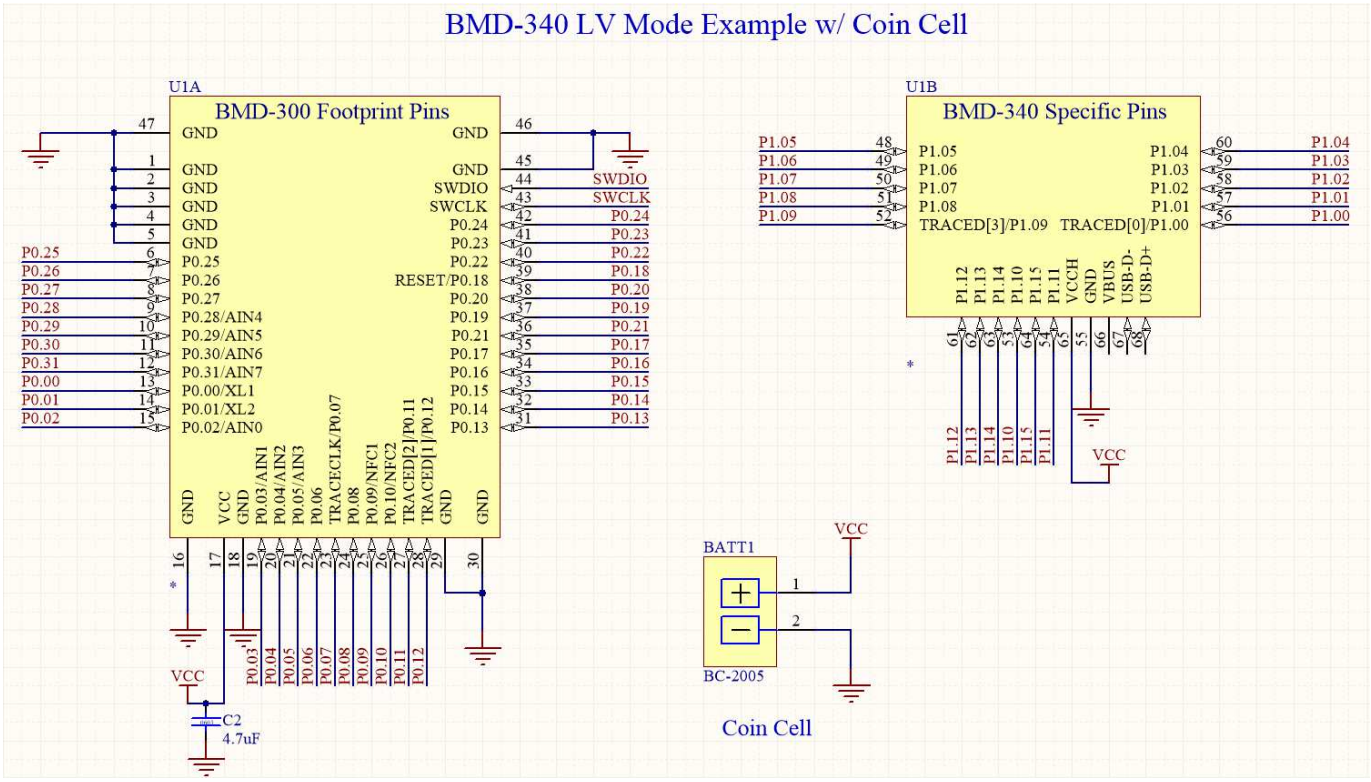



*Figure 7 – LV Mode w/ Coin Cell Example*

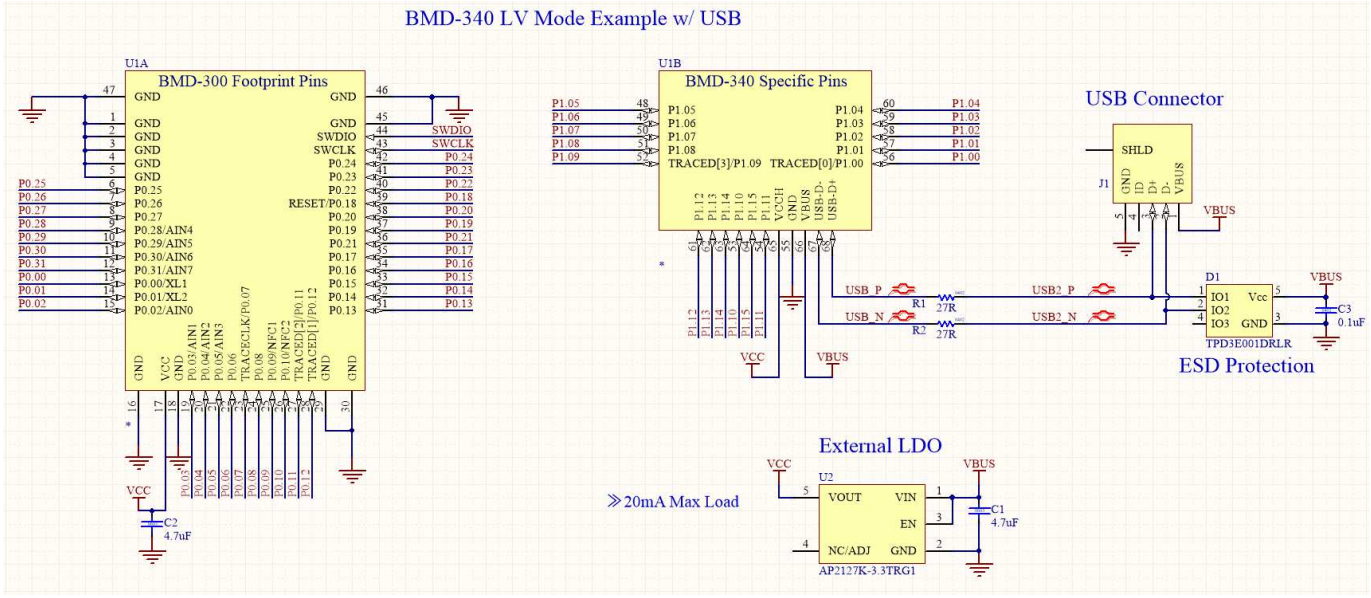



*Figure 8 – LV Mode Example w/ USB and External Regulator*

## 7.3.3 High Voltage (HV) Power Mode Examples

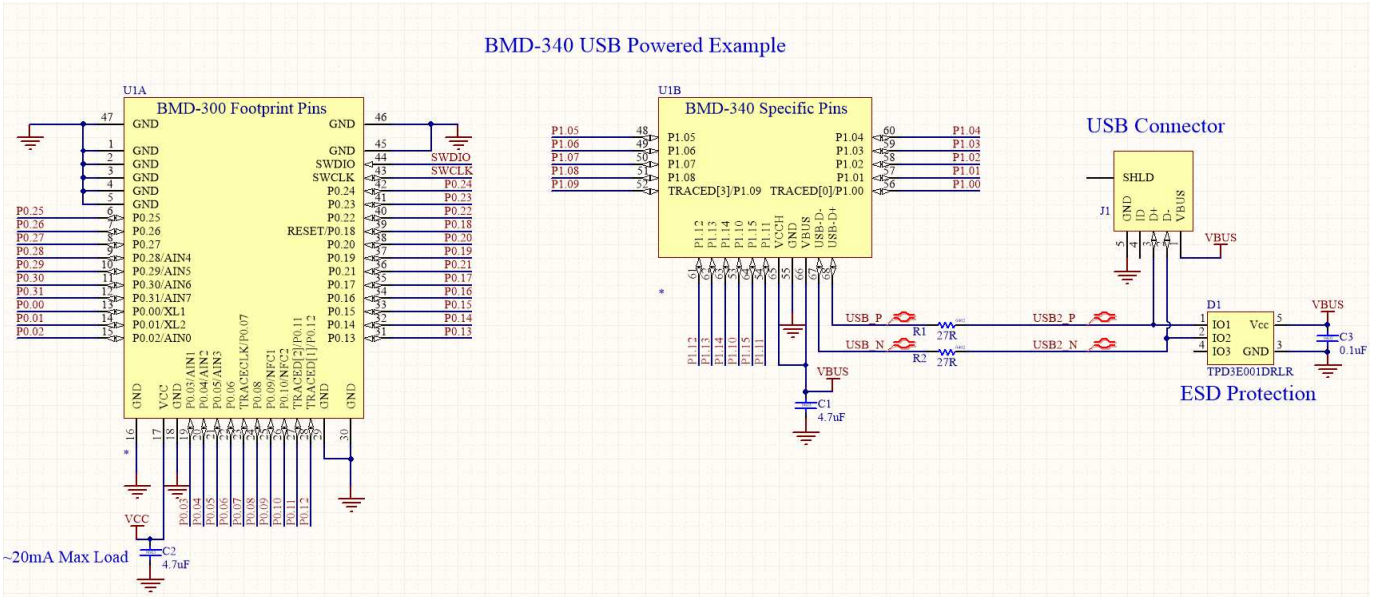



*Figure 9 – USB Powered HV Mode Example*

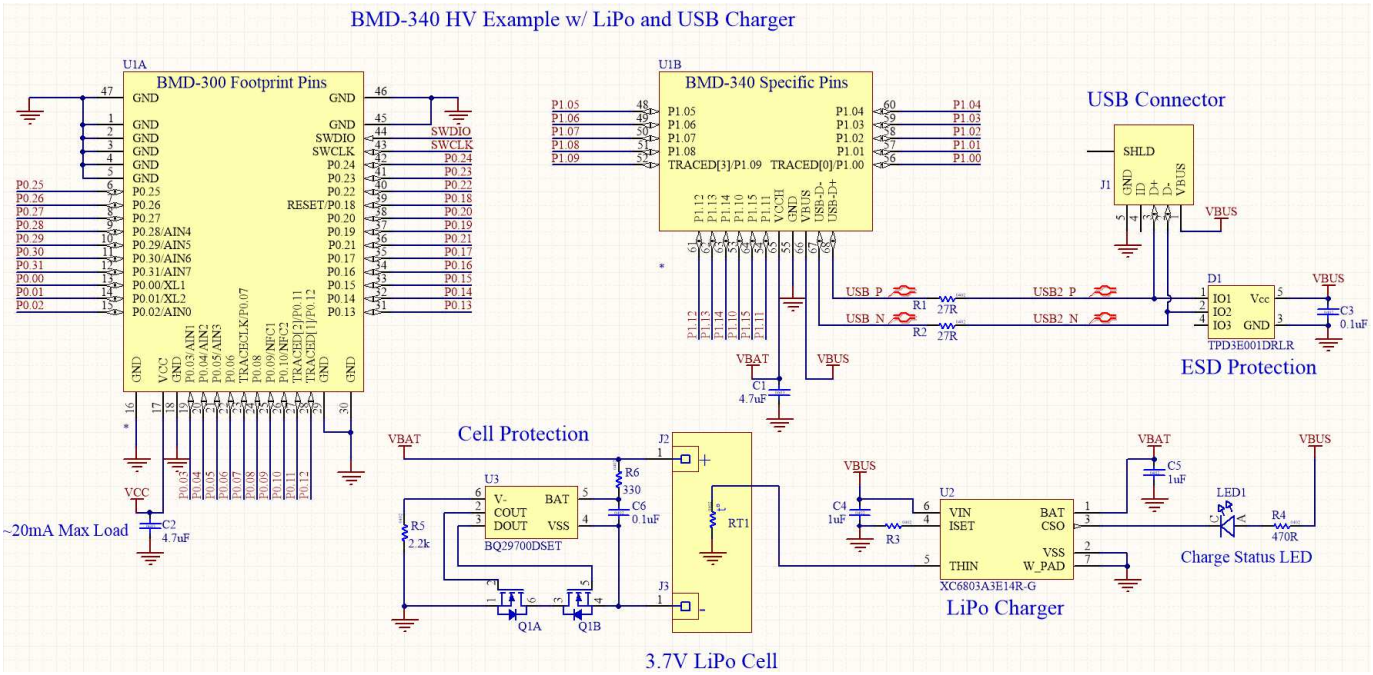



*Figure 10 – LiPo Powered HV Example w/ USB Charger*

**Important:** the LiPo circuit above is meant to be a generic example of how the BMD-340's power modes can be used. Great care must be taken when integrating Lithium-Ion batteries into a design. Protection circuits suitable for the type of battery used and the application must always be implemented.

## 7.4 General Purpose I/O

The general purpose I/O is organized as two ports enabling access and control of the 48 available GPIO pins. The first port allows access of P0.00 to P0.31, similar to the one port available on the BMD-300/301. The second port, new to the BMD-340, allows access to P1.00 to P1.15. Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- All pins can be individually configured to carry serial interface or quadrature demodulator signals

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 0.7 x $V_{CC}$ | - | $V_{CC}$ | V |
| $V_{IL}$ | Input Low Voltage | $V_{SS}$ | - | 0.3 x $V_{CC}$ | V |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ – 0.4 | - | $V_{CC}$ | V |
| $V_{OL}$ | Output Low Voltage | $V_{SS}$ | - | $V_{SS}$ + 0.4 | V |
| $R_{PU}$ | Pull-up Resistance | 11 | 13 | 16 | kΩ |
| $R_{PD}$ | Pull-down Resistance | 11 | 13 | 16 | kΩ |

*Table 10 – GPIO*

## 7.5 Module RESET

GPIO pin P0.18 may be used for a hardware reset. In order to utilize P0.18 as a hardware reset, the UICR registers PSELRESET[0] and PSELRESET[1] must be set alike, to the value of 0x7FFFFFD2. When P0.18 is programmed as $\overline{\text{RESET}}$, the internal pull-up is automatically enabled. Rigado and Nordic example applications and development kits program P0.18 as $\overline{\text{RESET}}$.

## 7.6 Debug & Programming

The BMD-340 supports the two pin Serial Wire Debug (SWD) interface and offers flexible and powerful mechanisms for non-intrusive debugging of program code. Breakpoints, single stepping, and instruction trace capture of code execution flow are part of this support.

The BMD-340 also supports ETM and ITM trace. Trace data from the ETM and the ITM is sent to an external debugger via a 4-bit wide parallel trace port. In addition to parallel trace, the TPIU supports serial trace via the Serial Wire Output (SWO) trace protocol.

## 7.7 Clocks

The BMD-340 requires two clocks, a high frequency clock and a low frequency clock.

The high frequency clock is provided on-module by a high-accuracy 32-MHz crystal as required by the nRF52840 for radio operation.

The low frequency clock can be provided internally by an RC oscillator or synthesized from the fast clock; or externally by a 32.768 kHz crystal. An external crystal provides the lowest power consumption and greatest accuracy. Using the internal RC oscillator with calibration provides acceptable performance for BLE applications at a reduced cost and slight increase in power consumption. Note: the ANT protocol requires the use of an external crystal.

### 32.768 kHz Crystal (LFXO)

| Symbol | Parameter | Typ. | Max. | Unit |
|---|---|---|---|---|
| $F_{NOM\_LFXO}$ | Crystal frequency | 32.768 | - | kHz |
| $F_{TOL\_LFXO\_BLE}$ | Frequency tolerance, BLE applications | - | ±250 | ppm |
| $C_{L\_LFXO}$ | Load Capacitance | - | 12.5 | pF |
| $C_{0\_LFXO}$ | Shunt Capacitance | - | 2 | pF |
| $R_{S\_LFXO}$ | Equivalent series resistance | - | 100 | kΩ |
| $C_{pin}$ | Input Capacitance on XL1 & XL2 pads | 4 | - | pF |

*Table 11 – 32.768 kHz Crystal*

### 32.768 kHz Oscillator Comparison

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LFXO}$ | Current for 32.768kHz Crystal Oscillator | - | 0.23 | - | µA |
| $I_{LFRC}$ | Current for 32.768kHz RC Oscillator | - | 0.7 | 1 | µA |
| $I_{LFSYNT}$ | Current for 32.768kHz Synthesized Oscillator | - | 100 | - | µA |
| $f_{TOL\_LFXO\_BLE}$ | Frequency Tolerance, 32.768kHz Crystal Oscillator (BLE Stack)[1] | - | - | ±250 | ppm |
| $f_{TOL\_LFXO\_ANT}$ | Frequency Tolerance, 32.768kHz Crystal Oscillator (ANT Stack)[1] | - | - | ±50 | ppm |
| $f_{TOL\_LFRC}$ | Frequency Tolerance, 32.768kHz RC Oscillator | - | - | ±2 | % |
| $f_{TOL\_CAL\_LFRC}$ | Frequency tolerance, 32.768kHz RC after calibration | - | - | ±250 | ppm |
| $f_{TOL\_LFSYNT}$ | Frequency Tolerance, 32.768kHz Synthesized Oscillator | - | - | ±48 | ppm |
| Note 1: $f_{TOL\_LFXO\_BLE}$ and $f_{TOL\_LFXO\_ANT}$ are the max allowed for BLE and ANT applications. Actual tolerance depends on the crystal used. | | | | | |

*Table 12 – 32.768 kHz Oscillator*

# 8. Firmware

## 8.1 Factory Image

The BMD-340 module is not loaded with a factory firmware image. The unique Rigado MAC address is printed on the module label and is also programmed into the UICR.

## 8.2 SoftDevices

Nordic Semiconductor protocol stacks for Bluetooth and ANT are known as SoftDevices. SoftDevices are pre-compiled, pre-linked binary files. SoftDevices can be programmed in nRF52 series SoCs and are downloadable from the Nordic website. The BMD-340 with the nRF52840 SoC supports the S140 (BLE Central & Peripheral) SoftDevice.

### 8.2.1 S140

The S140 SoftDevice is a Bluetooth® low energy (BLE) Central and Peripheral protocol stack solution supporting up to twenty connections with an additional Observer and a Broadcaster role all running concurrently. The S140 SoftDevice integrates a BLE Controller and Host, and provides a full and flexible API for building Bluetooth Smart nRF52 System on Chip (SoC) solutions. The S140 Softdevice is an extension of the S132 V3.0 Softdevice adding support for Bluetooth 5.

**Key Features**

- *Bluetooth 5 compliant low energy single-mode protocol stack suitable for Bluetooth Smart products*
- *Concurrent Central, Observer, Peripheral, and Broadcaster roles with up to twenty concurrent connections along with one observer and one broadcaster*
  - *Configurable number of connections and bandwidth per connection to optimize memory and performance*
  - *Configurable attribute table size*
  - *Custom UUID support*
  - *Link layer*
  - *LL Privacy*
  - *LE Data Packet Length Extension*
  - *L2CAP, ATT, and SM protocols*
  - *LE Secure Connections pairing model*
  - *GATT and GAP APIs*
  - *GATT Client and Server*
  - *Configurable ATT MTU*
- *Complementary nRF5 SDK including Bluetooth profiles and example applications*
- *Master Boot Record for over-the-air device firmware update*
  - *SoftDevice, application, and bootloader can be updated separately*
- *Memory isolation between the application and the protocol stack for robustness and security*
- *Thread-safe supervisor-call based API*
- *Asynchronous, event-driven behavior*
- *No RTOS dependency*
  - *Any RTOS can be used*
- *No link-time dependencies*
  - *Standard ARM® Cortex®-M4 project configuration for application development*
- *Support for concurrent and non-concurrent multiprotocol operation*
  - *Concurrent with the Bluetooth stack using Radio Timeslot API*
  - *Alternate protocol stack in application space*

## 8.3 IEEE 802.15.4 (Thread and Zigbee)

IEEE 802.15.4 based protocols, such as Thread and Zigbee, on the BMD-340 are not implemented using a Softdevice. Nordic Semiconductor provides an IEEE 802.15.4 compliant MAC stack which does not require a Softdevice to be loaded to operate. Nordic Semiconductor also provides pre-compiled Thread and Zigbee stacks. See developer.nordicsemi.com/nRF5_SDK/doc/ for more information on developing applications that utilize IEEE 802.15.4. Both allow for concurrent operation with BLE SoftDevices.

## 8.4 MAC Address Info

The BMD-340 modules comes preprogrammed with a unique MAC address from the factory. The MAC address is also printed on a 2D barcode on the top of the module.


*Figure 11 – BMD-340 MAC Address on Label*

The 6-byte BLE Radio MAC address is stored in the nRF52840 UICR at NRF_UICR_BASE+0x80 LSB first. Please read the MAC Address Provisioning application note if you are not using the built in bootloader to avoid erasing/overwriting the MAC address during programming. **Important:** If full memory protection is enabled, the UICR cannot be read via the SWD interface. If performing a full-erase, the MAC can then only be recovered from the 2D barcode and human-readable text.

**UICR Register:**
NRF_UICR + 0x80 (0x10001080): MAC_Addr [0] (0xZZ)
NRF_UICR + 0x81 (0x10001081): MAC_Addr [1] (0xYY)
NRF_UICR + 0x82 (0x10001082): MAC_Addr [2] (0xXX)
NRF_UICR + 0x83 (0x10001083): MAC_Addr [3] (0x93)
NRF_UICR + 0x84 (0x10001084): MAC_Addr [4] (0x54)
NRF_UICR + 0x85 (0x10001085): MAC_Addr [5] (0x94)

# 9. Mechanical Data

## 9.1 Mechanical Dimensions

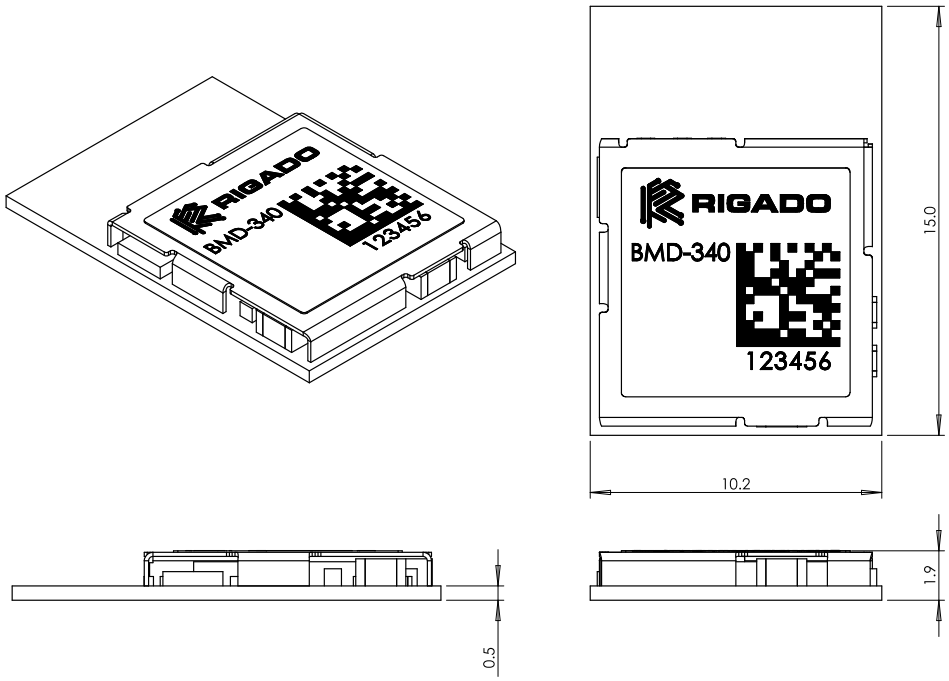



*Figure 12 – BMD-340 Module Dimensions*

**(All dimensions are in mm)**

## 9.2 Recommended PCB Land Pads

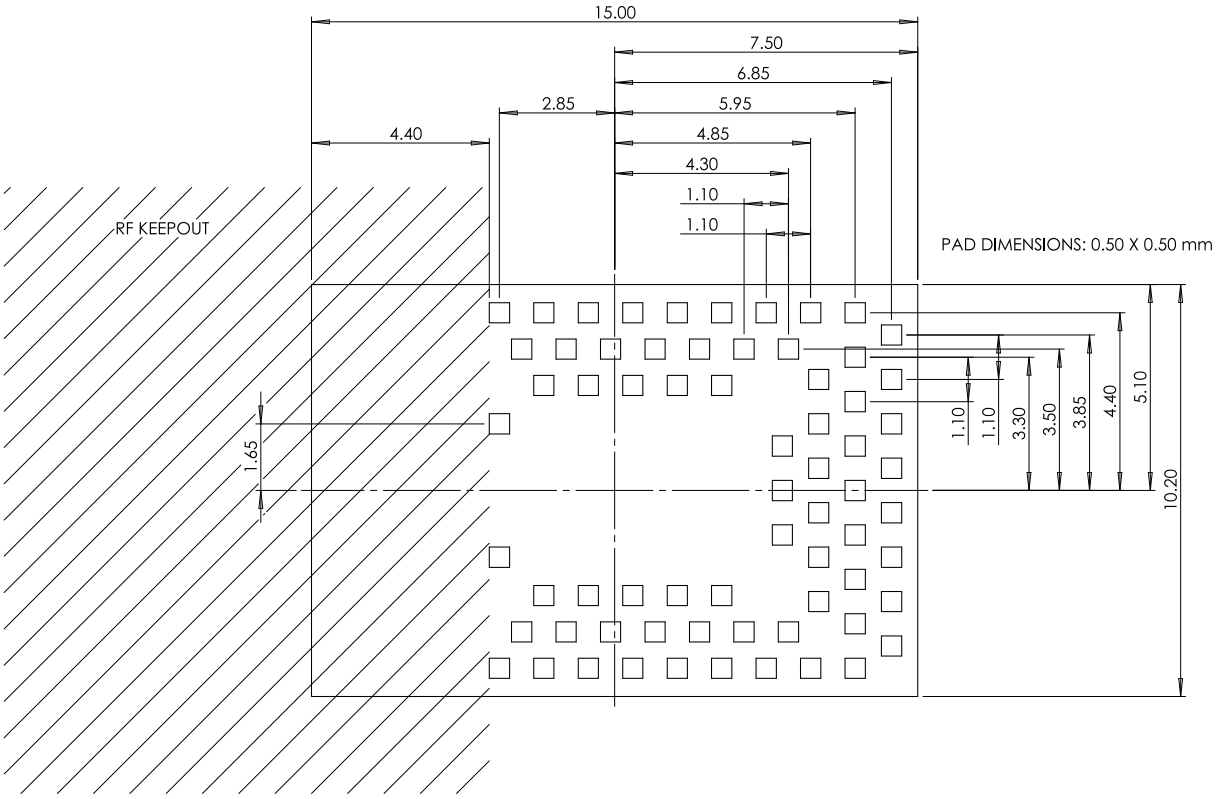



*Figure 13 – BMD-340/301 Dimensions (Top View)*

**(All dimensions are in mm)**

# 10. Module Marking


*Figure 14 – BMD-340 Module Marking*

# 11. RF Design Notes

## 11.1 Recommended RF Layout & Ground Plane

The integrated antenna requires a suitable ground plane to radiate effectively.
The area under and extending out from the antenna portion of the module should be kept clear of copper and other metal. The module should be placed at the edge of the PCB with the antenna edge facing out. Reducing the ground plane from that shown in Figure 15 will reduce the effective radiated power.

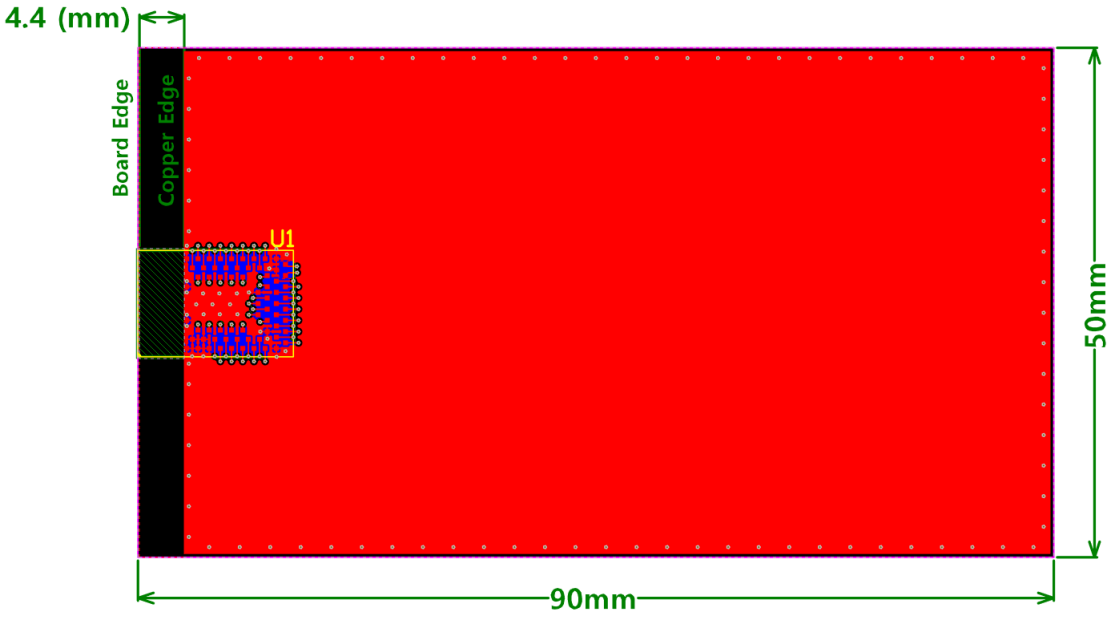



*Figure 15 – BMD-340 RF Example based on EVAL Board*

## 11.2 Mechanical Enclosure

Care should be taken when designing and placing the module into an enclosure. Metal should be kept clear from the antenna area, both above and below. Any metal around the module can negatively impact RF performance.

The module is designed and tuned for the antenna and RF components to be in free air. Any potting, epoxy fill, plastic over-molding, or conformal coating can negatively impact RF performance and must be evaluated by the customer.

## 11.3 Antenna Patterns

Antenna patterns are based on the BMD-340 Evaluation Kit with a ground plane size of 109mm x 56mm. X-Y-Z orientation is shown in Figure 16:

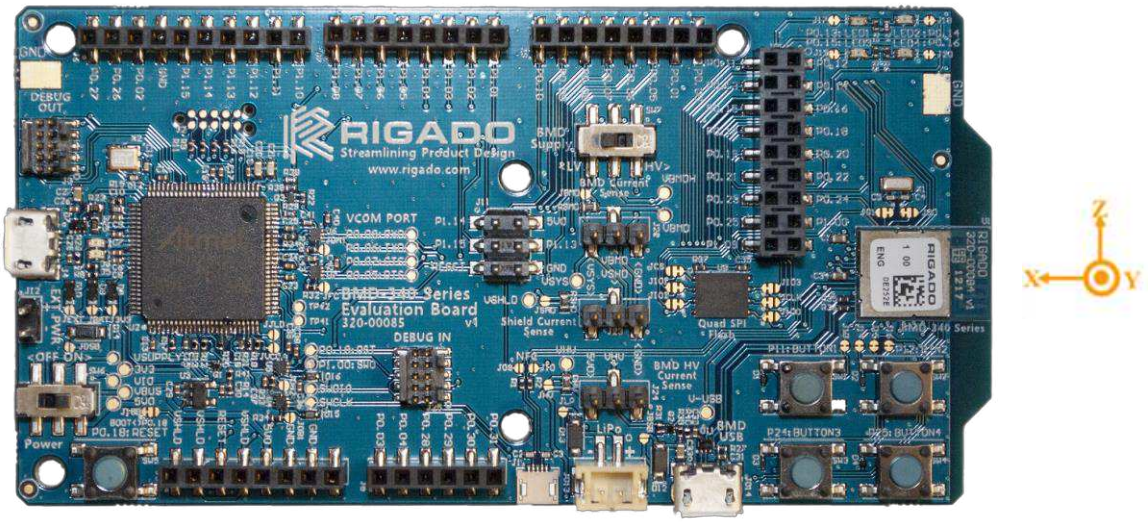
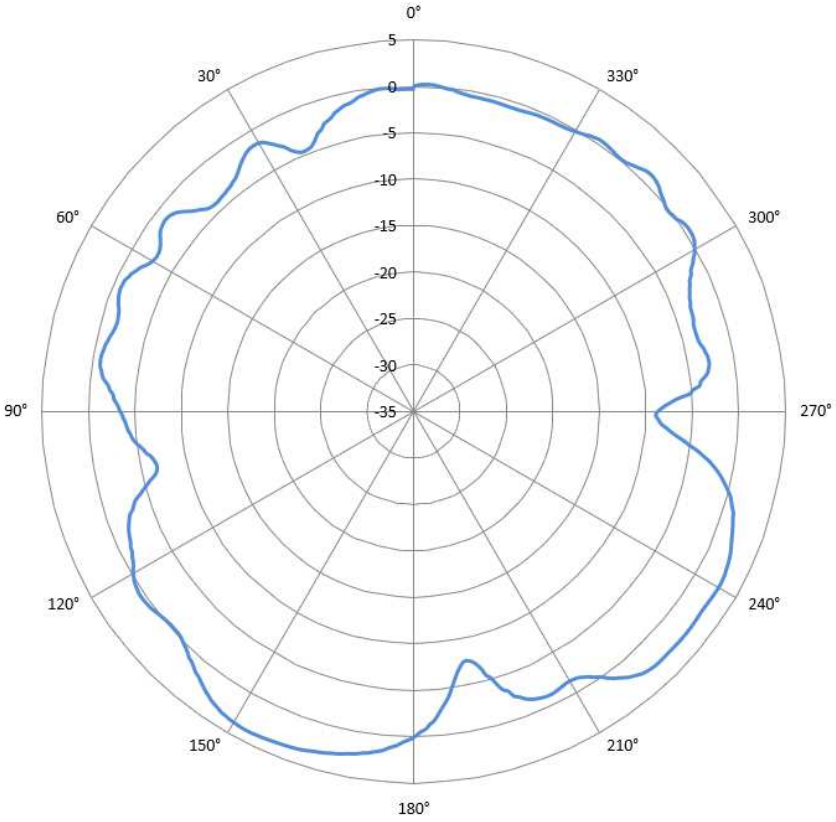
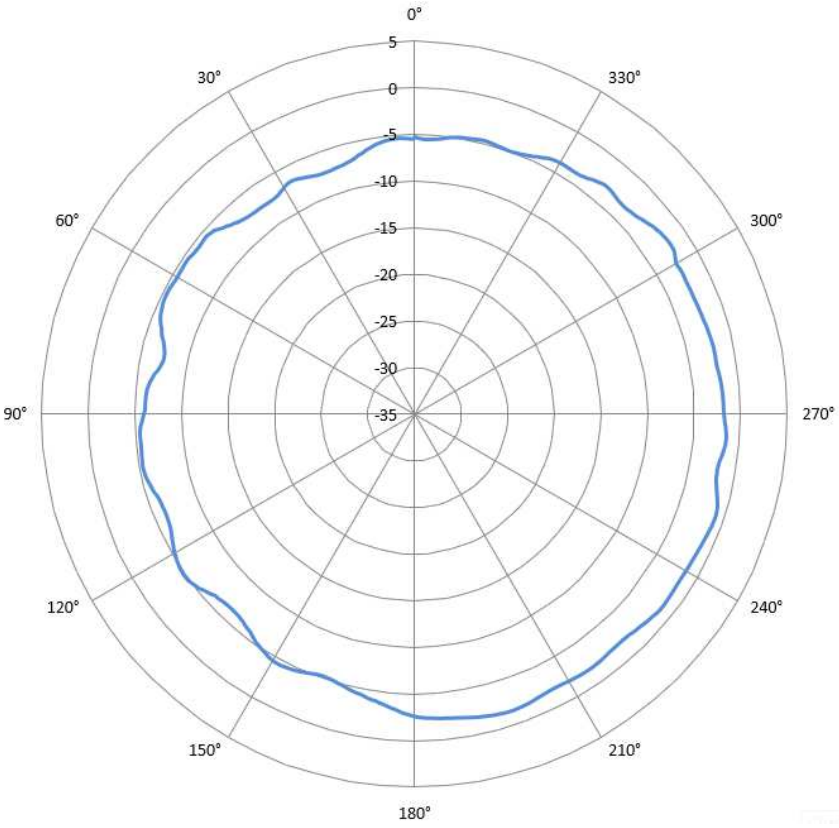



*Figure 16 – X-Y-Z Antenna Orientation*

#### 11.3.1.1 X-Z Plane




#### 11.3.1.2 Y-Z Plane



### 11.3.1.3 X-Y Plane