Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

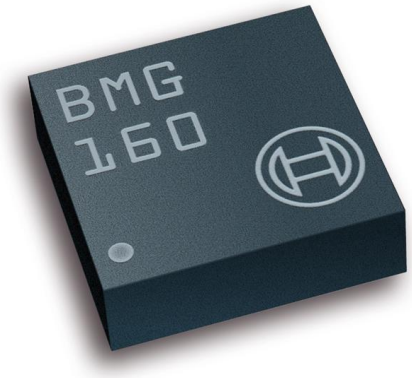
Data sheet

BMG160

Digital, triaxial gyroscope sensor

Bosch Sensortec

BOSCH
Invented for life



BMG160: Data sheet

Document revision	1.2
Document release date	06 May 2014
Document number	BST-BMG160-DS000-09
Technical reference code(s)	0 273 142 007
Notes	Data in this document are subject to change without notice. Product photos and pictures are for illustration purposes only and may differ from the real product's appearance. Not intended for publishing

BMG160

16BIT, DIGITAL, TRIAXIAL ±125°/S TO ±2000°/S GYROSCOPE SENSOR

3MM X 3MM X 0.95MM LGA PACKAGE

Key features

- 3-axis integrated gyroscope
- 16 bit digital resolution
- Switchable full-scale ranges: in total 5 ranges
- V_{DD}: 2.4 ... 3.6V / V_{DDIO}: 1.2 ... 3.6V
- Interrupt engine
- Low power consumption <5mA
- Short start-up time of 30ms
- Wake-up time in fast power-up mode only 10ms
- Operating temperature: -40°C ... +85°C
- I^2C and SPI interface (4-wire and 3-wire, SPI mode 0 and mode 3)
- Low-pass filters
- Fast and slow offset controller (FOC and SOC)
- Small footprint 12 pin LGA package, 3mm x 3mm x 0.95mm
- MSL level 1
- RoHS compliant, halogen-free, Pb-free
- Temperture Sensor

Typical applications

- Cell-phones
- Human machine interface devices
- Gaming
- Image stabilization
- Gesture recognition
- Indoor navigation

General Description

The BMG160 is a 3-axis angular rate sensor that is made of a surface micro machined sensing element and an evaluation ASIC.

Both parts are packed into one single LGA 3.0mm x 3.0mm x 0.95mm housing.

The BMG160 is designed to meet requirements for consumer applications such as image stabilization (DSC and camera-phone), gaming and pointing devices. It is capable to measure angular rates in three perpendicular room dimensions, the x-, y- and z-axis, and to provide the corresponding output signals. The BMG160 is fitted with digital bi-directional SPI and I^2C interfaces for optimum system integration.

The BMG160 offers a variable V_{DDIO} voltage range from 1.2V to 3.6V and can be programmed to optimize functionality, performance and power consumption in customer specific applications. In addition it features an on-chip interrupt controller enabling motion-based applications without use of a microcontroller.

Index of Contents

1. Specification

If not stated otherwise, the given values are over lifetime and full performance temperature and voltage ranges, minimum/maximum values are ±3σ.

1.1 Electrical specification

Table 1: Electrical parameter specification

GYROSCOPE OPERATING CONDITIONS						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Supply Voltage Internal Domains	V_{DD}		2.4	3.0	3.6	V
Supply Voltage I/O Domain	V_{DDIO}		1.2	2.4	3.6	V
Voltage Input Low Level	V_{IL}	SPI & I²C			$0.3V_{DDIO}$	-
Voltage Input High Level	V_{IH}	SPI & I²C	$0.7V_{DDIO}$			-
Voltage Output Low Level	V_{OL}	V_{DDIO} = 1.2V I_{OL} = 3mA, SPI & I²C			$0.23V_{DDIO}$	-
Voltage Output High Level	V_{OH}	V_{DDIO} = 1.2V I_{OH} = 3mA, SPI	$0.8V_{DDIO}$			-

1.2 Electrical and physical characteristics, measurement performance

Table 2: Electrical characteristics

GYROSCOPE OPERATING CONDITIONS						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Range	R_{FS125}	Selectable via serial digital interface		125		°/s
	R_{FS250}			250		°/s
	R_{FS500}			500		°/s
	R_{FS1000}			1,000		°/s
	R_{FS2000}			2,000		°/s

Supply Current in Normal Mode	I_{DD}	see[1]		5		mA
Supply Current in Fast Power-up Mode	I_{DDfpm}	see[1]		2.5		mA
Supply Current in Suspend - Mode	I_{DDsum}	see[1], digital and analog (only IF active)		25		µA
Supply Current in Deep Suspend - Mode	I_{DDdsum}	see[1]		<5		µA
Start-up time	t_{su}	to ±1°/s of final value; from power-off		30		ms
Wake-up time	t_{wusm}	From suspend- and deep suspend-modes		30		ms
Wake-up time	t_{wufpm}	From fast power-up mode		10		ms
Non-volatile memory (NVM) write-cycles	n_{NVM}				15	cycles
Operating Temperature	T_A	full performance	-40		+85	°C
Sensitivity		Ta=25°C, R_{FS2000}		16.4		LSB/°/s
		Ta=25°C, R_{FS1000}		32.8		LSB/°/s
		Ta=25°C, R_{FS500}		65.6		LSB/°/s
		Ta=25°C, R_{FS250}		131.2		LSB/°/s
		Ta=25°C, R_{FS125}		262.4		LSB/°/s
Sensitivity tolerance		Ta=25°C, R_{FS2000}		±1		%
Sensitivity Change over Temperature	TCS	Nominal V_{DD} supplies -40°C ≤ T_A ≤ +85°C R_{FS2000}		±0.03		%/K

[1] Conditions of current consumption if not specified otherwise: TA=25°C, BW_Gyro=1kHz, VDD=2.4V, VDDIO=1.8V, digital protocol on, no streaming data

Nonlinearity	NL	best fit straight line R_{FS1000}, R_{FS2000}		±0.05		%FS
g- Sensitivity		Sensitivity to acceleration stimuli in all three axis (frequency <20kHz)			0.1	°/s/g
Zero-rate Offset	Off Ω_x Ω_y and Ω_z	Nominal V_{DD} supplies T_A=25°C, Slow and fast offset cancellation off		±1		°/s
Zero-Ω Offset Change over Temperature	TCO	Nominal V_{DD} supplies -40°C ≤ T_A ≤ +85°C R_{FS2000}		±0.015		°/s per K
Output Noise	n_{rms}	rms, BW=47Hz (@ 0.014°/s/√Hz)		0.1		°/s
Bandwidth BW	f_{-3dB}			unfiltered 230 116 64 47 32 23 12		Hz
Data rate (set of x,y,z rate)				2000 1000 400 200 100		Hz
Data rate tolerance(set of x,y,z rate)				±0.3		%
Cross Axis Sensitivity		Sensitivity to stimuli in non-sense-direction		±1		%
Temperature Sensor Measurement Range	T_S		-40		85	°C

Temperature Sensor Slope	dT_S			0.5		K/LSB
Temperature Sensor Offset	OT_S			5 ±3		K

2. Absolute maximum ratings

Table 3: Absolute maximum ratings

Parameter	Condition	Min	Max	Units
Voltage at Supply Pin (<1s)	V_{DD} Pin	-0.3	4.25	V
	V_{DDIO} Pin	-0.3	4.25	V
Voltage at any Logic Pin	Non-Supply Pin	-0.3	V_{DDIO}+0.3	V
Passive Storage Temp. Range	≤ 65% rel. H.	-50	+150	°C
None-volatile memory (NVM) Data Retention	T = 85°C, after 15 cycles	10		y
Mechanical Shock	Duration ≤ 200µs		10,000	g
	Duration ≤ 1.0ms		2,000	g
	Free fall onto hard surfaces		1.8	m
ESD	HBM, at any Pin		2	kV
	CDM		500	V
	MM		200	V

Note:
Stress above these limits may cause damage to the device. Exceeding the specified electrical limits may affect the device reliability or cause malfunction.

3. Block diagram

Figure 1 shows the basic building blocks of the BMG160:

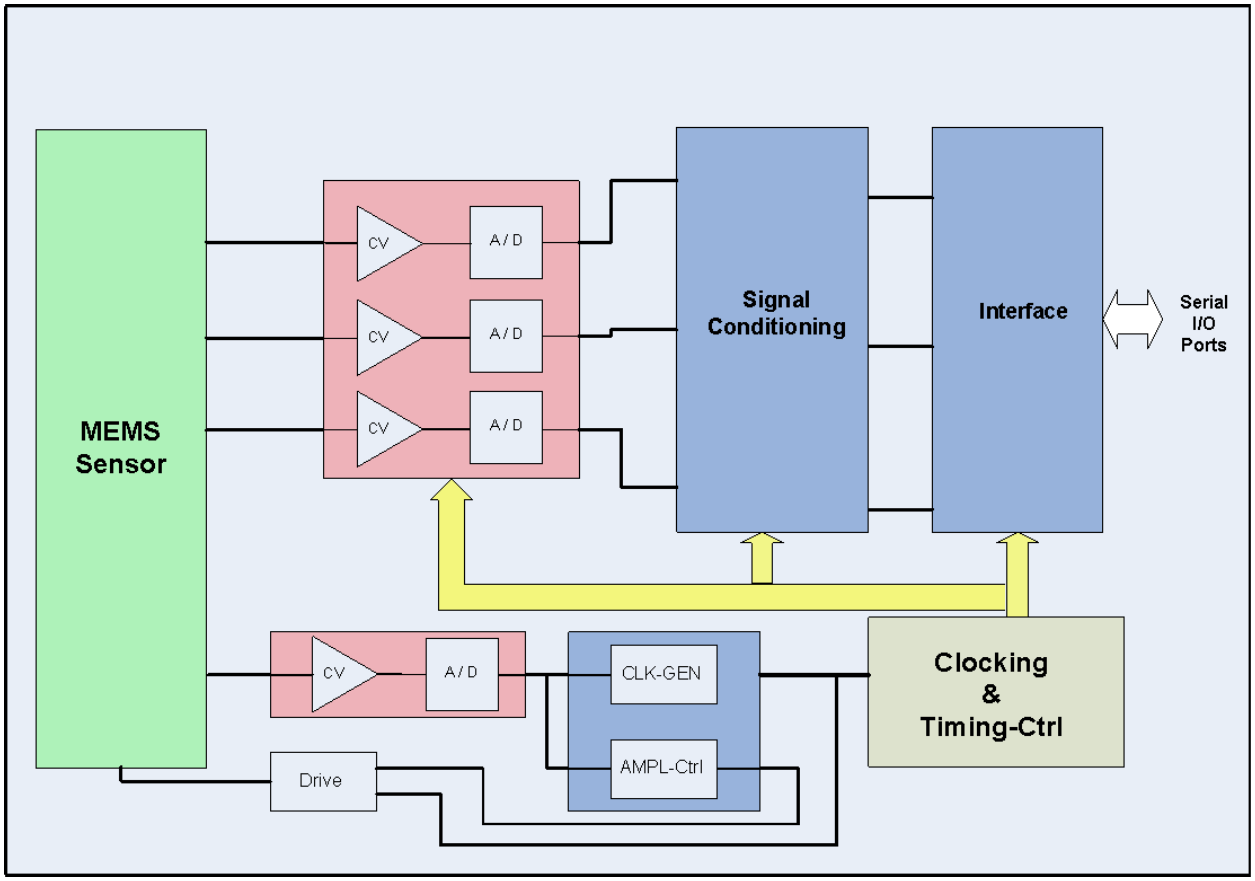


Figure 1: Block diagram of BMG160

4. Functional description

Note: Default values for registers can be found in chapter 6.

4.1 Supply voltage and power management

The BMG160 has two distinct power supply pins:
• V_{DD} is the main power supply for the internal blocks;
• V_{DDIO} is a separate power supply pin mainly used for the supply of the interface

There are no limitations on the voltage levels of both pins relative to each other, as long as each of them lies within its operating range. Furthermore, the device can be completely switched off (V_{DD} = 0V) while keeping the V_{DDIO} supply on (V_{DDIO} > 0V) or vice versa.

When the V_{DDIO} supply is switched off, all interface pins (CSB, SDI, SCK, PS) must be kept close to GND_{IO} potential.

The device contains a power-on reset (POR) generator. It resets the logic part and the register values after powering-on V_{DD} and V_{DDIO}. Please note, that all application specific settings which are not equal to the default settings (refer to 6.2 register map), must be re-set to their designated values after POR.

In case the I²C interface shall be used, a direct electrical connection between V_{DDIO} supply and the PS pin is needed in order to ensure reliable protocol selection. For SPI interface mode the PS pin must be directly connected to GND_{IO}.

4.2 Power modes

The BMG160 has 4 different power modes. Besides normal mode, which represents the fully operational state of the device, there are 3 energy saving modes: deep-suspend mode, suspend mode, and fast power up

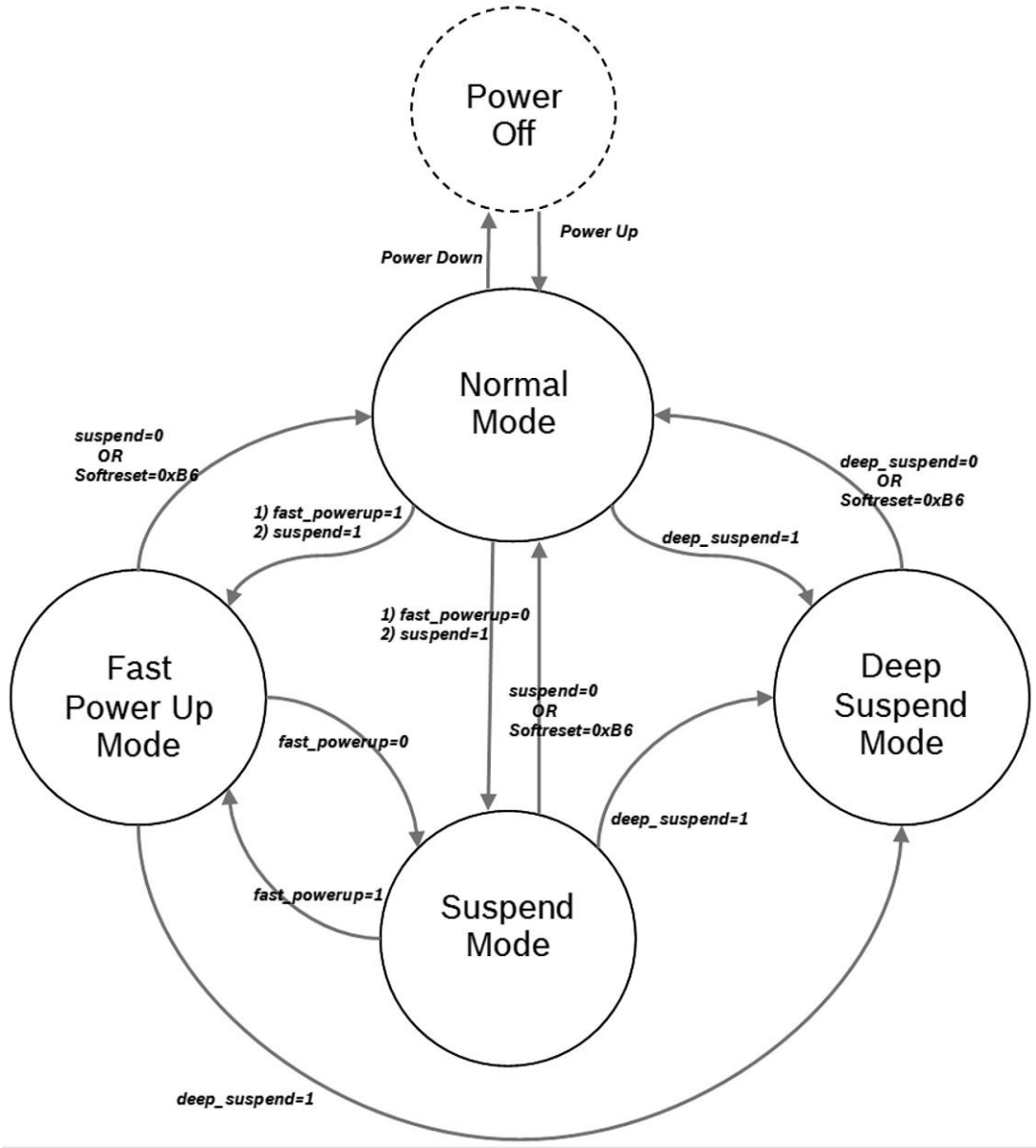


Figure 2: Block diagram of the power modes of BMG160

After power-up BMG160 is in normal mode so that all parts of the device are held powered-up and data acquisition is performed continuously.

In **deep-suspend mode** the device reaches the lowest possible power consumption. Only the interface section is kept alive. No data acquisition is performed and the content of the configuration registers is lost. Deep suspend mode is entered (left) by writing '1' ('0') to the *(0x11) deep_suspend* bit. The I^2C watchdog timer remains functional. The *(0x11) deep_suspend* bit, the *(0x34) spi3* bit, *(0x34) i2c_wdt_en* bit and the *(0x34) i2c_wdt_sel* bit are functional in deep-suspend mode. Equally the interrupt level and driver configuration registers *(0x20) int1_lvl*, *(0x20) int1_od*, *(0x20) int2_lvl*, and *(0x20) int2_od* are accessible. Still it is possible to enter normal mode by writing to the *(0x14) softreset* register. Please note, that all application specific settings which are not equal to the default settings (refer to 6.2 register map), must be re-set to its designated values after leaving deep-suspend mode.

In **suspend mode** the whole analog part is powered down. No data acquisition is performed. While in suspend mode the latest rate data and the content of all configuration registers are kept. The only supported operations are reading registers as well as writing to the *(0x14) softreset* register.

Suspend mode is entered (left) by writing ´1´ (´0´) to the *(0x11) suspend* bit. Bit *(0x12) fast_power_up* must be set to '0'.

Although write access to registers is supported at the full interface clock speed (SCL or SCK), a waiting period must be inserted between two consecutive write cycles (please refer also to section 7.2.1).

In **external wake-up mode**, when the device is in deep suspend mode or suspend mode, it can be woken-up by external trigger to Pin INT1/2. Register settings:

Table 4

ext_trig_sel<1:0>	Trigger source
'00'	No
'01'	INT1 pin
'10'	INT2 pin
'11'	SDO pin (SPI3 mode)

In **fast power-up mode** the sensing analog part is powered down, while the drive and the digital part remains operational. No data acquisition is performed. Reading and writing registers as well as writing to the *(0x14) softreset* register are supported without any restrictions. The latest rate data and the content of all configuration registers are kept. Fast power-up mode is entered (left) by writing ´1´ (´0´) to the *(0x11) suspend* bit with bit *(0x12) fast_power_up* set to '1'.

4.2.1 Advanced power-saving modes

In addition to the power modes described in Figure 2, there are other advanced power modes that can be used to optimize the power consumption of the BMG160.
The power_save_mode is set by setting power_save_mode=´1´ (reg 0x12). This power mode implements a duty cycle and change between normal mode and fast-power-up mode. By setting the sleep_dur (time in ms in fast-power-up mode) (0x11 bits <1:3>) and auto_sleep_dur

(time in ms in normal mode) (0x12 bits <0:2>) different timings can be used. Some of these settings allow the sensor to consume less than 3mA. See also diagram below:

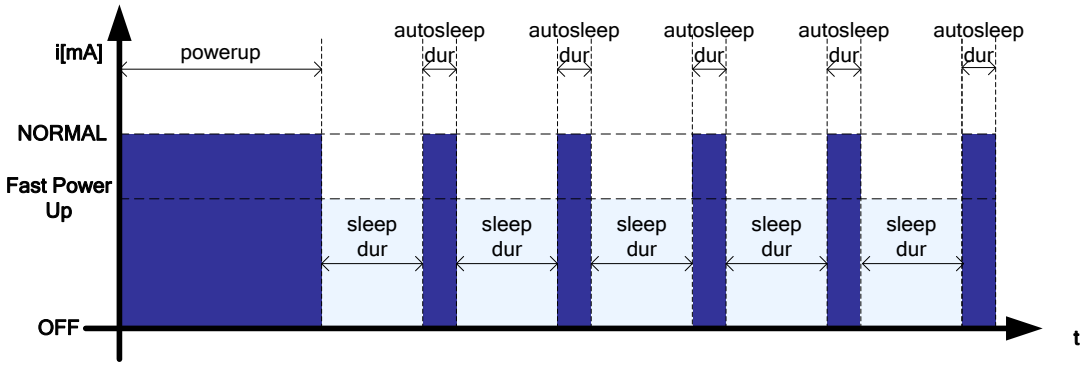


Figure 3: Duty-cycling

The possible configuration for the autosleep_dur and sleep_dur are indicated in the table below:

Table 5

sleep_dur<2:0>	Time (ms)
'000'	2 ms
'001'	4 ms
'010'	5 ms
'011'	8 ms
'100'	10 ms
'101'	15 ms
'110'	18 ms
'111'	20 ms

Table 6

autosleep_dur<2:0>	Time (ms)
'000'	Not allowed
'001'	4 ms
'010'	5 ms
'011'	8 ms
'100'	10 ms
'101'	15 ms
'110'	20 ms
'111'	40 ms

The only restriction for the use of the power save mode comes from the configuration of the digital filter bandwidth (reg 0x10). For each Bandwidth configuration, a minimum autlosleep_dur must be ensured. For example, for Bandwidth=47Hz, the minimum autosleep_dur is 5ms. This is specified in the table below. For sleep_dur there is no restriction.

Table 7

bw<3:0>	Bandwidth (Hz)	Mini Autosleep_dur (ms)
'0111'	32 Hz	20 ms
'0110'	64 Hz	10 ms
'0101'	12 Hz	20 ms
'0100'	23 Hz	10 ms
'0011'	47 Hz	5 ms
'0010'	116 Hz	4 ms
'0001'	230 Hz	4 ms
'0000'	Unfiltered (523Hz)	4 ms

4.3 Sensor data

4.3.1 Rate data

The angular rate data can be read-out through addresses 0x02 through 0x07. The angular rate data is in 2's complement form according to Table 8 below. In order to not corrupt the angular rate data, the LSB should always be read out first. Once the LSB of the x,y, or z read-out registers have been read, the MSBs are locked until the MSBs are read out.
This default behavior can be switched off by setting the address 0x13 bit 6 (shadow_dis) = '1'. In this case there is no MSB locking, and the data is updated between each read.

The burst-access mechanism provides an efficient way to read out the angular rate data in I^2C or SPI mode. During a burst-access, the BMG160 automatically increments the starting read address after each byte. Any address in the user space can be used as a starting address. When the address (0x3F – fifo_data) is reached, the address counter is stopped. In the user space address range, the 0x3F – fifo_data will be continuously read out until burst read ends. It is also possible to start directly with address 0x3F. In this case, the fifo_data (0x3F) data will be read out continuously. The burst-access allows data to be transferred over the I^2C bus with an up to 50% reduced data density. The angular rate data in all read-out registers is locked as long as the burst read access is active. Reading the chip angular rate registers in burst read access mode ensures that the angular rate values in all readout registers belong to the same sample.

Table 8: Gyroscope Register Content for 16bit mode

Decimal value	Angular rate (in 2000°/s range mode)
+32767	+ 2000°/s
…	…
0	0°/s
…	…
-32767	- 2000°/s

Per default, the bandwidth of the data being read-out is limited by the internal low-pass filters according to the filter configuration. Unfiltered (high-bandwidth) data can be read out through the serial interface when the data_high_bw (0x13 bit 7) is set to '1'.

4.3.2 Temperature sensor

The width of temperature data is 8 bits given in two´s complement representation. Temperature values are available in the *(0x08) temp* register.
The slope of the temperature sensor is 0.5K/LSB, its center temperature is 23°C [*(0x08) temp* = 0x00].

4.4 Angular rate read-out

Bandwidth configuration: The BMG160 processes the 2 kHz data out of the analog front end with a CIC/Decimation filter, followed by an IIR filter before sending this data to the interrupt handler. The possible decimation factors are 2, 5, 10 and 20. It is also possible to bypass these filters, and use the unfiltered 2 kHz data. The decimation factor / bandwidth of the filter can be set by setting the address space 0x10 bits<3:0> (bw<3:0>) as shown in the memory map section.

4.5 Self-test

A built-in self test (BIST) facility has been implemented which provides a quick way to determine if the device is operational within the specified conditions.

The BIST uses three parameters for evaluation of proper device operation:

- Drive voltage regulator
- Sense frontend offset regulator of x-,y- and z-channel
- Quad regulator for x-,y- and z-channel

If any of the three parameters is not within the limits the BIST result will be “Fail”.

To trigger the BIST ´bit0´ bite_trig in address 0x3C must be set `1´. When the test is performed, bit1 bist_rdy will be ´1´. If the result is failed the bit bist_failed will be set to ´1´, otherwise stay a ´0´.

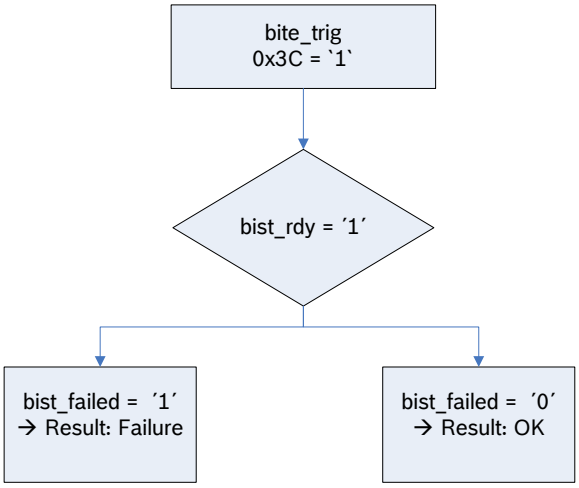


Figure 4: Flow Diagram

Another possibility to get information about the sensor status is to read out rate_ok 0x3C bit4. ´1´ indicates proper sensor function, no trigger is needed for this.

4.6 Offset compensation

Offsets in measured signals can have several causes but they are always unwanted and disturbing in many cases. Therefore, the BMG160 offers an advanced set of four digital offset compensation methods which are closely matched to each other. These are slow, fast, and manual compensation as well as inline calibration.

The compensation is performed with filtered data, and is then applied to both, unfiltered and filtered data. If necessary the result of this computation is saturated to prevent any overflow errors (the smallest or biggest possible value is set, depending on the sign). However, the registers used to read and write compensation values have a width of 8 bits.

The public offset compensation registers *(0x36) to (0x39)* are image of the corresponding registers in the NVM. With each image update (see section 4.6 Non-volatile memory for details) the contents of the NVM registers are written to the public registers. The public register can be over-written by the user at any time.

In case an internally computed compensation value is too small or too large to fit into the corresponding register, it is saturated in order to prevent an overflow error.

For every axes an offset up to 125°/s with 12 bits full resolution can be calibrated (resolution 0.06°/s).

The modes will be controlled using SPI/I2C commands.

By writing ´1´ to the *(0x21) offset_reset* bit, all dynamic (fast & slow) offset compensation registers are reset to zero.

4.6.1 Slow compensation

In slow regulation mode, the rate data is monitored permanently. If the rate data is above 0°/s for a certain period of time, an adjustable rate is subtracted by the offset controller. This procedure of monitoring the rate data and subtracting of the adjustable rate at a time is repeated continuously. Thus, the output of the offset converges to 0°/s.
The slow regulation can be enabled through the slow_offset_en_x/y/z (0x31 <0:2>) bits for each axis. The slow offset cancellation will work for filtered and unfiltered data (slow_offset_unfilt (0x1A <5>); slow_offset_unfilt=1 → unfiltered data are selected)

Slow Offset cancellation settings are the adjustable rate (slow offset_th 0x31 <7:6>) and the time period (slow_offset_dur 0x31 <5:3>)

4.6.2 Fast compensation

A fast offset cancellation controller is implemented in BMG160. The fast offset cancellation process is triggerable via SPI/I2C.
The fast offset cancellation can be enabled through the fast_offset_en_x/y/z (0x32 <0:2>) bits for each axis. The enable bits will not start the fast offset cancellation! The fast offset cancellation has to be started by setting the fast_offset_en (0x32 <3>) bit. Afterwards the algorithm will start and if the algorithm is finished the fast_offset_en (0x32 <3>) will be reset to 0.

The fast offset cancellation will work for filtered and unfiltered data (fast_offset_unfilt (0x1B <7>); fast_offset_unfilt=1 → unfiltered data are selected)
The fast offset cancellation parameters are fast_offset_wordlength (0x32 <5:4>)

The sample rate for the fast offset cancellation corresponds to the sample rate of the selected bandwidth. For unfiltered data and bandwidth settings 0-2 the sample rate for the fast offset cancellation will be 400Hz.

The resolution of the calculated offset values for the fast offset compensation depends on the, range setting being less accurate for higher range (e.g. range=2000°/s).Therefore we recommend a range setting of range=125°/s for fast offset compensation.

4.6.3 Manual compensation

The contents of the public compensation registers *(0x36 ... 0x39) offset_x/y/z* can be set manually via the digital interface. It is recommended to write into these registers directly after a new data interrupt has occurred in order not to disturb running offset computations.

Writing to the offset compensation registers is not allowed while the fast compensation procedure is running.

4.6.4 Inline calibration

For certain applications, it is often desirable to calibrate the offset once and to store the compensation values permanently. This can be achieved by using one of the aforementioned offset compensation methods to determine the proper compensation values and then storing these values permanently in the NVM. See section 4.7 Non-volatile memory for details of the storing procedure.

Each time the device is reset, the compensation values are loaded from the non-volatile memory into the image registers and used for offset compensation until they are possibly overwritten using one of the other compensation methods.

4.7 Non-volatile memory

The entire memory of the BMG160 consists of three different kinds of registers: hard-wired, volatile, and non-volatile. Part of it can be both read and written by the user. Access to non-volatile memory is only possible through (volatile) image registers.

Altogether, there are eight registers (octets) with NVM backup which are accessible by the user. The addresses of the image registers range from 0x36 to 0x3B. While the addresses up to 0x39 are used for offset compensation (see 4.4 Offset Compensation), addresses 0x3A and 0x3B are general purpose registers not linked to any sensor-specific functionality.

The content of the NVM is loaded to the image registers after a reset (either POR or softreset) or after a user request which is performed by writing ´1´ to the write-only bit *(0x33) nvm_load*. As long as the image update is in progress, bit *(0x33) nvm_rdy* is ´0´, otherwise it is ´1´.
In order to read out the correct values (after NVM loading) waiting time is min. 1ms.

The image registers can be read and written like any other register.

Writing to the NVM is a three-step procedure:

1. Write the new contents to the image registers.
2. Write ´1´ to bit *(0x33) nvm_prog_mode* in order to unlock the NVM.
3. Write ´1´ to bit *(0x33) nvm_prog_trig* and keep ´1´ in bit *(0x33) nvm_prog_mode* in order to trigger the write process.

Writing to the NVM always renews the entire NVM contents. It is possible to check the write status by reading bit *(0x33) nvm_rdy*. While *(0x33) nvm_rdy* = ´0´, the write process is still in progress; if *(0x33) nvm_rdy* = ´1´, then writing is completed. As long as the write process is ongoing, no change of power mode and image registers is allowed. Also, the NVM write cycle must not be initiated while image registers are updated, in suspend mode.

Please note that the number of permitted NVM write-cycles is limited as specified in Table 2. The number of remaining write-cycles can be obtained by reading bits *(0x33) nvm_remain*.

4.8 Interrupt controller

The BMG160 is equipped with 3 programmable interrupt engines. Each interrupt can be independently enabled and configured. If the trigger condition of an enabled interrupt is fulfilled, the corresponding status bit is set to ´1´ and the selected interrupt pin is activated. The BMG160 provides two interrupt pins, INT1 and INT2; interrupts can be freely mapped to any of these pins. The state of a specific interrupt pin is derived from a logic ´or´ combination of all interrupts mapped to it.

The interrupt status registers are updated when a new data word is written into the rate data registers. If an interrupt is disabled, all active status bits associated with it are immediately reset.

Gyro Interrupts are fully functional in normal mode, only. Interrupts are limited in their functionality in other operation modes. Please contact our technical support for further assistance.

4.8.1 General features

An interrupt is cleared depending on the selected interrupt mode, which is common to all interrupts. There are three different interrupt modes: non-latched, latched, and temporary. The mode is selected by the *(0x21) latch_int* bits according to Table 9.

Table 9: Interrupt mode selection

(0x21) latch_int	**Interrupt mode**
0000b	non-latched
0001b	temporary, 250ms
0010b	temporary, 500ms
0011b	temporary, 1s
0100b	temporary, 2s
0101b	temporary, 4s
0110b	temporary, 8s
0111b	latched
1000b	non-latched
1001b	temporary, 250µs
1010b	temporary, 500µs
1011b	temporary, 1ms
1100b	temporary, 12.5ms
1101b	temporary, 25ms
1110b	temporary, 50ms
1111b	latched

An interrupt is generated if its activation condition is met. It can not be cleared as long as the activation condition is fulfilled. In the non-latched mode the interrupt status bit and the selected pin (the contribution to the ´or´ condition for INT1 and/or INT2) are cleared as soon as the

activation condition is no more valid. Exception to this behavior is the new data interrupt, which is automatically reset after a fixed time.

In latched mode an asserted interrupt status and the selected pin are cleared by writing ´1´ to bit *(0x21) reset_int*. If the activation condition still holds when it is cleared, the interrupt status is asserted again with the next change of the rate registers.

In the temporary mode an asserted interrupt and selected pin are cleared after a defined period of time. The behaviour of the different interrupt modes is shown graphically in Figure 5. The timings in this mode are subject to the same tolerances as the bandwidths (see Table 2).

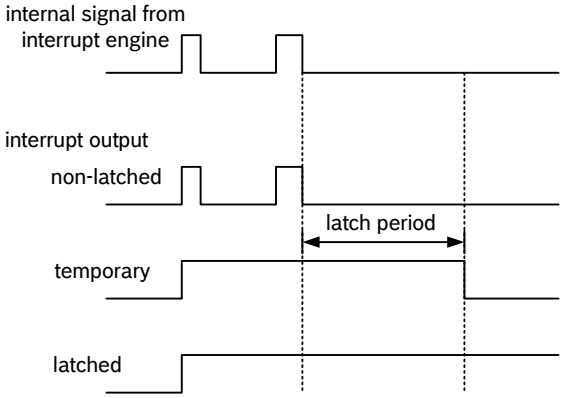


Figure 5: Interrupt modes

4.8.2 Mapping to physical interrupt pins (inttype to INT Pin#)

Registers *(0x17)* to *(0x19)* are dedicated to mapping of interrupts to the interrupt pins “INT1” or “INT2”. Setting *(0x17) int1*_”inttype” to ´1´ (´0´) maps (unmaps) “inttype” to pin “INT1”. Correspondingly setting *(0x19) int2*_”inttype” to ´1´ (´0´) maps (unmaps) “inttype” to pin “INT2”.

Note: “inttype” has to be replaced with the precise notation, given in the memory map in chapter 6.

4.8.3 Electrical behaviour (INT pin# to open-drive or push-pull)

Both interrupt pins can be configured to show the desired electrical behaviour. The ´active´ level of each interrupt pin is determined by the *(0x16) int1_lvl* and *(0x16) int2_lvl* bits.

If *(0x16) int1_lvl* = ´1´ (´0´) / *(0x16) int2_lvl* = ´1´ (´0´), then pin “INT1” / pin “INT2” is active ´1´ (´0´). The characteristic of the output driver of the interrupt pins may be configured with bits *(0x16) int1_od* and *(0x16) int2_od*. By setting bits *(0x16) int1_od* / *(0x16) int2_od* to ´1´, the output driver shows open-drive characteristic, by setting the configuration bits to ´0´, the output driver shows push-pull characteristic. When open-drive characteristic is selected in the design, external pull-up or pull-down resistor should be applied according the int_lvl configuration.

4.8.4 New data interrupt

This interrupt serves for synchronous reading of angular rate data. It is generated after storing a new value of z-axis angular rate data in the data register. The interrupt is cleared automatically after 280-400 µs (depending on Interrupt settings).

The interrupt mode of the new data interrupt is fixed to non-latched.

It is enabled (disabled) by writing ´1´ (´0´) to bit *(0x15) data_en*. The interrupt status is stored in bit *(0x0A) data_int*.

4.8.5 Any-motion detection / Interrupt

Any-motion (slope) detection uses the slope between successive angular rate signals to detect changes in motion. An interrupt is generated when the slope (absolute value of angular rate difference) exceeds a preset threshold. It is cleared as soon as the slope falls below the threshold. The principle is made clear in Figure 6.

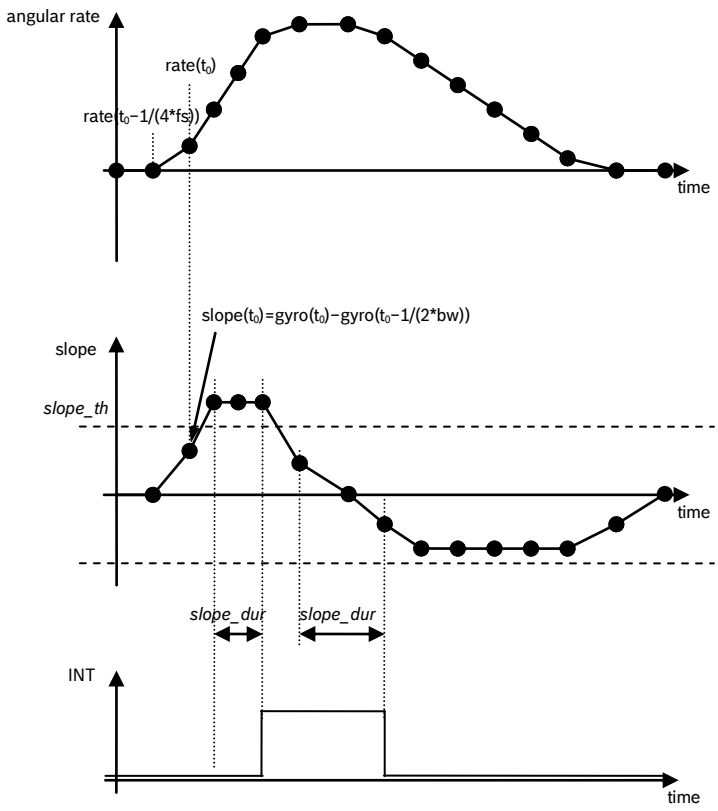


Figure 6 : Principle of any-motion detection

The threshold is defined through register *(0x1B) any_th*. In terms of scaling 1 LSB of *(0x1B) any_th* corresponds to 1 °/s in 2000°/s-range (0.5°/s in 1000°/s-range, 0.25°/s in 500°/s -range ...). Therefore the maximum value is 125°/s in 2000°/s-range (62.5°/s 1000°/s-range, 31.25 in 500°/s -range ...).

The time difference between the successive angular rate signals depends on the selected update rate(fs) which is coupled to the bandwidth and equates to 1/(4*fs) (t=1/(4*fs)). For bandwidhth settings with an update rate higher than 400Hz (bandwidth =0,1,2) fs is set to 400Hz.

In order to suppress false triggers, the interrupt is only generated (cleared) if a certain number *N* of consecutive slope data points is larger (smaller) than the slope threshold given by *(0x1B) any_th*. This number is set by the *(0x1C) any_dursample* bits. It is *N* = [*(0x1C) any_dursample*+ 1]*4 for *(0x1C)*. N is set in samples. Thus the time is scaling with the update rate (fs).

Example: *(0x1C) slope_dur* = 00b, ..., 11b = 4 samples, ..., 16 samples.