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Serial EEPROM series Standard EEPROM

I²C BUS EEPROM (2-Wire)

BR24G02-3A

●General Description

BR24G02-3A is a serial EEPROM of I²C BUS interface method

●Features

- All controls available by 2 ports of serial clock(SCL) and serial data(SDA)
- Other devices than EEPROM can be connected to the same port, saving microcontroller port
- 1.6V to 5.5V single power source action most suitable for battery use
- 1MHz action is possible (1.7V to 5.5V)
- Up to 8 bytes in page write mode
- Self-timed programming cycle
- Low current consumption
- Prevention of write mistake
  - ➢ Write (write protect) function added
  - ➢ Prevention of write mistake at low voltage
- More than 1 million write cycles
- More than 40 years data retention
- Noise filter built in SCL / SDA terminal
- Initial delivery state FFh

●Packages W(Typ.) x D(Typ.)x H(Max.)

DIP-T8
9.30mm x 6.50mm x 7.10mm

TSSOP-B8J
3.00mm x 4.90mm x 1.10mm

SOP8
5.00mm x 6.20mm x 1.71mm

MSOP8
2.90mm x 4.00mm x 0.90mm

SOP-J8
4.90mm x 6.00mm x 1.65mm

VSON008X2030
2.00mm x 3.00mm x 0.60mm

TSSOP-B8
3.00mm x 6.40mm x 1.20mm

Figure 1.

●BR24G02-3A

Capacity	Bit Format	Type	Power Source Voltage	Package
2Kbit	256×8	BR24G02-3A	1.6V to 5.5V	DIP-T8
		BR24G02F-3A		SOP8
		BR24G02FJ-3A		SOP-J8
		BR24G02FVT-3A		TSSOP-B8
		BR24G02FVJ-3A		TSSOP-B8J
		BR24G02FVM-3A		MSOP8
		BR24G02NUX-3A		VSON008X2030

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●**Absolute Maximum Ratings (Ta=25℃)**

Parameter	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{CC}	-0.3 to +6.5	V	
Power Dissipation	Pd	450 (SOP8)	mW	When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃.
		450 (SOP-J8)		When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃.
		330 (TSSOP-B8)		When using at Ta=25℃ or higher 3.3mW to be reduced per 1℃.
		310 (TSSOP-B8J)		When using at Ta=25℃ or higher 3.1mW to be reduced per 1℃.
		310 (MSOP8)		When using at Ta=25℃ or higher 3.1mW to be reduced per 1℃.
		300 (VSON008X2030)		When using at Ta=25℃ or higher 3.0mW to be reduced per 1℃.
		800 (DIP-T8)		When using at Ta=25℃ or higher 8.0mW to be reduced per 1℃.
Storage Temperature	Tstg	−65 to +150	℃	
Operation Temperature	Topr	−40 to +85	℃	
Input Voltage / Output Voltage	-	-0.3 to Vcc+1.0	V	The Max value of input voltage / output voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of input voltage / output voltage is not under -0.8V.
Junction Temperature	Tjmax	150	℃	Junction temperature at the storage condition
Electrostatic discharge voltage (human body model)	V_{ESD}	-4000 to +4000	V	

●**Memory Cell Characteristics (Ta=25℃, Vcc=1.6V to 5.5V)**

Parameter	Limits			Unit
	Min.	Typ.	Max	
Write cycles *1	1,000,000	−	−	Times
Data retention *1	40	−	−	Years

*1Not 100% TESTED

●**Recommended Operating Ratings**

Parameter	Symbol	Ratings	Unit
Supply voltage	Vcc	1.6 to 5.5	V
Input voltage	V_{IN}	0 to Vcc	

●**DC Characteristics (Unless otherwise specified, Ta=-40 to +85℃, Vcc =1.6 to 5.5V)**

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Input High Voltage1	VIH1	0.7Vcc	−	Vcc+1.0	V	1.7V≦Vcc≦5.5V
Input Low Voltage1	VIL1	−0.3*1	−	0.3Vcc	V	1.7V≦Vcc≦5.5V
Input High Voltage2	VIH2	0.8Vcc	−	Vcc+1.0	V	1.6V≦Vcc＜1.7V
Input Low Voltage2	VIL2	−0.3*1	−	0.2Vcc	V	1.6V≦Vcc＜1.7V
Output Low Voltage1	VOL1	−	−	0.4	V	IOL=3.0mA, 2.5V≦Vcc≦5.5V (SDA)
Output Low Voltage2	VOL2	−	−	0.2	V	I_{OL}=0.7mA, 1.6V≦Vcc＜2.5V (SDA)
Input Leakage Current	ILI	−1	−	1	μA	VIN=0 to Vcc
Output Leakage Current	ILO	−1	−	1	μA	VOUT=0 to Vcc (SDA)
Supply Current (Write)	ICC1	−	−	2.0	mA	Vcc=5.5V, fSCL=1MHz, tWR=5ms, Byte write, Page write
Supply Current (Read)	ICC2	-	-	2.0		Vcc=5.5V, fSCL=1MHz Random read, current read, sequential read
Standby Current	ISB	−	−	2.0	μA	Vcc=5.5V, SDA, SCL=Vcc A0, A1, A2=GND, WP=GND

*1 When the pulse width is 50ns or less, it is -0.8V.

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●**AC Characteristics (Unless otherwise specified, Ta=−40 to +85℃)**

Parameter	Symbol	Limits (1.6V≦Vcc＜1.7V)			Limits (1.7V≦Vcc≦5.5V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fSCL	-	-	400	—	—	1000	kHz
Data Clock “HIGH“ Period	tHIGH	0.6	-	-	0.3	—	—	µs
Data Clock “LOW“ Period	tLOW	1.2	-	-	0.5	—	—	µs
SDA, SCL (INPUT) Rise Time *1	tR	-	-	1	—	—	0.12	µs
SDA, SCL (INPUT) Fall Time *1	tF1	-	-	1	—	—	0.12	µs
SDA (OUTPUT) Fall Time *1	tF2	-	-	0.12	—	—	0.12	µs
Start Condition Hold Time	tHD:STA	0.6	-	-	0.25	—	—	µs
Start Condition Setup Time	tSU:STA	0.6	-	-	0.20	—	—	µs
Input Data Hold Time	tHD:DAT	0	-	-	0	—	—	ns
Input Data Setup Time	tSU:DAT	100	-	-	50	—	—	ns
Output Data Delay Time	tPD	0.1	-	0.9	0.05	—	0.45	µs
Output Data Hold Time	tDH	0.1	-	-	0.05	—	—	µs
Stop Condition Setup Time	tSU:STO	0.6	-	-	0.25	—	—	µs
Bus Free Time	tBUF	1.2	-	-	0.5	—	—	µs
Write Cycle Time	tWR	-	-	5	—	—	5	ms
Noise Spike Width (SDA, SCL)	tI	-	-	0.05	—	—	0.05	µs
WP Hold Time	tHD:WP	1.0	-	-	1.0	—	—	µs
WP Setup Time	tSU:WP	0.1	-	-	0.1	—	—	µs
WP High Period	tHIGH:WP	1.0	-	-	1.0	—	—	µs

*1 Not 100% tested

●**AC Characteristics Condition**

Parameter	Symbol	Condition	Unit
Load Capacitance	CL	100	pF
SDA, SCL (INPUT) Rise Time	tR	20	ns
SDA, SCL (INPUT) Fall Time	tF1	20	ns
Input Data Level	VIL1/VIH1	0.2Vcc/0.8Vcc	V
Input/Output Data Timing Reference Level	-	0.3Vcc/0.7Vcc	V

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●Serial Input / Output timing

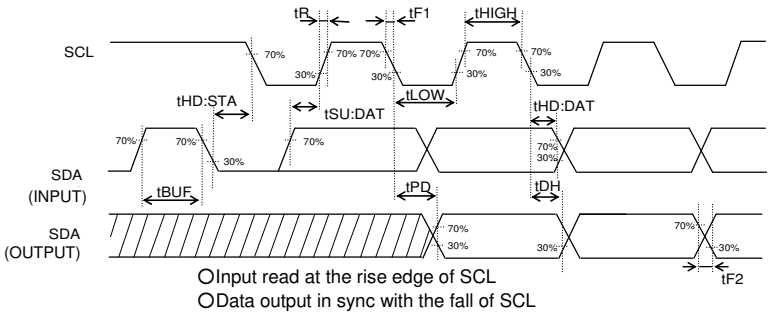

Figure 2-(a). Serial input / output timing

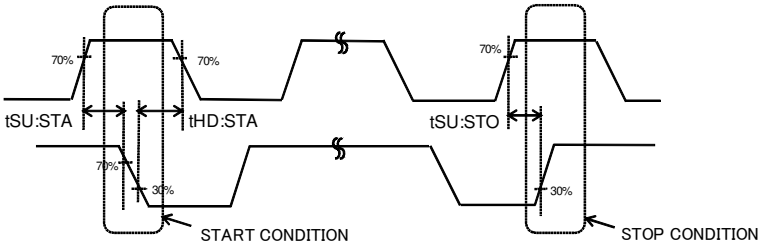

Figure 2-(b). Start-stop bit timing

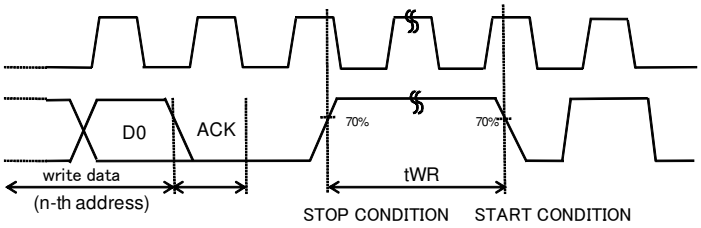

Figure 2-(c). Write cycle timing

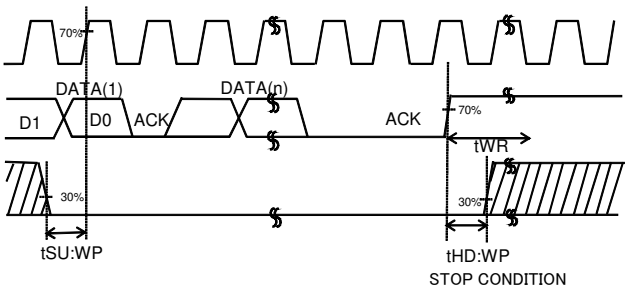

Figure 2-(d). WP timing at write execution

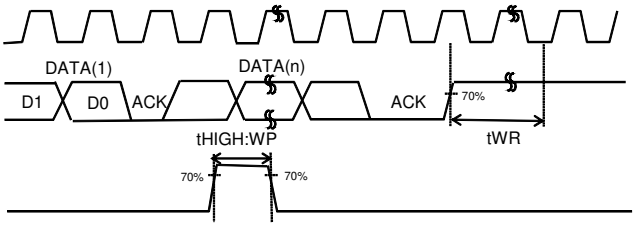

Figure 2-(e). WP timing at write cancel

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●Block Diagram

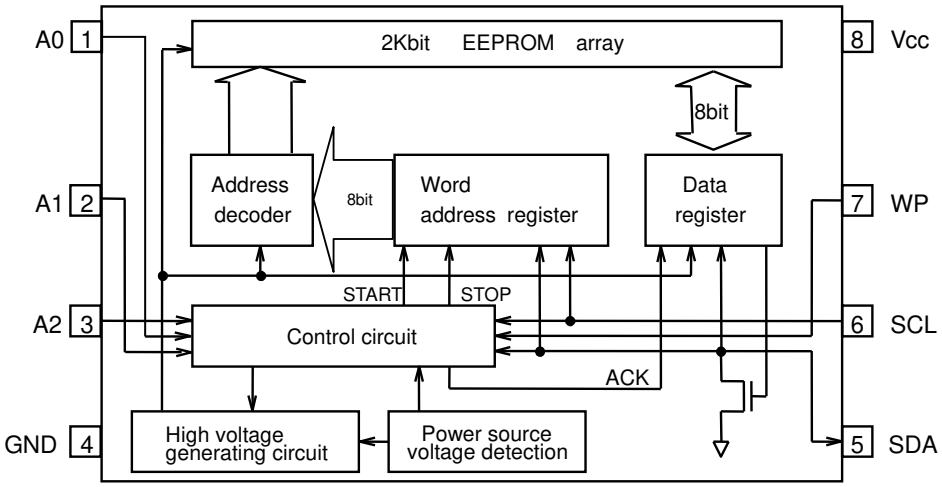
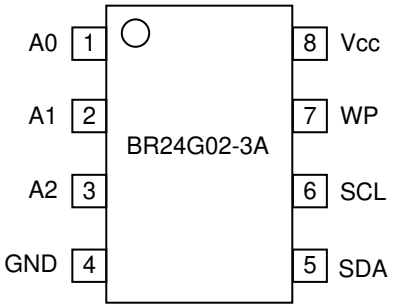


Figure 3. Block diagram

●Pin Configuration



●Pin Descriptions

Terminal Name	Input/ Output	Function
A0	Input	Slave address setting*
A1	Input	Slave address setting*
A2	Input	Slave address setting*
GND	—	Reference voltage of all input / output, 0V
SDA	Input/ output	Serial data input serial data output
SCL	Input	Serial clock input
WP	Input	Write protect terminal
Vcc	—	Connect the power source.

*A0, A1 and A2 are not allowed to use as open.

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●Typical Performance Curves

(The following values are Typ. ones)

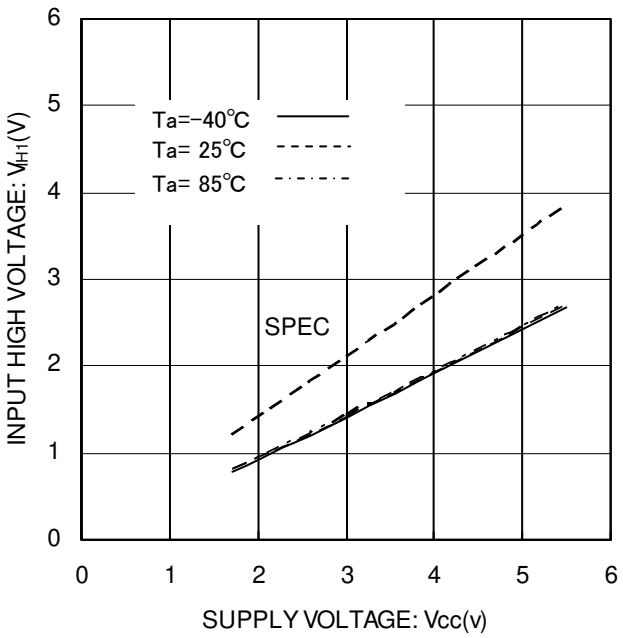

Figure 4. Input High Voltage1,2 VIH1,2
(A0, A1, A2, SCL, SDA, WP)

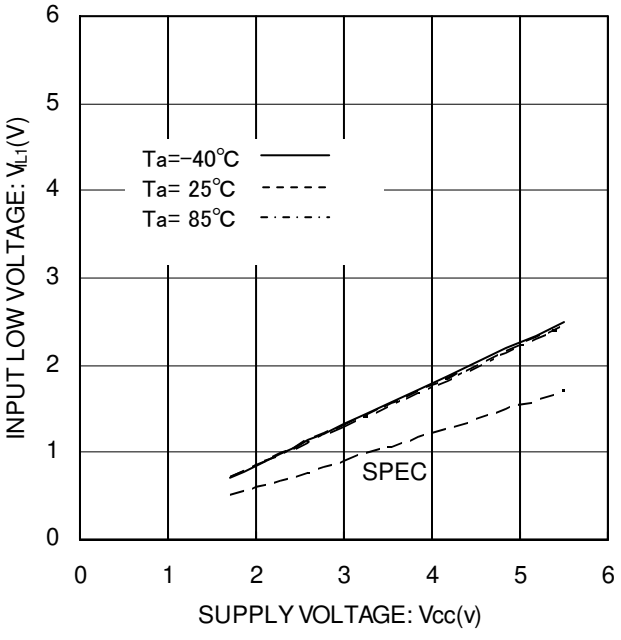

Figure 5. Input Low Voltage1,2 VIL1,2
(A0, A1, A2, SCL, SDA, WP)

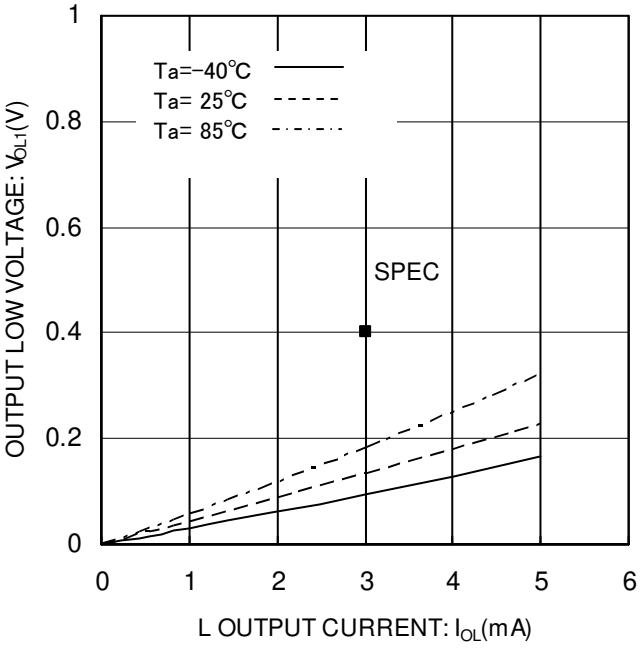

Figure 6. Output Low Voltage1 VOL1
(Vcc=2.5V)

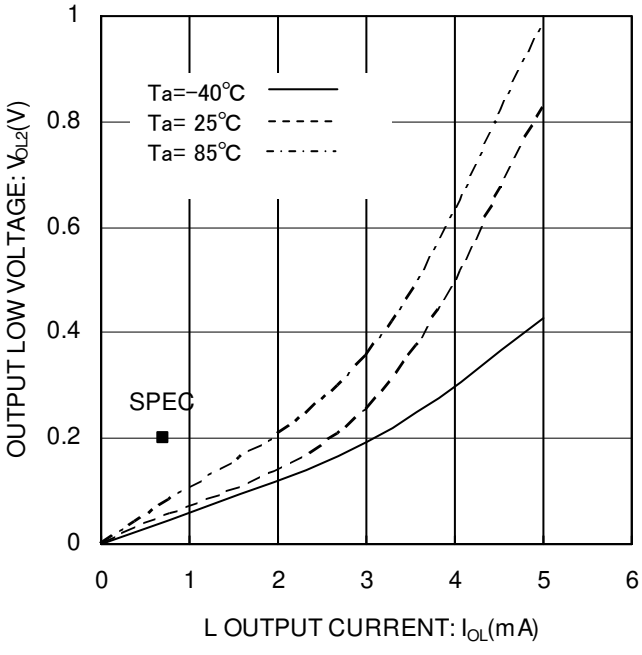

Figure 7. Output Low Voltage2 VOL2
(Vcc=1.6V)

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●**Typical Performance Curves - Continued**

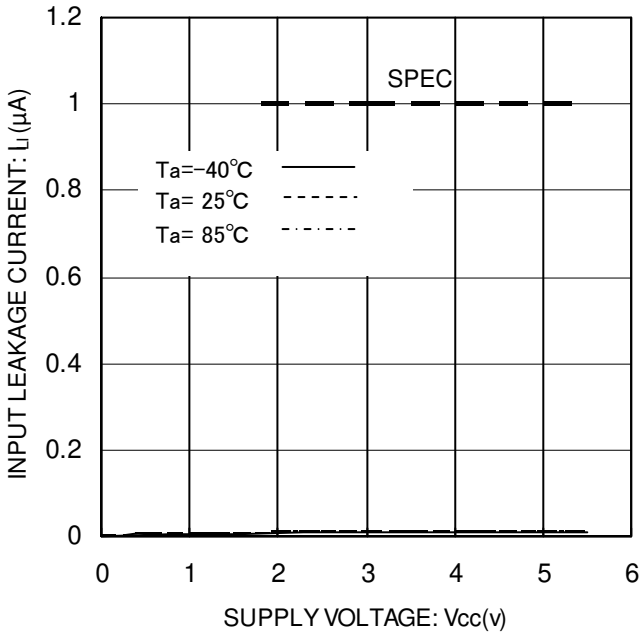

Figure 8. Input Leakage Current ILI
(A0, A1, A2, SCL, WP)

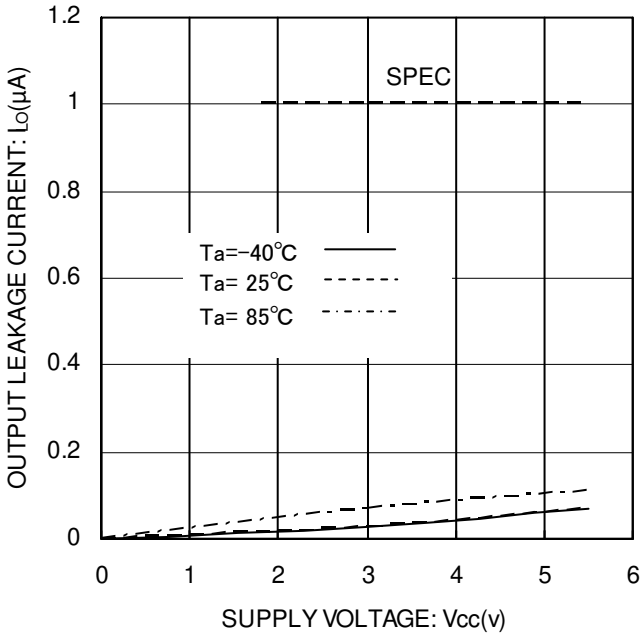

Figure 9. Output Leakage Current ILO (SDA)

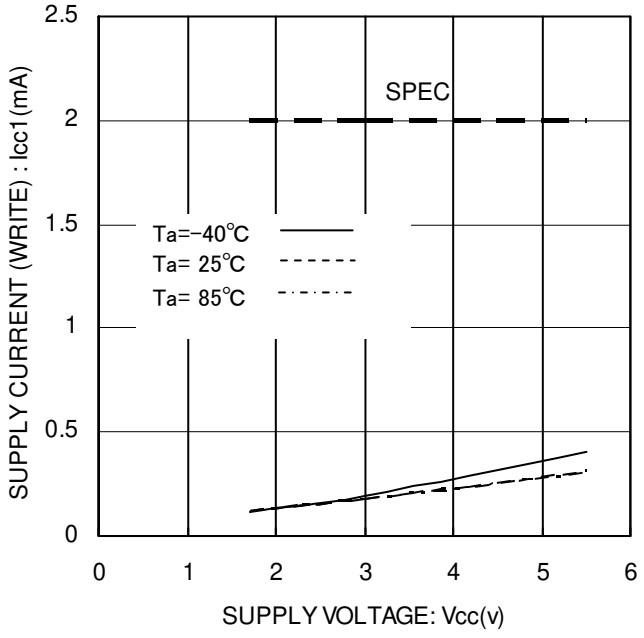

Figure 10. Supply Current (WRITE) ICC1
(fscl=1MHz)

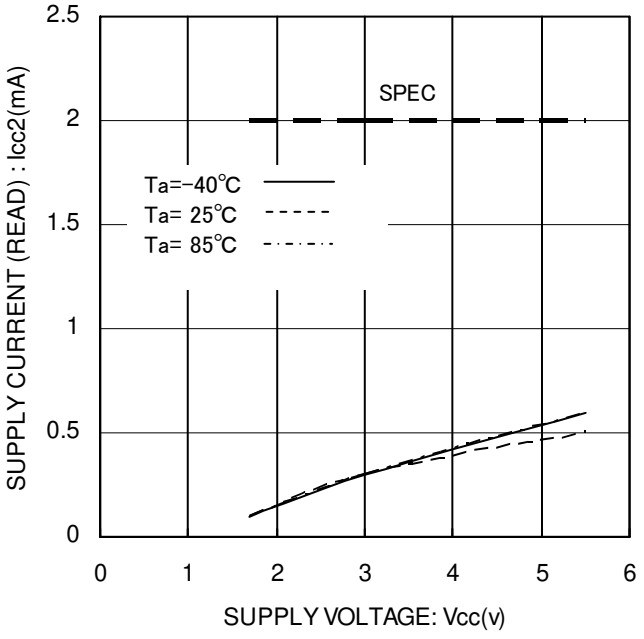

Figure 11. Supply Current (READ) ICC2
(fscl=1MHz)

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●**Typical Performance Curves - Continued**

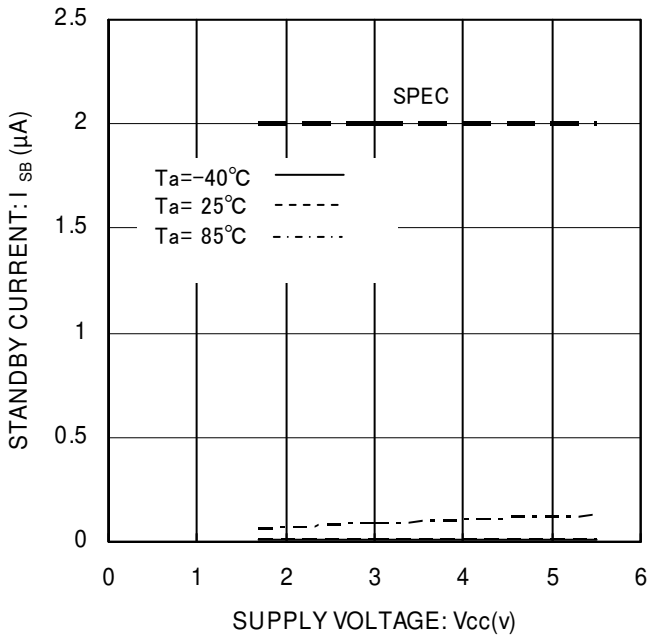

Figure 12. Standby Current ISB

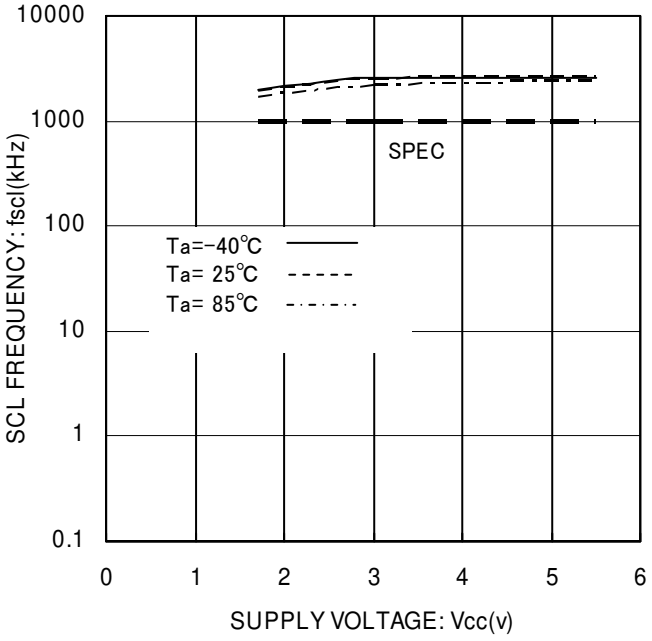

Figure 13. Clock Frequency fSCL

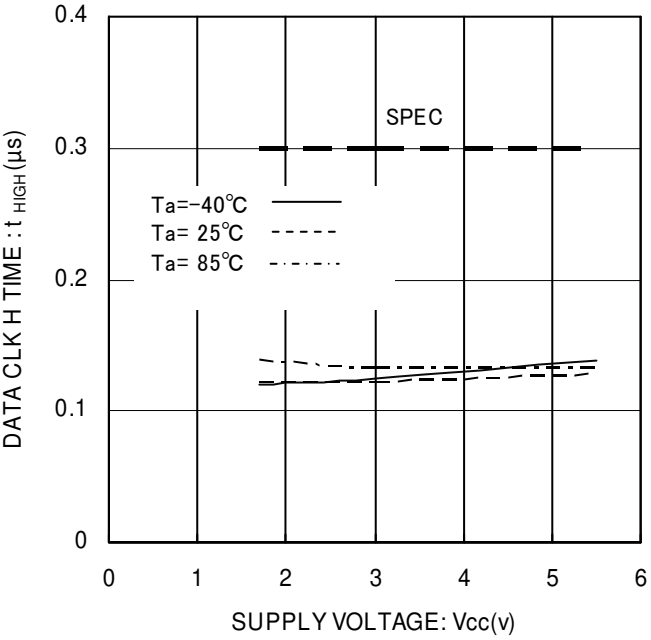

Figure 14. Data Clock High Period tHIGH

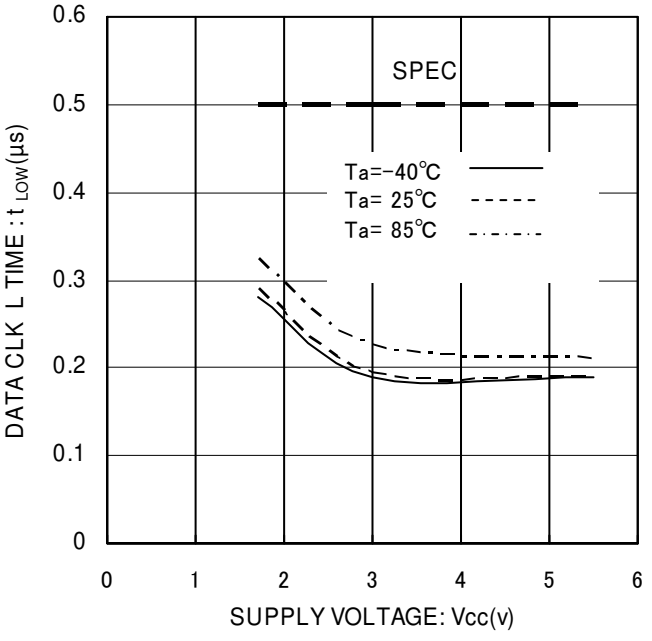

Figure 15. Data Clock Low Period tLOW

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●**Typical Performance Curves - Continued**

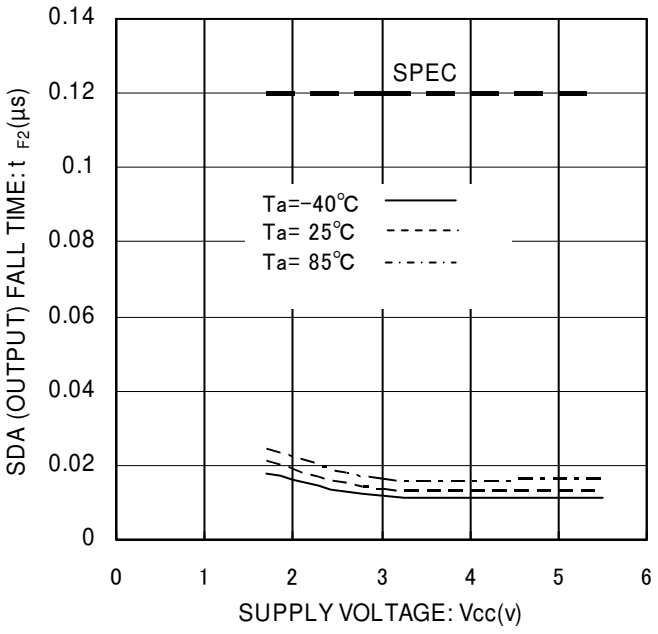

Figure 16. SDA (OUTPUT) Fall Time tF2

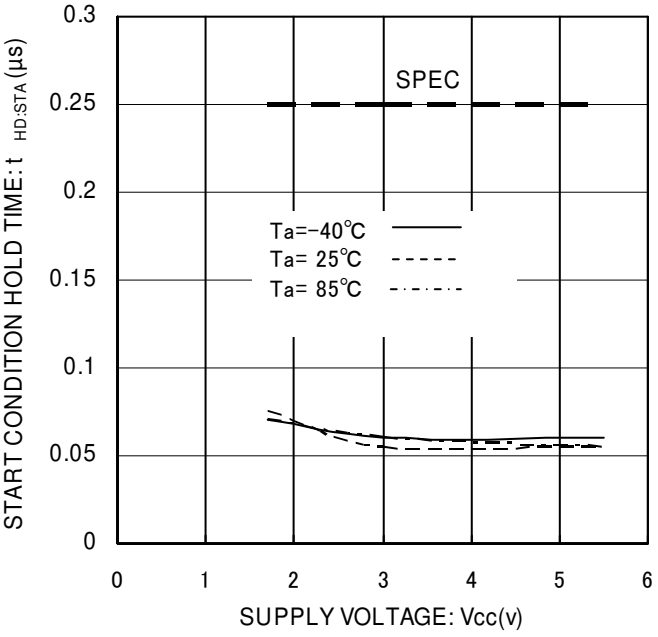

Figure 17. Start Condition Hold Time tHD:STA

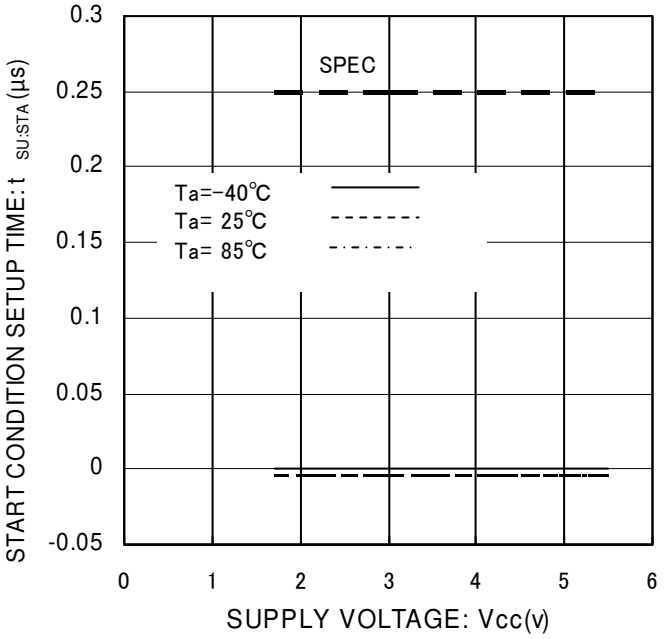

Figure 18. Start Condition Setup Time tSU:STA

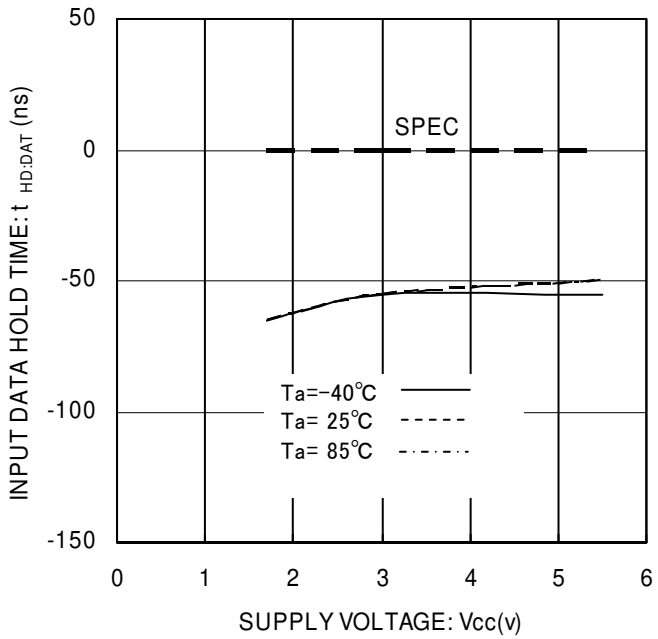

Figure 19. Input Data Hold Time tHD:DAT(HIGH)

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●**Typical Performance Curves - Continued**

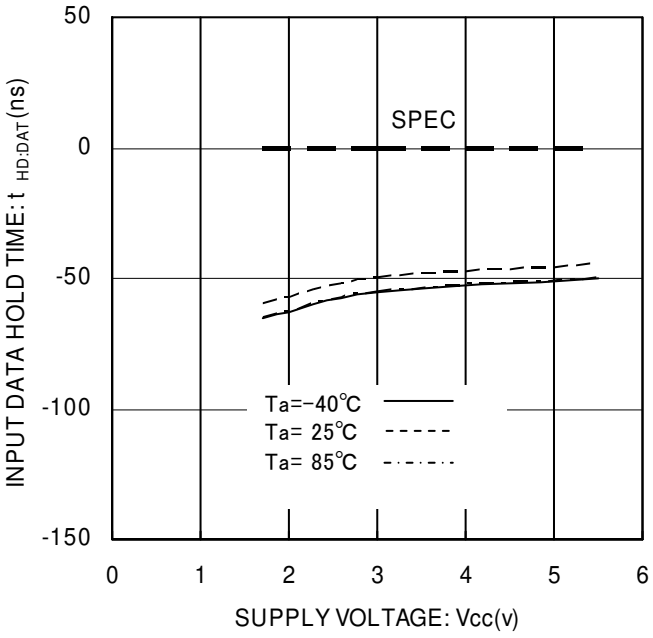

Figure 20. Input Data Hold Time tHD:DAT(LOW)

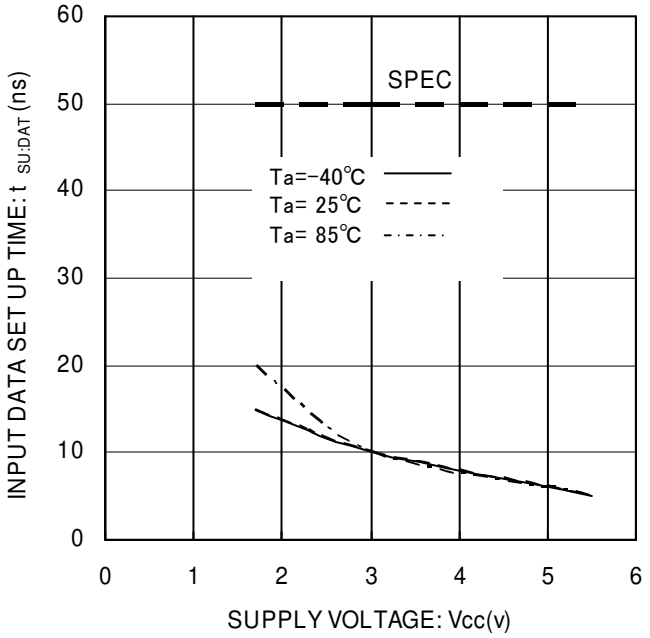

Figure 21. Input Data Setup Time tSU:DAT(HIGH)

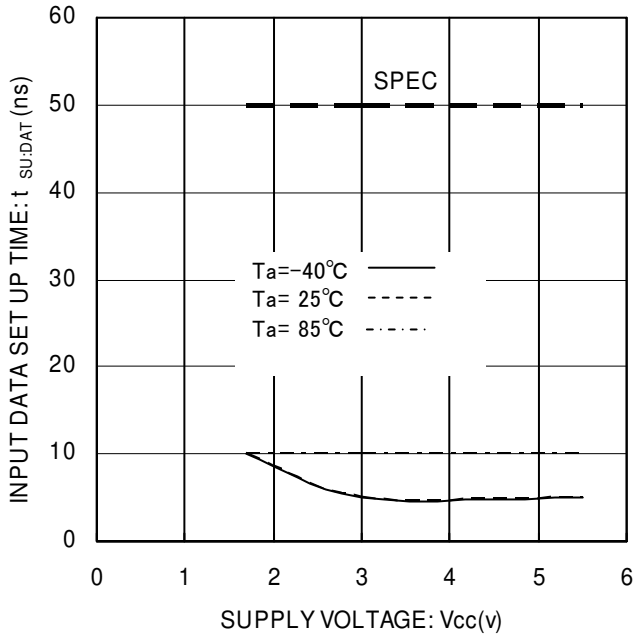

Figure 22. Input Data Setup Time tSU:DAT(LOW)

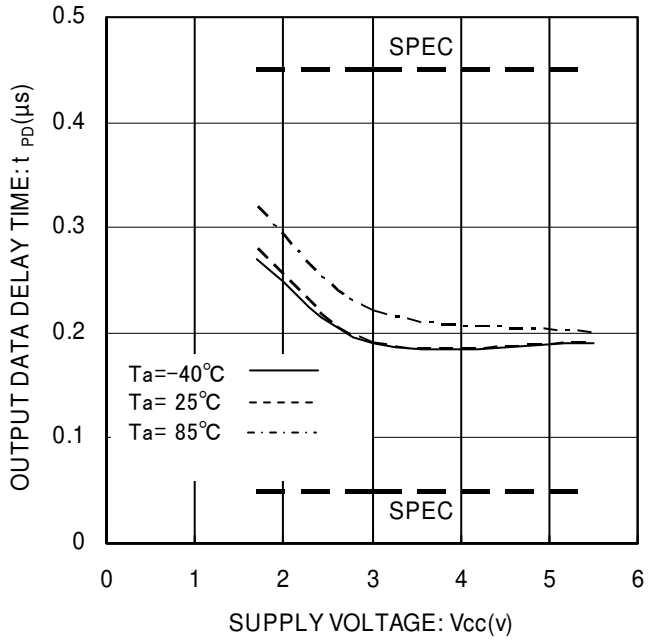

Figure 23. 'L' Output Data Delay Time tPD0

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●**Typical Performance Curves - Continued**

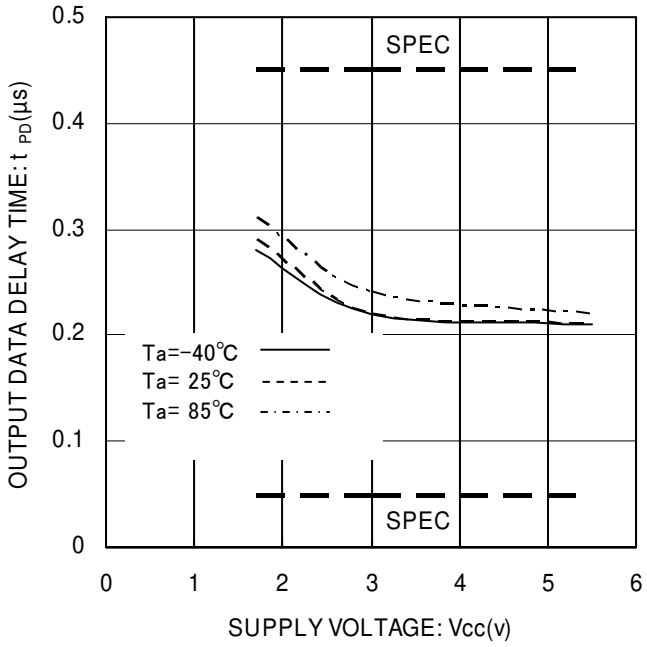

Figure 24. 'H' Output Data Delay Time tPD1

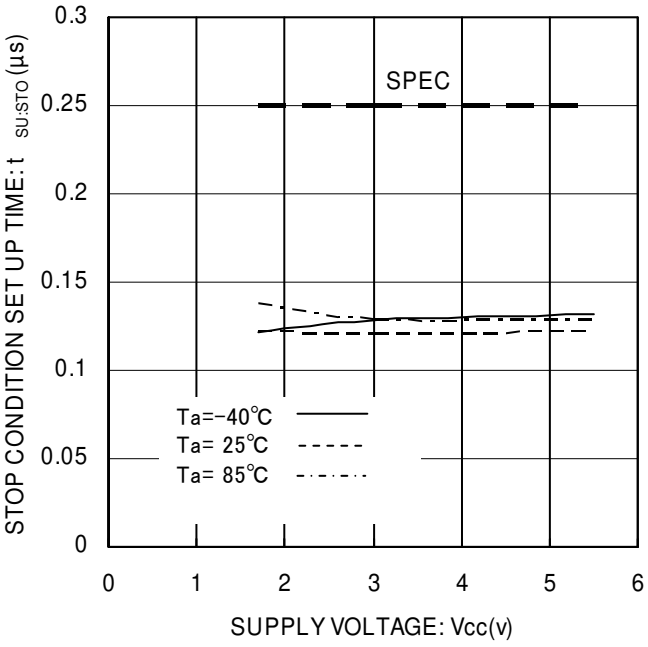

Figure 25. Stop Condition Setup Time tSU:STO

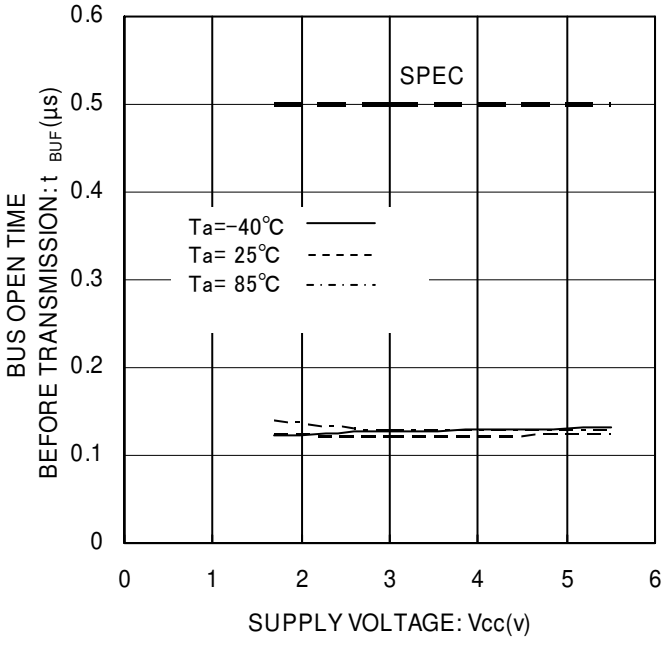

Figure 26. BUS Free Time tBUF

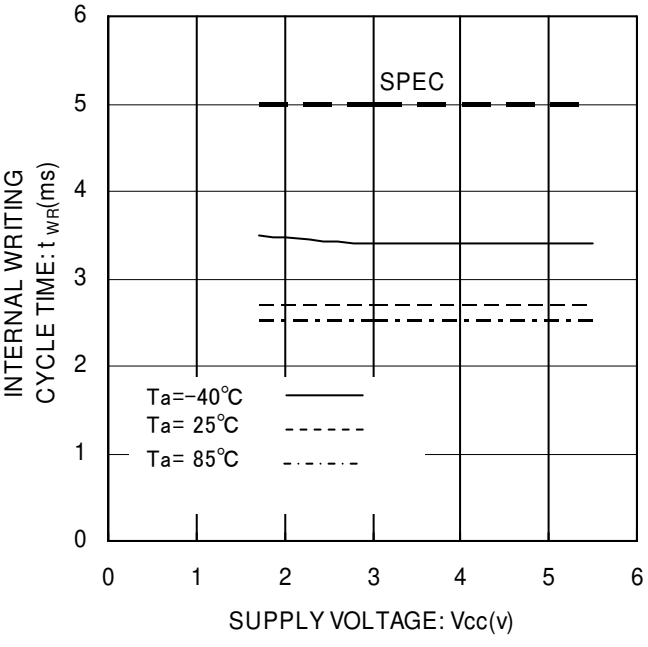

Figure 27. Write Cycle Time tWR

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●**Typical Performance Curves - Continued**

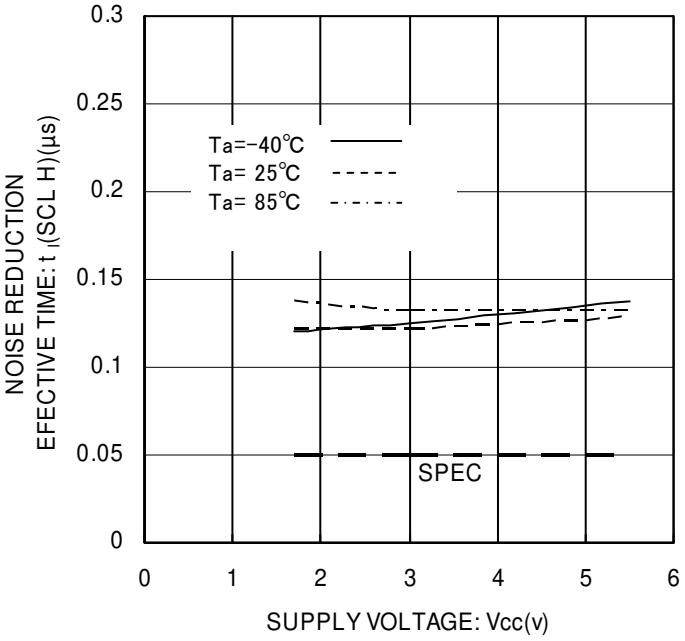

Figure 28. Noise Spike Width tI (SCL H)

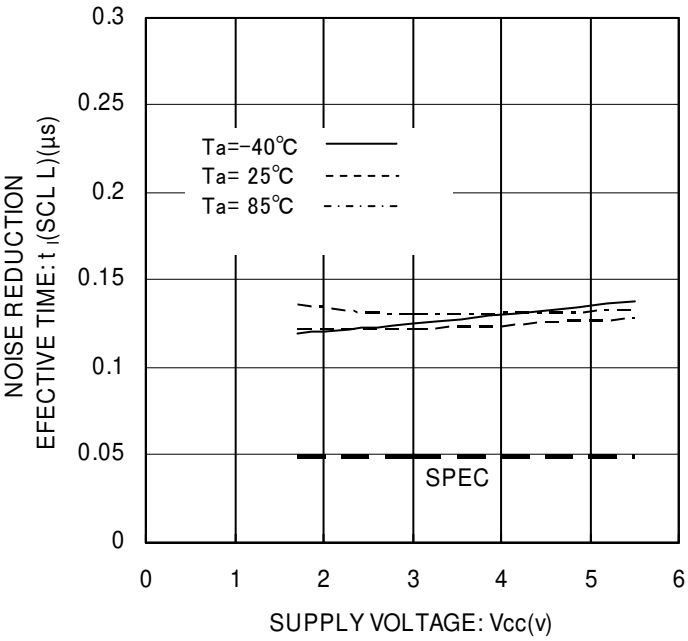

Figure 29. Noise Spike Width tI (SCL L)

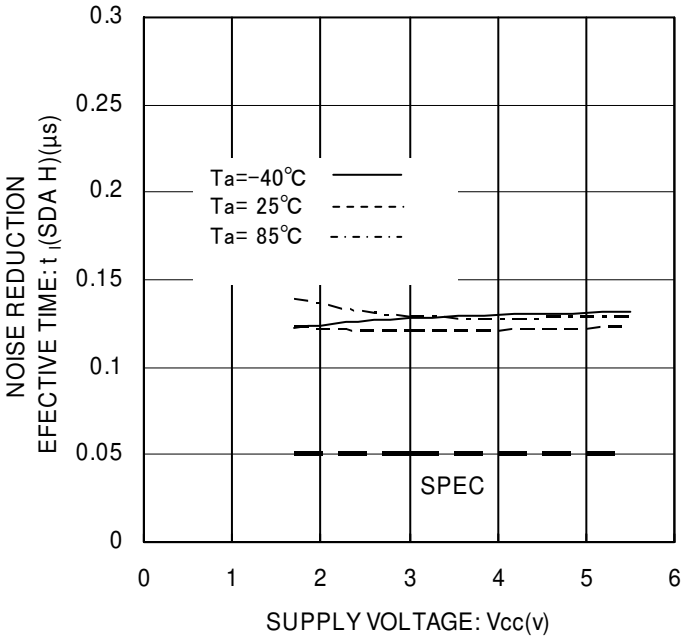

Figure 30. Noise Spike Width tI (SDA H)

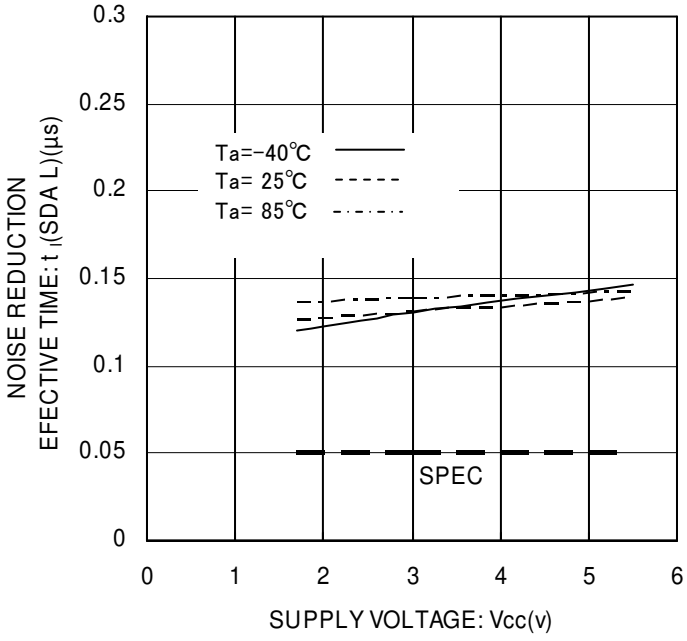

Figure 31. Noise Spike Width tI (SDA L)

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●**Typical Performance Curves - Continued**

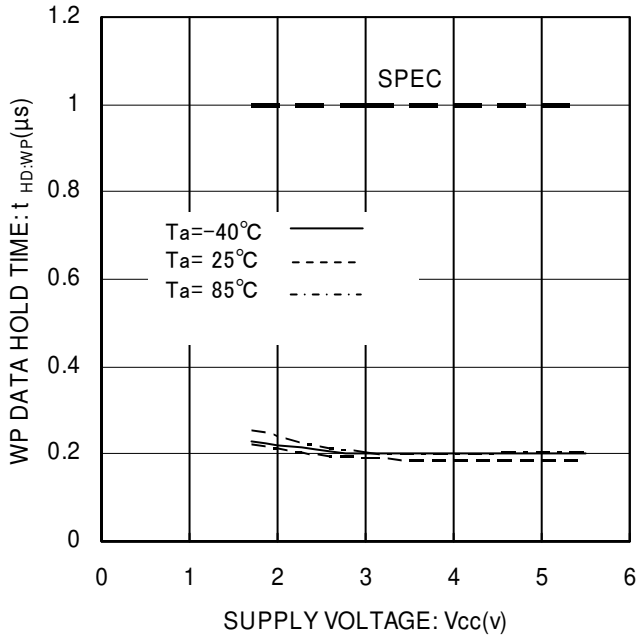

Figure 32. WP Hold Time tHD:WP

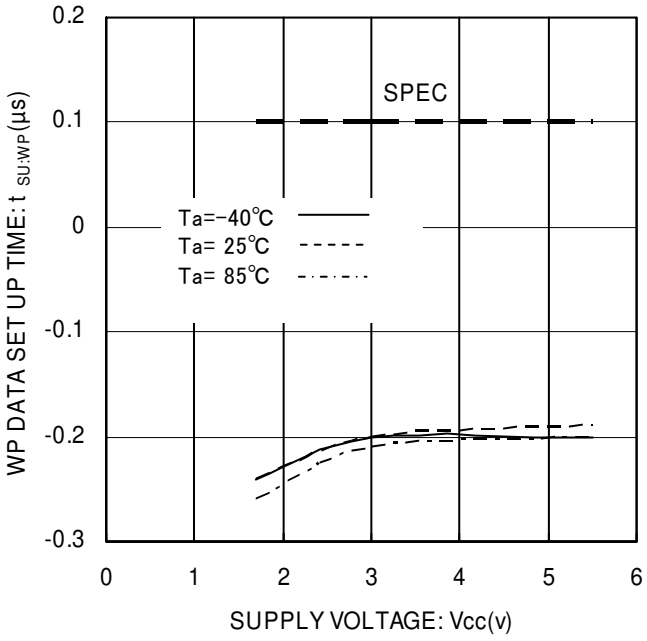

Figure 33. WP Setup Time tSU:WP

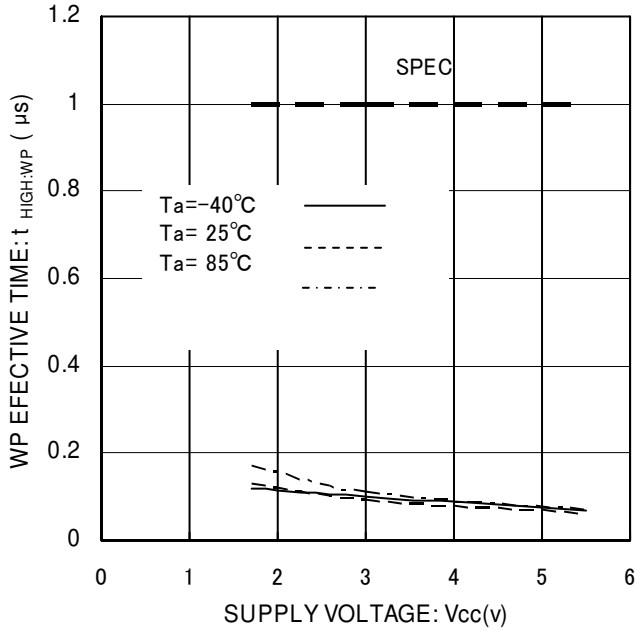

Figure 34. WP High Time tHIGH:WP

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●Timing Chart

○I²C BUS data communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).

Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by address peculiar to devices. EEPROM becomes “slave”. And the device that outputs data to bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

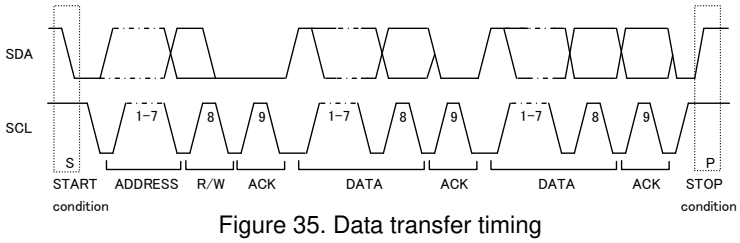

Figure 35. Data transfer timing

○Start condition (Start bit recognition)

- Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
- This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this confdition is satisfied, any command is executed.

○Stop condition (stop bit recongnition)

- Each command can be ended by SDA rising from 'LOW' to 'HIGH' when stop condition (stop bit), namely, SCL is 'HIGH'

○Acknowledge (ACK) signal

- This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device (μ-COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
- The device (this IC at slave address input of write command, read command, and μ-COM at data output of read command) at the receiver (receiving) side sets SDA 'LOW' during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
- Each write action outputs acknowledge signal (ACK signal) 'LOW', at receiving 8bit data (word address and write data).
- Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'. When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (μ-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop cindition (stop bit), and ends read action. And this IC gets in status.

○Device addressing

- Output slave address after start condition from master.
- The significant 4 bits of slave address are used for recognizing a device type.
  The device code of this IC is fixed to '1010'.
- Next slave addresses (A2 A1 A0 --- device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses.
- The most insignificant bit (R/$\overline{W}$ --- READ / $\overline{WRITE}$) of slave address is used for designating write or read action, and is as shown below.

Setting R / $\overline{W}$ to 0 ------- write (setting 0 to word address setting of random read)
Setting R / $\overline{W}$ to 1 ------- read

Type	Slave address	Maximum number of Connected buses
BR24G02-3A	1 0 1 0 A2 A1 A0 R/$\overline{W}$	8

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●Write Command

○Write cycle

・Arbitrary data is written to EEPROM. When to write only 1 byte, byte write is normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle. Up to 8 arbitrary bytes can be written.

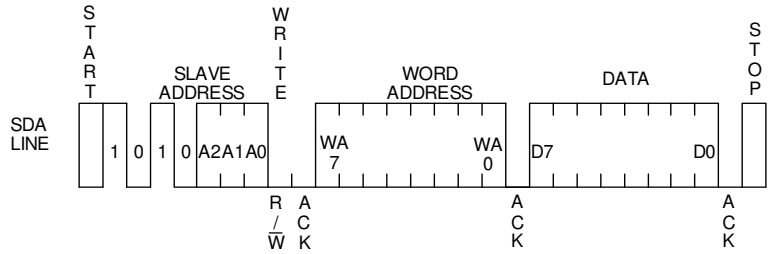

Figure 36. Byte write cycle

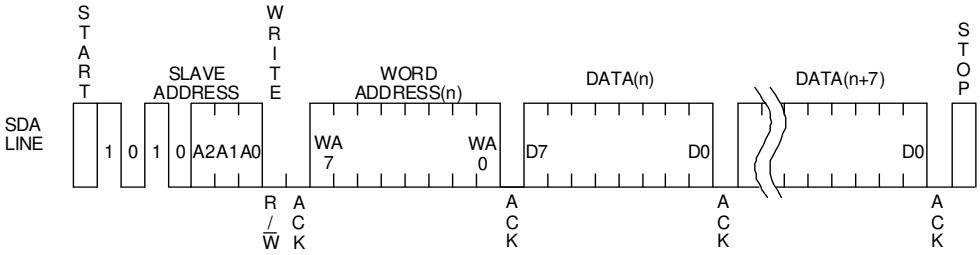

Figure 37. Page write cycle

・During internal write execution, all input commands are ignored, therefore ACK is not sent back.
・Data is written to the address designated by word address (n-th address)
・By issuing stop bit after 8bit data input, write to memory cell inside starts.
・When internal write is started, command is not accepted for tWR (5ms at maximum).
・By page write cycle, data up to 8 bytes can be written in bulk.

And when data of the maximum bytes or higher is sent, data from the first byte is overwritten.
(Refer to "Internal address increment")

・As for page write cycle of BR24G02-3A, after the significant 5 bits of word address are designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 3 bits is incremented internally, and data up to 8 bytes can be written.

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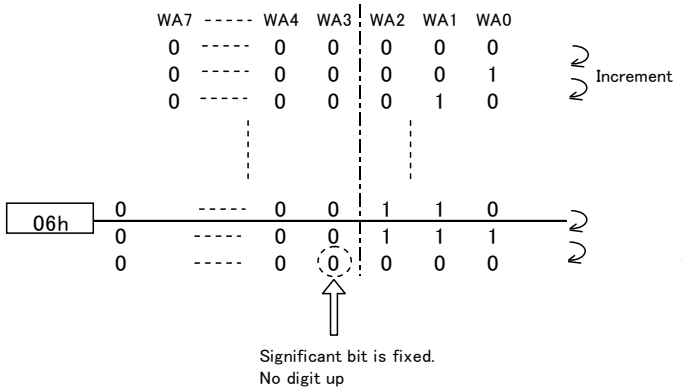
○Notes on write cycle continuous input

The maximum page numbers of BR24G02-3A are 8 bytes. Any bytes below these can be written.

1 page=8bytes, but the page write cycle time is 5ms at maximum for 8byte bulk write.
It does not stand 5ms at maximum × 8byte=40ms(Max.)

○Internal address increment
Page write mode



For example, when it is started from address 06h, therefore, increment is made as below,
06h→07h→00h→01h・・・ which please note.

※06h・・・06 in hexadecimal, therefore, 00000110 becomes a binary number.

○Write protect (WP) terminal

・Write protect (WP) function

When WP terminal is set Vcc (H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not use it open.

In the case of use it as an ROM, it is recommended to connect it to pull up or Vcc.

At extremely low voltage at power ON / OFF, by setting the WP terminal 'H', mistake write can be prevented.

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●Read Command

○Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle.

Random read cycle is a command to read data by designating address, and is used generally.

Current read cycle is a command to read data of internal address register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data can be read in succession.

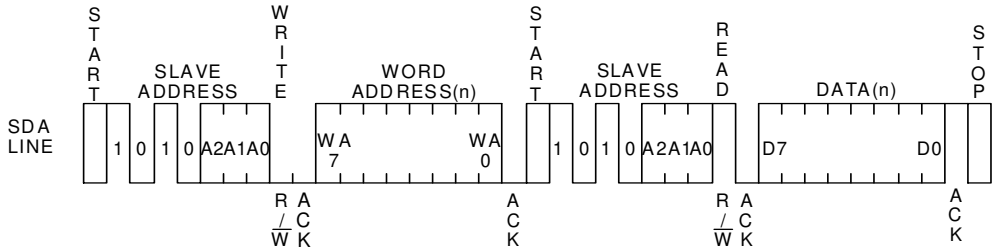

Figure 38. Random read cycle

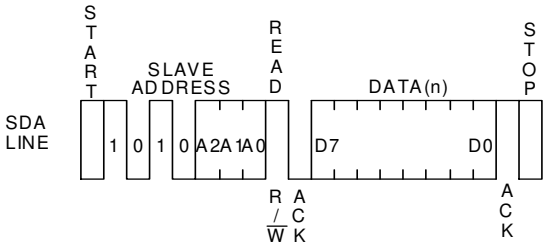

Figure 39. Current read cycle

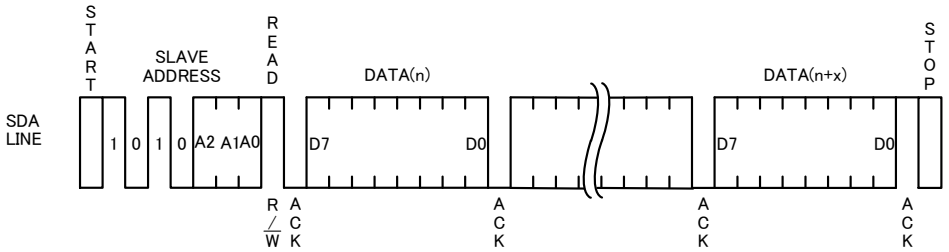

Figure 40. Sequential read cycle (in the case of current read cycle)

- In random read cycle, data of designated word address can be read.
- When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th address, i.e., data of the (n+1)-th address is output.
- When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (μ-COM) side, the next address data can be read in succession.
- Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal is started at SCL signal 'H' .
- When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.

  Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input 'H' to ACK signal after D0, and to start SDA at SCL signal 'H'.
- Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is started at SCL signal 'H'.

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●Software Reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Figure 41-(a), Figure 41-(b), Figure 41-(c)) In dummy clock input area, release the SDA bus ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

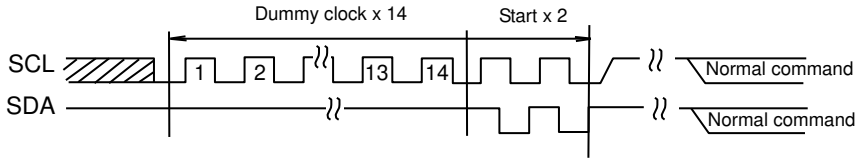

Figure 41-(a). Dummy clock x 14 + START + START + command input

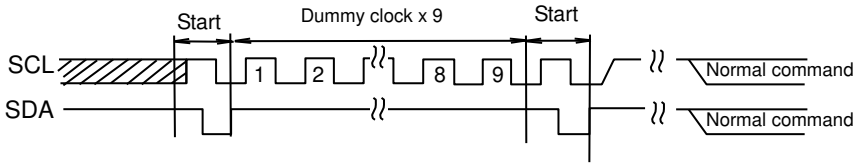

Figure 41-(b). START + dummy clock x 9 + START + command input

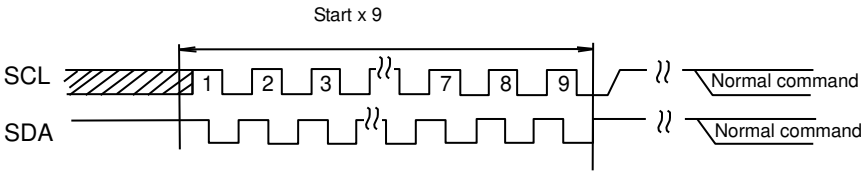

Figure 41-(c). START x 9 + command input

※Start command from START input.

●Acknowledge Polling

During internal write execution, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write action, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR = 5ms.

When to write continuously, R/$\overline{W}$ = 0, when to carry out current read cycle after write, slave address R/$\overline{W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

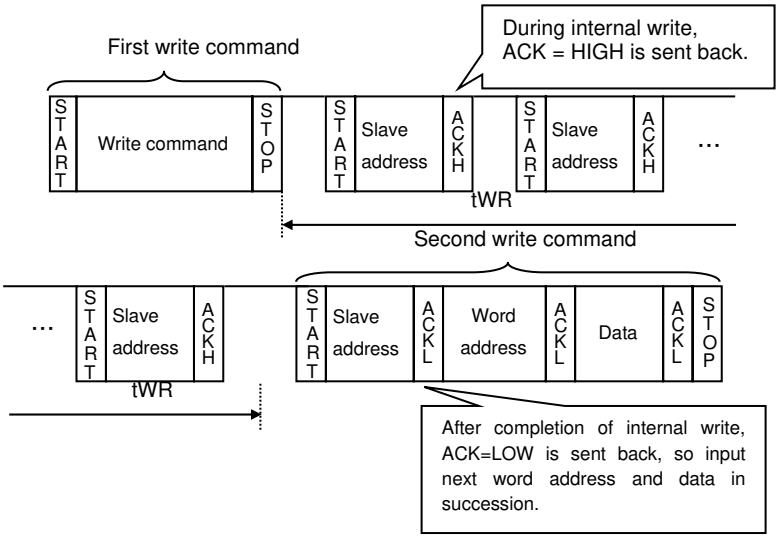

Figure 42. Case to continuously write by acknowledge polling

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●WP Valid Timing (Write Cancel)

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing. During write cycle execution, in cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data(in page write cycle, the first byte data) is cancel invalid area.
WP input in this area becomes don't care. The area from the rise of SCL to take in D0 to input the stop condition is cancel valid area. And, after execution of forced end by WP, standby status gets in.

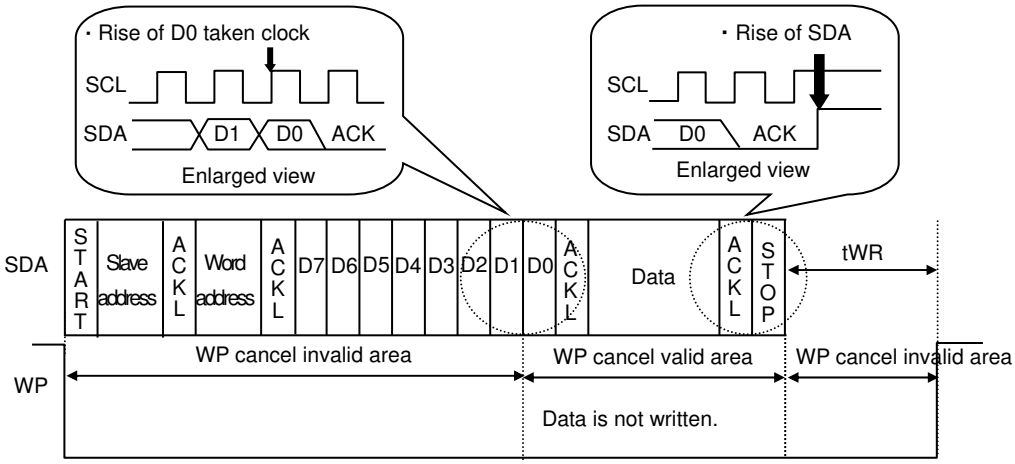

Figure 43. WP valid timing

●Command Cancel by Start Condition and Stop Condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Figure 44)
However, in ACK output area and during data read, SDA bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

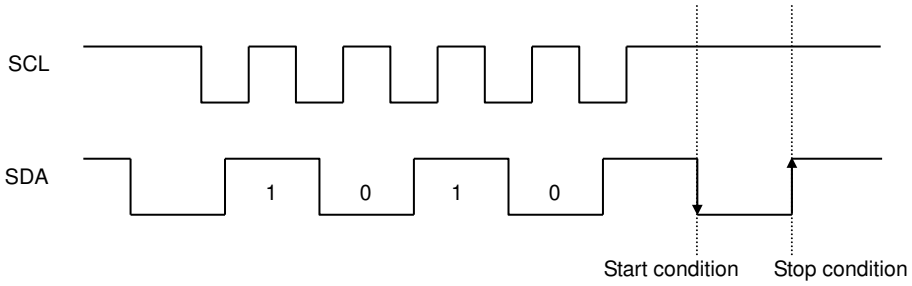

Figure 44. Case of cancel by start, stop condition during slave address input

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●I/O Peripheral Circuit

○Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value (R_{PU}), select an appropriate value to this resistance value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, action frequency is limited. The smaller the R_{PU}, the larger the supply current.

○Maximum value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

①SDA rise time to be determined by the capacitance (CBUS) of bus line of R_{PU} and SDA should be tR or below.
And AC timing should be satisfied even when SDA rise time is late.

②The bus electric potential Ⓐ to be determined by input leak total (I_L) of device connected to bus at output of 'H' to SDA bus and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin 0.2Vcc.

$$VCC - ILRPU - 0.2\,VCC \geqq VIH$$

$$\therefore \quad R_{PU} \leqq \frac{0.8V_{CC} - V_{IH}}{I_L}$$

Ex.) VCC =3V IL=10μA VIH=0.7 VCC

from②

$$R_{PU} \leqq \frac{0.8\times3 - 0.7\times3}{10\times10^{-6}}$$

$$\leqq 30 \ [k\Omega]$$

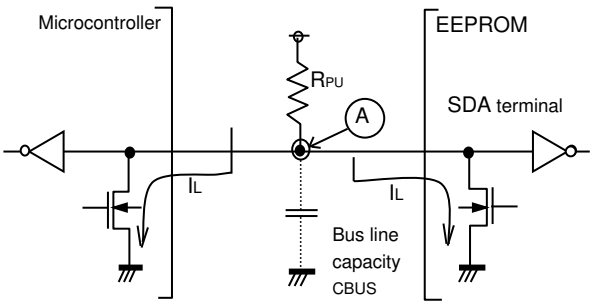

Figure 45. I/O circuit diagram

○ Minimum value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

When IC outputs LOW, it should be satisfied that V_{OLMAX}=0.4V and I_{OLMAX}=3mA.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{V_{CC} - V_{OL}}{I_{OL}}$$

②VOLMAX=0.4V should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including recommended noise margin 0.1Vcc.

$$VOLMAX \leqq VIL - 0.1\,VCC$$

Ex.) VCC =3V, VOL=0.4V, IOL=3mA, microcontroller, EEPROM V_{IL}=0.3Vcc

from①

$$R_{PU} \geqq \frac{3 - 0.4}{3\times10^{-3}}$$

$$\geqq 867 \ [\Omega]$$

And VOL=0.4 [V]

VIL=0.3×3

=0.9 [V]

Therefore, the condition ② is satisfied.

○Pull up resistance of SCL terminal

When SCL control is made at CMOS output port, there is no need, but in the case there is timing where SCL becomes 'Hi-Z', add a pull up resistance. As for the pull up resistance, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

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●Cautions on Microcontroller Connection

○RS

In I²C BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance Rpu and the SDA terminal of EEPROM. This is controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. Rs also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, Rs can be used.

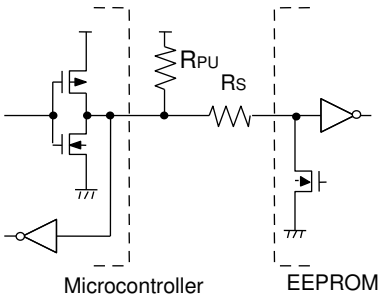

Figure 46. I/O circuit diagram

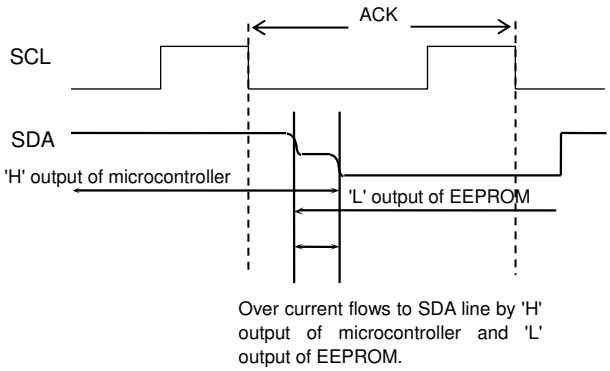

Figure 47. Input / output collision timing

○Maximum value of Rs

The maximum value of Rs is determined by the following relations.

①SDA rise time to be determined by the capacity (CBUS) of bus line of Rpu and SDA should be tR or below.
And AC timing should be satisfied even when SDA rise time is late.

②The bus electric potential Ⓐ to be determined by Rpu and Rs the moment when EEPROM outputs 'L' to SDA bus sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin 0.1Vcc.

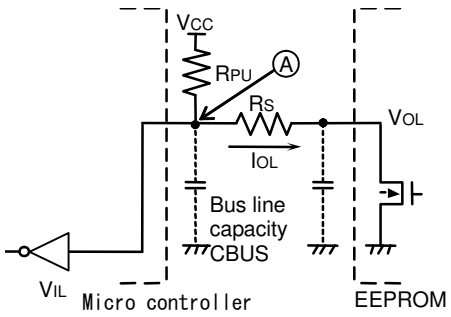

Figure 48. I/O Circuit Diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Ex.) V_{CC}=3V V_{IL}=0.3V_{CC} V_{OL}=0.4V R_{PU}=20kΩ

$$R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67[k\Omega]$$

○Minimum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

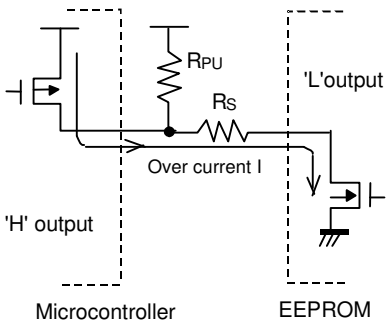

Figure 49. I/O circuit diagram

$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{V_{CC}}{I}$$

Ex.) VCC=3V, I=10mA

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300[\Omega]$$

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●I/O Equivalence Circuit

○Input (A2,A1,A0,SCL, WP)

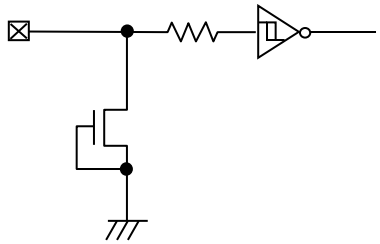

Figure 50. Input pin circuit diagram

○Input / output (SDA)

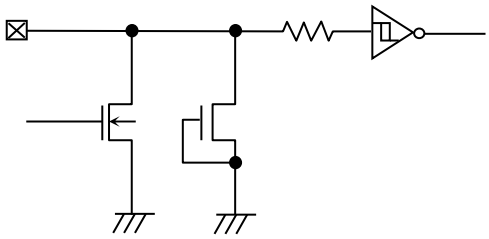

Figure 51. Input / output pin circuit diagram

●Power-up / Down Conditions

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the action, observe the following conditions at power on.

1. Set SDA = 'H' and SCL ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of t_R, t_{OFF}, and Vbot for operating POR circuit.

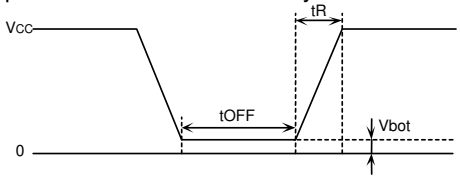

Figure 52. Rise waveform diagram

Recommended conditions of tR, tOFF,Vbot

tR	tOFF	Vbot
10ms or below	10ms or larger	0.3V or below
100 or below	10ms or larger	0.2V or below

3. Set SDA and SCL so as not to become 'Hi-Z'.

When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

a) In the case when the above condition 1 cannot be observed. When SDA becomes 'L' at power on .
→Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

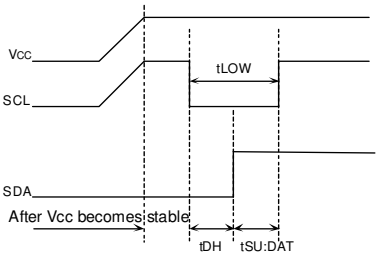

Figure 53. When SCL= 'H' and SDA= 'L'

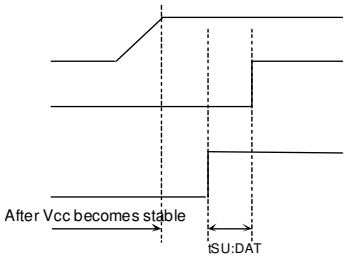

Figure 54. When SCL='L' and SDA='L'

b) In the case when the above condition 2 cannot be observed.
→After power source becomes stable, execute software reset(P18).

c) In the case when the above conditions 1 and 2 cannot be observed.
→Carry out a), and then carry out b).

●Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite action at low power, and prevents wrong write. At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

●Noise Countermeasures

○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible.
And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

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●Operational Notes

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5) Terminal design

In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

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●**Part Numbering**

B	R	2	4	G	0	2	x	x	x	-	3	A	x	x	x	x

BUS type
24 : I²C

Operating temperature/
Operating Voltage
-40℃ to +85℃ / 1.6V to 5.5V

Capacity
02=2K

Package
Blank : DIP-T8
FJ : SOP-J8
FVJ : TSSOP-B8J
NUX : VSON008X2030
F : SOP8
FVT : TSSOP-B8
FVM : MSOP8

Process code

Revision

G : Halogen free
Blank : Not Halogen free
As an exception, VSON008X2030 package will be Halogen free with “Blank”

T : 100% Sn
Blank : 100% Sn

Packaging and forming specification
E2 : Embossed tape and reel
(SOP8, SOP-J8, TSSOP-B8, TSSOP-B8J)
TR : Embossed tape and reel
(MSOP8, VSON008X2030)
None : Tube
(DIP-T8)

Lineup

Capacity	Package		Orderable Part Number		Remark	
	Type	Quantity				
2K	DIP-T8	Tube of 2000	BR24G02	-3A	Not Halogen free	100% Sn
	SOP8	Reel of 2500	BR24G02F	-3AGTE2	Halogen free	100% Sn
	SOP-J8		BR24G02FJ	-3AGTE2	Halogen free	100% Sn
	TSSOP-B8	Reel of 3000	BR24G02FVT	-3AGE2	Halogen free	100% Sn
	TSSOP-B8J	Reel of 2500	BR24G02FVJ	-3AGTE2	Halogen free	100% Sn
	MSOP8	Reel of 3000	BR24G02FVM	-3AGTTR	Halogen free	100% Sn
	VSON008X2030	Reel of 4000	BR24G02NUX	-3ATTR	Halogen free	100% Sn

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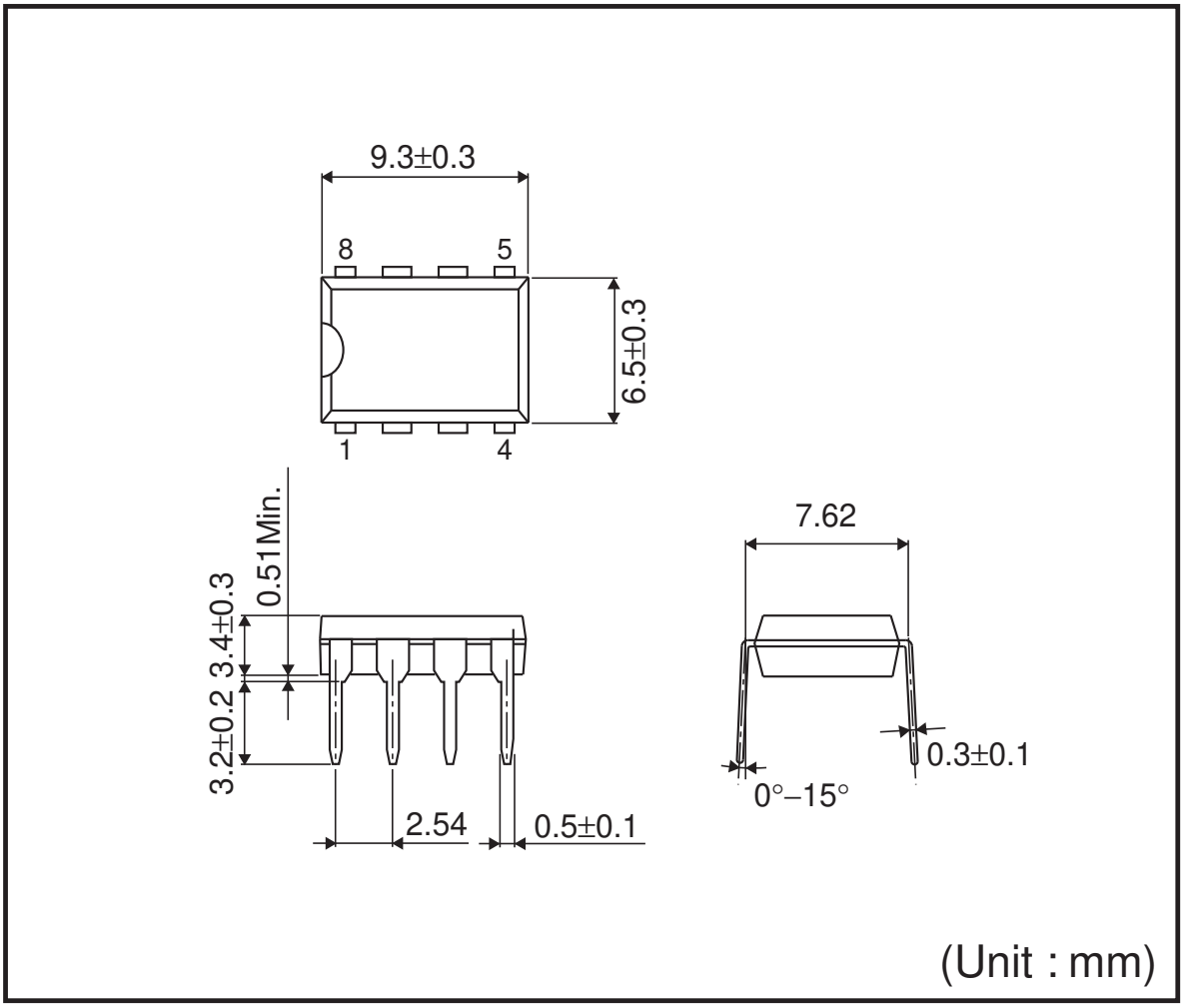
●**Physical Dimensions Tape and Reel Information**

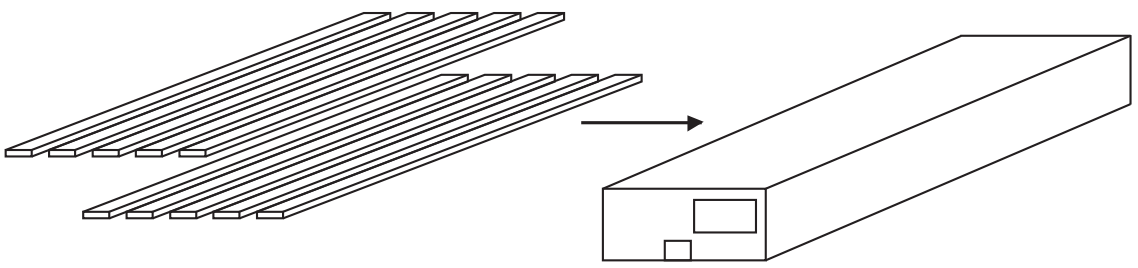
DIP-T8



(Unit : mm)

<Tape and Reel information>

Container	Tube
Quantity	2000pcs
Direction of feed	Direction of products is fixed in a container tube



∗Order quantity needs to be multiple of the minimum quantity.

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