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Serial EEPROM Series Standard EEPROM

I²C BUS EEPROM (2-Wire)

BR24Gxxx-3A (128K 256K 1M)

General Description

BR24Gxxx-3A is a serial EEPROM of I²C BUS Interface Method

Features

- All controls available by 2 ports of serial clock(SCL) and serial data(SDA)
- Other devices than EEPROM can be connected to the same port, saving microcontroller port
- 1.7V to 5.5V Single Power Source Operation most suitable for battery use
- 1.7V to 5.5V wide limit of operating voltage, possible 1MHz operation
- Page Write Mode useful for initial value write at factory shipment
- Self-timed Programming Cycle
- Low Current Consumption
- Prevention of Write Mistake
  - Write (Write Protect) Function added
  - Prevention of Write Mistake at Low Voltage
- More than 1 million write cycles
- More than 40 years data retention
- Noise filter built in SCL / SDA terminal
- Initial delivery state FFh

Packages W(Typ) x D(Typ)x H(Max)

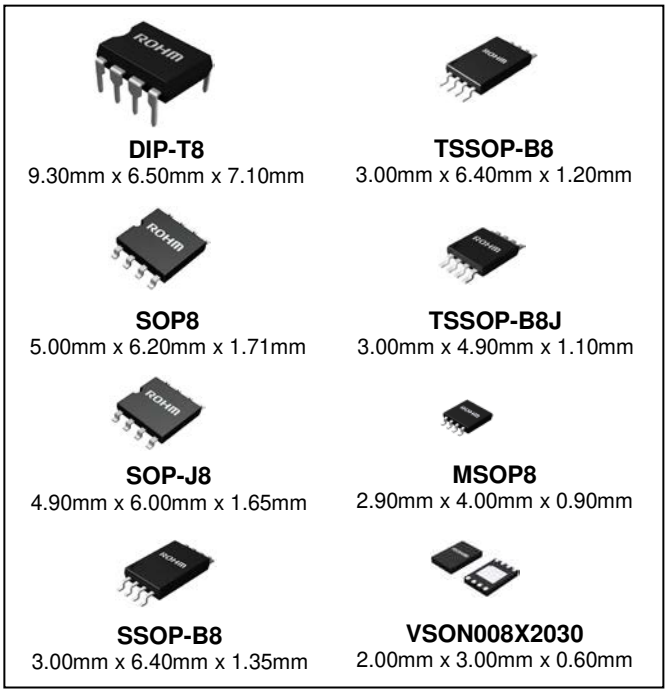


Figure 1.

Page Write

Number of Pages	64Byte	256Byte
Product Number	BR24G128-3A BR24G256-3A	BR24G1M-3A

BR24G128-3A

Capacity	Bit Format	Type	Power Source Voltage	Package
128kbit	16k×8	BR24G128-3A	1.7V to 5.5V	DIP-T8
		BR24G128F-3A		SOP8
		BR24G128FJ-3A		SOP-J8
		BR24G128FV-3A		SSOP-B8
		BR24G128FVT-3A		TSSOP-B8
		BR24G128FVJ-3A		TSSOP-B8J
		BR24G128FVM-3A		MSOP8
		BR24G128NUX-3A		VSON008X2030

BR24G256-3A

Capacity	Bit Format	Type	Power Source Voltage	Package
256kbit	32k×8	BR24G256-3A	1.7V to 5.5V	DIP-T8
		BR24G256F-3A		SOP8
		BR24G256FJ-3A		SOP-J8
		BR24G256FV-3A		SSOP-B8
		BR24G256FVT-3A		TSSOP-B8

BR24G1M-3A

Capacity	Bit Format	Type	Power Source Voltage	Package
1Mbit	128k×8	BR24G1M-3A	1.7V to 5.5V	DIP-T8
		BR24G1MF-3A		SOP8
		BR24G1MFJ-3A		SOP-J8

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	Vcc	-0.3 to +6.5	V	
Power Dissipation	Pd	0.45 (SOP8)	W	Derate by 4.5mW/°C when operating above Ta=25°C
		0.45 (SOP-J8)		Derate by 4.5mW/°C when operating above Ta=25°C
		0.30 (SSOP-B8)		Derate by 3.0mW/°C when operating above Ta=25°C
		0.33 (TSSOP-B8)		Derate by 3.3mW/°C when operating above Ta=25°C
		0.31 (TSSOP-B8J)		Derate by 3.1mW/°C when operating above Ta=25°C
		0.31 (MSOP8)		Derate by 3.1mW/°C when operating above Ta=25°C
		0.30 (VSON008X2030)		Derate by 3.0mW/°C when operating above Ta=25°C
		0.80 (DIP-T8)		Derate by 8.0mW/°C when operating above Ta=25°C
Storage Temperature	Tstg	-65 to +150	°C	
Operating Temperature	Topr	-40 to +85	°C	
Input Voltage / Output Voltage	-	-0.3 to Vcc+1.0	V	The Max value of Input Voltage/Output Voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value Input Voltage/Output Voltage is not lower than -1.0V.
Junction Temperature	Tjmax	150	°C	Junction temperature at the storage condition
Electrostatic discharge voltage (human body model)	V_{ESD}	-4000 to +4000	V	

Memory Cell Characteristics (Ta=25°C, Vcc=1.7V to 5.5V)

Parameter	Limit			Unit
	Min	Typ	Max	
Write Cycles (1)	1,000,000	-	-	Times
Data Retention (1)	40	-	-	Years

(1) Not 100% TESTED

Recommended Operating Ratings

Parameter	Symbol	Rating	Unit
Power Source Voltage	Vcc	1.7 to 5.5	V
Input Voltage	V_{IN}	0 to Vcc	

DC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, Vcc =1.7V to 5.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input High Voltage 1	V_{IH1}	0.7Vcc	-	Vcc+1.0	V	
Input Low Voltage 1	V_{IL1}	-0.3(2)	-	+0.3Vcc	V	
Output Low Voltage 1	V_{OL1}	-	-	0.4	V	I_{OL}=3.0mA, 2.5V≦Vcc≦5.5V (SDA)
Output Low Voltage 2	V_{OL2}	-	-	0.2	V	I_{OL}=0.7mA, 1.7V≦Vcc＜2.5V (SDA)
Input Leakage Current	I_{LI}	-1	-	+1	μA	V_{IN}=0 to Vcc
Output Leakage Current	I_{LO}	-1	-	+1	μA	V_{OUT}=0 to Vcc (SDA)
Supply Current (Write)	I_{CC1}	-	-	2.5	mA	V_{CC}=5.5V, f_{SCL}=1MHz, t_{WR}=5ms, Byte write, Page write BR24G128/256-3A
		-	-	4.5		V_{CC}=5.5V, f_{SCL}=1MHz, t_{WR}=5ms, Byte write, Page write BR24G1M-3A
Supply Current (Read)	I_{CC2}	-	-	2.0	mA	V_{CC}=5.5V, f_{SCL}=1MHz Random read, current read, sequential read
Standby Current	I_{SB}	-	-	2.0	μA	V_{CC}=5.5V, SDA・SCL=Vcc A0, A1, A2=GND, WP=GND BR24G128/256-3A
		-	-	3.0		V_{CC}=5.5V, SDA・SCL=Vcc A0, A1, A2=GND, WP=GND BR24G1M-3A

(2) When the pulse width is 50ns or less, it is -1.0V.

AC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, Vcc=1.7V to 5.5V)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Clock Frequency	f_{SCL}	-	-	1000	kHz
Data Clock “HIGH“ Period	t_{HIGH}	0.30	-	-	µs
Data Clock “LOW“ Period	t_{LOW}	0.5	-	-	µs
SDA, SCL (INPUT) Rise Time (1)	t_R	-	-	0.12	µs
SDA, SCL (INPUT) Fall Time (1)	t_{F1}	-	-	0.12	µs
SDA (OUTPUT) Fall Time (1)	t_{F2}	-	-	0.12	µs
Start Condition Hold Time	$t_{HD:STA}$	0.25	-	-	µs
Start Condition Setup Time	$t_{SU:STA}$	0.20	-	-	µs
Input Data Hold Time	$t_{HD:DAT}$	0	-	-	ns
Input Data Setup Time	$t_{SU:DAT}$	50	-	-	ns
Output Data Delay Time	t_{PD}	0.05	-	0.45	µs
Output Data Dold Time	t_{DH}	0.05	-	-	µs
Stop Condition Setup Time	$t_{SU:STO}$	0.25	-	-	µs
Bus Free Time	t_{BUF}	0.5	-	-	µs
Write Cycle Time	t_{WR}	-	-	5	ms
Noise Spike Width (SDA, SCL)	t_I	-	-	0.05	µs
WP Hold Time	$t_{HD:WP}$	1.0	-	-	µs
WP Setup Time	$t_{SU:WP}$	0.1	-	-	µs
WP High Period	$t_{HIGH:WP}$	1.0	-	-	µs

(1) Not 100% tested

AC Characteristics Condition

Parameter	Symbol	Conditions	Unit
Load Capacitance	C_L	100	pF
SDA, SCL (INPUT) Rise Time	t_R	20	ns
SDA, SCL (INPUT) Fall Time	t_{F1}	20	ns
Input Data Level	V_{IL1}/V_{IH1}	$0.2V_{CC}/0.8Vcc$	V
Input/Output Data Timing Reference Level	-	$0.3V_{CC}/0.7Vcc$	V

Serial Input / Output Timing

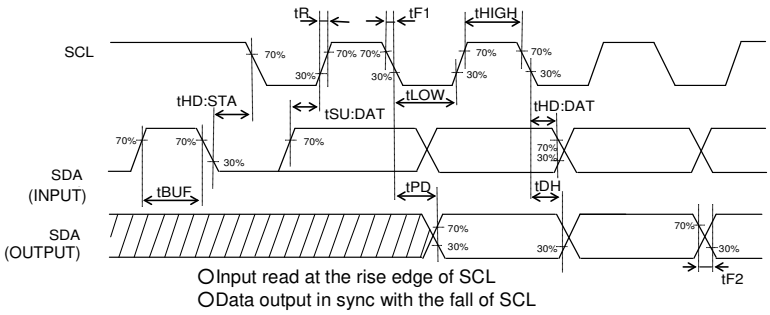


Figure 2-(a). Serial Input / Output Timing

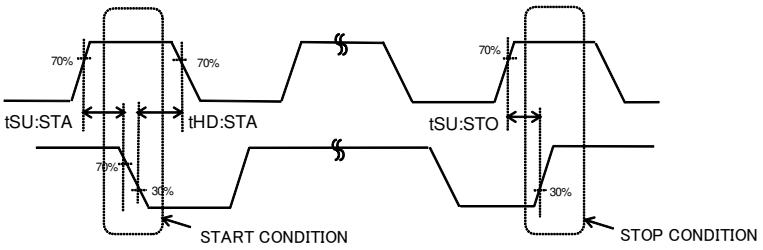


Figure 2-(b). Start-Stop Bit Timing

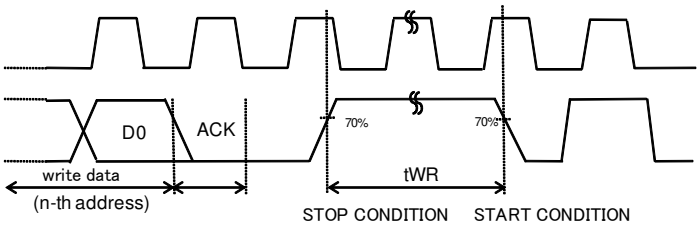


Figure 2-(c). Write Cycle Timing

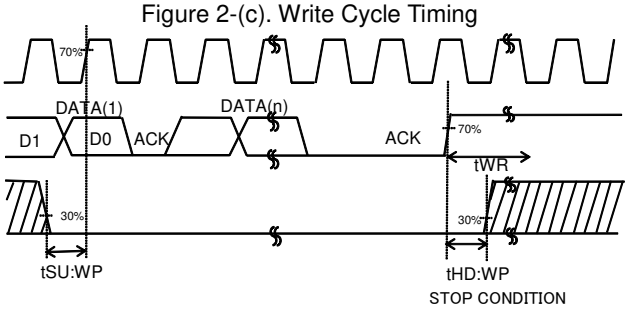


Figure 2-(d). WP Timing at Write Execution

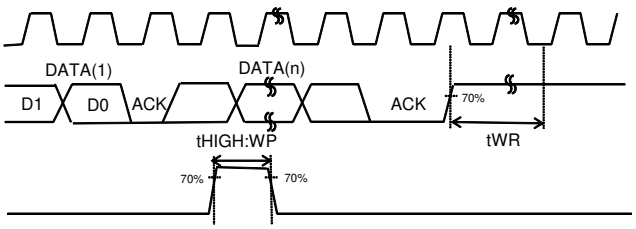
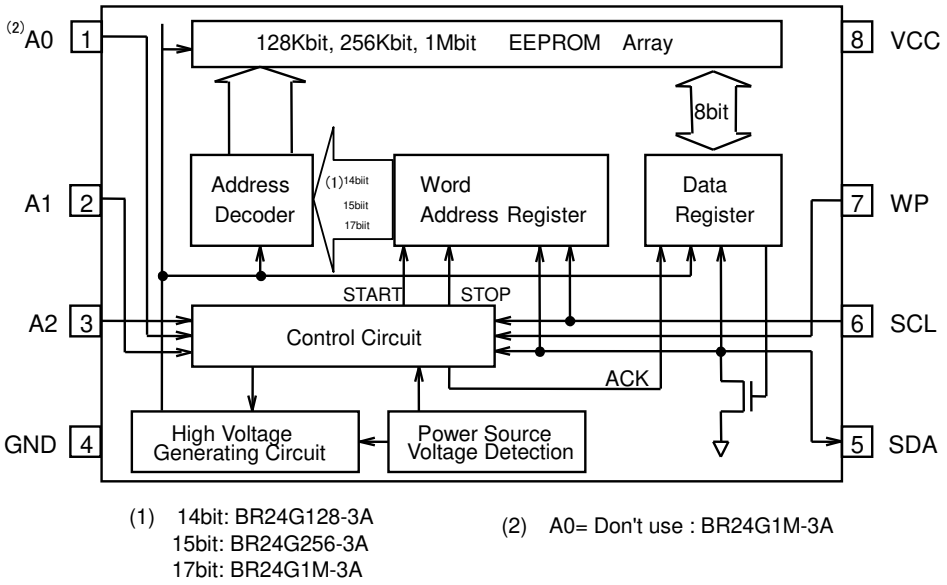


Figure 2-(e). WP Timing at Write Cancel

Block Diagram

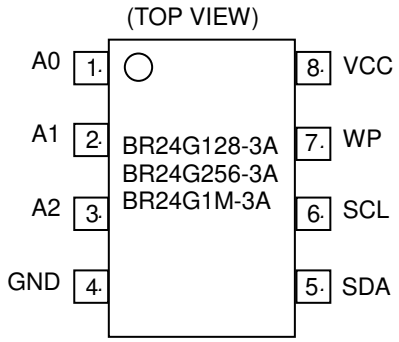


(1) 14bit: BR24G128-3A
15bit: BR24G256-3A
17bit: BR24G1M-3A

(2) A0= Don't use : BR24G1M-3A

Figure 3. Block Diagram

Pin Configuration



Pin Descriptions

Terminal Name	Input/ Output	Descriptions	
		BR24G128/256-3A	BR24G1M-3A
A0	Input	Slave address setting(2)	Don't use(1)
A1	Input	Slave address setting(2)	
A2	Input	Slave address setting(2)	
GND	-	Reference voltage of all input / output, 0V	
SDA	Input/ Output	Serial data input serial data output	
SCL	Input	Serial clock input	
WP	Input	Write protect terminal	
VCC	-	Connect the power source.	

(1) Pins not used as device address may be set to any of 'H', 'L', and 'Hi-Z'.
(2) A0, A1 and A2 are not allowed to use as open

Typical Performance Curves

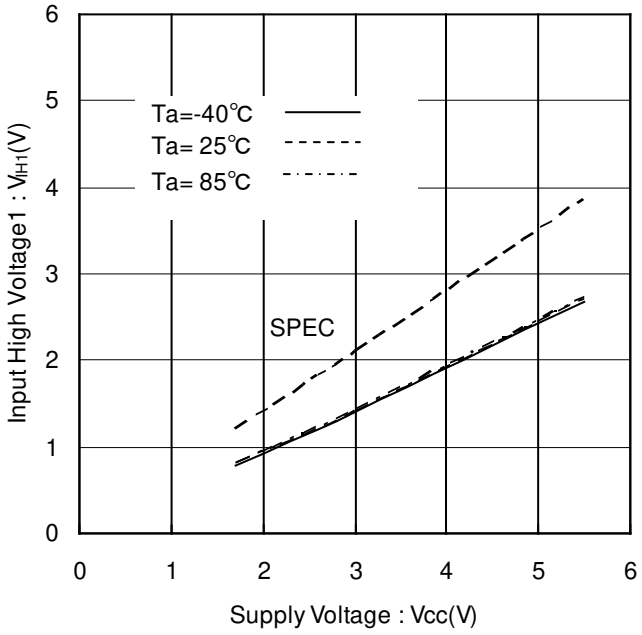


Figure 4. Input High Voltage1 vs Supply Voltage
(A0, A1, A2, SCL, SDA, WP)

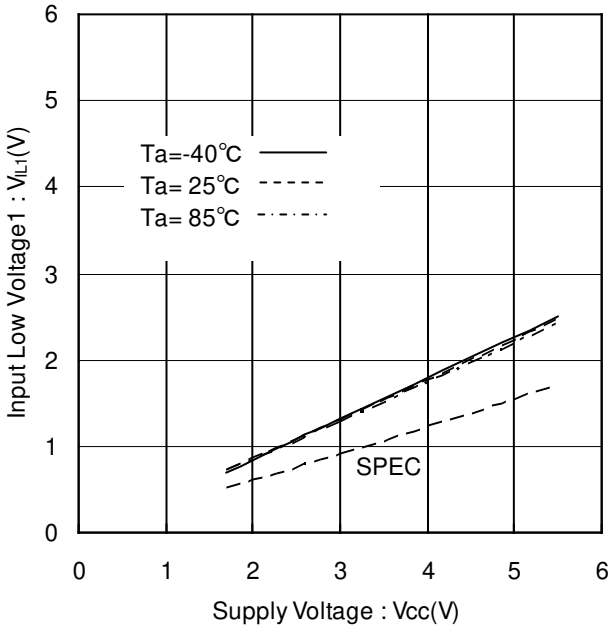


Figure 5. Input Low Voltage1 vs Supply Voltage
(A0, A1, A2, SCL, SDA, WP)

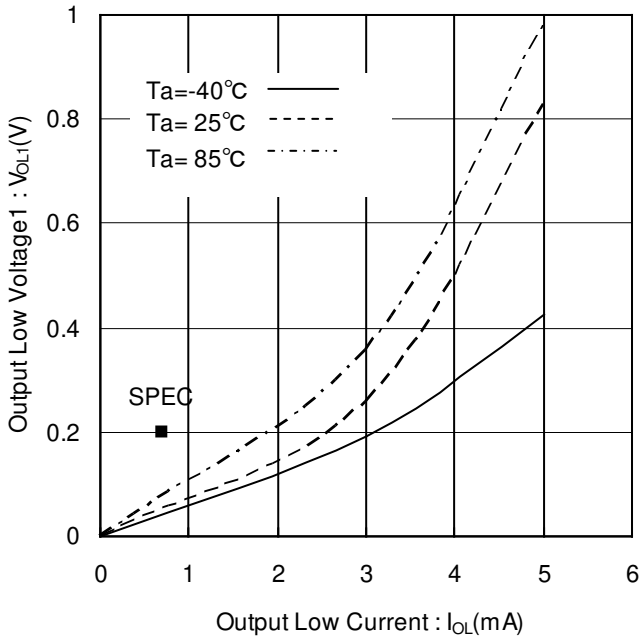


Figure 6. Output Low Voltage1 vs Output Low Current
(Vcc=2.5V)

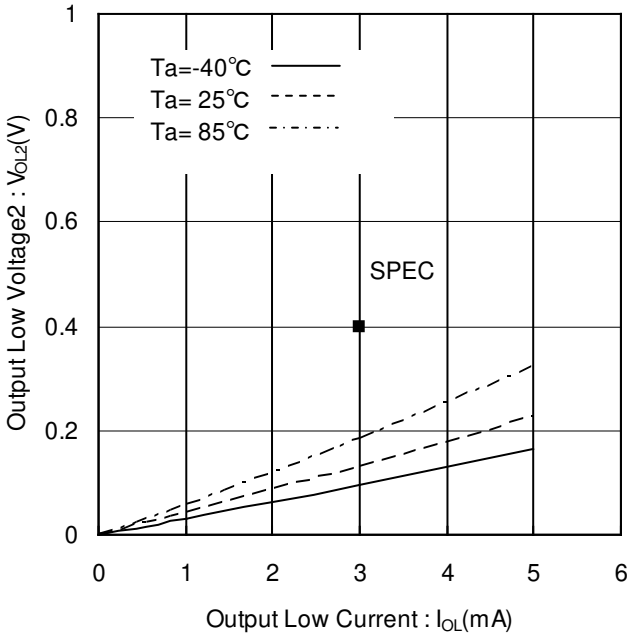


Figure 7. Output Low Voltage2 vs Output Low Current
(Vcc=1.7V)

Typical Performance Curves - continued

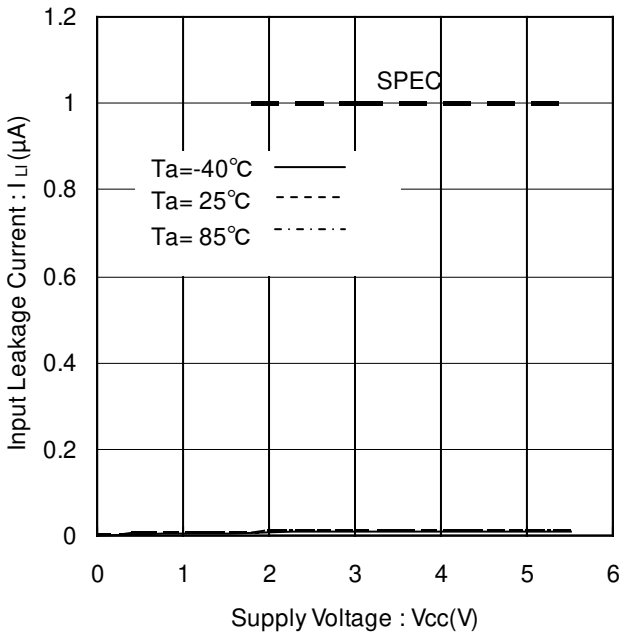


Figure 8. Input Leakage Current vs Supply Voltage (A0, A1, A2, SCL, WP)

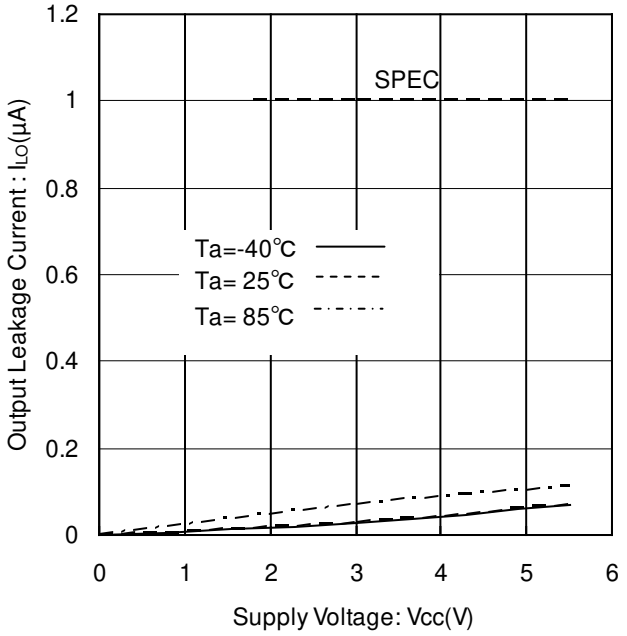


Figure 9. Output Leakage Current vs Supply Voltage (SDA)

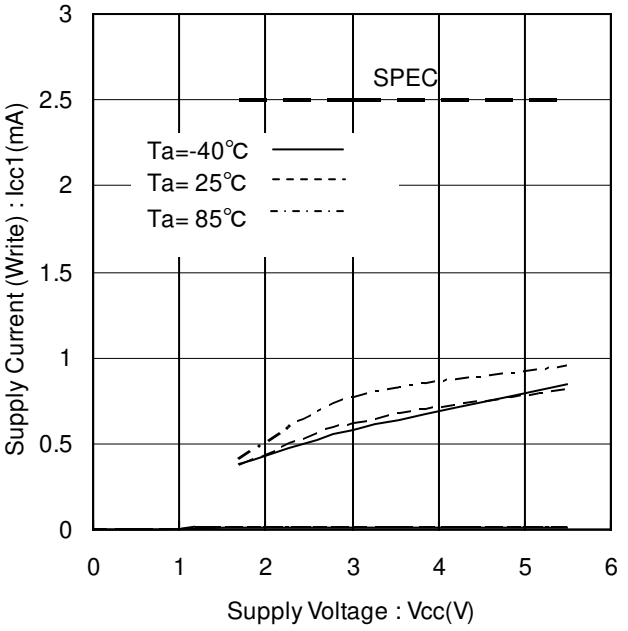


Figure 10. Supply Current (Write) vs Supply Voltage (f_{SCL}=1MHz BR24G128/256-3A)

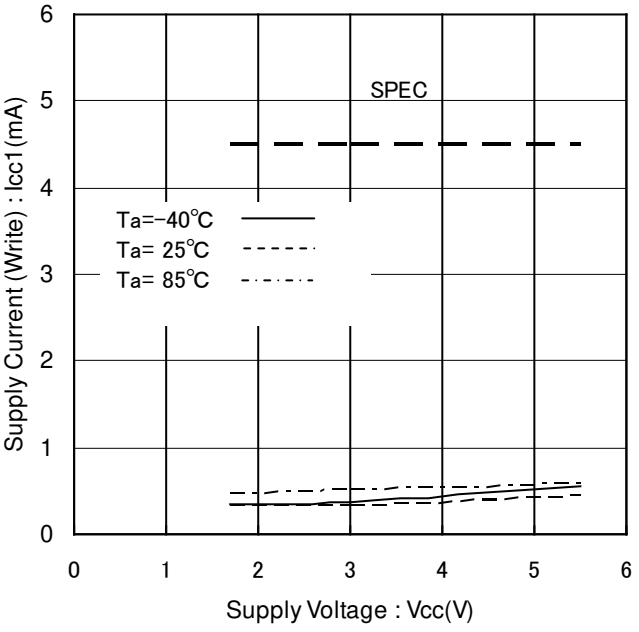


Figure 11. Supply Current (Write) vs Supply Voltage (f_{SCL}=1MHz BR24G1M-3A)

Typical Performance Curves - continued

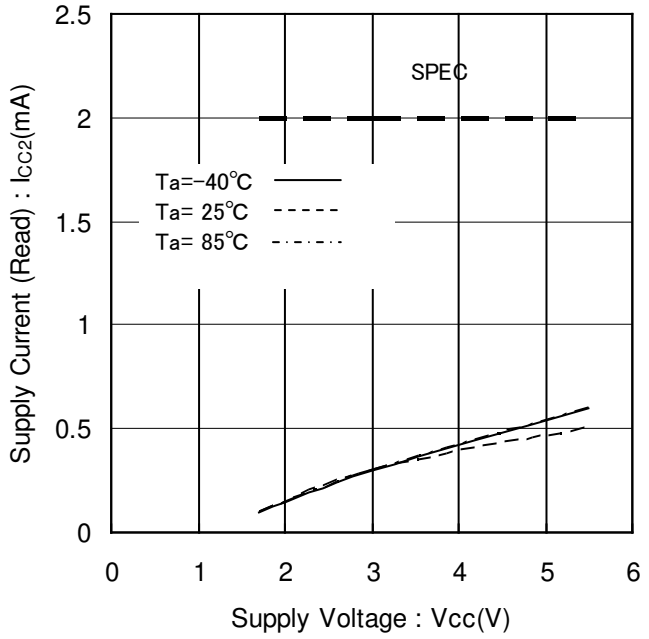


Figure 12. Supply Current (Read) vs Supply Voltage (f_{scl}=1MHz)

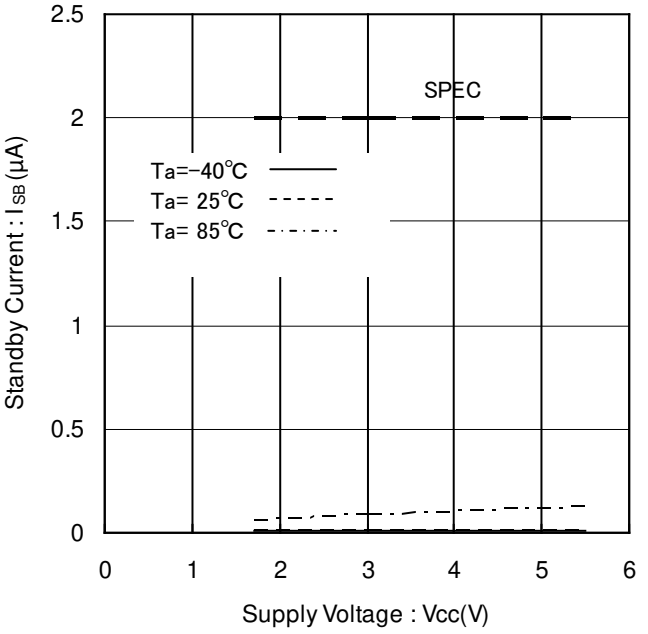


Figure 13. Standby Current vs Supply Voltage (BR24G128/256-3A)

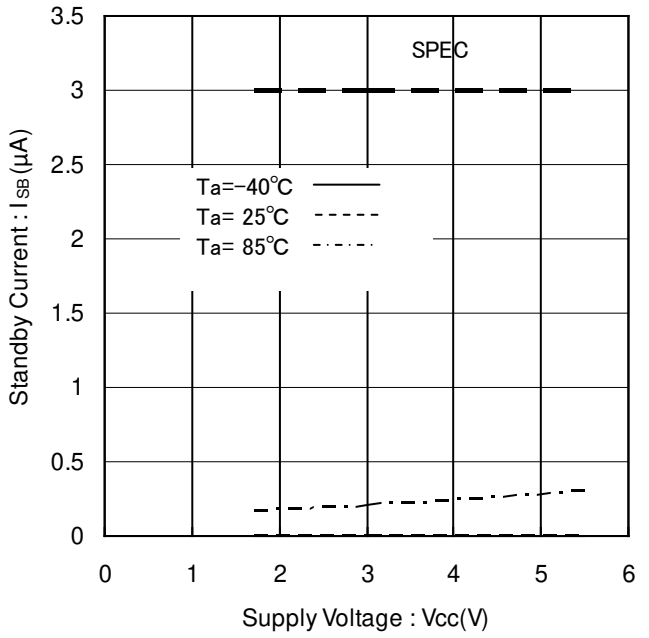


Figure 14. Standby Current vs Supply Voltage (BR24G1M-3A)

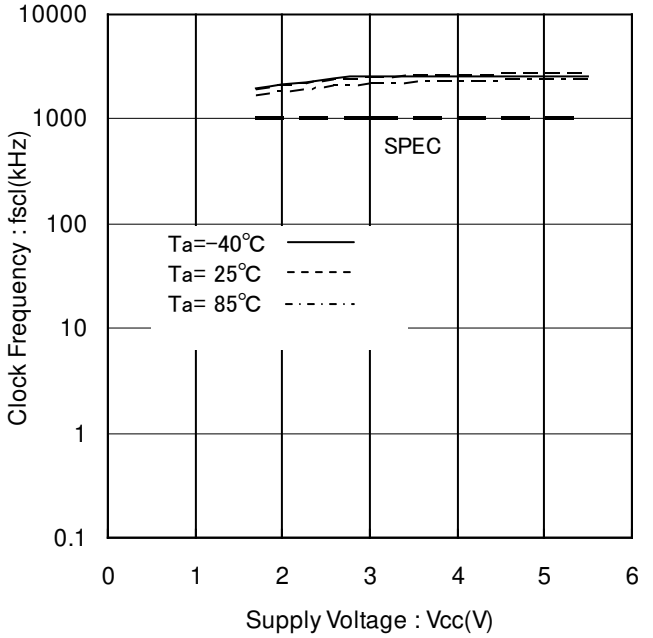


Figure 15. Clock Frequency vs Supply Voltage

Typical Performance Curves - continued

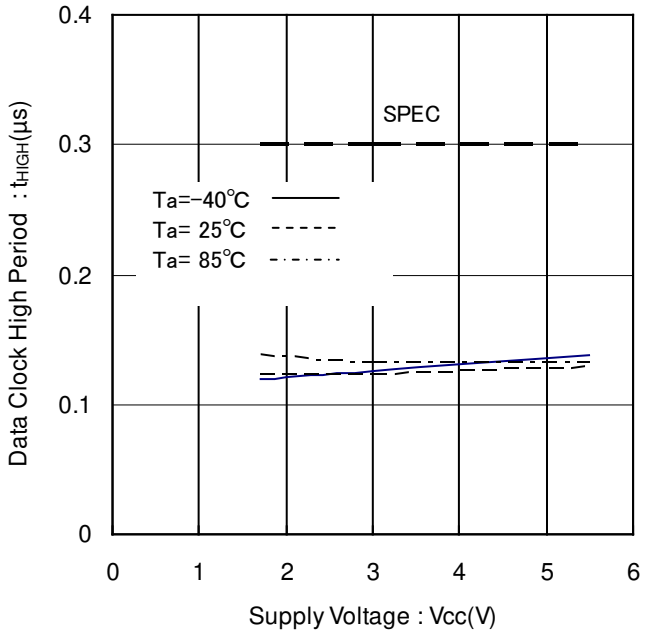


Figure 16. Data Clock High Period vs Supply Voltage

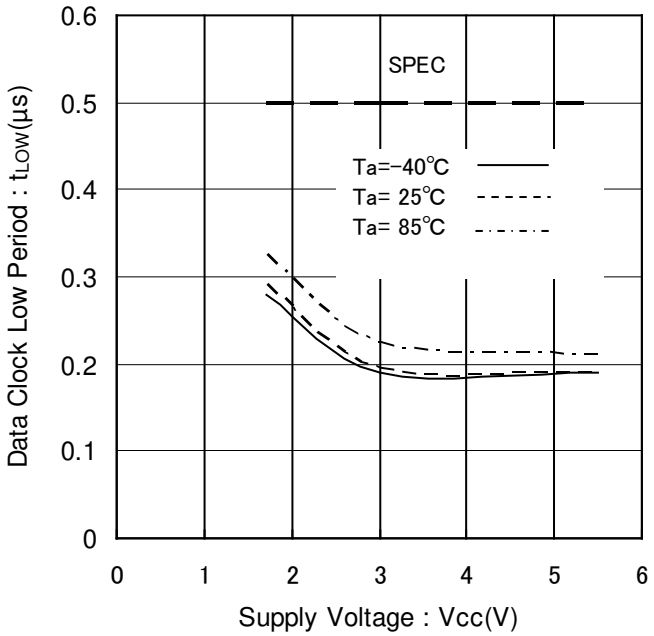


Figure 17. Data Clock Low Period vs Supply Voltage

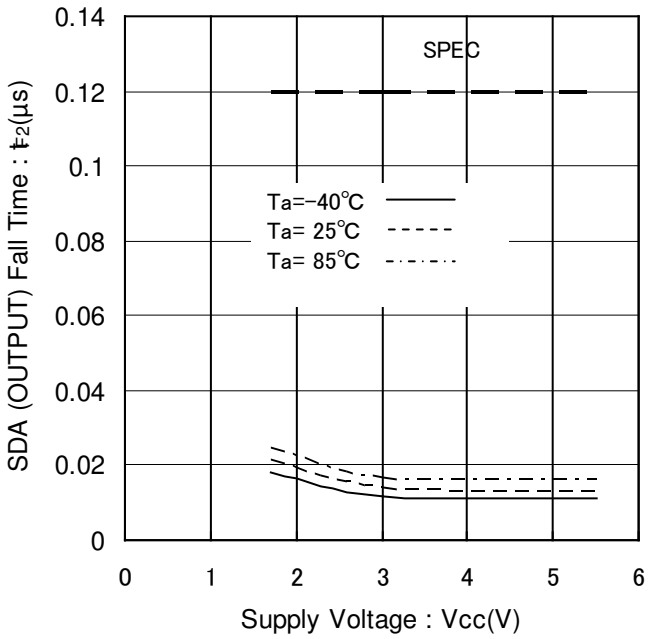


Figure18. SDA (OUTPUT) Fall Time vs Supply Voltage

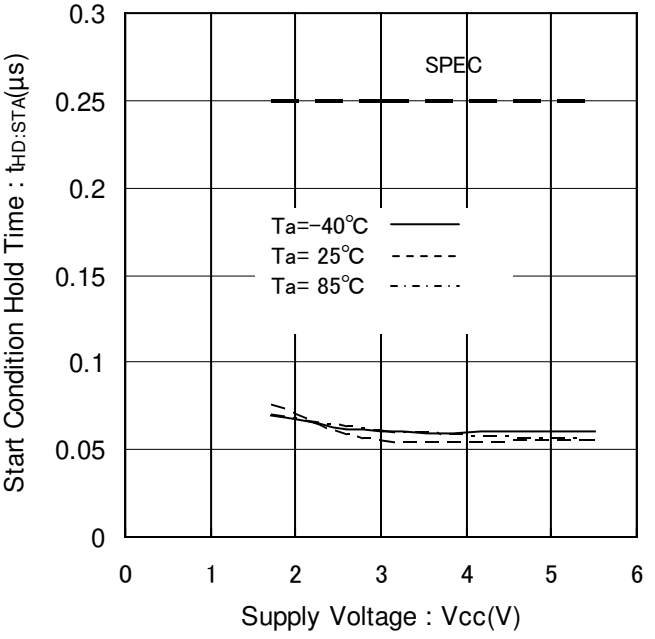


Figure 19. Start Condition Hold Time vs Supply Voltage

Typical Performance Curves - continued

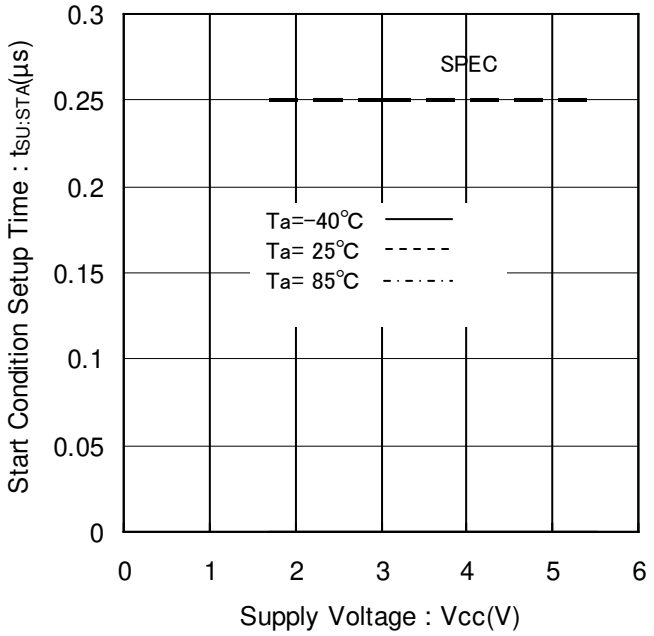


Figure 20. Start Condition Setup Time vs Supply Voltage

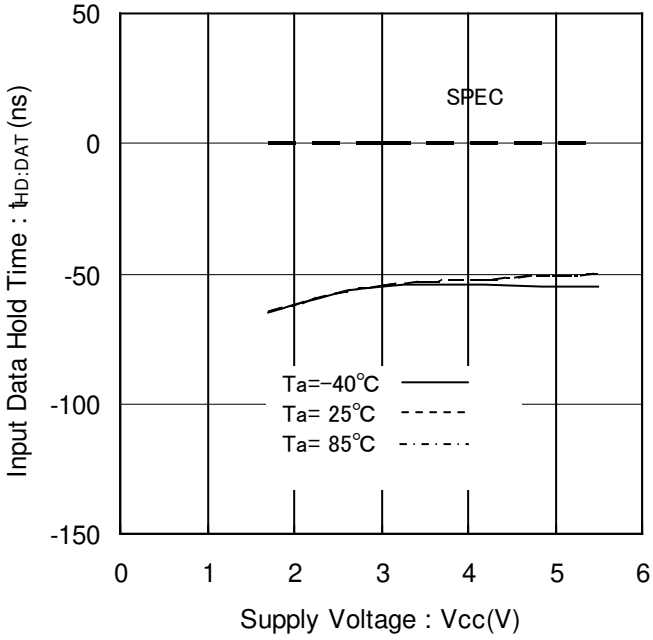


Figure 21. Input Data Hold Time vs Supply Voltage (HIGH)

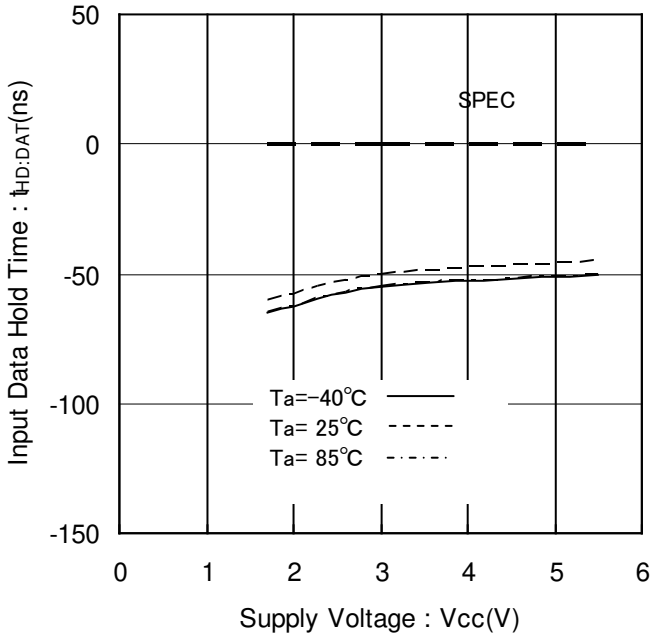


Figure 22. Input Data Hold Time vs Supply Voltage (LOW)

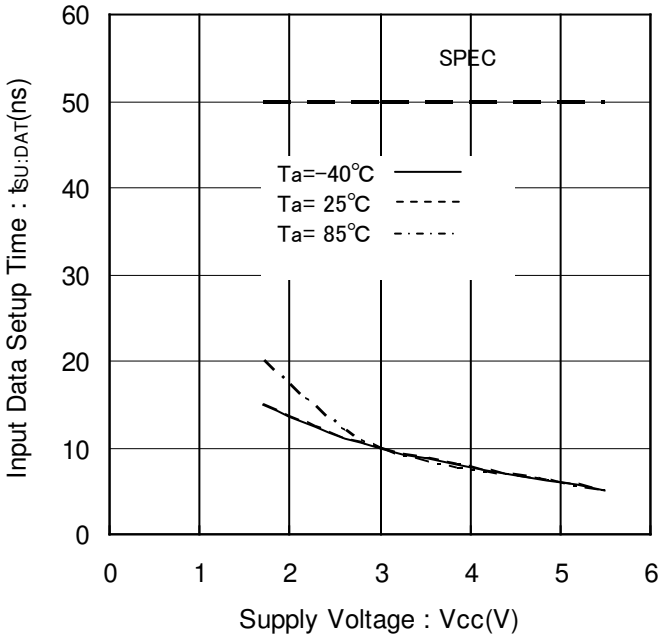


Figure 23 Input Data Setup Time vs Supply Voltage (HIGH)

Typical Performance Curves - continued

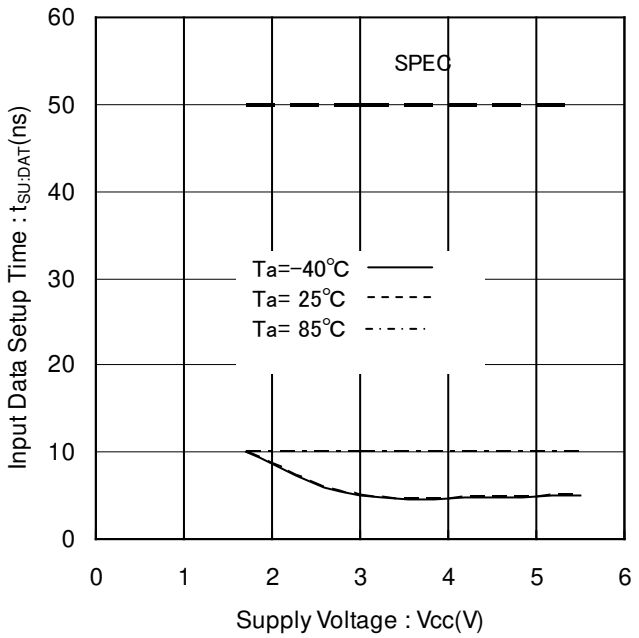


Figure 24. Input Data Setup Time vs Supply Voltage (LOW)

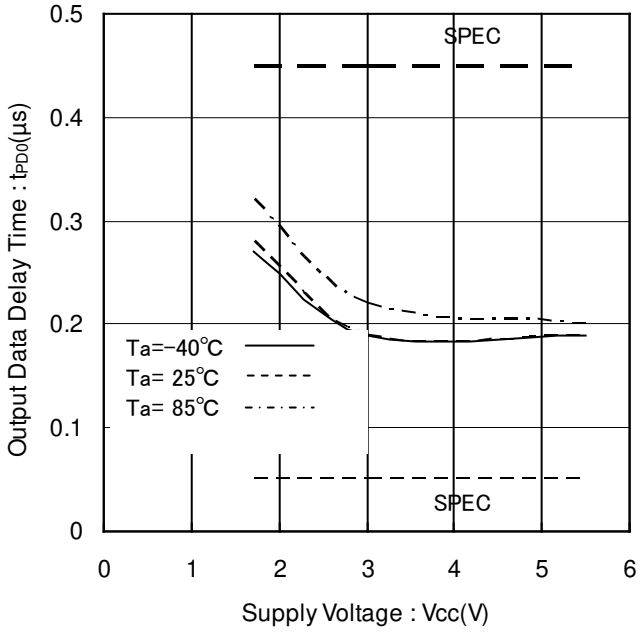


Figure 25. Output Data Delay Time vs Supply Voltage

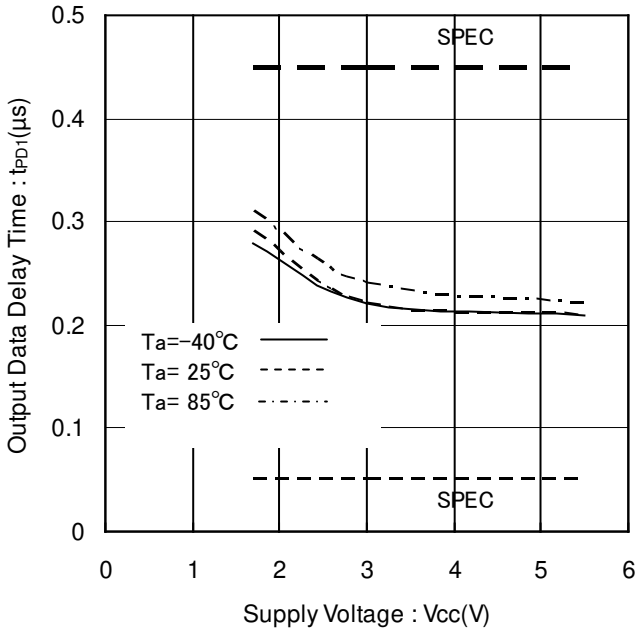


Figure 26. Output Data Delay Time vs Supply Voltage

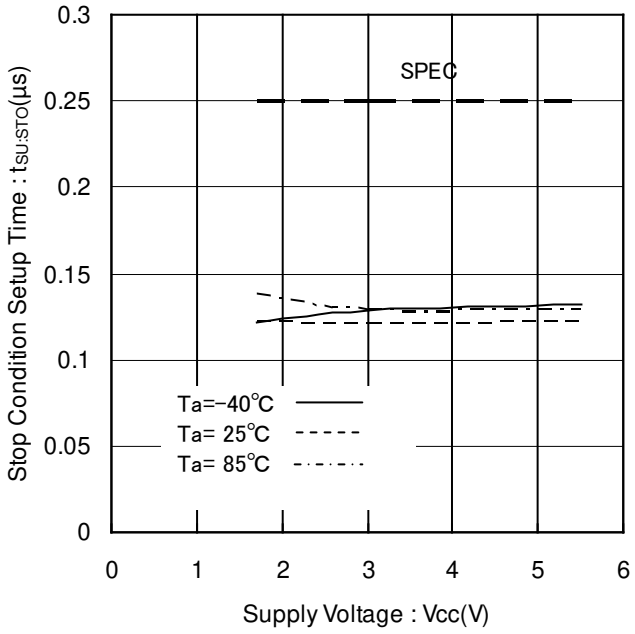


Figure 27. Stop Condition Setup Time vs Supply Voltage

Typical Performance Curves - continued

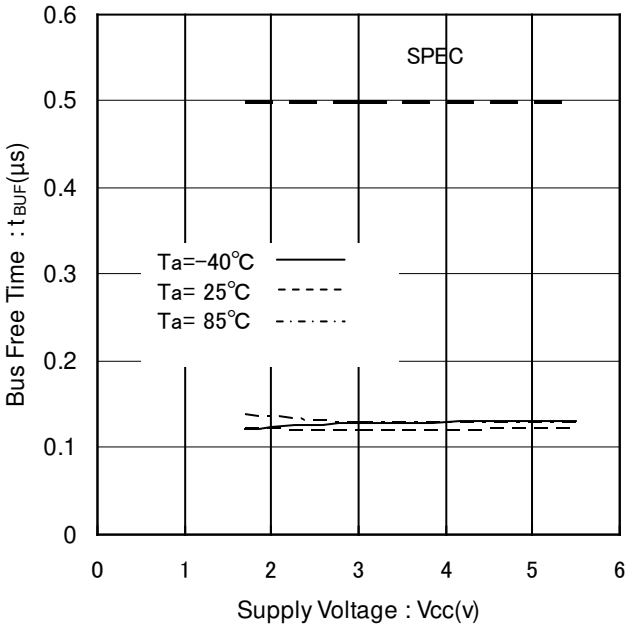


Figure 28. Bus Free Time vs Supply Voltage

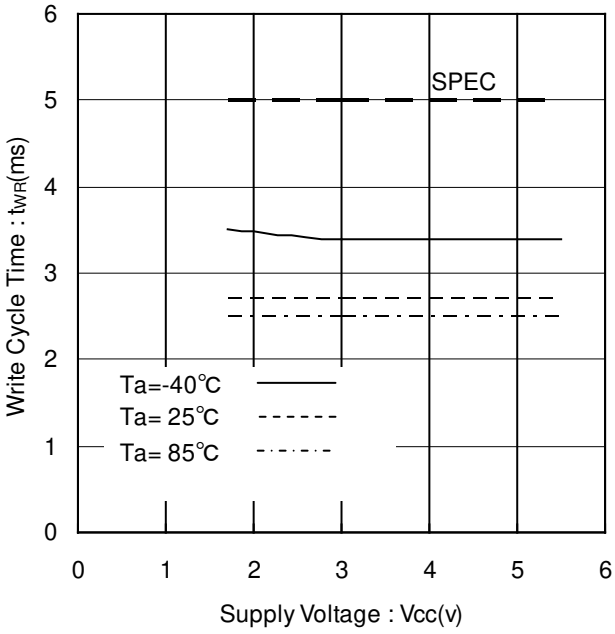


Figure 29. Write Cycle Time vs Supply Voltage

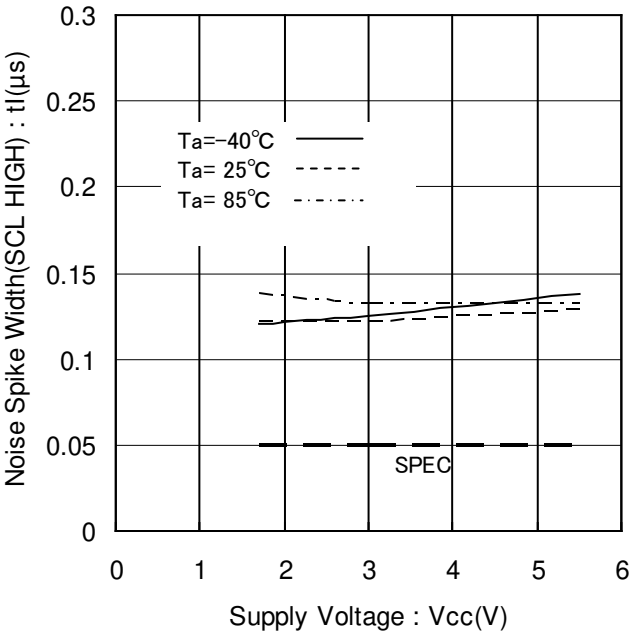


Figure 30. Noise Spike Width vs Supply Voltage (SCL HIGH)

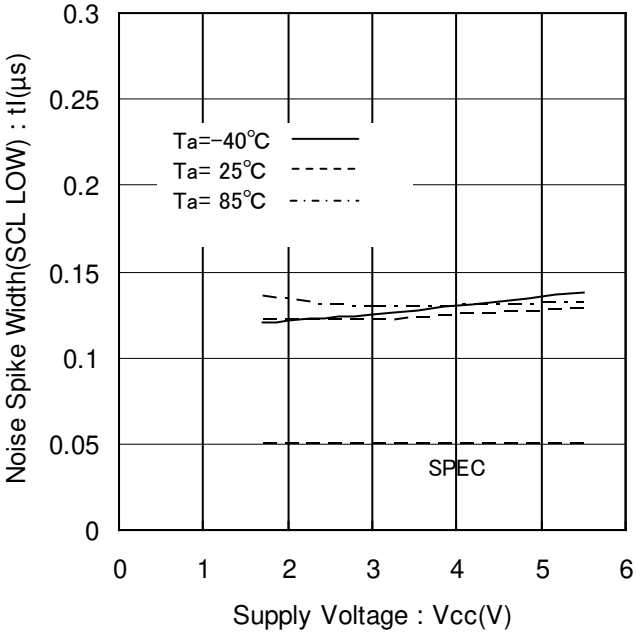


Figure 31. Noise Spike Width vs Supply Voltage (SCL LOW)

Typical Performance Curves - continued

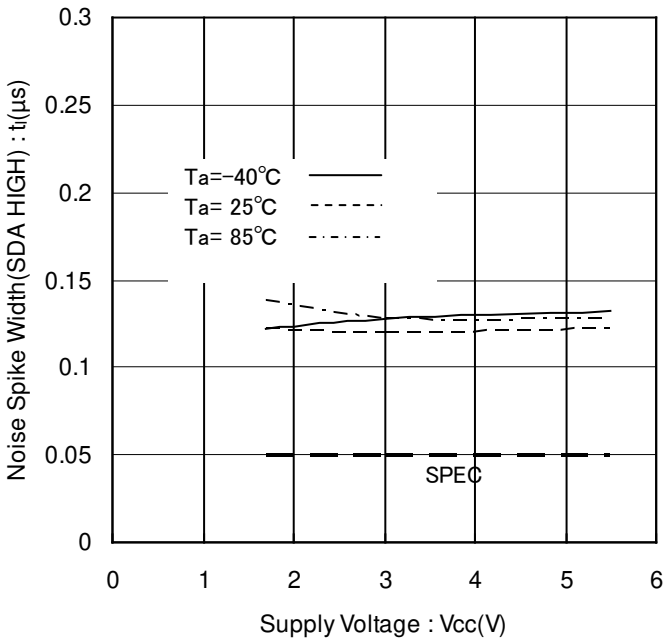


Figure 32. Noise Spike Width vs Supply Voltage (SDA HIGH)

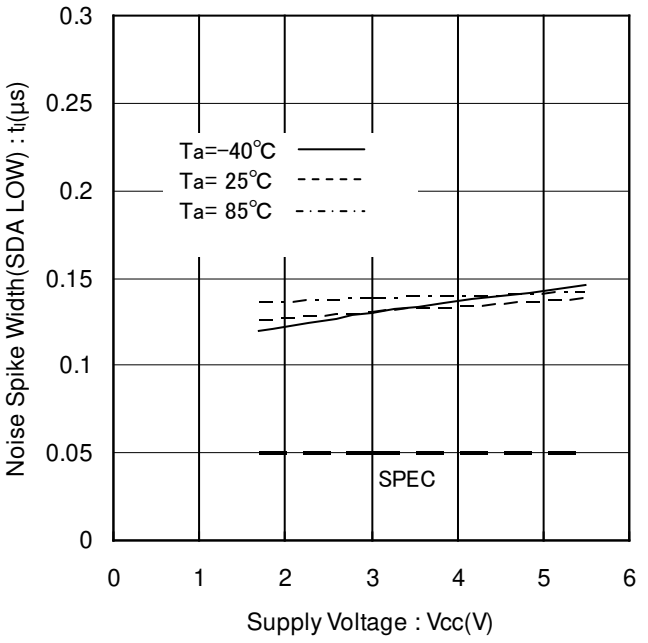


Figure 33. Noise Spike Width vs Supply Voltage (SDA LOW)

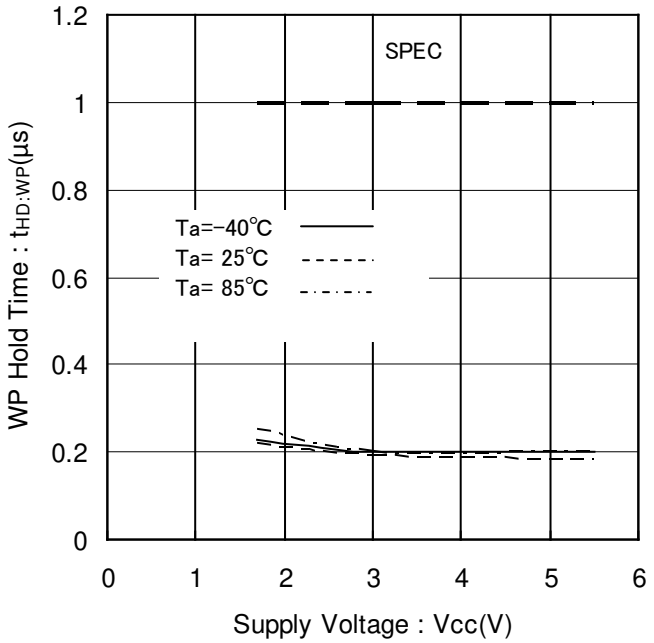


Figure 34. WP Hold Time vs Supply Voltage

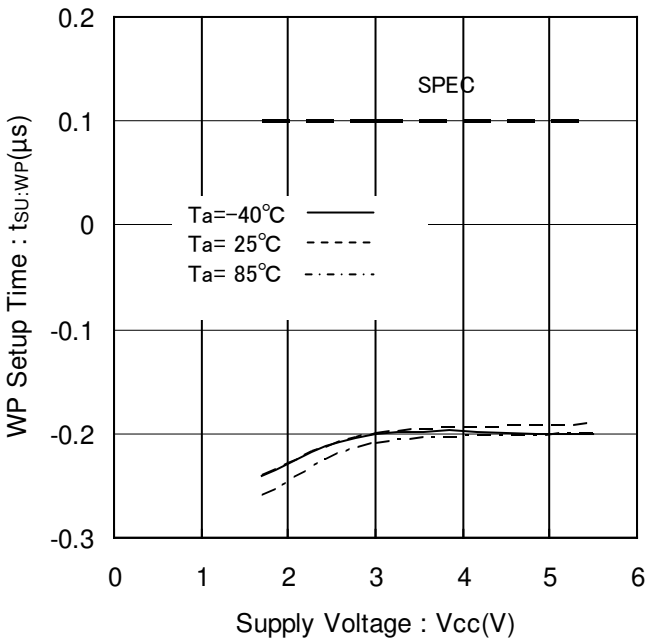


Figure 35. WP Setup Time vs Supply Voltage

Typical Performance Curves - continued

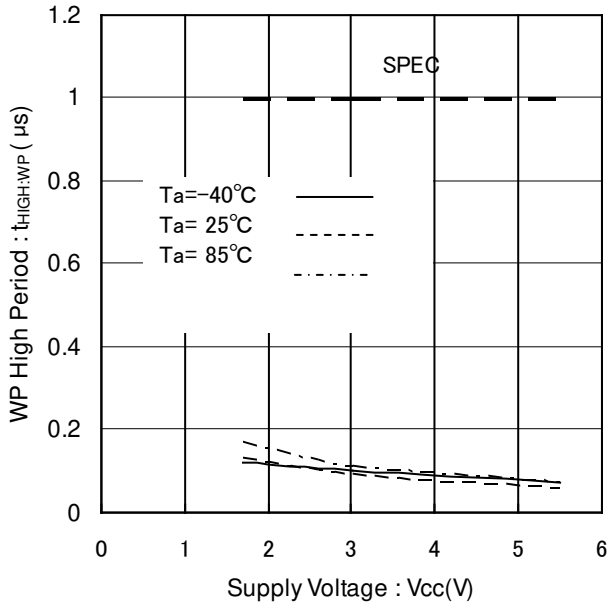


Figure 36. WP High Period vs Supply Voltage

Timing Chart

1. I²C BUS Data Communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS data communication with several devices is possible by connecting with 2 communication lines: serial data (SDA) and serial clock (SCL).
Among the devices, there should be a “master” that generates clock and control communication start and end. The rest become “slave” which are controlled by an address peculiar to each device, like this EEPROM. The device that outputs data to the bus during data communication is called “transmitter”, and the device that receives data is called “receiver”..

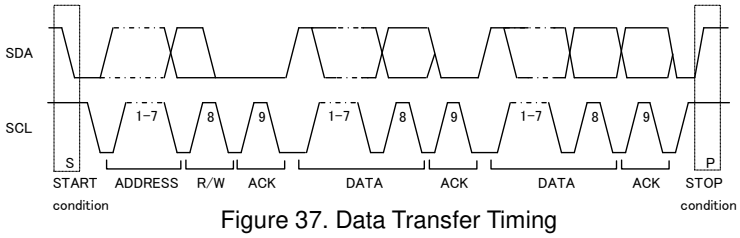


Figure 37. Data Transfer Timing

2. Start Condition (Start Bit Recognition)

(1) Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
(2) This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command cannot be executed.

3. Stop Condition (Stop Bit Recognition)

(1) Each command can be ended by a stop condition (stop bit) where SDA goes from 'LOW' to 'HIGH' while SCL is 'HIGH'.

4. Acknowledge (ACK) Signal

(1) This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master-slave communication, the device (Ex. µ-COM sends slave address input for write or read command to this IC) at the transmitter (sending) side releases the bus after output of 8bit data.
(2) The device (Ex. This IC receives the slave address input for write or read command from the µ-COM) at the receiver (receiving) side sets SDA 'LOW' during 9th clock cycle, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
(3) This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
(4) After receiving 8bit data (word address and write data) during each write operation, this IC outputs acknowledge signal (ACK signal) 'LOW'.
(5) During read operation, this IC outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'. When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (µ-COM) side, this IC continues to output data. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop condition (stop bit), and ends read operation. Then this IC becomes ready for another transmission.

5. Device Addressing

(1) Slave address comes after start condition from master.
(2) The significant 4 bits of slave address are used for recognizing a device type.
The device code of this IC is fixed to '1010'.
(3) Next slave addresses (A2 A1 A0 --- device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses.
(4) The most insignificant bit (R/$\overline{W}$ --- READ/$\overline{WRITE}$) of slave address is used for designating write or read action, and is as shown below.

Setting R / $\overline{w}$ to 0 ------- write (setting 0 to word address setting of random read)
Setting R / $\overline{w}$ to 1 ------- read

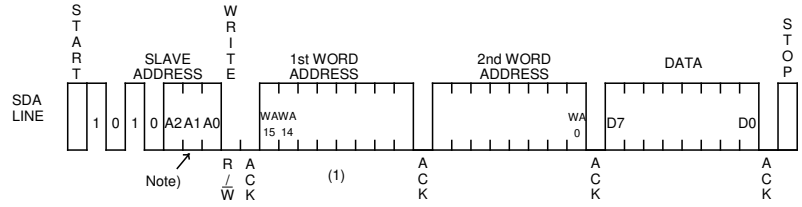
Type	Slave address	Maximum number of Connected buses
BR24G128-3A, BR24G256-3A,	1 0 1 0 A2 A1 A0 R/$\overline{W}$	8
BR24G1M-3A	1 0 1 0 A2 A1 P0 R/$\overline{W}$	4

P0 is page select bit.

Write Command

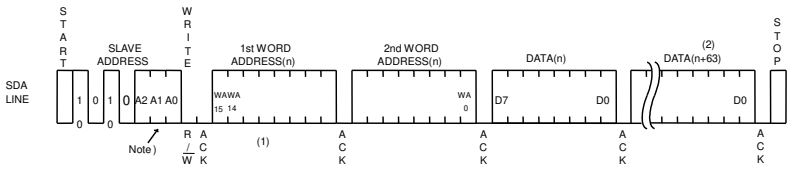
1. Write Cycle

(1) Arbitrary data can be written to EEPROM. When writing only 1 byte, Byte Write is normally used, and when writing continuous data of 2 bytes or more, simultaneous write is possible by Page Write cycle. The maximum number of write bytes is specified per device of each capacity.
Up to 256 arbitrary bytes can be written.（In the case of BR24G1M-3A）



(1) As for WA14, BR24G128-3A becomes don't care.
As for WA15, BR24G128/256-3A becomes don't care.

Figure 38. Byte Write Cycle

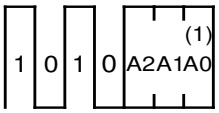


(1) As for WA14, BR24G128-3A becomes don't care.
As for WA15, BR24G128/256-3A becomes don't care.

(2) As for BR24G128/256-3A becomes (n+63)
As for BR24G1M-3A becomes (n+255)

Figure 39. Page Write Cycle

Note)



(1) In BR24G1M-3A A0 becomes P0.

Figure 40. Difference of Slave Address of Each Type

(2) During internal write execution, all input commands are ignored, therefore ACK is not returned.
(3) Data is written to the address designated by word address (n-th address)
(4) By issuing stop bit after 8bit data input, internal write to memory cell starts.
(5) When internal write is started, command is not accepted for t_{WR} (5ms at maximum).
(6) Using page write cycle, writing in bulk is done as follows: Up to 64Byte (BR24G128-3A, BR24G256-3A）
Up to 256Byte (BR24G1M-3A）
The bytes in excess overwrite the data already sent first.
(Refer to "Internal Address Increment")
(7) As for page write cycle of BR24G128-3A and BR24G256-3A, where 2 or more bytes of data is intended to be written, after the 8 significant bits (BR24G128-3A) or 9 significant bits (BR24G256-3A) of word address are designated arbitrarily, only the value of 6 least significant bits in the address is incremented internally, so that data up to 64 bytes of memory only can be written.
(8) As for page write cycle of BR24G1M-3A, where 2 or more bytes of data is intended to be written, after the page select bit ‘P0’ of slave, and the 8 significant bits of word address are designated arbitrarily, only the value of 8 least significant bits in the address is incremented internally, so that data up to 256 bytes of memory only can be written

2. Notes on Write Cycle Continuous Input

List of numbers of page write

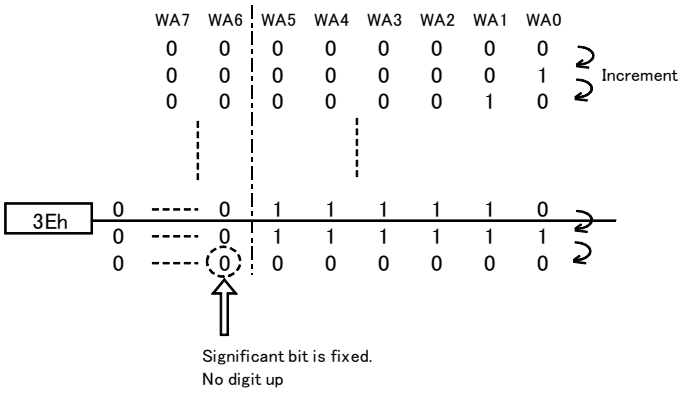
Number of Pages	64Byte	256Byte
Product number	BR24G128-3A BR24G256-3A	BR24G1M-3A

The above numbers are maximum bytes for respective types.
Any bytes below these can be written.

In the case BR24G256-3A, 1 page=64bytes, but the page write cycle time is 5ms at maximum for 64byte bulk write.
It does not stand 5ms at maximum × 64byte=320ms(Max)

3. Internal Address Increment

Page write mode (in the case of BR24G128-3A)



For example, when it is started from address 3Eh,
then, increment is made as below,
3Eh→3Fh→00h→01h･･･ please take note.

※3Eh･･･3E in hexadecimal, therefore, 00111110 becomes a binary number.

4. Write Protect (WP) Terminal

Write protect (WP) function

When WP terminal is set at Vcc (H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not leave it open.

In case of using it as ROM, it is recommended to connect it to pull up or Vcc. At extremely low voltage at power ON/OFF, by setting the WP terminal 'H', write error can be prevented.

Read Command

1. Read Cycle

Read cycle is when data of EEPROM is read. Read cycle could be random read cycle or current read cycle. Random read cycle is a command to read data by designating a specific address, and is used generally. Current read cycle is a command to read data of internal address register without designating an address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available where the next address data can be read in succession.

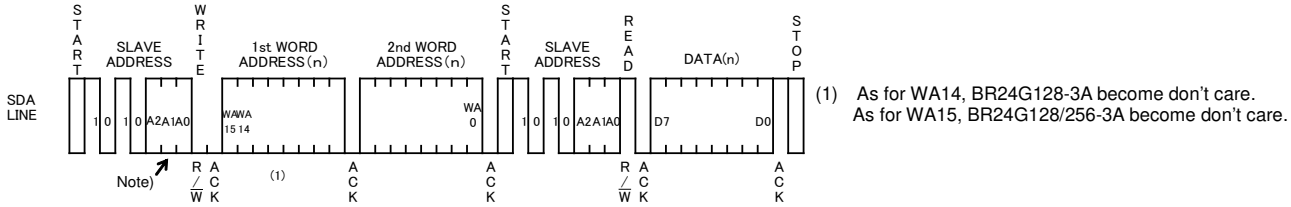


Figure 41. Random Read Cycle

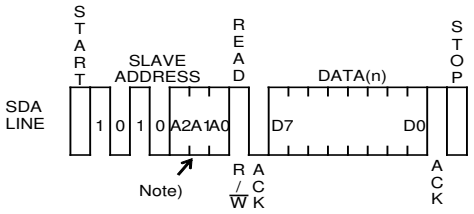


Figure 42. Current Read Cycle

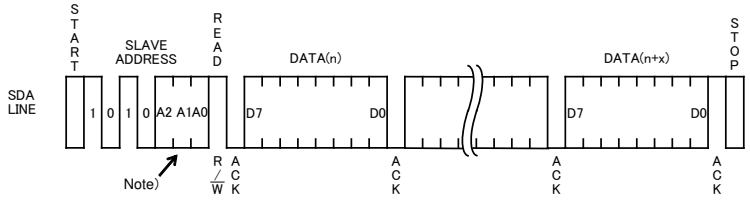
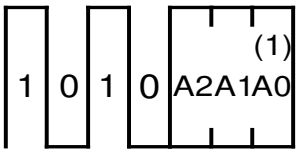


Figure 43. Sequential Read Cycle (in the case of current read cycle)

(1) In random read cycle, data of designated word address can be read.
(2) When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th, i.e., data of the (n+1)-th address is output.
(3) When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (μ-COM) side, the next address data can be read in succession.
(4) Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal goes from 'L' to 'H' while at SCL signal is 'H'.
(5) When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.
Therefore, read command cycle cannot be ended. To end read command cycle, be sure to input 'H' to ACK signal after D0, and the stop condition where SDA goes from 'L' to 'H' while SCL signal is 'H'.
(6) Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is asserted from 'L' to 'H' while SCL signal is 'H'.

Note)



(1) In BR24G1M-3A, A0 becomes P0.

Figure 44. Difference of Slave Address of Each Type

Software Reset

Software reset is executed to avoid malfunction after power ON, and during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Figure 45-(a), Figure 45-(b), Figure 45-(c)) Within the dummy clock input area, the SDA bus is released ('H' by pull up) and ACK output and read data '0' (both 'L' level) may be output from EEPROM. Therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

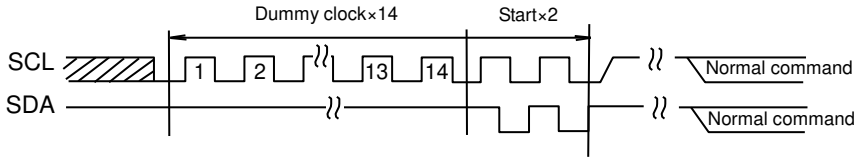


Figure 45-(a). The Case of Dummy Clock × 14 +START+START+ Command Input

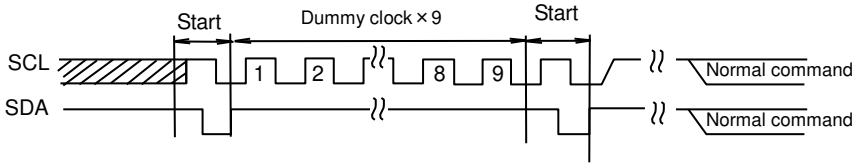


Figure 45-(b). The Case of START + Dummy Clock × 9 +START+ Command Input

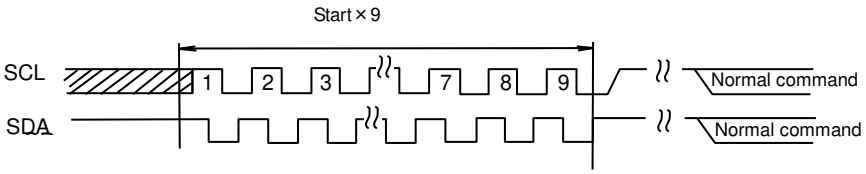


Figure 45-(c). START×9+ Command Input

※Start command from START input.

Acknowledge Polling

During internal write execution, all input commands are ignored, therefore ACK is not returned. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write operation, else 'H' is returned, which means writing is still in progress. By the use of acknowledge polling, next command can be executed without waiting for t_{WR} = 5ms.

To write continuously, R/$\overline{W}$ = 0, then to carry out current read cycle after write, slave address with R/$\overline{W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

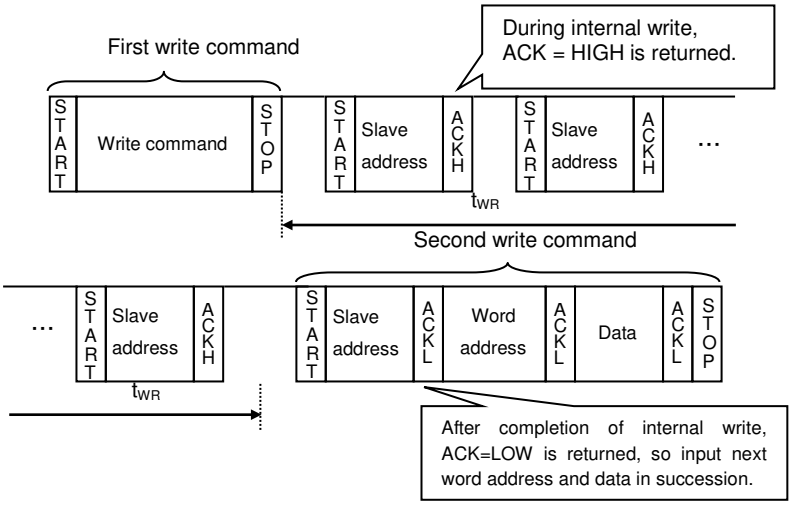


Figure 46. Case to Continuous Write by Acknowledge Polling

WP Valid Timing (Write Cancel)

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so on, pay attention to the following WP valid timing. During write cycle execution, inside cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to take in D0 of data(in page write cycle, the first byte data) is the cancel invalid area.
WP input in this area becomes 'Don't care'. The area from the rise of SCL to take in D0 to the stop condition input is the cancel valid area. Furthermore, after the execution of forced end by WP, the IC enters standby status..

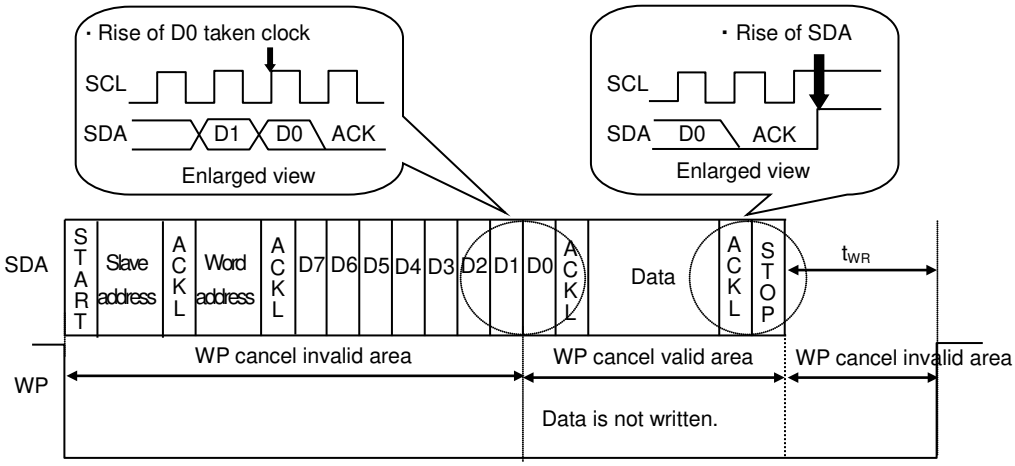


Figure 47. WP Valid Timing

Command Cancel by Start Condition and Stop Condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Figure 48.) However, within ACK output area and during data read, SDA bus may output 'L'. In this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. When command is cancelled by start-stop condition during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined. Therefore, it is not possible to carry out current read cycle in succession. To carry out read cycle in succession, carry out random read cycle.

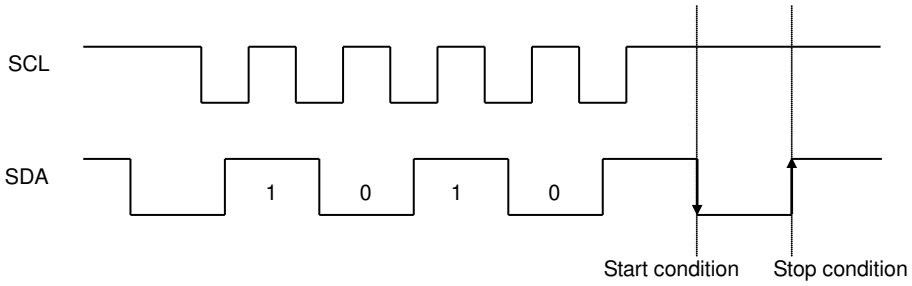


Figure 48. Case of Cancel by Start, Stop Condition during Slave Address Input

I/O Peripheral Circuit

1. Pull Up Resistance of SDA Terminal

SDA is NMOS open drain, so it requires a pull up resistor. As for this resistor value (R_{PU}), select an appropriate value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, operating frequency is limited. The smaller the R_{PU}, the larger is the supply current (Read).

2. Maximum Value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

(1)SDA rise time to be determined by the capacitance (C_{BUS}) of bus line of R_{PU} and SDA should be t_R or lower.
Furthermore, AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by input leak total (I_L) of device connected to bus at output of 'H' to SDA bus and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin of $0.2V_{CC}$.

$$V_{CC}-I_L R_{PU}-0.2\,V_{CC} \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leqq \frac{0.8V_{CC}-V_{IH}}{I_L}$$

Ex.) V_{CC} =3V I_L=10μA V_{IH}=0.7 V_{CC}

From (2)

$$R_{PU} \leqq \frac{0.8\times3-0.7\times3}{10\times10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

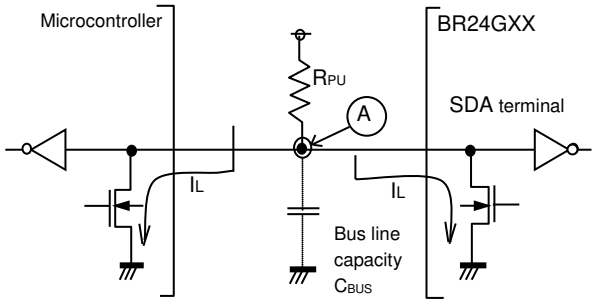


Figure 49. I/O Circuit Diagram

3. Minimum Value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

(1) When IC outputs LOW, it should be satisfied that V_{OLMAX}=0.4V and I_{OLMAX}=3mA.

$$\frac{V_{CC}-V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{V_{CC}-V_{OL}}{I_{OL}}$$

(2) V_{OLMAX}=0.4V should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including recommended noise margin $0.1V_{CC}$.

$$V_{OLMAX} \leqq V_{IL}-0.1\,V_{CC}$$

Ex.) V_{CC} =3V, V_{OL}=0.4V, I_{OL}=3mA, microcontroller, EEPROM $V_{IL}=0.3V_{CC}$

from (1) $$R_{PU} \geqq \frac{3-0.4}{3\times10^{-3}}$$

$$\geqq 867\ [\Omega]$$

And V_{OL}=0.4 [V]

$V_{IL}=0.3\times3$

=0.9 [V]

Therefore, the condition (2) is satisfied.

4. Pull Up Resistance of SCL Terminal

When SCL control is made at the CMOS output port, there is no need for a pull up resistor. But when there is a time where SCL becomes 'Hi-Z', add a pull up resistor. As for the pull up resistor value, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

Cautions on Microcontroller Connection

1. R_S

In I²C BUS, it is recommended that SDA port is of open drain input/output. However, when using CMOS input / output of tri state to SDA port, insert a series resistance R_S between the pull up resistor R_{PU} and the SDA terminal of EEPROM. This is to control over current that may occur when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. R_S also plays the role of protecting the SDA terminal against surge. Therefore, even when SDA port is open drain input/output, R_S can be used.

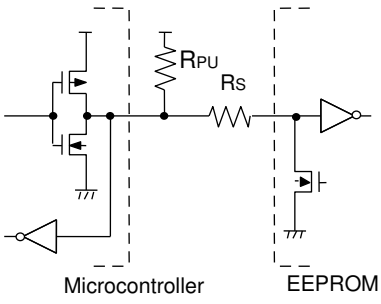


Figure 50. I/O Circuit Diagram

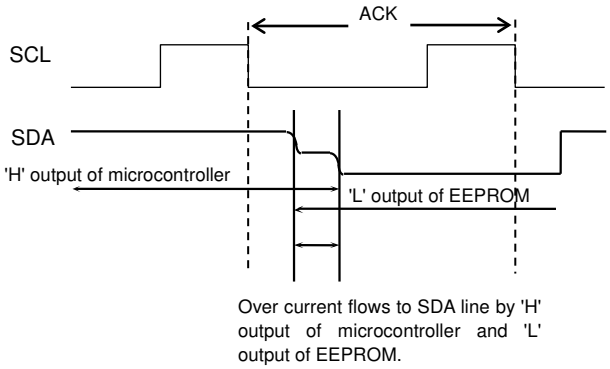


Figure 51. Input / Output Collision Timing

2. Maximum Value of R_S

The maximum value of R_S is determined by the following relations.

(1) SDA rise time to be determined by the capacitance (C_{BUS}) of bus line and R_{PU} of SDA should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.

(2) The bus electric potential Ⓐ to be determined by R_{PU} and R_S the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin of $0.1V_{CC}$.

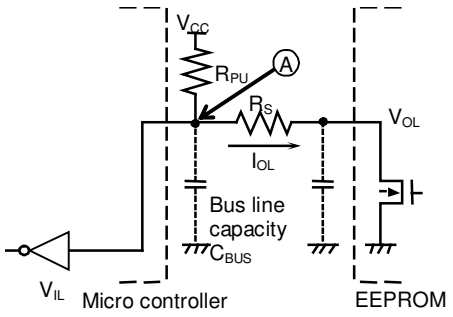


Figure 52. I/O Circuit Diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Ex.) V_{CC}=3V V_{IL}=0.3V_{CC} V_{OL}=0.4V R_{PU}=20kΩ

$$R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67\ [k\Omega]$$

3. Minimum Value of R_S

The minimum value of R_S is determined by over current at bus collision. When over current flows, noises in power source line and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of the impedance of power source line in set and so forth. Set the over current to EEPROM to 10mA or lower.

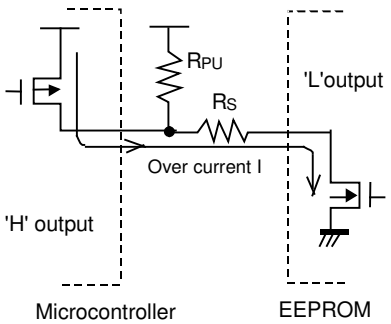


Figure 53. I/O Circuit Diagram

$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{V_{CC}}{I}$$

Ex.) Vcc=3V, I=10mA

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300\ [\Omega]$$

I/O Equivalence Circuit

1. Input (A0, A1, A2, SCL, WP)

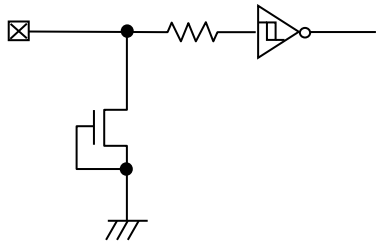


Figure 54. Input Pin Circuit Diagram

2. Input / Output (SDA)

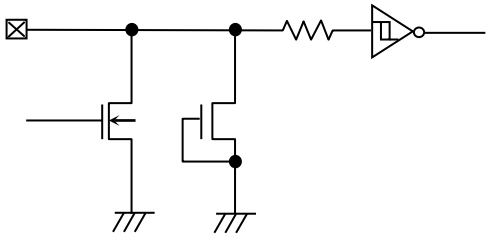


Figure 55. Input / Output Pin Circuit Diagram

Power-Up/Down Conditions

At power on, the IC's internal circuits may go through unstable low voltage area as the Vcc rises, making the IC's internal logic circuit not completely reset, hence, malfunction may occur. To prevent this, the IC is equipped with POR circuit and LVCC circuit. To assure the operation, observe the following conditions at power ON.

1. Set SDA = 'H' and SCL ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of t_R, t_{OFF}, and V_{bot} for operating POR circuit.

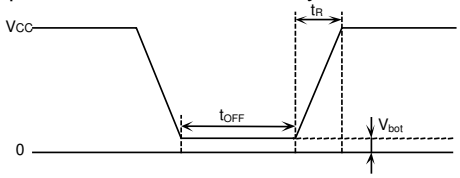


Figure 56. Rise Waveform Diagram

Recommended conditions of t_R, t_{OFF}, V_{bot}

t_R	t_{OFF}	V_{bot}
10ms or below	10ms or larger	0.3V or below
100ms or below	10ms or larger	0.2V or below

3. Set SDA and SCL so as not to become 'Hi-Z'.
   When the above conditions 1 and 2 cannot be observed, take the following countermeasures.
   (1) In the case when the above condition 1 cannot be observed such that SDA becomes 'L' at power ON.
   →Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

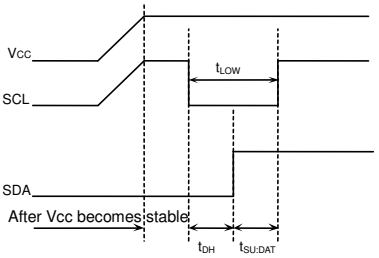


Figure 57. When SCL= 'H' and SDA= 'L'

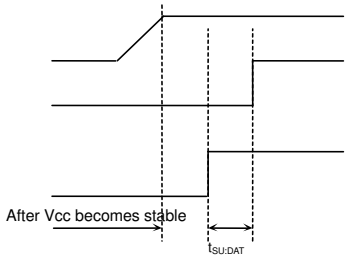


Figure 58. When SCL='L' and SDA='L'

   (2) In the case when the above condition 2 cannot be observed.
   →After power source becomes stable, execute software reset(Page19).
   (3) In the case when the above conditions 1 and 2 cannot be observed.
   →Carry out (1), and then carry out (2).

Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite operation at low power, and prevents write error. At LVCC voltage (Typ =1.2V) or below, data rewrite is prevented.

Noise Countermeasures

1. Bypass Capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, it is recommended to connect a bypass capacitor (0.1μF) between the IC's V_{CC} and GND pins. Connect the capacitor as close to IC as possible. In addition, it is also recommended to connect a bypass capacitor between board's V_{CC} and GND.

Operational Notes

1. Described numeric values and data are design representative values only, and the values are not guaranteed.

2. We believe that the application circuit examples in this document are recommendable. However, in actual use, confirm characteristics further sufficiently. If changing the fixed number of external parts is desired, make your decision with sufficient margin in consideration of static characteristics, transient characteristics, and fluctuations of external parts and our LSI.

3. Absolute maximum ratings
   If the absolute maximum ratings such as supply voltage, operating temperature range, and so on are exceeded, LSI may be destroyed. Do not supply voltage or subject the IC to temperatures exceeding the absolute maximum ratings. In case of fear of exceeding the absolute maximum ratings, take physical safety countermeasures such as adding fuses, and see to it that conditions exceeding the absolute maximum ratings should not be supplied to the LSI.

4. GND electric potential
   Set the voltage of GND terminal lowest at any operating condition. Make sure that each terminal voltage is not lower than that of GND terminal.

5. Thermal design
   Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.

6. Short between pins and mounting errors
   Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

7. Operating the IC in the presence of strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.