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ROHM SEMICONDUCTOR

Serial EEPROM Series Standard EEPROM

I²C BUS EEPROM (2-Wire)

BR24G32-3A

General Description

BR24G32−3A is a 32Kbit serial EEPROM of I²C BUS Interface Method

Features

- All controls available by 2 ports of serial clock(SCL) and serial data(SDA)
- Other devices than EEPROM can be connected to the same port, saving microcontroller port
- 1.6V to 5.5V Single Power Source Operation most suitable for battery use
- 1MHz action is possible(1.7V to 5.5V)
- Up to 32 Byte in Page Write Mode
- Bit format 4K x 8bit
- Self-timed Programming Cycle
- Low Current Consumption
- Prevention of Write Mistake
  - ➤ WP (Write Protect) Function added
  - ➤ Prevention of Write Mistake At Low Voltage
- More than 1 million write cycles
- More than 40 years data retention
- Noise filter built in SCL / SDA terminal
- Initial delivery state FFh
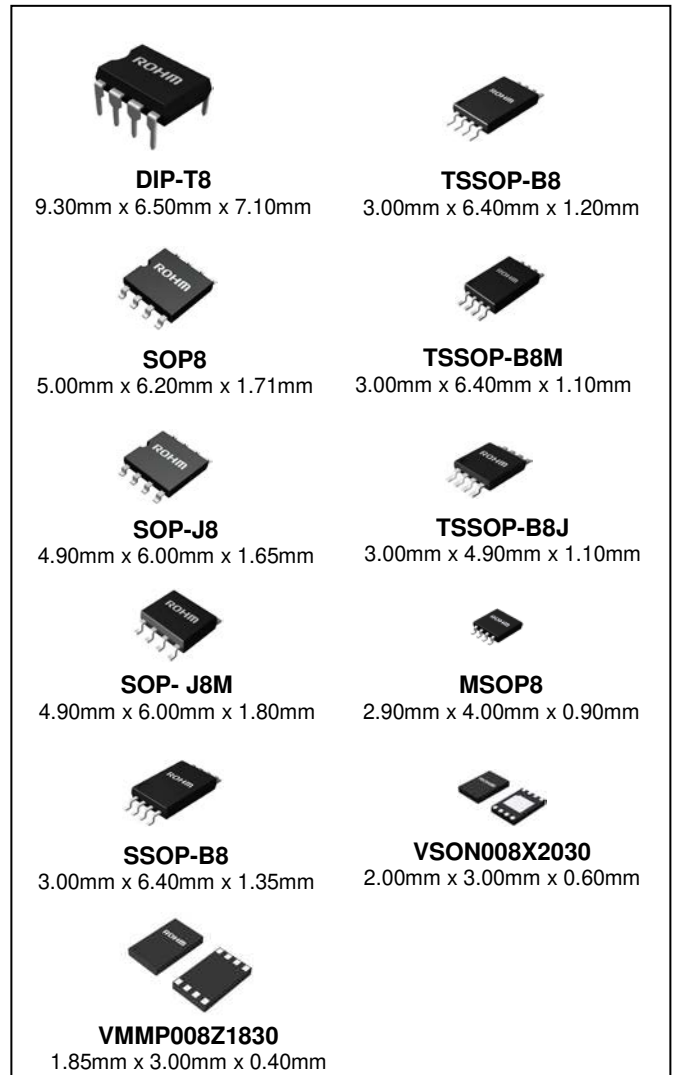
Packages W(Typ) x D(Typ) x H(Max)

DIP-T8
9.30mm x 6.50mm x 7.10mm

TSSOP-B8
3.00mm x 6.40mm x 1.20mm

SOP8
5.00mm x 6.20mm x 1.71mm

TSSOP-B8M
3.00mm x 6.40mm x 1.10mm

SOP-J8
4.90mm x 6.00mm x 1.65mm

TSSOP-B8J
3.00mm x 4.90mm x 1.10mm

SOP- J8M
4.90mm x 6.00mm x 1.80mm

MSOP8
2.90mm x 4.00mm x 0.90mm

SSOP-B8
3.00mm x 6.40mm x 1.35mm

VSON008X2030
2.00mm x 3.00mm x 0.60mm

VMMP008Z1830
1.85mm x 3.00mm x 0.40mm

Figure 1.

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	V_{CC}	-0.3 to +6.5	V	
Permissible Dissipation	Pd	0.45 (SOP8)	W	Derate by 4.5mW/°C when operating above Ta=25°C
		0.45 (SOP-J8M)		Derate by 4.5mW/°C when operating above Ta=25°C
		0.45 (SOP-J8)		Derate by 4.5mW/°C when operating above Ta=25°C
		0.30 (SSOP-B8)		Derate by 3.0mW/°C when operating above Ta=25°C
		0.33 (TSSOP-B8)		Derate by 3.3mW/°C when operating above Ta=25°C
		0.33 (TSSOP-B8M)		Derate by 3.3mW/°C when operating above Ta=25°C
		0.31 (TSSOP-B8J)		Derate by 3.1mW/°C when operating above Ta=25°C
		0.31 (MSOP8)		Derate by 3.1mW/°C when operating above Ta=25°C
		0.30 (VSON008X2030)		Derate by 3.0mW/°C when operating above Ta=25°C
		0.80 (DIP-T8)		Derate by 8.0mW/°C when operating above Ta=25°C
		0.21 (VMMP008Z1830)		Derate by 2.1mW/°C when operating above Ta=25°C
Storage Temperature	Tstg	-65 to +150	°C	
Operating Temperature	Topr	-40 to +85	°C	
Input Voltage / Output Voltage	-	-0.3 to V_{CC}+1.0	V	The Max value of Input Voltage/Output Voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of Input Voltage/Output Voltage is not lower than -1.0V.
Junction Temperature	Tjmax	150	°C	Junction temperature at the storage condition
Electrostatic discharge voltage (human body model)	V_{ESD}	-4000 to +4000	V	

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Memory Cell Characteristics (Ta=25°C, V_{CC}=1.6V to 5.5V)

Parameter	Limit			Unit
	Min	Typ	Max	
Write Cycles [Note1]	1,000,000	-	-	Times
Data Retention [Note1]	40	-	-	Years

(Note1) Not 100% TESTED

Recommended Operating Ratings

Parameter	Symbol	Rating	Unit
Power Source Voltage	V_{CC}	1.6 to 5.5	V
Input Voltage	V_{IN}	0 to V_{CC}	

DC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, V_{CC} =1.6V to 5.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input High Voltage 1	V_{IH1}	$0.7V_{CC}$	-	V_{CC}+1.0	V	$1.7V \leq V_{CC} \leq 5.5V$
Input Low Voltage 1	V_{IL1}	-0.3 [Note1]	-	$+0.3V_{CC}$	V	$1.7V \leq V_{CC} \leq 5.5V$
Input High Voltage 2	V_{IH2}	$0.8V_{CC}$	-	V_{CC}+1.0	V	$1.6V \leq V_{CC} < 1.7V$
Input Low Voltage 2	V_{IL2}	-0.3 [Note1]	-	$+0.2V_{CC}$	V	$1.6V \leq V_{CC} < 1.7V$
Output Low Voltage 1	V_{OL1}	-	-	0.4	V	I_{OL}=3.0mA, $2.5V \leq V_{CC} \leq 5.5V$ (SDA)
Output Low Voltage 2	V_{OL2}	-	-	0.2	V	I_{OL}=0.7mA, $1.6V \leq V_{CC} < 2.5V$ (SDA)
Input Leakage Current	I_{LI}	-1	-	+1	µA	V_{IN}=0 to V_{CC}
Output Leakage Current	I_{LO}	-1	-	+1	µA	V_{OUT}=0 to V_{CC} (SDA)
Supply Current (Write)	I_{CC1}	-	-	2.0	mA	V_{CC}=5.5V, f_{SCL}=1MHz, t_{WR}=5ms, Byte write, Page write
Supply Current (Read)	I_{CC2}	-	-	2.0		V_{CC}=5.5V, f_{SCL}=1MHz Random read, current read, sequential read
Standby Current	I_{SB}	-	-	2.0	µA	V_{CC}=5.5V, SDA, SCL=V_{CC} A0, A1, A2=GND, WP=GND

(Note1) When the pulse width is 50ns or less, it is -1.0V.

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AC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C)

Parameter	Symbol	Limits (1.6V≤V$_{CC}$≤5.5V)			Limits (1.7V≤V$_{CC}$≤5.5V)			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Frequency	f$_{SCL}$	-	-	400	-	-	1000	kHz
Data Clock High Period	t$_{HIGH}$	0.6	-	-	0.30	-	-	µs
Data Clock Low Period	t$_{LOW}$	1.2	-	-	0.5	-	-	µs
SDA, SCL (INPUT) Rise Time (Note1)	t$_R$	-	-	1	-	-	0.12	µs
SDA, SCL (INPUT) Fall Time (Note1)	t$_{F1}$	-	-	1	-	-	0.12	µs
SDA (OUTPUT) Fall Time (Note1)	t$_{F2}$	-	-	0.3	-	-	0.12	µs
Start Condition Hold Time	t$_{HD:STA}$	0.6	-	-	0.25	-	-	µs
Start Condition Setup Time	t$_{SU:STA}$	0.6	-	-	0.20	-	-	µs
Input Data Hold Time	t$_{HD:DAT}$	0	-	-	0	-	-	ns
Input Data Setup Time	t$_{SU:DAT}$	100	-	-	50	-	-	ns
Output Data Delay Time	t$_{PD}$	0.1 (Note2)	-	0.9	0.05	-	0.45	µs
		0.05 (Note3)	-	0.9				
Output Data Hold Time	t$_{DH}$	0.1 (Note2)	-	-	0.05	-	-	µs
		0.05 (Note3)	-	-				
Stop Condition Setup Time	t$_{SU:STO}$	0.6	-	-	0.25	-	-	µs
Bus Free Time	t$_{BUF}$	1.2	-	-	0.5	-	-	µs
Write Cycle Time	t$_{WR}$	-	-	5	-	-	5	ms
Noise Spike Width (SDA, SCL)	t$_I$	-	-	0.05	-	-	0.05	µs
WP Hold Time	t$_{HD:WP}$	1.0	-	-	1.0	-	-	µs
WP Setup Time	t$_{SU:WP}$	0.1	-	-	0.1	-	-	µs
WP High Period	t$_{HIGH:WP}$	1.0	-	-	1.0	-	-	µs

(Note1) Not 100% tested
(Note2) At 1.6V≤V$_{CC}$<1.7V
(Note3) At 1.7V≤V$_{CC}$≤5.5V

AC Characteristics Condition

Parameter	Symbol	Conditions	Unit
Load Capacitance	C$_L$	100	pF
SDA, SCL (INPUT) Rise Time	t$_R$	20	ns
SDA, SCL (INPUT) Fall Time	t$_{F1}$	20	ns
Input Data Level	V$_{IL}$/V$_{IH}$	0.2V$_{CC}$/0.8V$_{CC}$	V
Input/Output Data Timing Reference Level	-	0.3V$_{CC}$/0.7V$_{CC}$	V

Serial Input / Output Timing
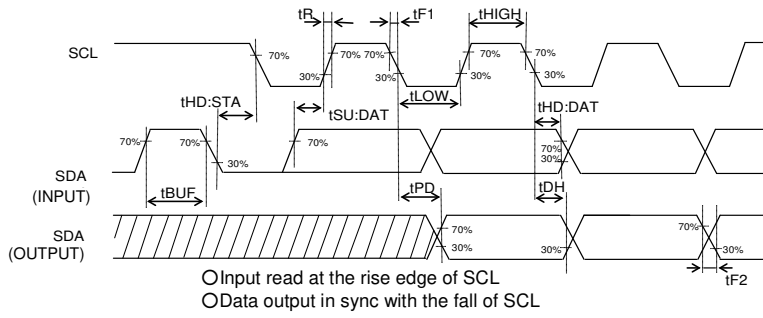
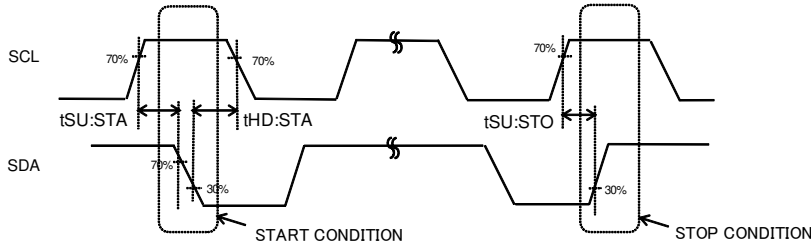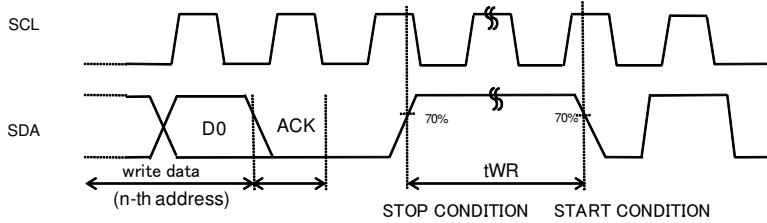Figure 2-(a). Serial Input / Output Timing

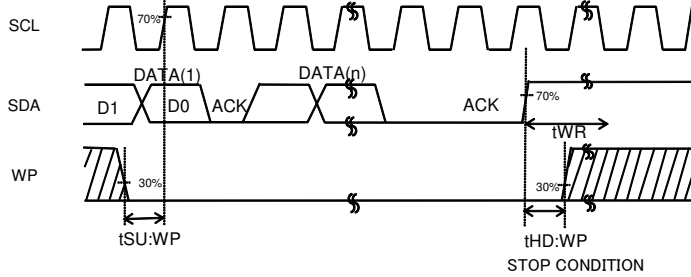Figure 2-(b). Start-Stop Bit Timing

Figure 2-(c). Write Cycle Timing

Figure 2-(d). WP Timing at Write Execution

Figure 2-(e). WP Timing at Write Cancel
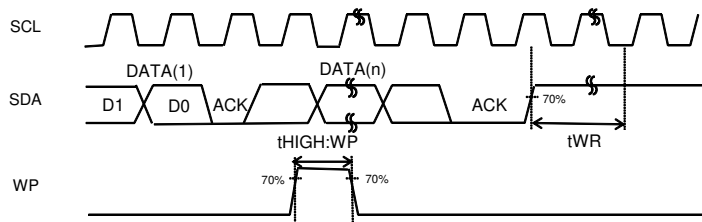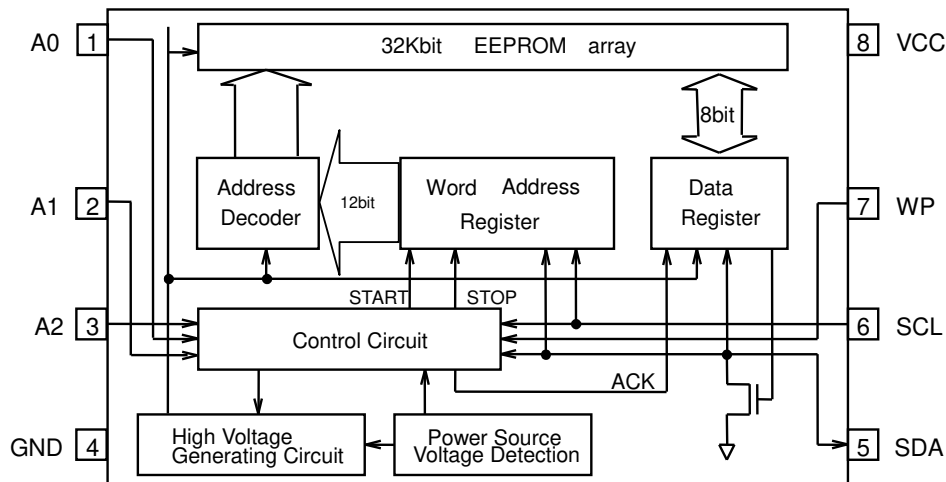
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Block Diagram

Figure 3. Block Diagram

Pin Configuration

(TOP VIEW)
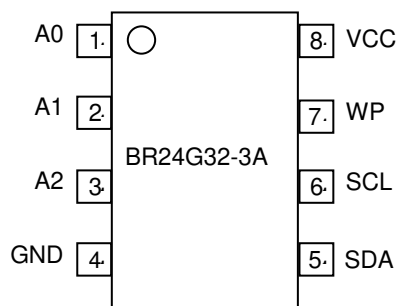
Pin Descriptions

Terminal Name	Input/ Output	Descriptions
A0	Input	Slave address setting[Note1]
A1	Input	Slave address setting[Note1]
A2	Input	Slave address setting[Note1]
GND	-	Reference voltage of all input / output, 0V
SDA	Input/ output	Serial data input serial data output
SCL	Input	Serial clock input
WP	Input	Write protect terminal
VCC	-	Connect the power source.

(Note1) A0,A1 and A2 are not allowed to use as open.

Typical Performance Curves
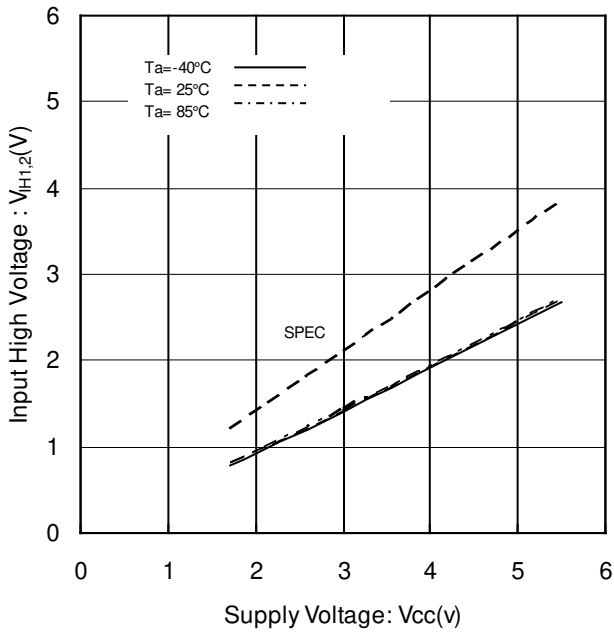
Figure 4. Input High Voltage1,2 vs Supply Voltage
(A0, A1, A2, SCL, SDA, WP)
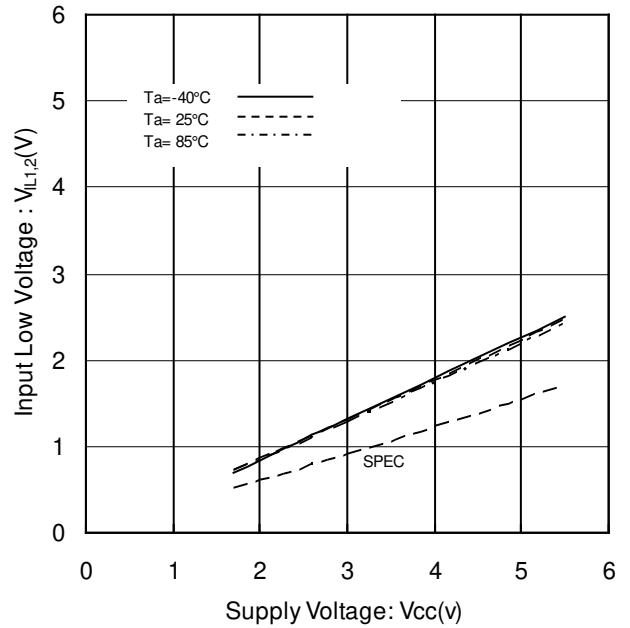
Figure 5. Input Low Voltage1,2 vs Supply Voltage
(A0, A1, A2, SCL, SDA, WP)
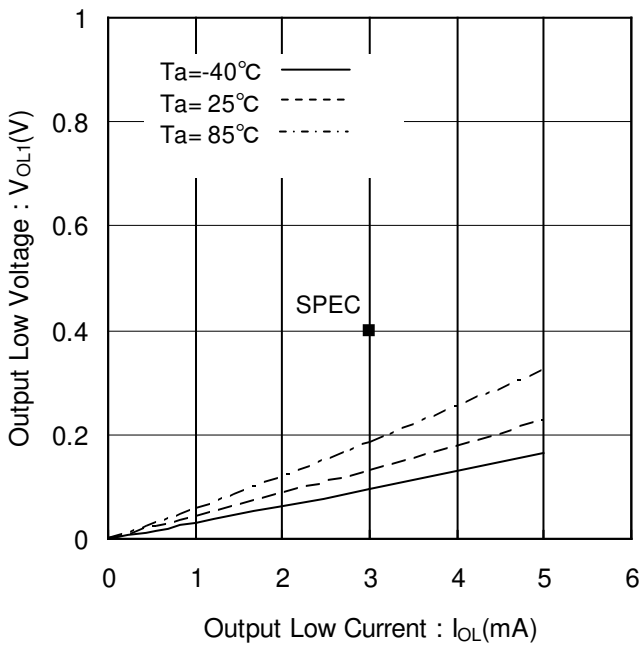
Figure 6. Output Low Voltage1 vs Output Low Current
(Vcc=2.5V)
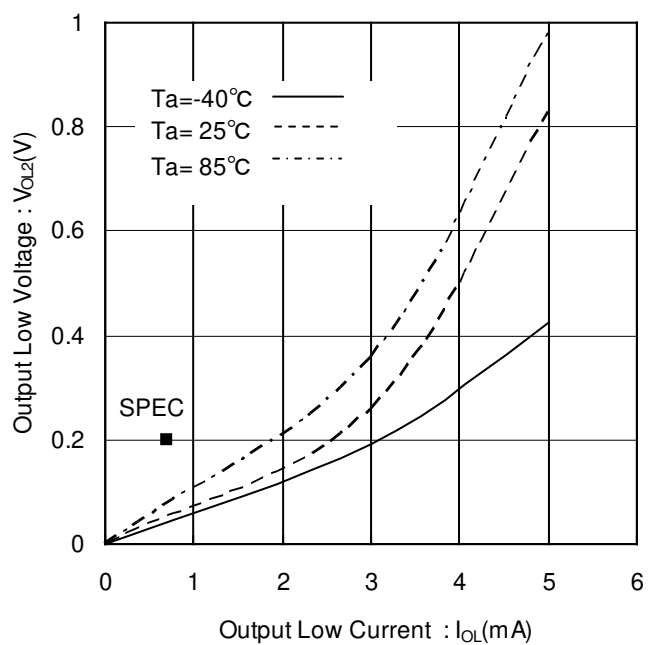
Figure 7. Output Low Voltage2 vs Output Low Current
(Vcc=1.6V)

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Typical Performance Curves - Continued
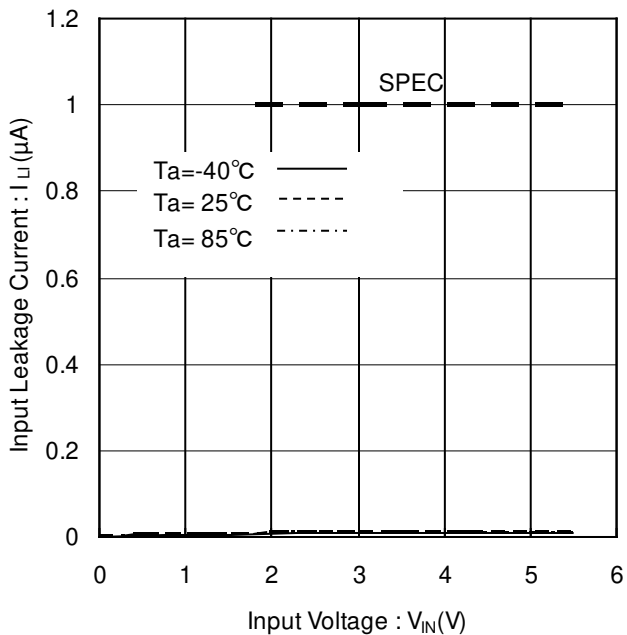
Figure 8. Input Leakage Current vs Supply Voltage
(A0,A1,A2,SCL,WP)
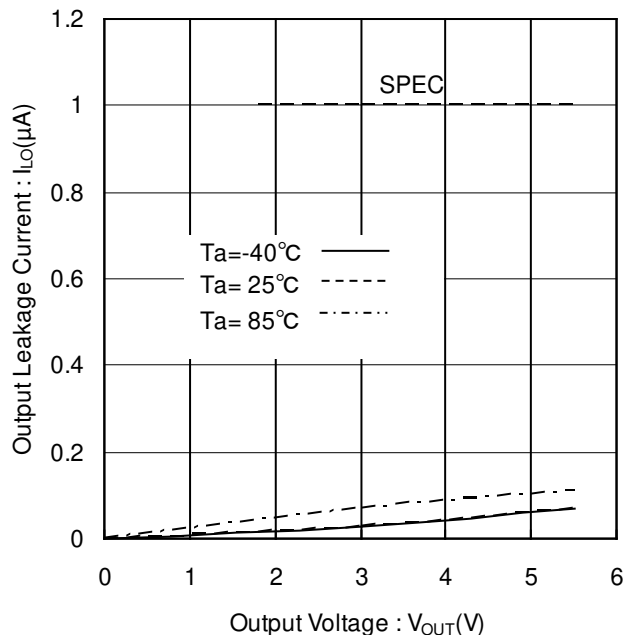
Figure 9. Output Leakage Current vs Supply Voltage
(SDA)
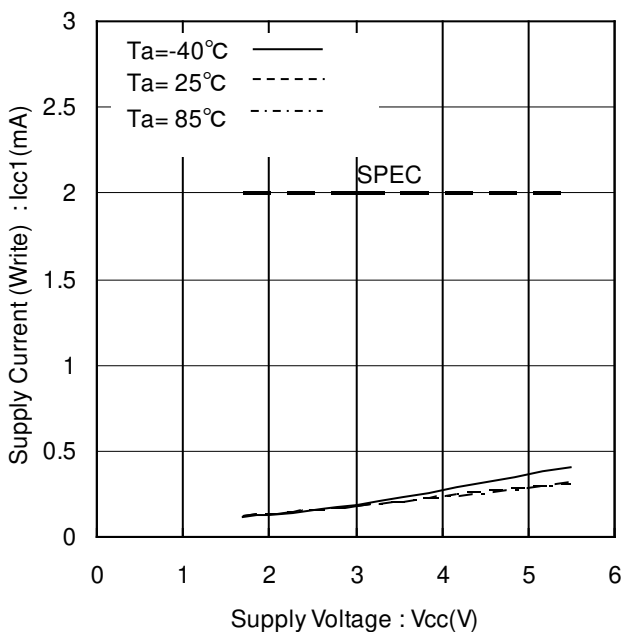
Figure 10. Supply Current (Write) vs Supply Voltage
(f_{SCL}=1MHz)
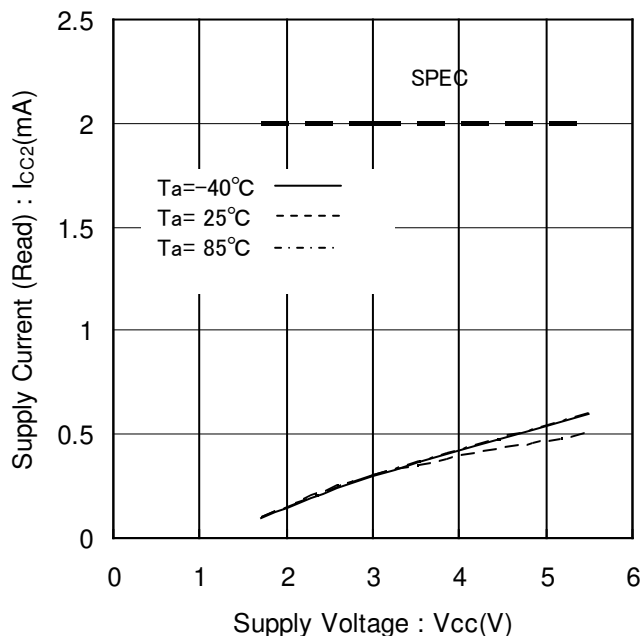
Figure 11. Supply Current (Read) vs Supply Voltage
(f_{SCL}=1MHz)

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Typical Performance Curves - Continued
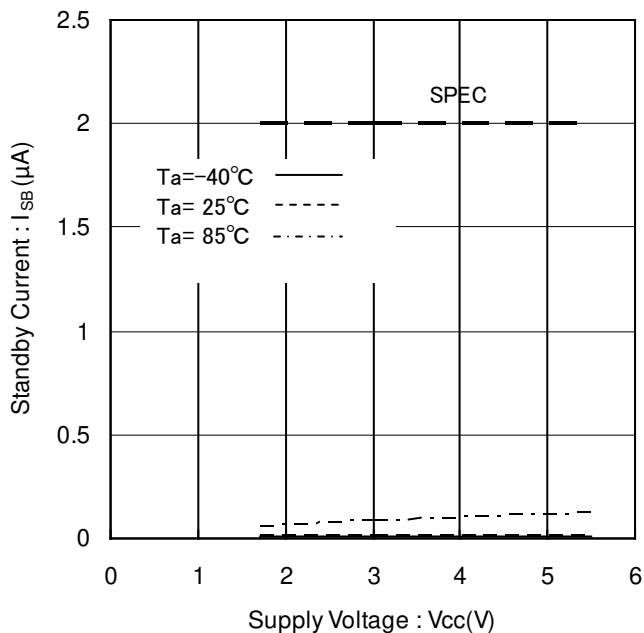
Figure 12. Standby Current vs Supply Voltage
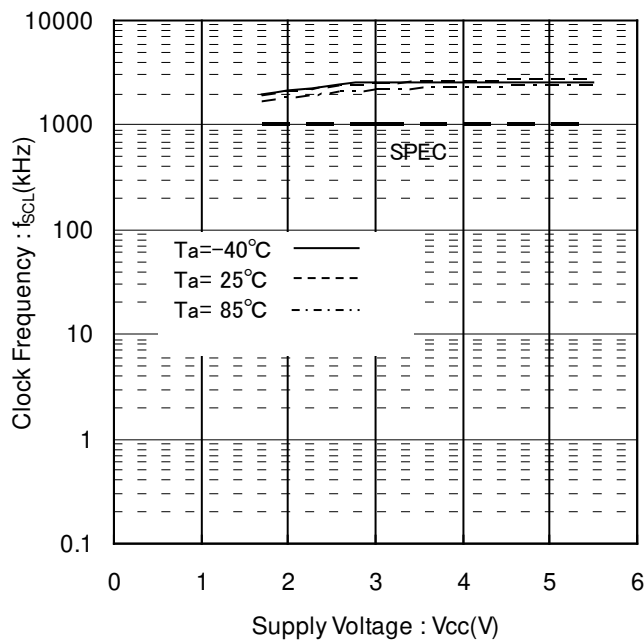
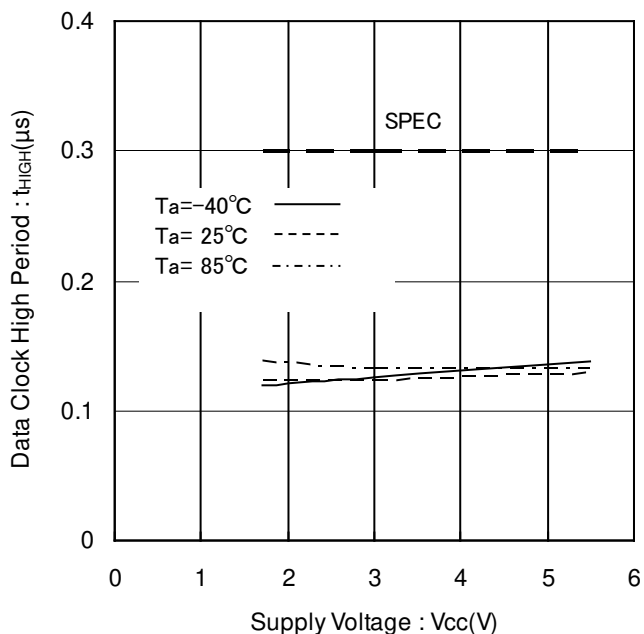Figure 13. Clock Frequency vs Supply Voltage

Figure 14. Data Clock High Period vs Supply Voltage
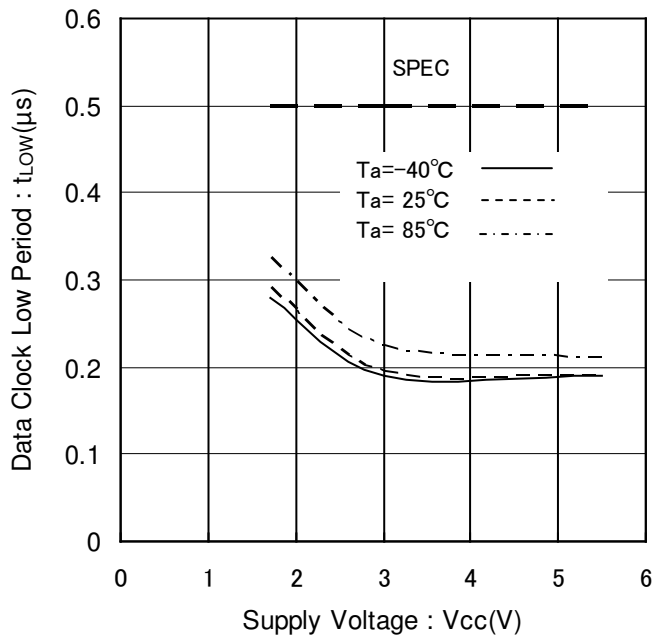

Figure 15. Data Clock Low Period vs Supply Voltage

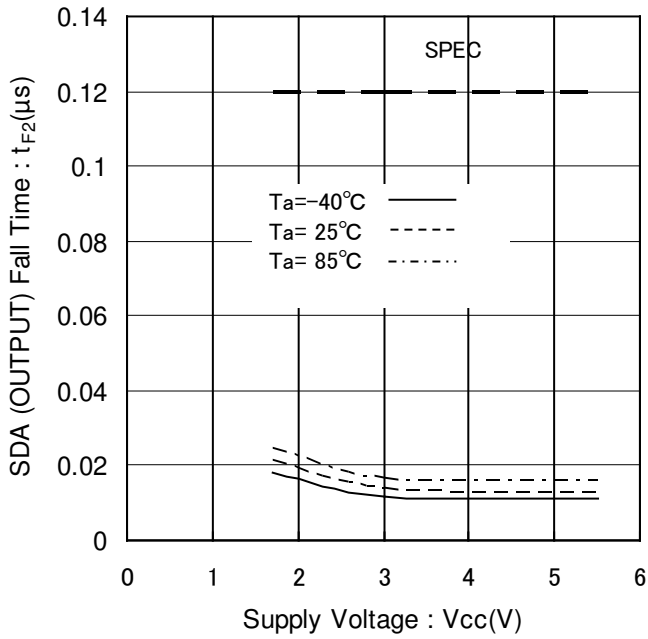**Typical Performance Curves - Continued**

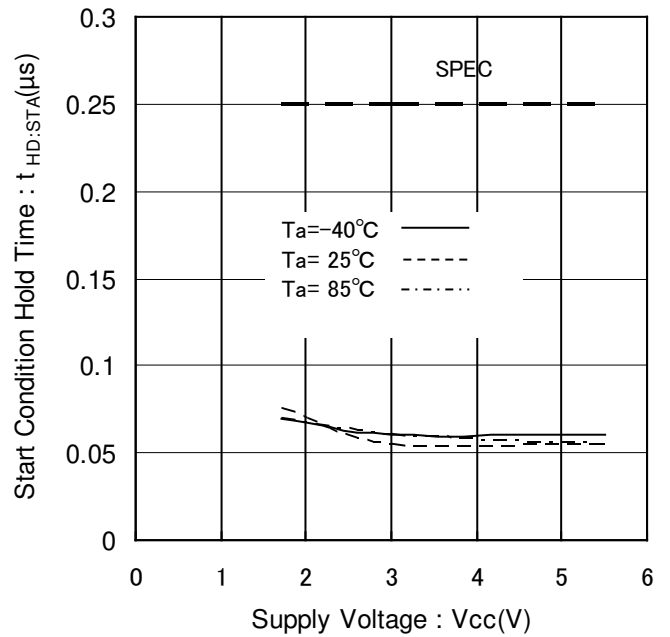Figure 16. SDA (OUTPUT) Fall Time vs Supply Voltage

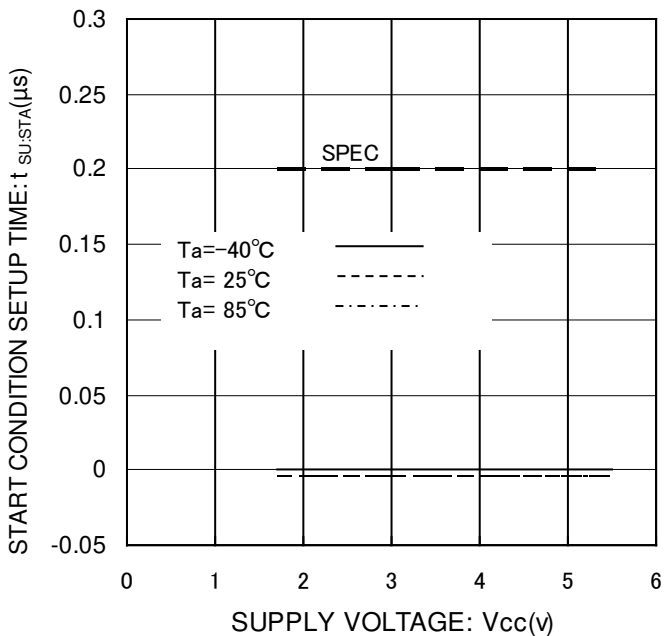Figure 17. Start Condition Hold Time vs Supply Voltage

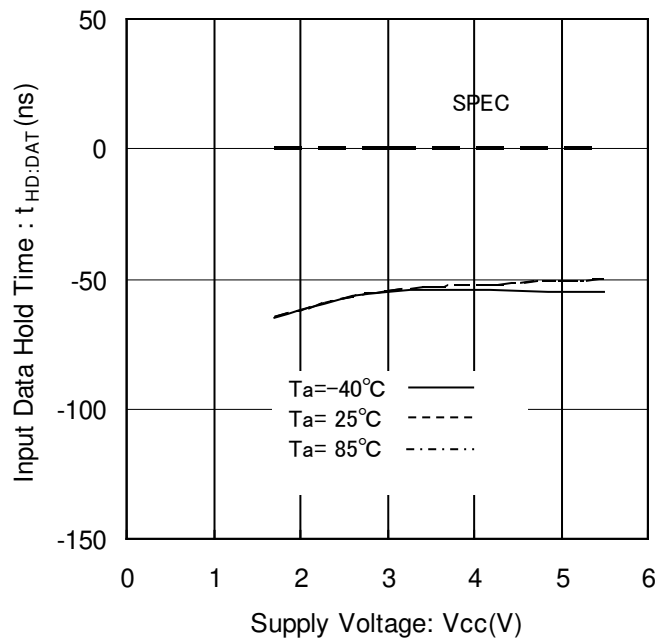Figure 18. Start Condition Setup Time vs Supply Voltage

Figure 19. Input Data Hold Time vs Supply Voltage (HIGH)

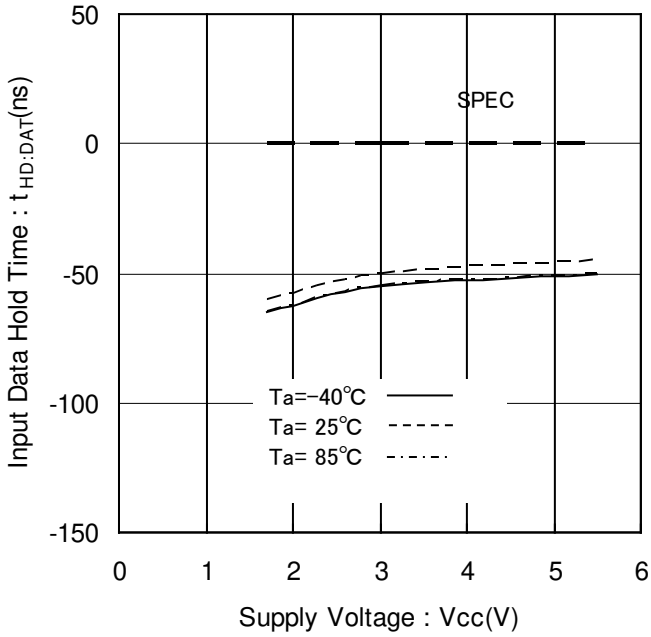## Typical Performance Curves - Continued

Figure 20. Input Data Hold Time vs Supply Voltage
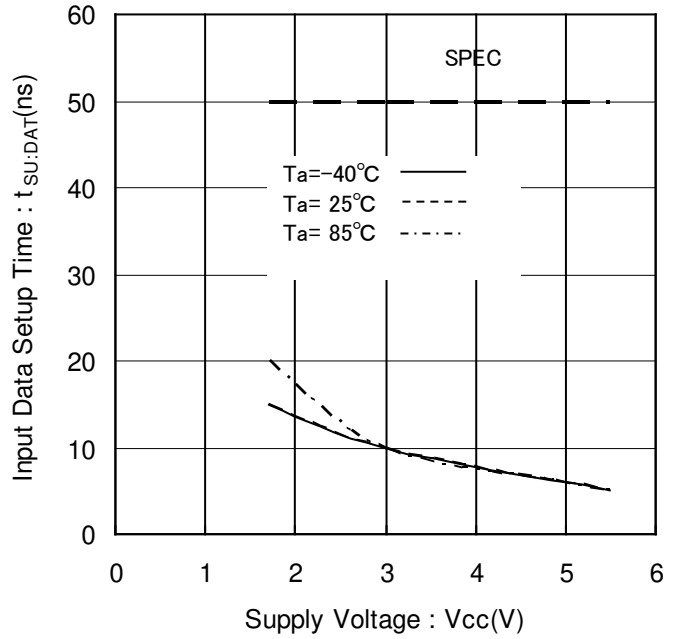(LOW)

Figure 21. Input Data Setup Time vs Supply Voltage
(HIGH)
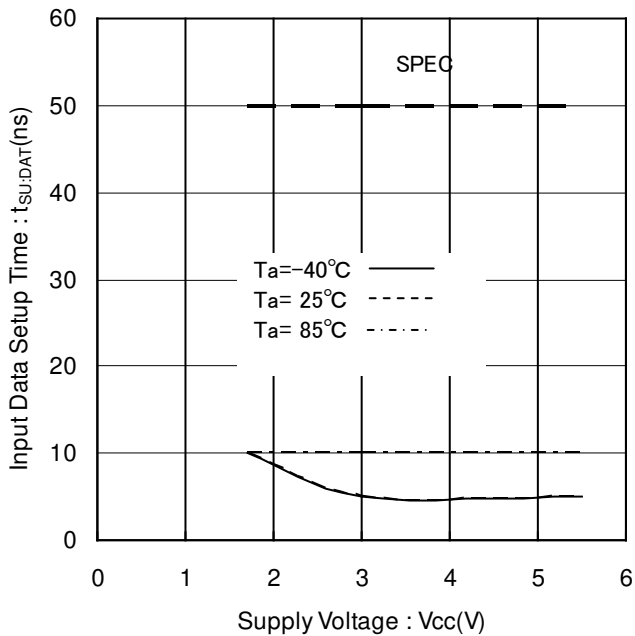
Figure 22. Input Data Setup Time vs Supply Voltage
(LOW)
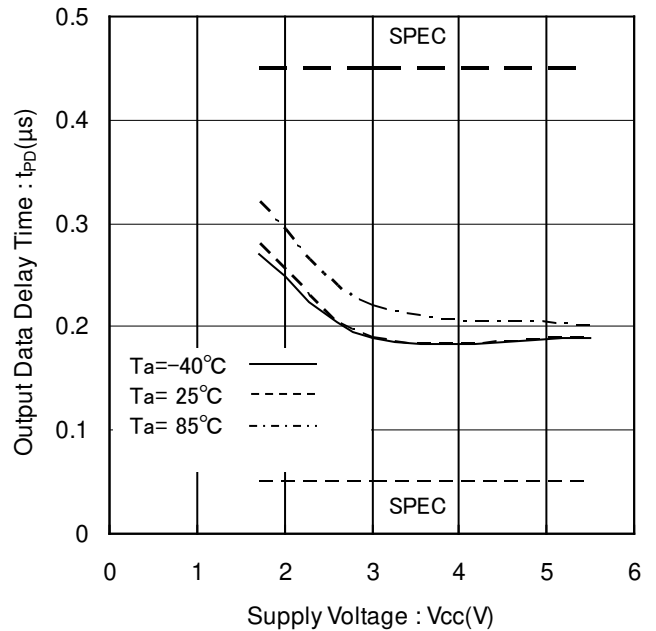
Figure 23. Output Data Delay Time vs Supply Voltage
(LOW)

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Typical Performance Curves - Continued
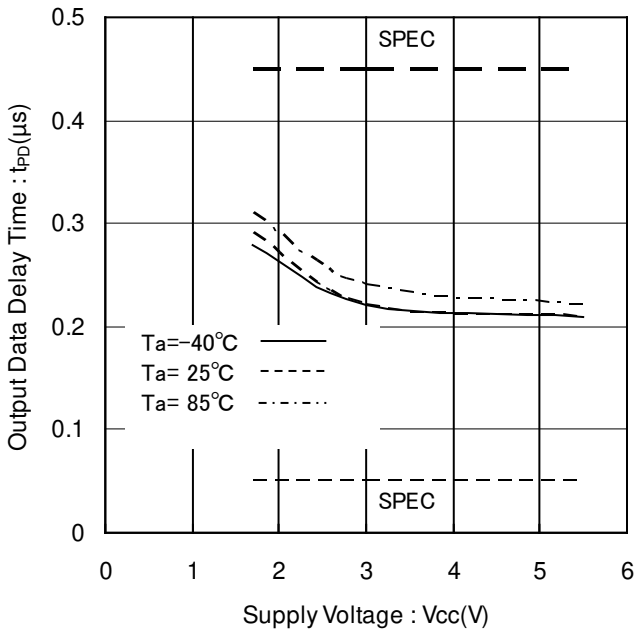
Figure 24. Output Data Delay Time vs Supply Voltage (HIGH)
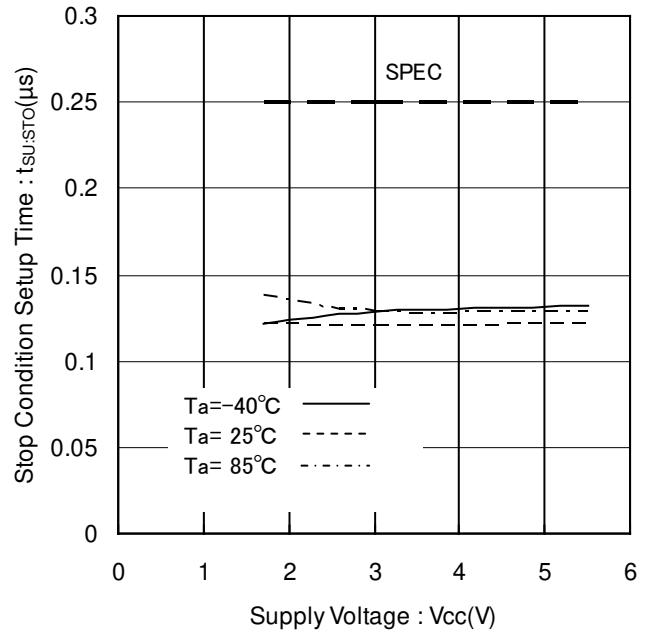
Figure 25. Stop Condition Setup Time vs Supply Voltage
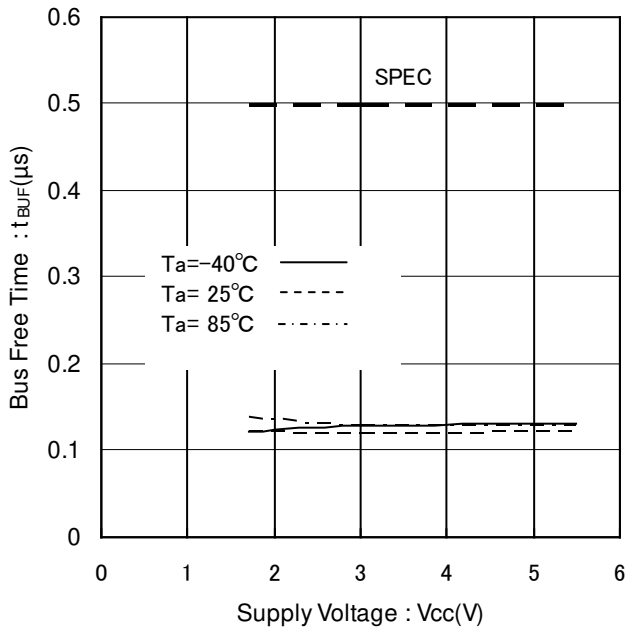
Figure 26. Bus Free Time vs Supply Voltage
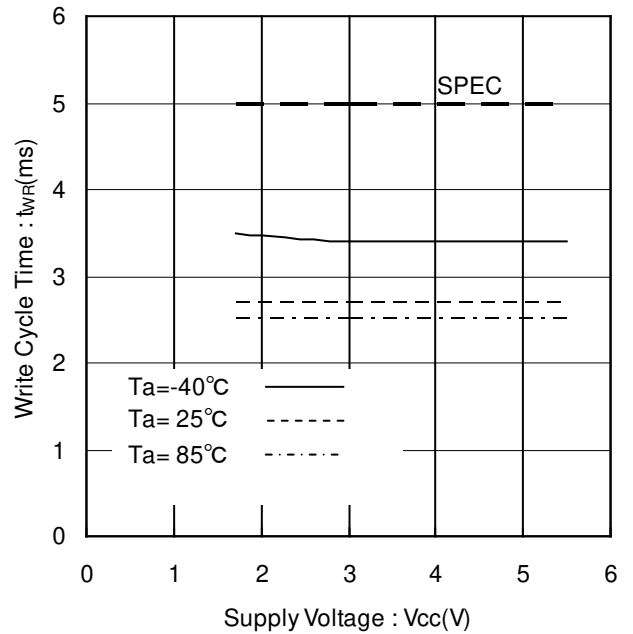
Figure 27. Write Cycle Time vs Supply Voltage

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Typical Performance Curves - Continued

Figure 28. Noise Spike Width vs Supply Voltage
(SCL HIGH)
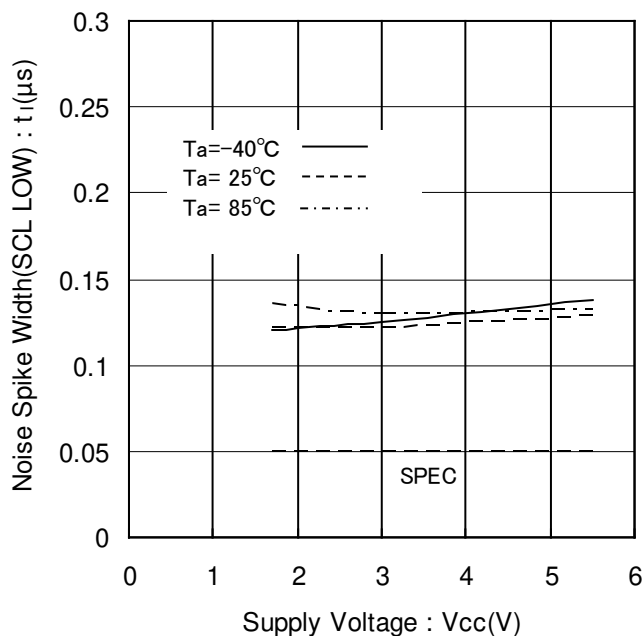
Figure 29. Noise Spike Width vs Supply Voltage
(SCL LOW)
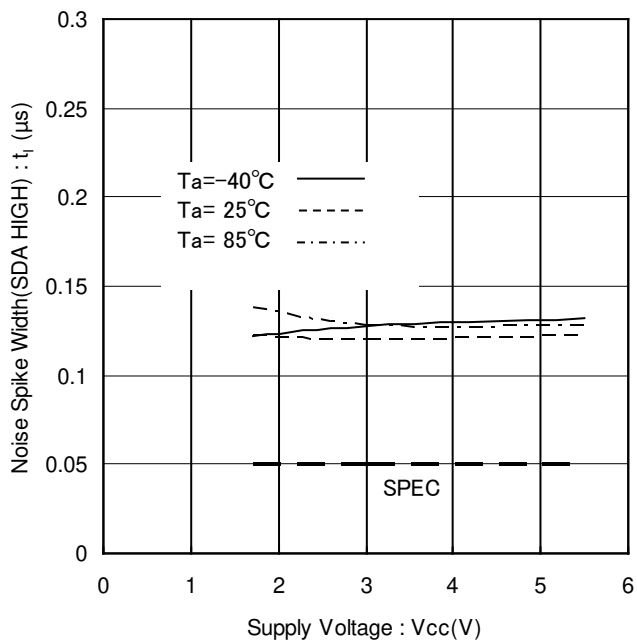
Figure 30. Noise Spike Width vs Supply Voltage
(SDA HIGH)

Figure 31. Noise Spike Width vs Supply Voltage
(SDA LOW)

Typical Performance Curves - Continued

Figure 32. WP Hold Time vs Supply Voltage

Figure 33. WP Setup Time vs Supply Voltage

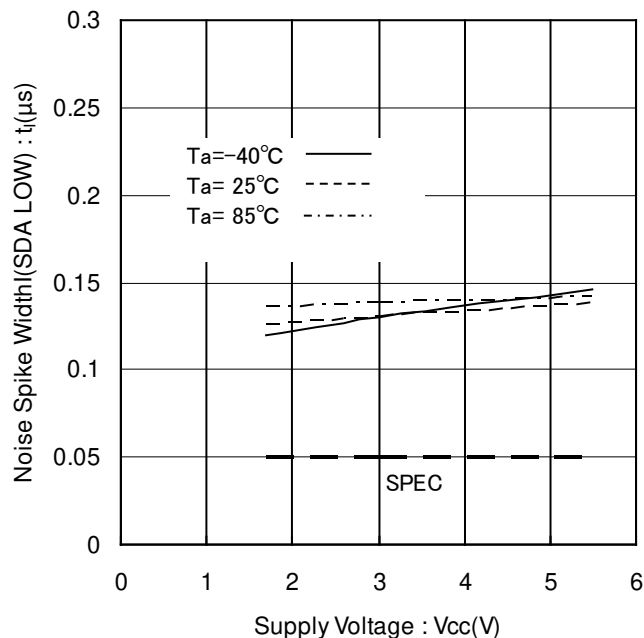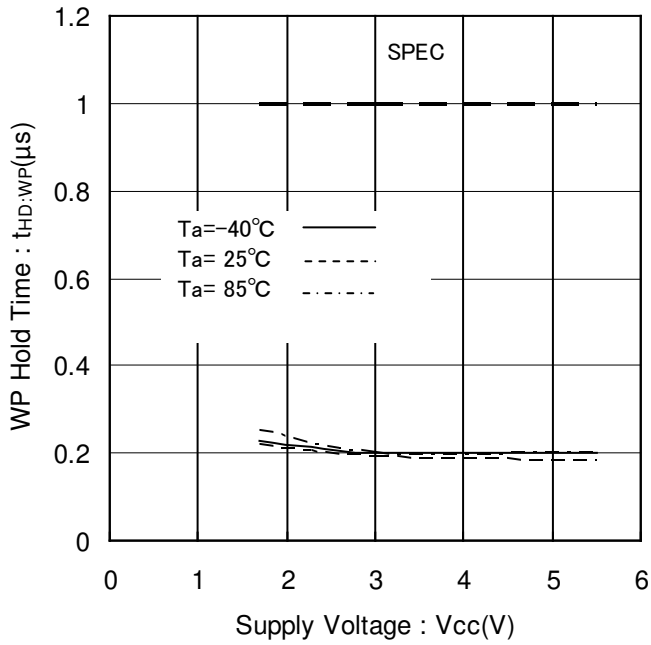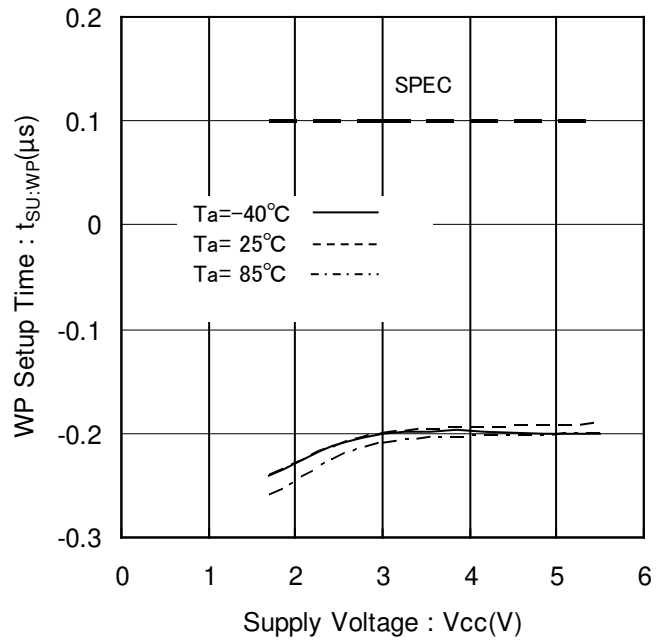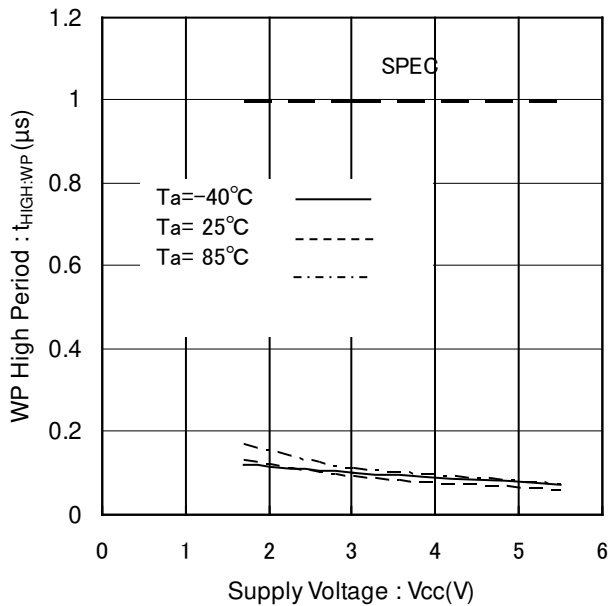Figure 34. WP High Period vs Supply Voltage

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Timing Chart

1. I²C BUS Data Communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS data communication with several devices is possible by connecting with 2 communication lines: serial data (SDA) and serial clock (SCL).

Among the devices, there should be a "master" that generates clock and control communication start and end. The rest become "slave" which are controlled by an address peculiar to each device, like this EEPROM. The device that outputs data to the bus during data communication is called "transmitter", and the device that receives data is called "receiver".
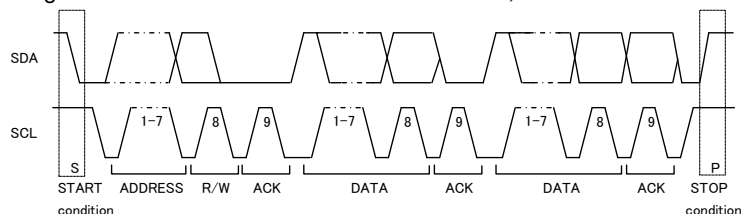
Figure 35. Data Transfer Timing

2. Start Condition (Start Bit Recognition)

(1) Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.

(2) This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command cannot be executed.

3. Stop Condition (Stop Bit Recognition)

(1) Each command can be ended by a stop condition (stop bit) where SDA goes from 'LOW' to 'HIGH' while SCL is 'HIGH'.

4. Acknowledge (ACK) Signal

(1) This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master-slave communication, the device (Ex. μ-COM sends slave address input for write or read command to this IC) at the transmitter (sending) side releases the bus after output of 8bit data.

(2) The device (Ex. This IC receives the slave address input for write or read command from the μ-COM) at the receiver (receiving) side sets SDA 'LOW' during 9th clock cycle, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.

(3) This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.

(4) After receiving 8bit data (word address and write data) during each write operation, this IC outputs acknowledge signal (ACK signal) 'LOW'.

(5) During read operation, this IC outputs 8bit data (read data) and detects acknowledge signal (ACK signal) 'LOW'. When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (μ-COM) side, this IC continues to output data. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, recognizes stop condition (stop bit), and ends read operation. Then this IC becomes ready for another trasmission.

5. Device Addressing

(1) Slave address comes after start condition from master.

(2) The significant 4 bits of slave address are used for recognizing a device type.

(3) The device code of this IC is fixed to '1010'.

(4) Next slave addresses (A2 A1 A0 --- device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses.

(5) The most insignificant bit (R/$\overline{W}$ --- READ/$\overline{WRITE}$) of slave address is used for designating write or read operation, and is as shown below.

Setting R / $\overline{w}$ to 0 ------- write (setting 0 to word address setting of random read)
Setting R / $\overline{w}$ to 1 ------- read

Type	Slave address								Maximum number of Connected buses
BR24G32-3A	1	0	1	0	A2	A1	A0	R/$\overline{w}$	8

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Write Command

1. Write Cycle

(1) Arbitrary data can be written to EEPROM. When writing only 1 byte, Byte Write is normally used, and when writing continuous data of 2 Bytes or more, simultaneous write is possible by Page Write cycle. The maximum number of Bytes is specified per device of each capacity. Up to 32 arbitrary Bytes can be written.

Figure 36. Byte Write Cycle

*1 WA12 to WA15 become don't care.

Figure 37. Page Write Cycle

*1 WA12 to WA15 become don't care.
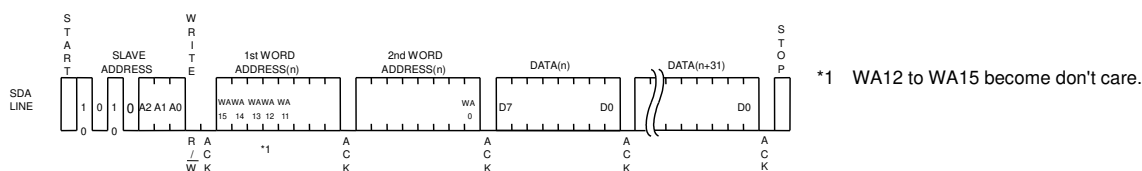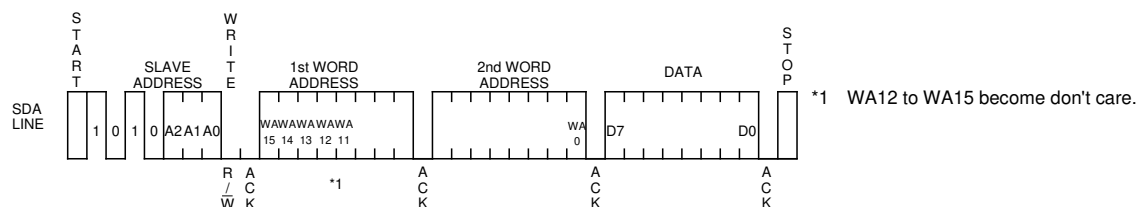
(2) During internal write execution, all input commands are ignored, therefore ACK is not returned.

(3) Data is written to the address designated by word address (n-th address)

(4) By issuing stop bit after 8bit data input, internal write to memory cell starts.

(5) When internal write is started, command is not accepted for t_{WR} (5ms at maximum).

(6) Using page write cycle, writing in bulk is done as follows: When data of more than 32 Bytes is sent, the bytes in excess overwrite the data already sent first.
(Refer to "Internal Address Increment")

(7) As for page write cycle of BR24G32-3A, where 2 or more bytes of data is intended to be written, after the 7 significant bits of word address are designated arbitrarily, only the value of 5 least significant bits in the address is incremented internally, so that data up to 32 bytes of memory only can be written.

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2. Notes on Write Cycle Continuous Input
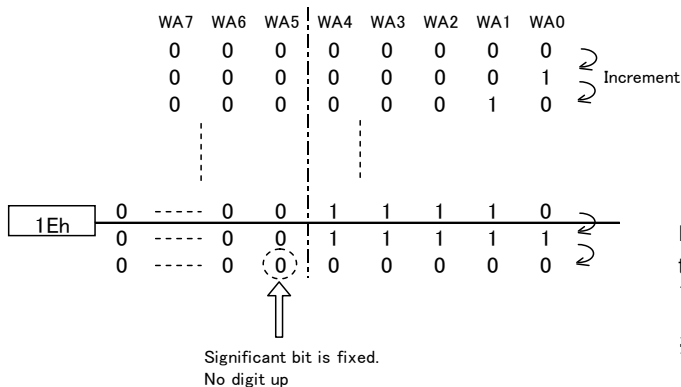
The maximum page numbers of BR24G32-3A are 32 Bytes. Any bytes below these can be written.

1 page = 32 Bytes, but the page write cycle time is 5ms at maximum for 32 Byte bulk write.
It does not stand 5ms at maximum x 32 Byte=160ms (Max)

3. Internal Address Increment
Page write mode

WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	0

Increment

1Eh
0	-----	0	0	1	1	1	1	0
0	-----	0	0	1	1	1	1	1
0	-----	0	(0)	0	0	0	0	0

Significant bit is fixed.
No digit up

For example, when it is started from address 1Eh, then, increment is made as below, 1Eh→1Fh→00h→01h··· please take note.

※1Eh···1E in hexadecimal, therefore, 00011110 becomes a binary number.

4. Write Protect (WP) Terminal
Write Protect (WP) Function
When WP terminal is set at V_{CC} (H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to V_{CC} or GND, or control it to H level or L level. Do not leave it open.
In case of using it as ROM, it is recommended to connect it to pull up or V_{CC}. At extremely low voltage at power ON/OFF, by setting the WP terminal 'H', write error can be prevented.

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Read Command

1. Read Cycle

Read cycle is when data of EEPROM is read. Read cycle could be random read cycle or current read cycle. Random read cycle is a command to read data by designating a specific address, and is used generally. Current read cycle is a command to read data of internal address register without designating an address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available where the next address data can be read in succession.
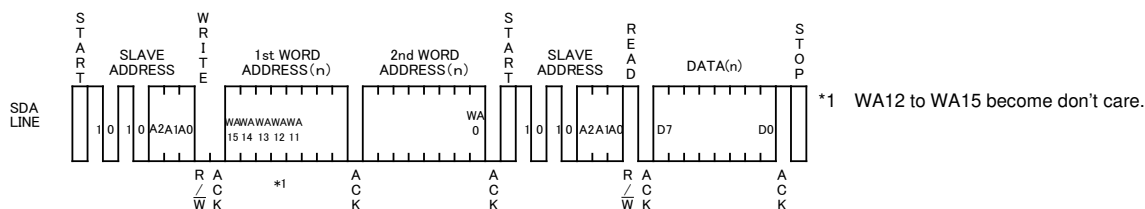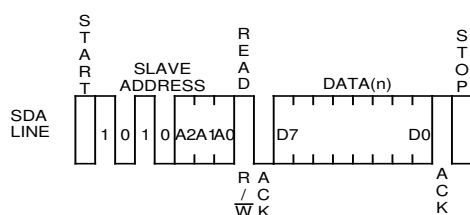

Figure 38. Random Read cycle

*1 WA12 to WA15 become don't care.

Figure 39. Current Read Cycle
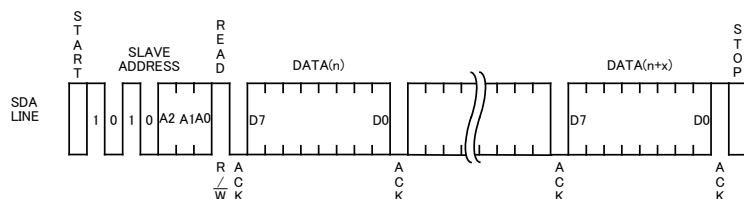

Figure 40. Sequential Read Cycle (in the case of Current Read Cycle)

(1) In random read cycle, data of designated word address can be read.
(2) When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th, i.e., data of the (n+1)-th address is output.
(3) When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (μ-COM) side, the next address data can be read in succession.
(4) Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal goes from 'L' to 'H' while SCL signal is 'H'.
(5) When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.
    Therefore, read command cycle cannot be ended. To end read command cycle, be sure to input 'H' to ACK signal after D0, and the stop condition where SDA goes from 'L' to 'H' while SCL signal is 'H'.
(6) Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is asserted from 'L' to 'H' while SCL signal is 'H'.

Software Reset

Software reset is executed to avoid malfunction after power ON, and during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Figure 41-(a), Figure 41-(b), Figure 41-(c).) Within the dummy clock input area, the SDA bus is released ('H' by pull up) and ACK output and read data '0' (both 'L' level) may be output from EEPROM. Therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.
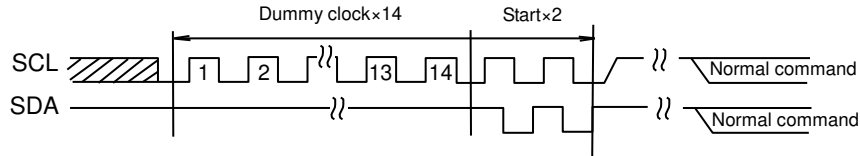

Figure 41-(a). The case of dummy clock × 14 +START+START+ command input
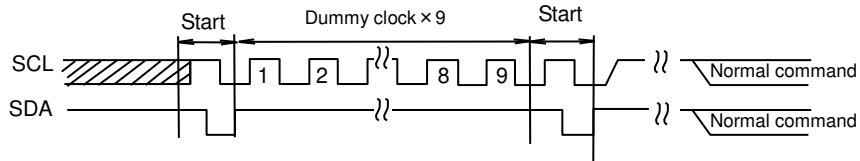
Figure 41-(b). The case of START + dummy clock × 9 +START+ command input
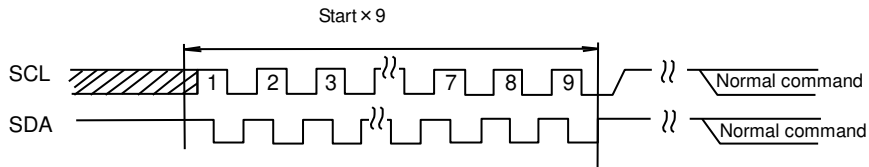
Figure 41-(c). START×9+ command input

※Start nomal command from START input.

Acknowledge Polling

During internal write execution, all input commands are ignored, therefore ACK is not returned. During internal automatic write execution after write cycle input, next command (slave address) is sent. If the first ACK signal sends back 'L', then it means end of write operation, else 'H' is returned, which means writing is still in progress. By the use of acknowledge polling, next command can be executed without waiting for t_{WR} = 5ms.
To write continuously, R/W = 0, then to carry out current read cycle after write, slave address with $\overline{R/W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

Figure 42. Case of Continuous Write by Acknowledge Polling

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WP Valid Timing (Write Cancel)

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so on, pay attention to the following WP valid timing. During write cycle execution, inside cancel valid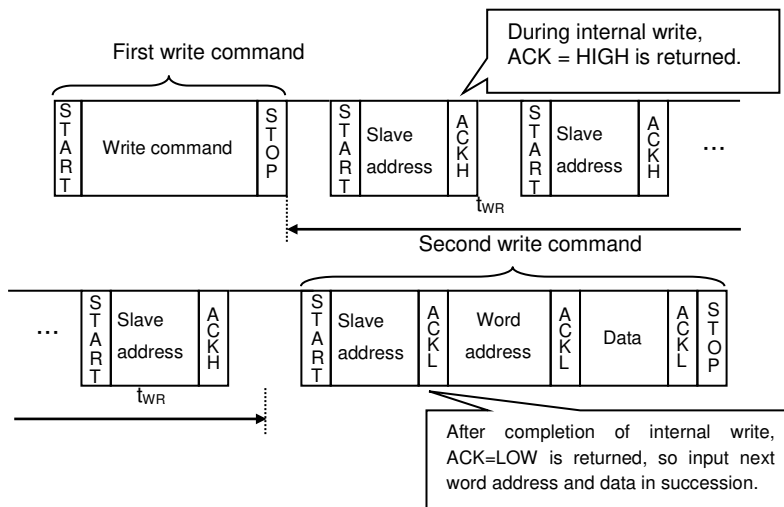 area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to take in D0 of data(in page write cycle, the first byte data) is the cancel invalid area.

WP input in this area becomes 'Don't care'. The area from the rise of SCL to take in D0 to the stop condition input is the cancel valid area. Furthermore, after the execution of forced end by WP, the IC enters standby status.
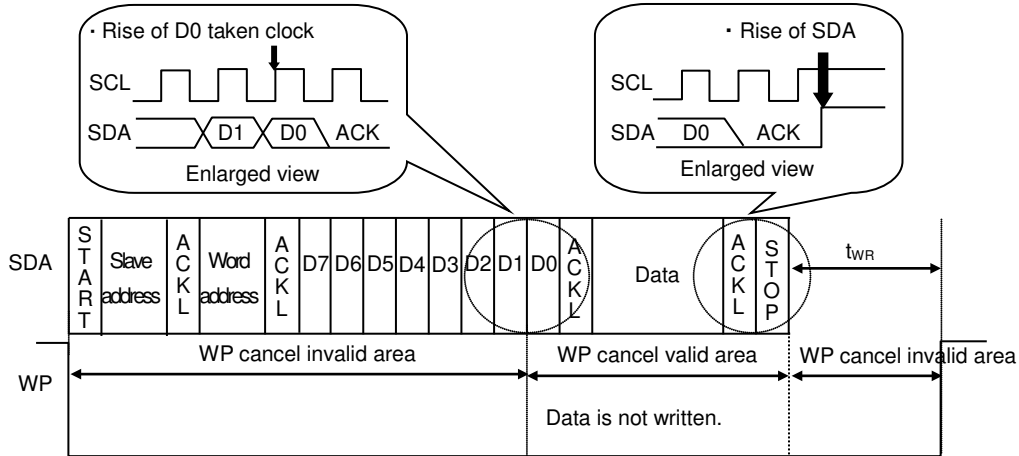
Figure 43. WP Valid Timing

Command Cancel by Start Condition and Stop Condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Figure 44.) However, within ACK output area and during data read, SDA bus may output 'L'. In this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. When command is cancelled by start-stop condition during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined. Therefore, it is not possible to carry out current read cycle in succession. To carry out read cycle in succession, carry out random read cycle.

Figure 44. Case of cancel by start, stop condition during slave address input

I/O Peripheral Circuit

1. Pull-up Resistance of SDA Terminal

SDA is NMOS open drain, so it requires a pull up resistor. As for this resistor value (R_{PU}), select an appropriate value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, operating frequency is limited. The smaller the R_{PU}, the larger is the supply current (Read).
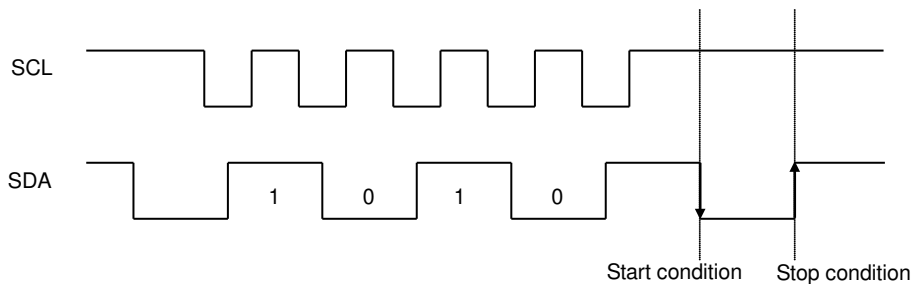
2. Maximum value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

(1) SDA rise time to be determined by the capacitance (C_{BUS}) of bus line of SDA and R_{PU} should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.

(2) The bus' electric potential Ⓐ to be determined by input current leak total (I_L) of the device connected to the bus with output of 'H' to SDA line and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin of $0.2V_{CC}$.

$$V_{CC} - I_L R_{PU} - 0.2\,V_{CC} \geqq V_{IH}$$

$$\therefore\quad R_{PU} \leqq \frac{0.8 V_{CC} - V_{IH}}{I_L}$$

Ex.) $V_{CC} = 3V$ $I_L = 10\mu A$ $V_{IH} = 0.7\,V_{CC}$
From (2)

$$R_{PU} \leqq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leqq 30\quad [k\Omega]$$

Figure 45. I/O Circuit Diagram

3. Minimum value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

(1) When IC outputs LOW, it should be satisfied that $V_{OLMAX} = 0.4V$ and $I_{OLMAX} = 3mA$.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore\quad R_{PU} \geqq \frac{V_{CC} - V_{OL}}{I_{OL}}$$

(2) $V_{OLMAX} = 0.4V$ should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including recommended noise margin $0.1V_{CC}$.

$$V_{OLMAX} \leqq V_{IL} - 0.1\,V_{CC}$$

Ex.) $V_{CC} = 3V$, $V_{OL} = 0.4V$, $I_{OL} = 3mA$, microcontroller, EEPROM $V_{IL} = 0.3 V_{CC}$

From (1) $R_{PU} \geqq \dfrac{3 - 0.4}{3 \times 10^{-3}}$

$$\geqq 867\quad [\Omega]$$

And $V_{OL} = 0.4\,[V]$
$V_{IL} = 0.3 \times 3$
$= 0.9\,[V]$

Therefore, the condition (2) is satisfied.

4. Pull-up Resistance of SCL Terminal

When SCL control is made at the CMOS output port, there is no need for a pull up resistor. But when there is a time where SCL becomes 'Hi-Z', add a pull up resistor. As for the pull up resistor value, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.
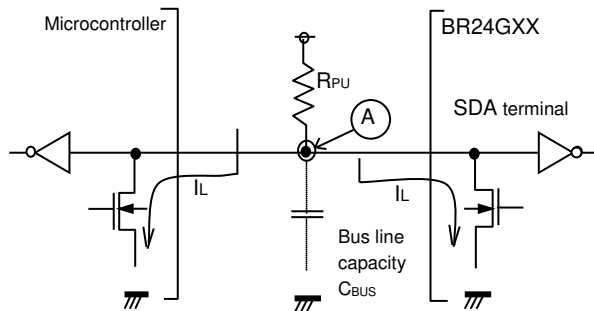
Cautions on Microcontroller Connection

1. R_S

In I²C BUS, it is recommended that SDA port is of open drain input/output. However, when using CMOS input / output of tri state to SDA port, insert a series resistance R_S between the pull up resistor R_{PU} and the SDA terminal of EEPROM. This is to control over current that may occur when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. R_S also plays the role of protecting the SDA terminal against surge. Therefore, even when SDA port is open drain input/output, R_S can be used.
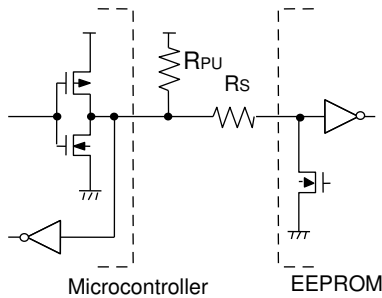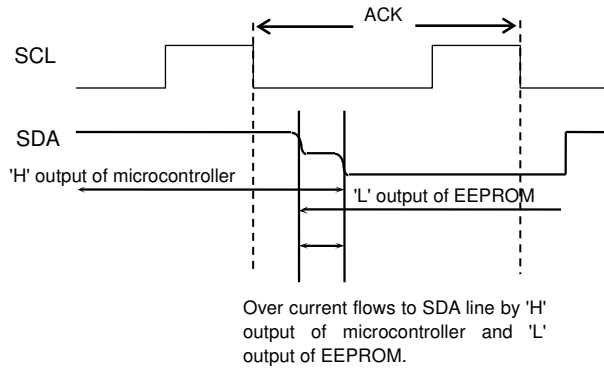
Figure 46. I/O Circuit Diagram

Figure 47. Input / Output Collision Timing

2. Maximum value of R_S

The maximum value of R_S is determined by the following relations.

(1) SDA rise time to be determined by the capacitance (C_{BUS}) of bus line of SDA and R_{PU} should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.

(2) The bus' electric potential Ⓐ to be determined by R_{pu} and R_S the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin of $0.1V_{CC}$.
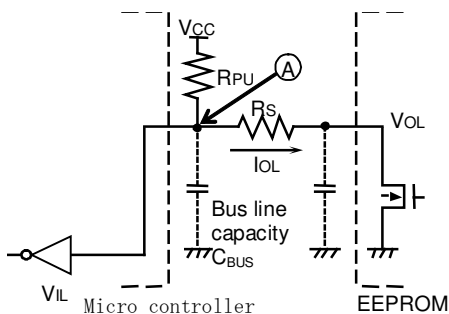
Figure 48. I/O Circuit Diagram

$$\frac{(V_{CC}-V_{OL}) \times R_S}{R_{PU}+R_S} + V_{OL} + 0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

$$\text{Ex.)} \; V_{CC}=3V \quad V_{IL}=0.3V_{CC} \quad V_{OL}=0.4V \quad R_{PU}=20k\Omega$$

$$R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67 \; k\Omega$$

3. Minimum value of R_S

The minimum value of R_S is determined by over current at bus collision. When over current flows, noises in power source line and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of the impedance of power source line in set and so forth. Set the over current to EEPROM at 10mA or lower.
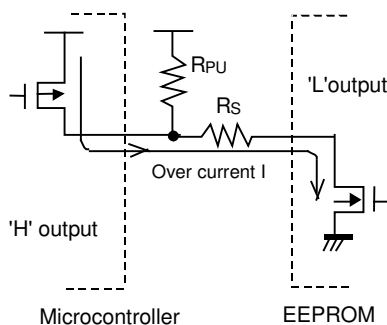
Figure 49. I/O Circuit Diagram

$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{V_{CC}}{I}$$

$$\text{Ex.)} \; V_{CC}=3V, \; I=10mA$$

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300 \; [\Omega]$$

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I/O Equivalence Circuit
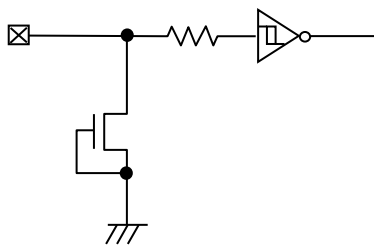
1. Input (A0, A1, A2, SCL, WP)

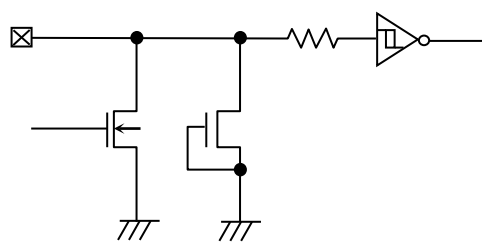Figure 50. Input Pin Circuit Diagram

2. Input / Output (SDA)

Figure 51. Input / Output Pin Circuit Diagram

Power-Up/Down Conditions

At power on, the IC's internal circuits may go through unstable low voltage area as the V_{CC} rises, making the IC's internal logic circuit not completely reset, hence, malfunction may occur. To prevent this, the IC is equipped with POR circuit and LVCC circuit. To assure the operation, observe the following conditions at power ON.

1. Set SDA = 'H' and SCL ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of t_R, t_{OFF}, and V_{bot} for operating POR circuit.
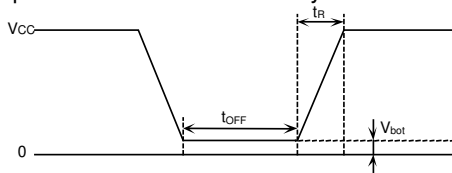
Figure 52. Rise Waveform Diagram

Recommended conditions of t_R, t_{OFF}, V_{bot}

t_R	t_{OFF}	V_{bot}
10ms or below	10ms or larger	0.3V or below
100ms or below	10ms or larger	0.2V or below

3. Set SDA and SCL so as not to become 'Hi-Z'.
   When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

   (1) In the case when the above condition 1 cannot be observed such that SDA becomes 'L' at power ON.
       →Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.
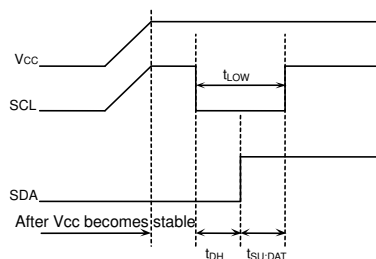
Figure 53. When SCL= 'H' and SDA= 'L'
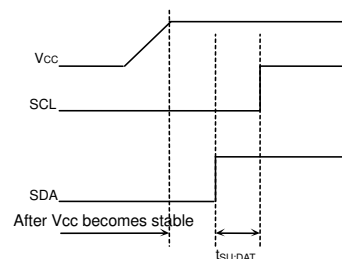
Figure 54. When SCL='L' and SDA='L'

   (2) In the case when the above condition 2 cannot be observed.
       →After power source becomes stable, execute software reset(Page 18).
   (3) In the case when the above conditions 1 and 2 cannot be observed.
       →Carry out (1), and then carry out (2).

Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite operation at low power, and prevents write error. At LVCC voltage (Typ=1.2V) or below, data rewrite is prevented.

Noise Countermeasures

1. Bypass Capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, it is recommended to connect a bypass capacitor (0.1µF) between the IC's V_{CC} and GND pins. Connect the capacitor as close to the IC as possible. In addition, it is also recommended to connect a bypass capacitor between board's V_{CC} and GND.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

Part Numbering

| B | R | 2 | 4 | G | 3 | 2 | x | x | x | - | 3 | A | | x | x | x | x | x |

BUS Type
24 : I²C

Operating Temperature/
Operating Voltage
-40°C to +85°C / 1.6V to 5.5V

Capacity
32=32Kbit

Package
Blank : DIP-T8   FJ   : SOP-J8M/SOP-J8
F   : SOP8   FVT : TSSOP-B8/TSSOP-B8M
FV   : SSOP-B8   FVM : MSOP8
FVJ   : TSSOP-B8J   QUZ : VMMP008Z1830
NUX : VSON008X2030

Process code

Revision

N	:	**SOP-J8M, TSSOP-B8M**
Blank	:	**DIP-T8, SOP8, SOP-J8, SSOP-B8, TSSOP-B8,**
		TSSOP-B8J, MSOP8, VSON008X2030, VMMP008Z1830

G   :   Halogen free
Blank :   Not Halogen free
 As an exception, SOP-J8M, TSSOP-B8M, VSON008X2030, VMMP008Z1830
 package will be Halogen free with "Blank"

T   :   100% Sn
Blank :   100% Sn
 As an exception, VMMP008Z1830 will be coated by Ni/Pd/Au

Packaging and forming specification
   E2   : Embossed tape and reel
                (SOP8, SOP-J8M, SOP-J8, SSOP-B8, TSSOP-B8, TSSOP-B8M, TSSOP-B8J)
   TR   : Embossed tape and reel
                (MSOP8, VSON008X2030, VMMP008Z1830)
   None   : Tube
                (DIP-T8)

Lineup

| Capacity | Package | | Orderable Part Number | | Remark | |
	Type	Quantity				
32Kbit	DIP-T8	Tube of 2000	BR24G32	-3A	Not Halogen free	100% Sn
	SOP8	Reel of 2500	BR24G32F	-3AGTE2	Halogen free	100% Sn
	SOP-J8M	Reel of 2500	BR24G32FJ	-3ANE2	Halogen free	100% Sn
	SOP-J8	Reel of 2500	BR24G32FJ	-3AGTE2	Halogen free	100% Sn
	SSOP-B8	Reel of 2500	BR24G32FV	-3AGTE2	Halogen free	100% Sn
	TSSOP-B8	Reel of 3000	BR24G32FVT	-3AGE2	Halogen free	100% Sn
	TSSOP-B8M	Reel of 3000	BR24G32FVT	-3ANE2	Halogen free	100% Sn
	TSSOP-B8J	Reel of 2500	BR24G32FVJ	-3AGTE2	Halogen free	100% Sn
	MSOP8	Reel of 3000	BR24G32FVM	-3AGTTR	Halogen free	100% Sn
	VSON008X2030	Reel of 4000	BR24G32NUX	-3ATTR	Halogen free	100% Sn
	VMMP008Z1830	Reel of 4000	BR24G32QUZ	-3ATR	Halogen free	Ni/Pd/Au

Physical Dimension, Tape and Reel Information

Package Name	DIP-T8

9. 3±0. 3

8   5

6. 5±0. 3

1   4

7. 6 2

0. 3±0. 1

0. 5 1 M I N
0. 3 4±0. 3
3. 2±0. 2
2. 5 4
0. 5±0. 1

0˚ ~1 5˚
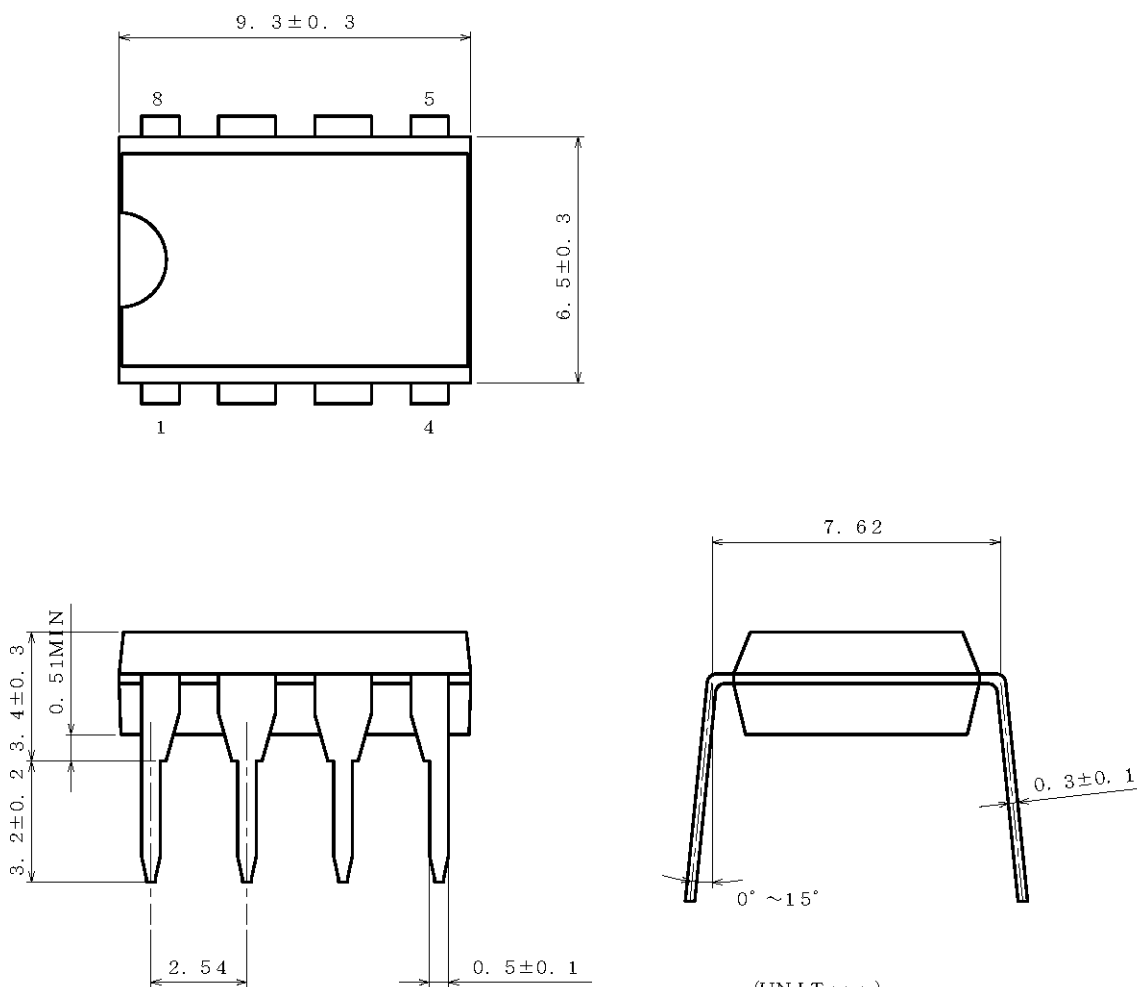
(U N I T : mm)
P G K : D I P−T 8
D r a w i n g No. E X 6 0 2−5 0 0 1

<Tape and Reel information>

Container	Tube
Quantity	2000pcs
Direction of feed	Direction of products is fixed in a container tube

＊Order quantity needs to be multiple of the minimum quantity.

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