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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



- ◇ STRUCTURE Silicon Monolithic Integrated Circuit
- ◇ PRODUCT SPI BUS Serial EEPROMs
- ◇ SERIES ADVANTAGE SERIES
- ◇ FAMILY BR25□□0 family
- ◇ TYPE Supply voltage 1.8V~5.5V/Operating temperature -40°C~+85°Ctype
- ◇ PART NUMBER BR25□□0-10□U-1.8

PART NUMBER	PACKAGE	DENSITY
BR25010N -10SU-1.8	8-lead JEDECSOIC	1Kbit
BR25020N -10SU-1.8		2Kbit
BR25040N -10SU-1.8		4Kbit
BR25080N -10SU-1.8		8Kbit
BR25160N -10SU-1.8		16Kbit
BR25320N -10SU-1.8		32Kbit
BR25010 -10TU-1.8	8-lead TSSOP	1Kbit
BR25020 -10TU-1.8		2Kbit
BR25040 -10TU-1.8		4Kbit
BR25080 -10TU-1.8		8Kbit
BR25160 -10TU-1.8		16Kbit

- ◇ FEATURES SPI BUS interface
 Endurance : 1,000,000 erase/write cycles
 Data retention : 100 years
 Initial Data: Memory array FFh

◇ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
T _{STG}	Storage Temperature	-65	125	°C
V _{IN}	Input range	-0.3	V _{CC} +0.3	V
V _{CC}	Supply Voltage	-0.3	6.5	V

◇ POWER DISSIPATION (T_a=25°C)

PACKAGE	Rating	Unit
8-lead JEDEC SOIC	450 *1	mW
8-lead TSSOP	330 *2	mW

* Degradation is done at 4.5mW/°C(*1), 3.3mW/°C(*2)for operation above 25°C

◇ DC OPERATING CHARACTERISTICS

(BR25010/020/040, Unless otherwise specified, T_μ=40°C to 85°C, VCC=+1.8V to +5.5V)

Parameter	Symbol	Specification			Units	Test Conditions
		Min.	Typ.	Max.		
Supply Current	I _{CC1}	-	-	3.0	mA	V _{CC} =5.0V, f _{SOCK} =1MHz, SO=Open, Read
Supply Current	I _{CC2}	-	-	6.0	mA	V _{CC} =5.0V, f _{SOCK} =2MHz, SO=Open, Read, Write
Standby Current	I _{S81}	-	-	1.0	μA	V _{CC} =1.8V, CS=HOLD=WP=V _{CC} , SCK=SI=V _{CC} or GND, SO=OPEN
Standby Current	I _{S82}	-	-	5.0	μA	V _{CC} =2.7V, CS=HOLD=WP=V _{CC} , SCK=SI=V _{CC} or GND, SO=OPEN
Standby Current	I _{S83}	-	-	10.0	μA	V _{CC} =5.0V, CS=HOLD=WP=V _{CC} , SCK=SI=V _{CC} or GND, SO=OPEN
Input Leakage	I _L	-0.8	-	3.0	μA	V _I =0V~V _{CC}
Output Leakage	I _{OL}	-0.8	-	3.0	μA	V _O =0V~V _{CC} , T _A =0°C~70°C
Input Low Voltage	V _{IL}	-	-	V _{CC} x0.3	V	-
Input High Voltage	V _{IH}	V _{CC} x0.7	-	-	V	-
Output Low Voltage	V _{OL1}	-	-	0.4	V	4.5V ≤ V _{CC} ≤ 5.5V, I _{OL} =2.0mA
Output High Voltage	V _{OH1}	V _{CC} -0.8	-	-	V	4.5V ≤ V _{CC} ≤ 5.5V, I _{OH} =-1.0mA
Output Low Voltage	V _{OL2}	-	-	0.2	V	1.8V ≤ V _{CC} ≤ 5.5V, I _{OL} =0.15mA
Output High Voltage	V _{OH2}	V _{CC} -0.2	-	-	V	1.8V ≤ V _{CC} ≤ 5.5V, I _{OH} =-100 μA

◇ DC OPERATING CHARACTERISTICS

(BR25080/160/320, Unless otherwise specified, T_μ=40°C to 85°C, VCC=+1.8V to +5.5V)

Parameter	Symbol	Specification			Units	Test Conditions
		Min.	Typ.	Max.		
Supply Current	I _{CC1}	-	-	3.0	mA	V _{CC} =5.0V, f _{SOCK} =1MHz, SO=Open, Read
Supply Current	I _{CC2}	-	-	5.0	mA	V _{CC} =5.0V, f _{SOCK} =2MHz, SO=Open, Read, Write
Standby Current	I _{S81}	-	0.1	1.0	μA	V _{CC} =1.8V, CS=HOLD=WP=V _{CC} , SCK=SI=V _{CC} or GND, SO=OPEN
Standby Current	I _{S82}	-	0.2	2.0	μA	V _{CC} =2.7V, CS=HOLD=WP=V _{CC} , SCK=SI=V _{CC} or GND, SO=OPEN
Standby Current	I _{S83}	-	2.0	5.0	μA	V _{CC} =5.0V, CS=HOLD=WP=V _{CC} , SCK=SI=V _{CC} or GND, SO=OPEN
Input Leakage	I _L	-3.0	-	3.0	μA	V _I =0V~V _{CC}
Output Leakage	I _{OL}	-3.0	-	3.0	μA	V _O =0V~V _{CC} , T _A =0°C~70°C
Input Low Voltage	V _{IL}	-	-	V _{CC} x0.3	V	-
Input High Voltage	V _{IH}	V _{CC} x0.7	-	-	V	-
Output Low Voltage	V _{OL1}	-	-	0.4	V	4.5V ≤ V _{CC} ≤ 5.5V, I _{OL} =3.0mA
Output High Voltage	V _{OH1}	V _{CC} -0.8	-	-	V	4.5V ≤ V _{CC} ≤ 5.5V, I _{OH} =-1.8mA
Output Low Voltage	V _{OL2}	-	-	0.2	V	1.8V ≤ V _{CC} ≤ 5.5V, I _{OL} =0.15mA
Output High Voltage	V _{OH2}	V _{CC} -0.2	-	-	V	1.8V ≤ V _{CC} ≤ 5.5V, I _{OH} =-100 μA

◇ AC OPERATING CHARACTERISTICS

(BR25010/020/040, Unless otherwise specified, T_μ=40°C to 85°C, VCC=+1.8V to +5.5V, C_I=100pF)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
SCK Clock Frequency	f _{SOCK}	0	-	3.0	MHz	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Input Rise Time	t _{RI}	-	-	2	μs	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Input Fall Time	t _{FI}	-	-	2	μs	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
SCK High Time	t _{HH}	133	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
SCK Low Time	t _{HL}	133	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
CS High Time	t _{CS}	250	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
CS Setup Time	t _{CS}	250	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
CS Hold Time	t _{CSH}	250	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Data In Setup Time	t _{SU}	50	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Data In Hold Time	t _H	50	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Hold Setup Time	t _{SD}	100	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Hold Hold Time	t _{SD}	200	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Output Valid	t _V	0	-	133	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Output Hold Time	t _{HO}	0	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Hold to Output Low Z	t _{LZ}	0	-	100	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Hold to Output High Z	t _{HZ}	-	-	100	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Output Disable Time	t _{OS}	-	-	250	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Write Cycle Time	t _{WC}	-	-	5	ms	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Endurance *1	-	1M	-	-	Write Cycles	-

*1 This parameter is characterized and is not 100% tested.

○ This product is not designed for protection against radioactive rays.

◇ AC OPERATING CHARACTERISTICS

(BR25080/160/320, Unless otherwise specified, T_μ=40°C to 85°C, VCC=+1.8V to +5.5V, C_I=100pF)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
SCK Clock Frequency	f _{SOCK}	0	-	3.0	MHz	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Input Rise Time	t _{RI}	-	-	2	μs	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Input Fall Time	t _{FI}	-	-	2	μs	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
SCK High Time	t _{HH}	133	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
SCK Low Time	t _{HL}	133	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
CS High Time	t _{CS}	250	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
CS Setup Time	t _{CS}	250	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
CS Hold Time	t _{CSH}	250	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Data In Setup Time	t _{SU}	50	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Data In Hold Time	t _H	50	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Hold Setup Time	t _{SD}	100	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Hold Hold Time	t _{SD}	200	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Output Valid	t _V	0	-	133	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Output Hold Time	t _{HO}	0	-	-	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Hold to Output Low Z	t _{LZ}	0	-	100	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Hold to Output High Z	t _{HZ}	-	-	100	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Output Disable Time	t _{OS}	-	-	250	ns	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Write Cycle Time	t _{WC}	-	-	5	ms	4.5V ≤ V _{CC} ≤ 5.5V, 2.7V ≤ V _{CC} ≤ 5.5V, 1.8V ≤ V _{CC} ≤ 5.5V
Endurance *1	-	1M	-	-	Write Cycles	-

*1 This parameter is characterized and is not 100% tested.

◇ BLOCK DIAGRAM

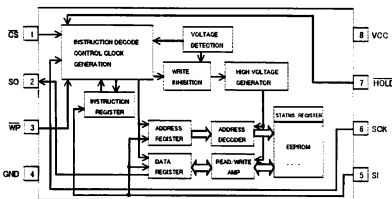


Fig.-1 BLOCK DIAGRAM

◇ PIN No., PIN NAME

PIN No.	PIN NAME
1	CS
2	SO
3	WP
4	GND
5	SI
6	SCK
7	HOLD
8	VCC

◇NOTES FOR POWER SUPPLY

In order to prevent an inadvertent write, the device has the feature of P.O.R.
 After the power is on, the device is in the write disable mode. P.O.R. works only during power up. The noise may force the device write enable mode with \overline{CS} ="H" during power ON/OFF. In the case of power up, keep the following conditions to ensure to make the function of P.O.R.

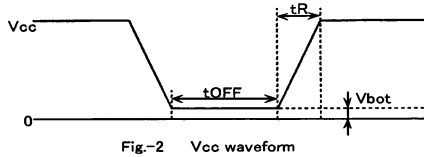


Fig.-2 Vcc waveform

◇RECOMMENDED CONDITIONS OF tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

Please keep \overline{CS} "H" during power ON/OFF.

The device is an active state during \overline{CS} is low. The extraordinary function or data collaption may occur because of noise etc., if power-up is done with \overline{CS} "L". In order to prevent above errors from happening, keep \overline{CS} "H" (=Vcc) during power ON. (The device does not receive any command during \overline{CS} is high.)

It may continue at low Vcc by capacitance of Vcc line during power off.

Please keep \overline{CS} "H" during power off because of the device may make malfunction and inadvertent write.

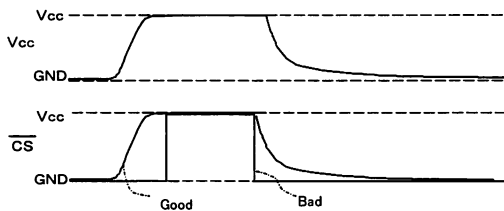


Fig.-3 \overline{CS} TIMING DURING POWER ON/OFF

(Good example)
 \overline{CS} follows Vcc. (\overline{CS} is pull up to Vcc)

(Bad example)
 \overline{CS} is low during power ON/OFF.

Please take more than 10ms between power ON and power OFF, or the internal circuit is not always reset.

◇CAUTIONS ON USE

(1) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(3) Thermal design

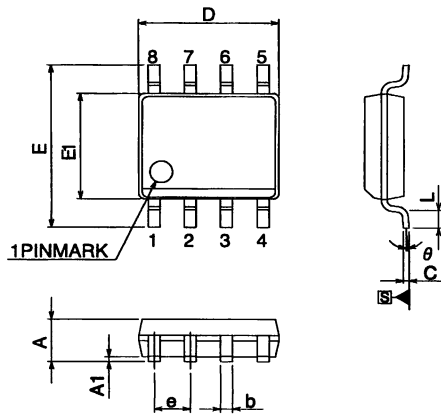
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇ PHYSICAL DIMENSION



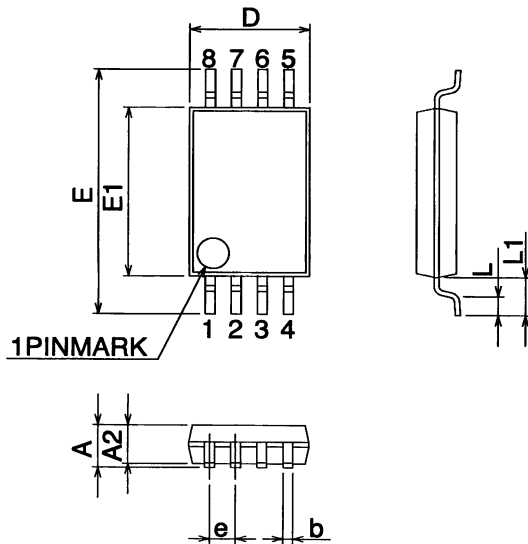
- Notes**
- 1.This drawing is subject to change without notice.
 - 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 - 3.Reference JEDEC MS-012 variation AA.

Fig.-4 8-lead JEDEC SOIC Package Outline

◇ 8-lead JEDEC SOIC Package Size Data

Symbol	mm			inches		
	Typ.	Min.	Max	Typ.	Min.	Max
A	-	1.35	1.75	-	0.053	0.069
A1	-	0.10	0.25	-	0.004	0.010
b	-	0.31	0.51	-	0.012	0.020
c	-	0.17	0.25	-	0.007	0.010
D	-	4.80	5.00	-	0.189	0.197
e	1.27 BSC	-	-	0.050 BSC	-	-
E	-	5.79	6.20	-	0.228	0.244
E1	-	3.81	3.99	-	0.150	0.157
L	-	0.40	1.27	-	0.016	0.050
θ	-	0°	8°	-	0°	8°

◇ 8-lead TSSOP Package Size Data



- Notes**
- 1.This drawing is subject to change without notice.
 - 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 - 3.Reference JEDEC MO-153.

Fig.-5 8-lead TSSOP Package Outline

Symbol	mm			inches		
	Typ.	Min.	Max	Typ.	Min.	Max
A	-	-	1.20	-	-	0.047
A2	1.00	0.80	1.05	0.039	0.031	0.041
b	-	0.19	0.30	-	0.007	0.012
D	3.00	2.90	3.10	0.118	0.114	0.122
e	0.65 BSC	-	-	0.025	-	-
E	6.40 BSC	-	-	0.252	-	-
E1	4.40	4.30	4.50	0.173	0.169	0.177
L	0.60	0.45	0.75	0.023	0.017	0.030
L1	1.00 BSC	-	-	0.039	-	-

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U.S.A / San Diego	TEL : +1(858)625-3630	FAX : +1(858)625-3670
Atlanta	TEL : +1(770)754-5972	FAX : +1(770)754-0691
Dallas	TEL : +1(972)312-8818	FAX : +1(972)312-0330
Germany / Dusseldorf	TEL : +49(2154)9210	FAX : +49(2154)921400
United Kingdom / London	TEL : +44(1)908-282-666	FAX : +44(1)908-282-528
France / Paris	TEL : +33(0)1 56 97 30 60	FAX : +33(0) 1 56 97 30 80
China / Hong Kong	TEL : +852(2)740-6262	FAX : +852(2)375-8971
Shanghai	TEL : +86(21)6279-2727	FAX : +86(21)6247-2066
Dilian	TEL : +86(411)8230-8549	FAX : +86(411)8230-8537
Beijing	TEL : +86(10)8525-2483	FAX : +86(10)8525-2489
Taiwan / Taipei	TEL : +866(2)2500-6956	FAX : +866(2)2503-2869
Korea / Seoul	TEL : +82(2)8182-700	FAX : +82(2)8182-715
Singapore	TEL : +65-6332-2322	FAX : +65-6332-5662
Malaysia / Kuala Lumpur	TEL : +60(3)7958-8355	FAX : +60(3)7958-8377
Philippines / Manila	TEL : +63(2)807-6872	FAX : +63(2)809-1422
Thailand / Bangkok	TEL : +66(2)254-4890	FAX : +66(2)256-6334

Japan /
(Internal Sales)

Tokyo	2-1-1, Yaesu, Chuo-ku, Tokyo 104-0082	TEL : +81(3)5203-0321	FAX : +81(3)5203-0300
Yokohama	2-4-8, Shin Yokohama, Kohoku-ku, Yokohama, Kanagawa 222-8575	TEL : +81(45)476-2131	FAX : +81(45)476-2128
Nagoya	Dainagayo Building 9F 3-28-12, Meieki, Nakamura-ku, Nagoya, Aichi 450-0002	TEL : +81(52)581-8521	FAX : +81(52)561-2173
Kyoto	579-32 Higashi Shiokouji-cho, Karasuma Nishi-iru, Shiokoujidori, Shimogyo-ku, Kyoto 600-8216	TEL : +81(75)311-2121	FAX : +81(75)314-6559

(Contact address for overseas customers in Japan)

Yokohama	TEL : +81(45)476-9270	FAX : +81(045)476-9271
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