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Serial EEPROM Series Automotive EEPROM  
**105°C Operation SPI BUS EEPROM**
**BR25A512-3M**
**General Description**

BR25A512-3M is a 512Kbit Serial EEPROM of SPI BUS Interface.

**Features**

- High Speed Clock Action up to 10MHz (Max)
- Wait Function by HOLDB Terminal
- Part or Whole of Memory Arrays Settable as Read only Memory Area by Program
- 2.5V to 5.5V Single Power Source Operation Most Suitable for Battery Use
- Up to 128 Bytes in Page Write Mode
- For SPI Bus Interface (CPOL, CPHA) = (0, 0), (1, 1)
- Self-timed Programming Cycle
- Low Current Consumption
  - At Write Action (5V) : 0.7mA (Typ)
  - At Read Action (5V) : 2.4mA (Typ)
  - At Standby Action (5V) : 0.1µA (Typ)
- Address Auto Increment Function at Read Action
- Prevention of Write Mistake
  - Write Prohibition at Power On
  - Write Prohibition by Command Code (WRDI)
  - Write Prohibition by WPB Pin
  - Write Prohibition Block Setting by Status Registers (BP1, BP0)
  - Prevention of Write Mistake at Low Voltage
- More than 100 years Data Retention
- More than 1 Million Write Cycles
- Bit Format 64K × 8
- Initial Delivery Data
  - Memory Array : FFh
  - Status Register : WPEN, BP1, BP0 : 0

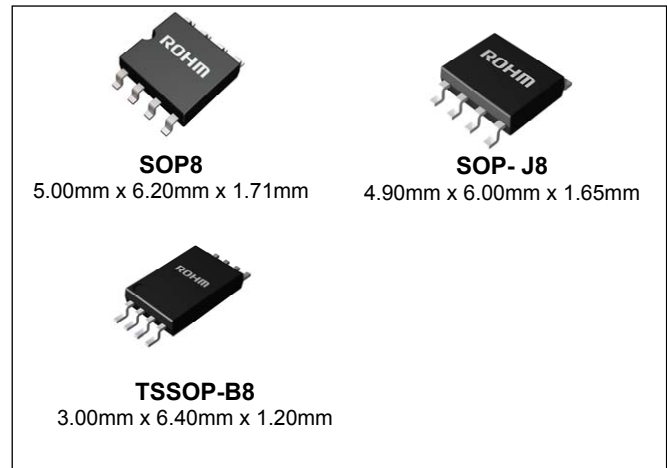
**Packages W(Typ) x D(Typ) x H(Max)**


Figure 1.

**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	V <sub>CC</sub>	-0.3 to +6.5	V	
Power Dissipation	P <sub>d</sub>	0.45 (SOP8)	W	When using at Ta=25°C or higher 4.5mW to be reduced per 1°C.
		0.45 (SOP-J8)		When using at Ta=25°C or higher 4.5mW to be reduced per 1°C.
		0.33 (TSSOP-B8)		When using at Ta=25°C or higher 3.3mW to be reduced per 1°C.
Storage Temperature	T <sub>stg</sub>	- 65 to +150	°C	
Operating Temperature	T <sub>opr</sub>	- 40 to +105	°C	
Input Voltage / Output Voltage	-	- 0.3 to V <sub>CC</sub> +1.0	V	The Max value of Input Voltage/Output Voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of Input Voltage/Output Voltage is not under -1.0V.
Junction Temperature	T <sub>jmax</sub>	150	°C	Junction temperature at the storage condition
Electrostatic discharge voltage (human body model)	V <sub>ESD</sub>	-4000 to +4000	V	

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Memory Cell Characteristics (Ta=25°C, V<sub>CC</sub>=2.5V to 5.5V)**

Parameter	Limits			Unit	Condition
	Min	Typ	Max		
Write Cycles (Note1)	1,000,000	-	-	Times	Ta≤25°C
	150,000	-	-	Times	Ta≤105°C
Data Retention (Note1)	100	-	-	Years	Ta≤25°C
	20	-	-	Years	Ta≤105°C

(Note1) Not 100% TESTED

**Recommended Operating Ratings**

Parameter	Symbol	Ratings		Unit
		Min	Max	
Power Source Voltage	V <sub>CC</sub>	2.5	5.5	V
Input Voltage	V <sub>IN</sub>	0	V <sub>CC</sub>	V
Bypass capacitor	C	0.1	-	μF

**Input / Output Capacity (Ta=25°C, frequency=5MHz)**

Parameter	Symbol	Min	Max	Unit	Conditions
Input Capacity (Note1)	C <sub>IN</sub>	-	8	pF	V <sub>IN</sub> =GND
Output Capacity (Note1)	C <sub>OUT</sub>	-	8		V <sub>OUT</sub> =GND

(Note1) Not 100% TESTED.

**DC Characteristics (Unless otherwise specified, Ta=-40°C to +105°C, V<sub>CC</sub>=2.5V to 5.5V)**

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input High Voltage	V <sub>IH</sub>	0.7 x V <sub>CC</sub>	-	V <sub>CC</sub> +1.0	V	
Input Low Voltage	V <sub>IL</sub>	-0.3 (Note1)	-	0.3 x V <sub>CC</sub>	V	
Output Low Voltage	V <sub>OL</sub>	0	-	0.4	V	I <sub>OL</sub> =3.0mA
Output High Voltage	V <sub>OH</sub>	V <sub>CC</sub> -0.2	-	V <sub>CC</sub>	V	I <sub>OH</sub> =-2.0mA
Input Leakage Current	I <sub>LI</sub>	- 1	-	1	μA	V <sub>IN</sub> =0 to V <sub>CC</sub>
Output Leakage Current	I <sub>LO</sub>	- 1	-	1	μA	V <sub>OUT</sub> =0 to V <sub>CC</sub> , CSB=V <sub>CC</sub>
Supply Current (Write)	I <sub>CC1</sub>	-	-	1.5	mA	V <sub>CC</sub> =2.5V, f <sub>SCK</sub> =5MHz, t <sub>EW</sub> =5ms Byte Write, Page Write, Write Status Register
	I <sub>CC2</sub>	-	-	2	mA	V <sub>CC</sub> =5.5V, f <sub>SCK</sub> =10MHz, t <sub>EW</sub> =5ms Byte Write, Page Write, Write Status Register
Supply Current (Read)	I <sub>CC3</sub>	-	-	4	mA	V <sub>CC</sub> =5.5V, f <sub>SCK</sub> =10MHz, SO=OPEN Read, Read Status Register VIH/VIL=0.9V <sub>CC</sub> /0.1V <sub>CC</sub>
Standby Current	I <sub>SB</sub>	-	-	10	μA	V <sub>CC</sub> =5.5V, SO=OPEN CSB=HOLDB=WPB=V <sub>CC</sub> , SCK=SI=V <sub>CC</sub> or GND

(Note1) When the pulse width is 50ns or less, it is -1.0V.

## AC Characteristics (Ta=-40°C to +105°C, 2.5V≤Vcc&lt;4.0V CL=30pF, 4.0V≤Vcc≤5.5V CL=50pF)

Parameter	Symbol	2.5V≤Vcc≤5.5V			4.0V≤Vcc≤5.5V			Unit
		Min	Typ	Max	Min	Typ	Max	
SCK Frequency	f <sub>SCK</sub>	0.01	-	5	0.01	-	10	MHz
SCK High Time	t <sub>SCKWH</sub>	80	-	-	40	-	-	ns
SCK Low Time	t <sub>SCKWL</sub>	80	-	-	40	-	-	ns
CSB High Time	t <sub>CS</sub>	40	-	-	40	-	-	ns
CSB Setup Time	t <sub>CSS</sub>	30	-	-	30	-	-	ns
CSB Hold Time	t <sub>CSH</sub>	30	-	-	30	-	-	ns
SCK Setup Time	t <sub>SCKS</sub>	20	-	-	20	-	-	ns
SCK Hold Time	t <sub>SCKH</sub>	20	-	-	20	-	-	ns
SI Setup Time	t <sub>DIS</sub>	10	-	-	10	-	-	ns
SI Hold Time	t <sub>DIH</sub>	10	-	-	10	-	-	ns
Data Output Delay Time	t <sub>PD</sub>	-	-	70	-	-	40	ns
Output Hold Time	t <sub>OH</sub>	0	-	-	0	-	-	ns
Output Disable Time	t <sub>OZ</sub>	-	-	40	-	-	40	ns
HOLDB Setting Setup Time	t <sub>HFS</sub>	0	-	-	0	-	-	ns
HOLDB Setting Hold Time	t <sub>HFH</sub>	20	-	-	10	-	-	ns
HOLDB Release Setup Time	t <sub>HRS</sub>	0	-	-	0	-	-	ns
HOLDB Release Hold Time	t <sub>HRH</sub>	20	-	-	10	-	-	ns
Time from HOLDB to Output High-Z	t <sub>HOZ</sub>	-	-	40	-	-	40	ns
Time from HOLDB to Output change	t <sub>HPD</sub>	-	-	40	-	-	40	ns
SCK Rise Time (Note1)	t <sub>RC</sub>	-	-	2	-	-	2	μs
SCK Fall Time (Note1)	t <sub>FC</sub>	-	-	2	-	-	2	μs
OUTPUT Rise Time (Note1)	t <sub>RO</sub>	-	-	40	-	-	40	ns
OUTPUT Fall Time (Note1)	t <sub>FO</sub>	-	-	40	-	-	40	ns
Write Cycle Time	t <sub>EW</sub>	-	-	5	-	-	5	ms

(Note1) NOT 100% TESTED

## AC Timing Characteristics Conditions

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Load Capacity	CL	-	-	30	pF	2.5V≤Vcc<4.0V
		-	-	50	pF	4.0V≤Vcc≤5.5V
Input Voltage	-	0.2Vcc/0.8Vcc			V	
Input / Output Judgment Voltage	-	0.3Vcc/0.7Vcc			V	

## Serial Input / Output Timing

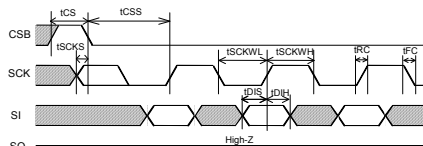


Figure 2-(a). Input timing

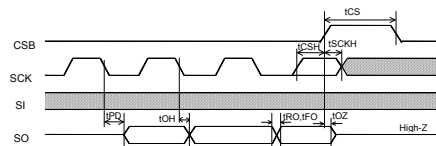


Figure 2-(b). Input / Output timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the most significant bit MSB.

SO is output in sync with data fall edge of SCK. Data is output from the most significant bit MSB.

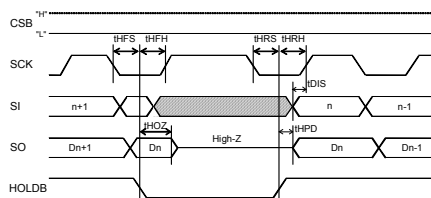


Figure 2-(c). HOLD timing

## Block Diagram

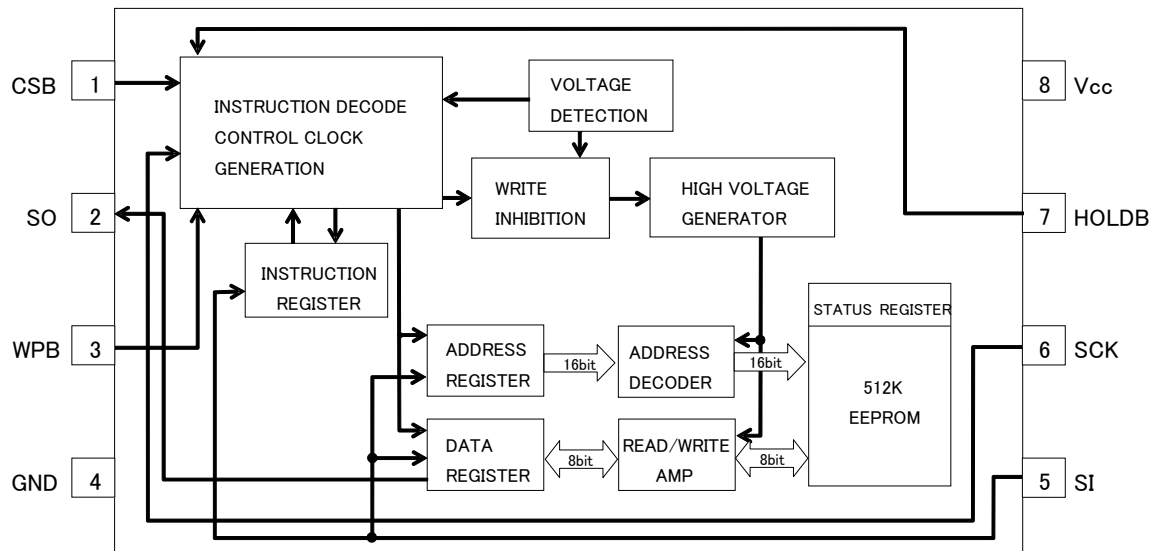


Figure 3. Block Diagram

## Pin Configuration

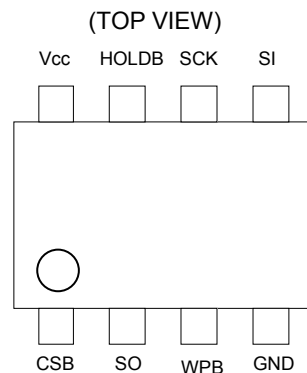


Figure 4. Pin Configuration

## Pin Descriptions

Terminal name	Input /Output	Function
Vcc	-	Power source to be connected
GND	-	All input / output reference voltage, 0V
CSB	Input	Chip select input
SCK	Input	Serial clock input
SI	Input	Op code, address, and serial data input
SO	Output	Serial data output
HOLDB	Input	Hold input Command communications may be suspended temporarily (HOLD status)
WPB	Input	Write protect input Write status register command is prohibited

**Typical Performance Curves**

(The following characteristic data are Typ Values.)

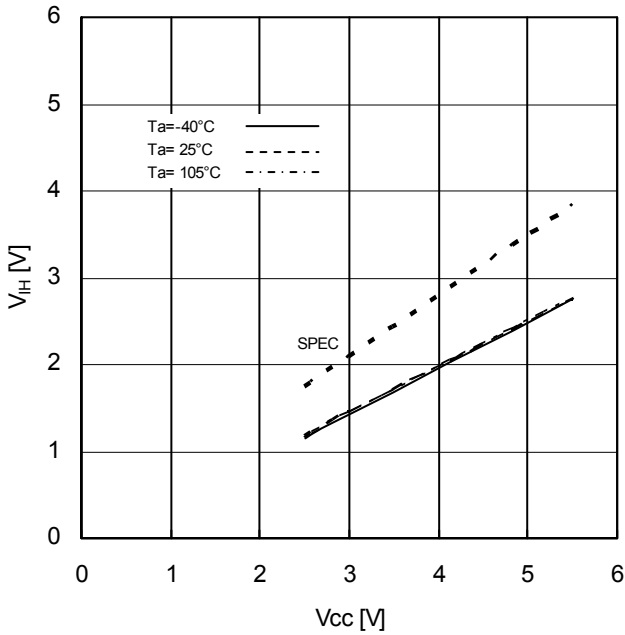


Figure 5. Input High Voltage vs Supply Voltage (CSB,SCK,SI,HOLDB,WPB)

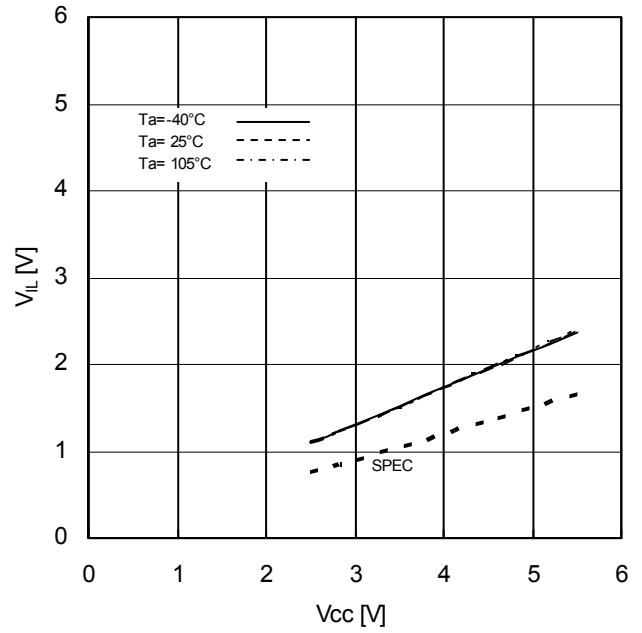


Figure 6. Input Low Voltage vs Supply Voltage (CSB,SCK,SI,HOLDB,WPB)

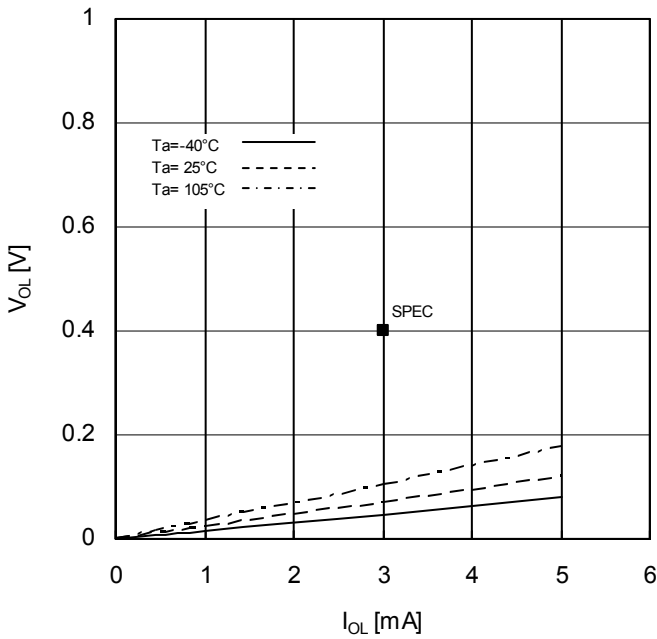


Figure 7. Output Low Voltage vs Output Current (Vcc=2.5V)

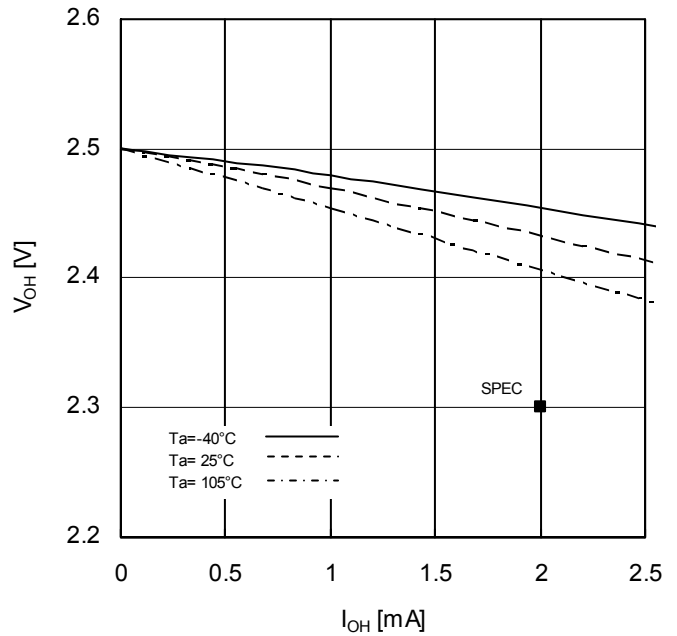


Figure 8. Output High Voltage vs Output Current (Vcc=2.5V)



Typical Performance Curves - Continued

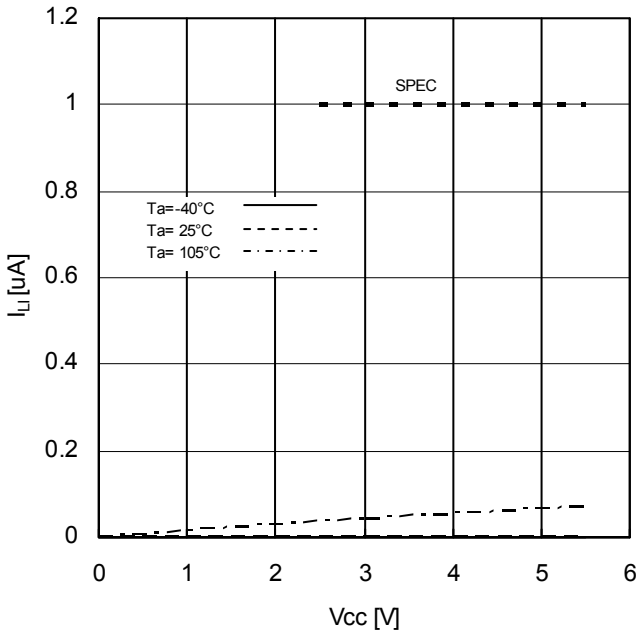


Figure 9. Input Leakage Current vs Supply Voltage (CSB,SCK,SI,HOLDB,WPB)

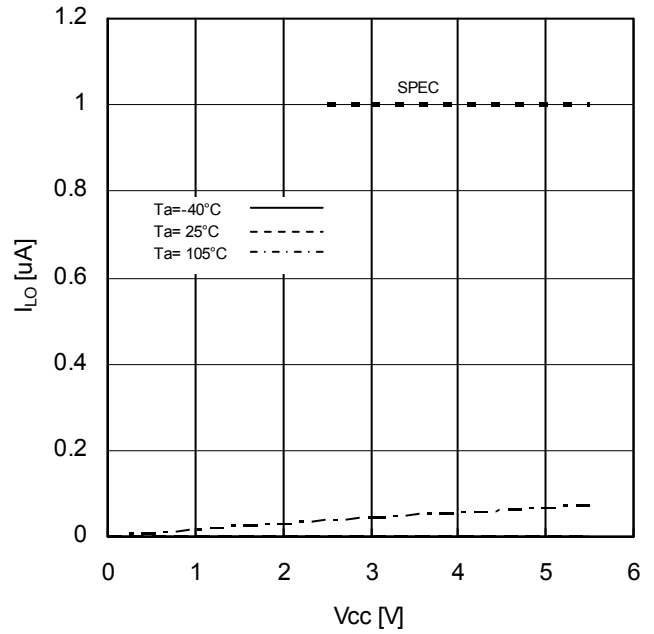


Figure 10. Output Leakage Current vs Supply Voltage (SO)

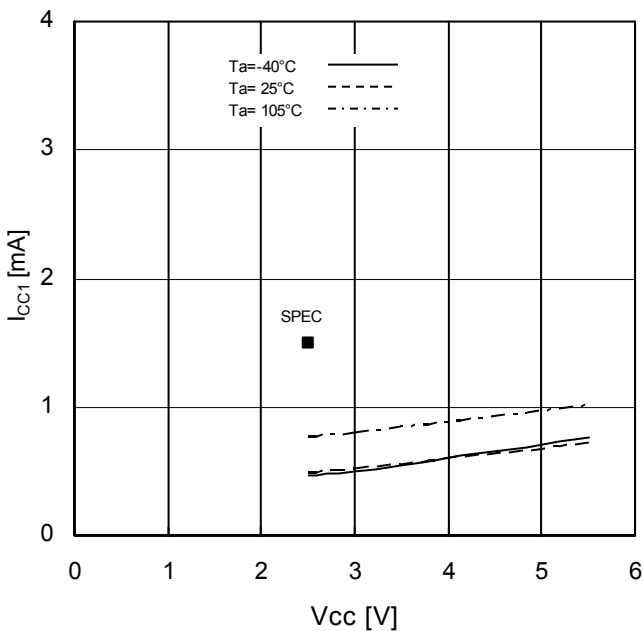


Figure 11. Supply Current (Write) vs Supply Voltage (fSCK=5MHz)

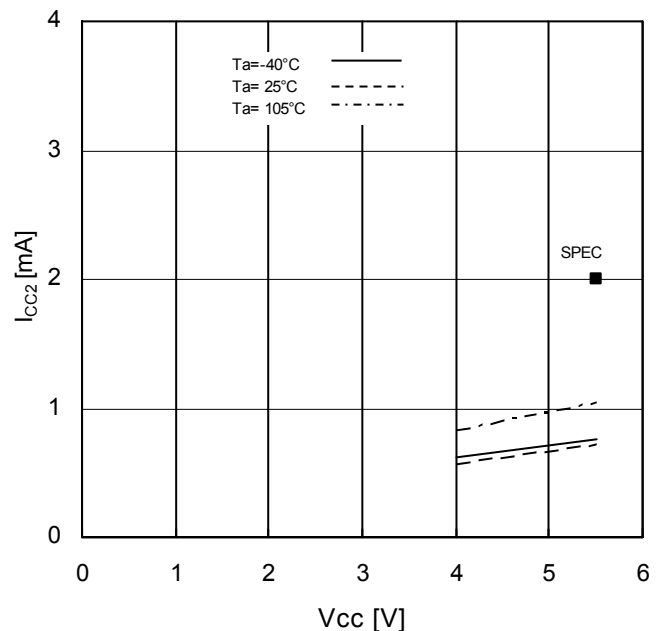


Figure 12. Supply Current (Write) vs Supply Voltage (fSCK=10MHz)

Typical Performance Curves - Continued

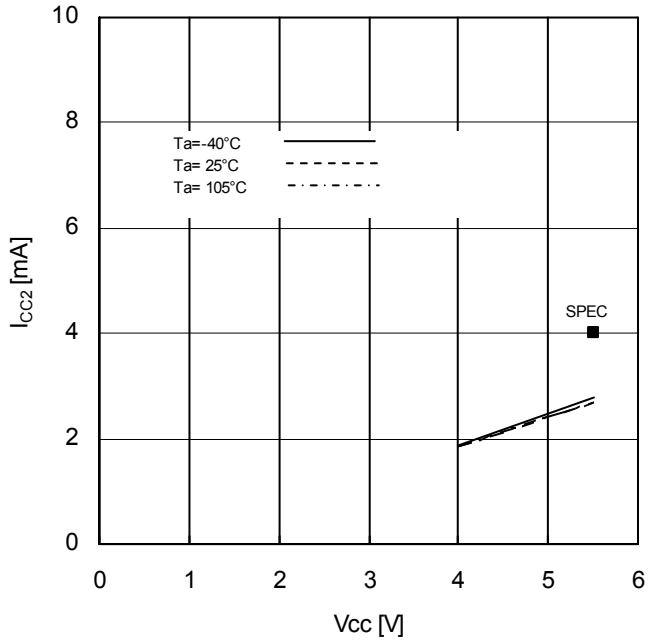


Figure 13. Supply Current (Read) vs Supply Voltage (fSCK=10MHz)

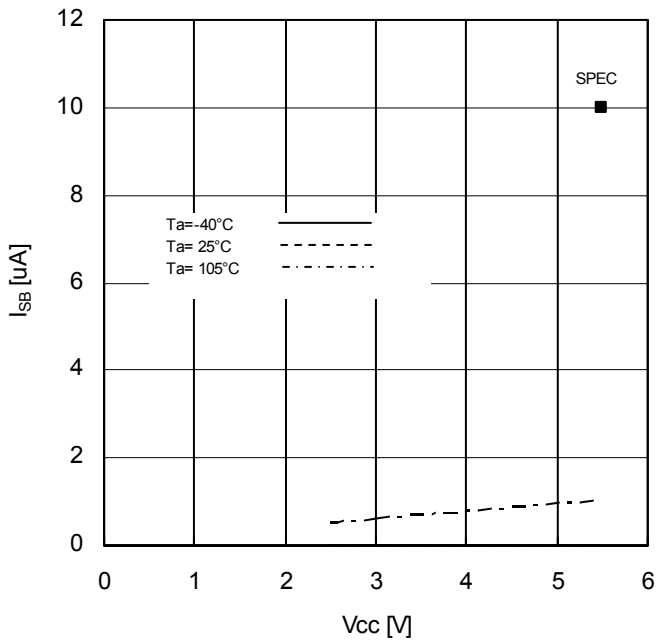


Figure 14. Standby Current vs Supply Voltage

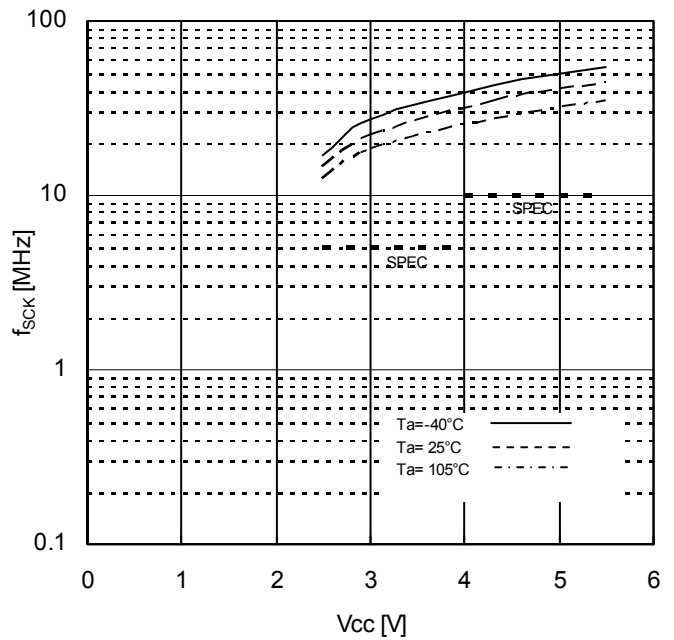


Figure 15. SCK Frequency vs Supply Voltage



Typical Performance Curves - Continued

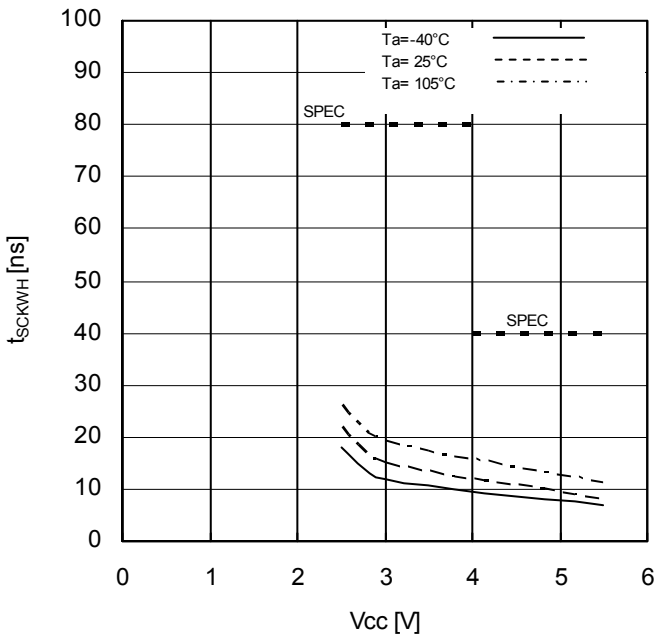


Figure 16. SCK High Time vs Supply Voltage

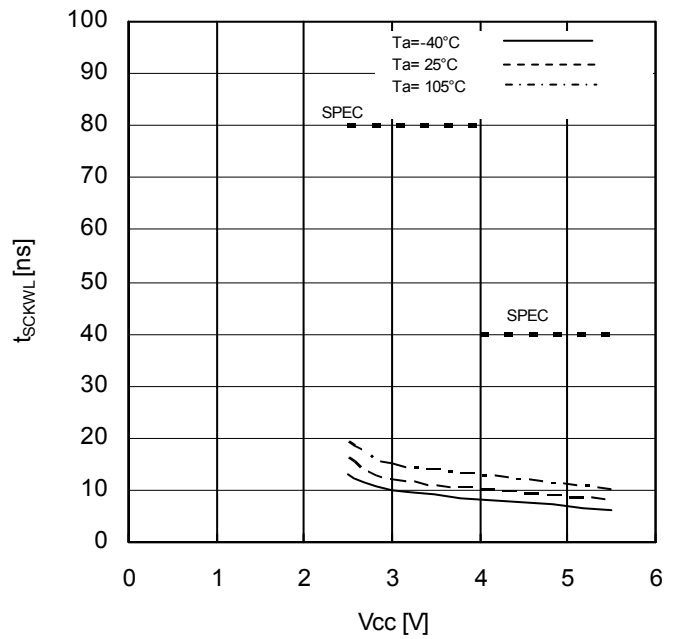


Figure 17. SCK Low Time vs Supply Voltage

Typical Performance Curves - Continued

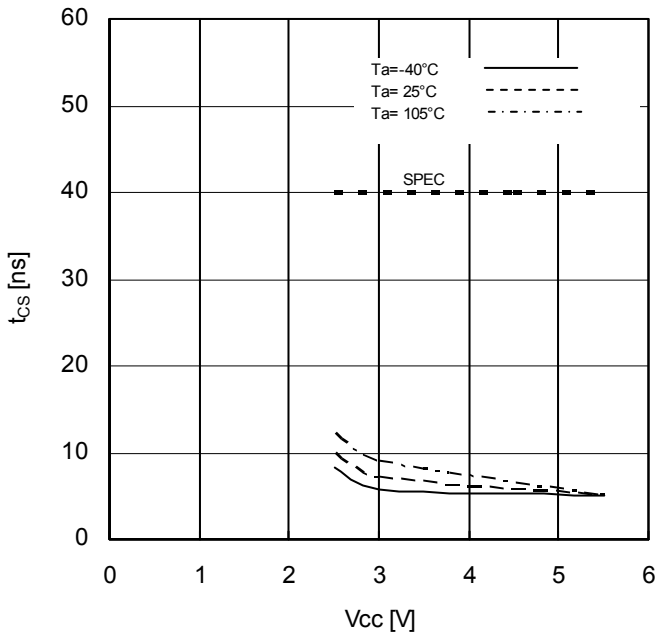


Figure 18. CSB High Time vs Supply Voltage

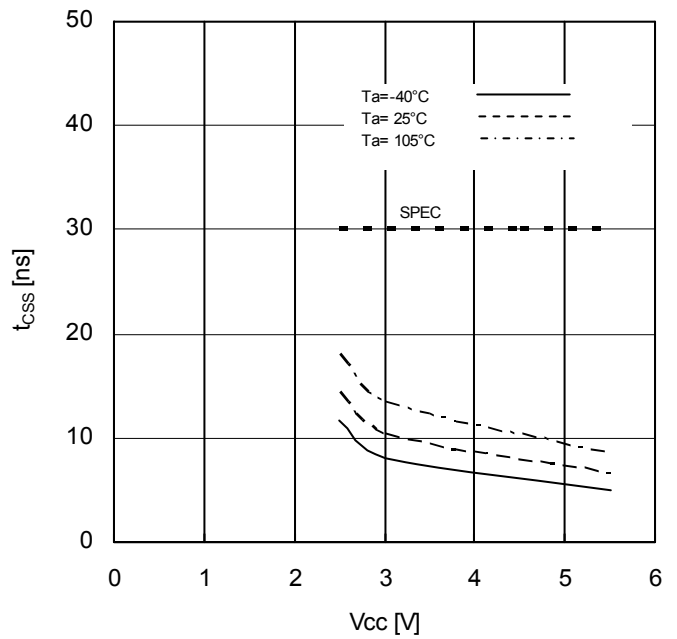


Figure 19. CSB Setup Time vs Supply Voltage

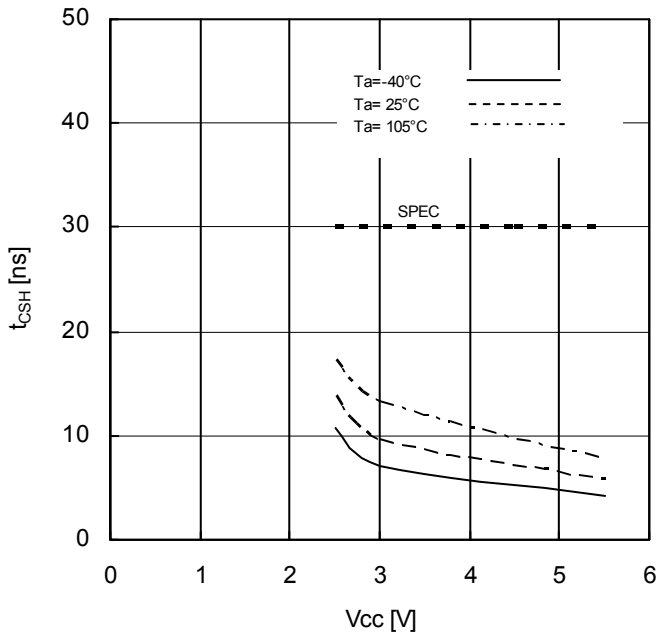


Figure 20. CSB Hold Time vs Supply Voltage

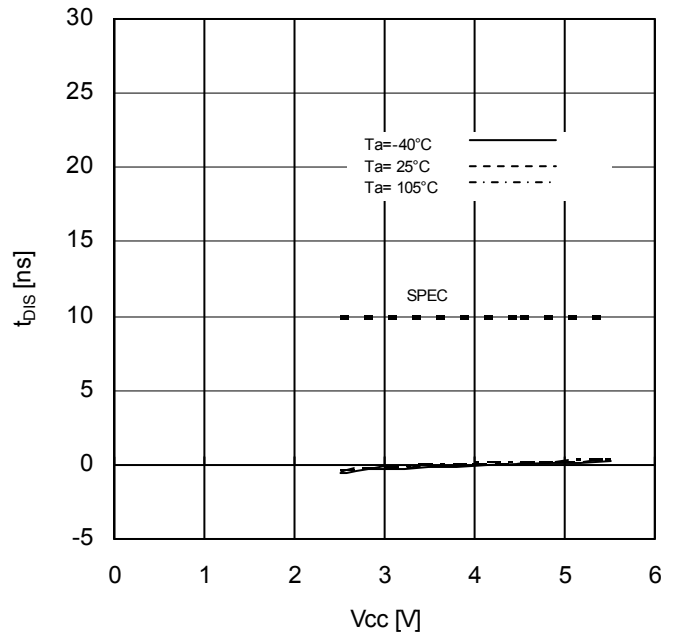


Figure 21. SI Setup Time vs Supply Voltage

Typical Performance Curves - Continued

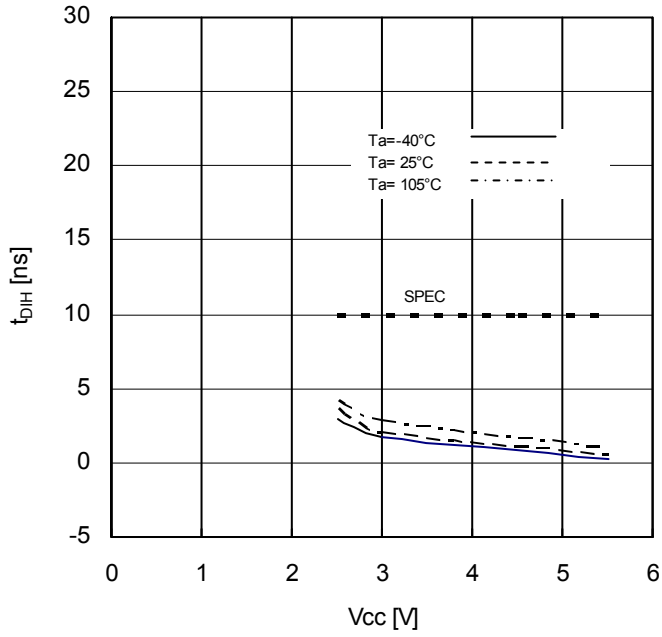


Figure 22. SI Hold Time vs Supply Voltage

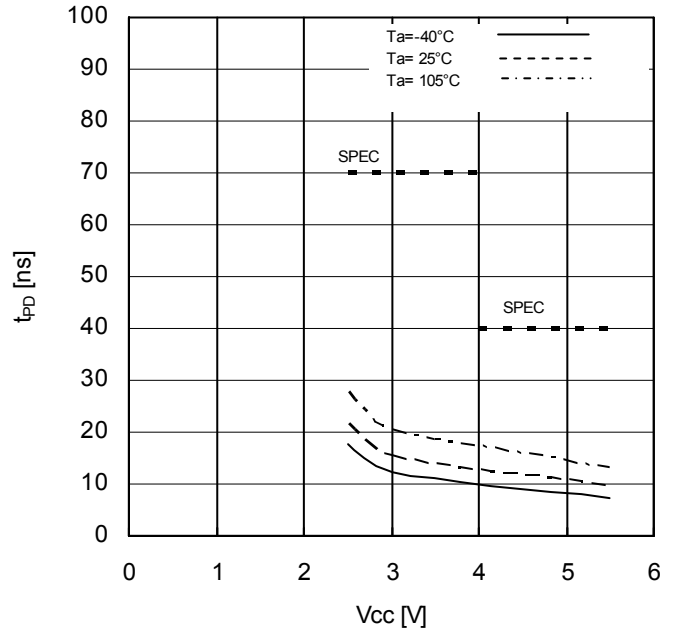


Figure 23. Data Output Delay Time vs Supply Voltage

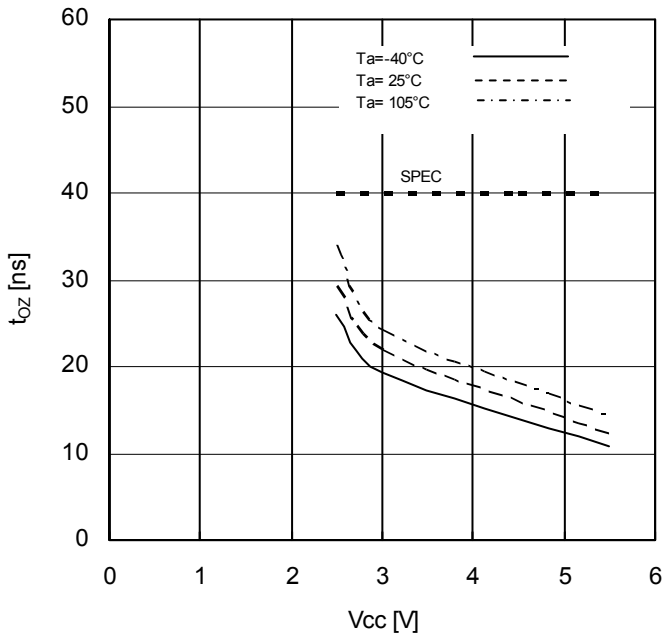


Figure 24. Output Disable Time vs Supply Voltage

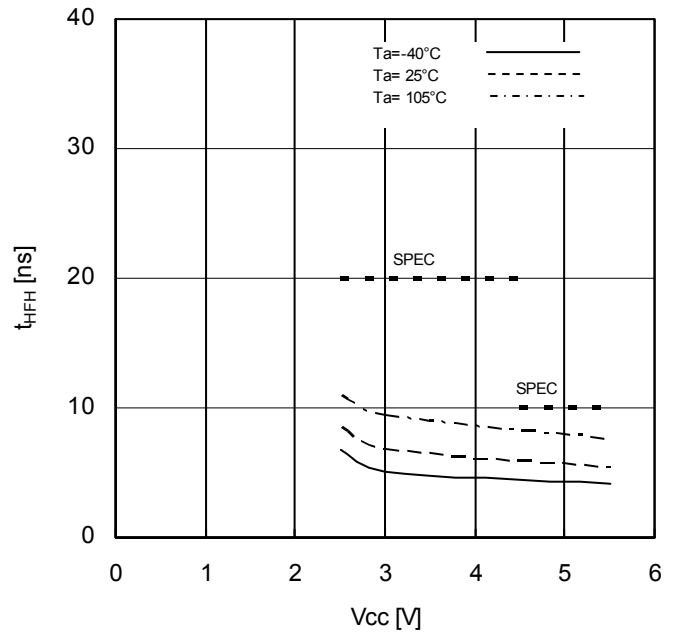


Figure 25. HOLDB Setting Hold Time vs Supply Voltage

Typical Performance Curves - Continued

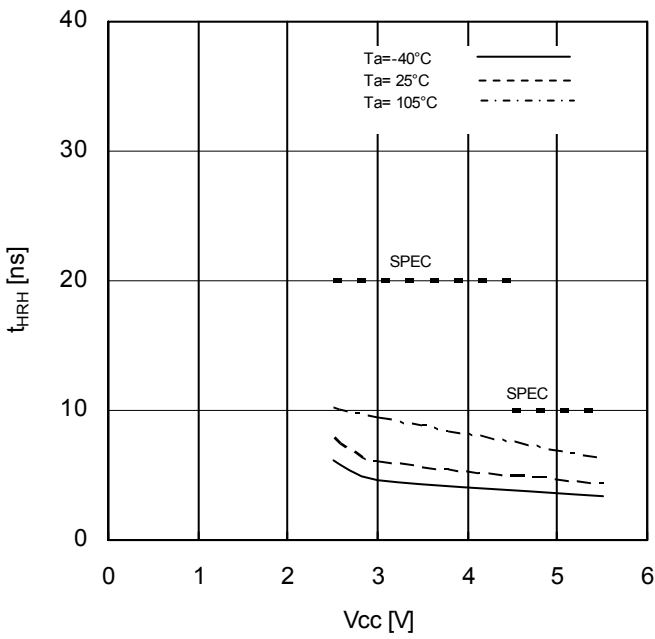


Figure 26. HOLDB Release Hold Time vs Supply Voltage

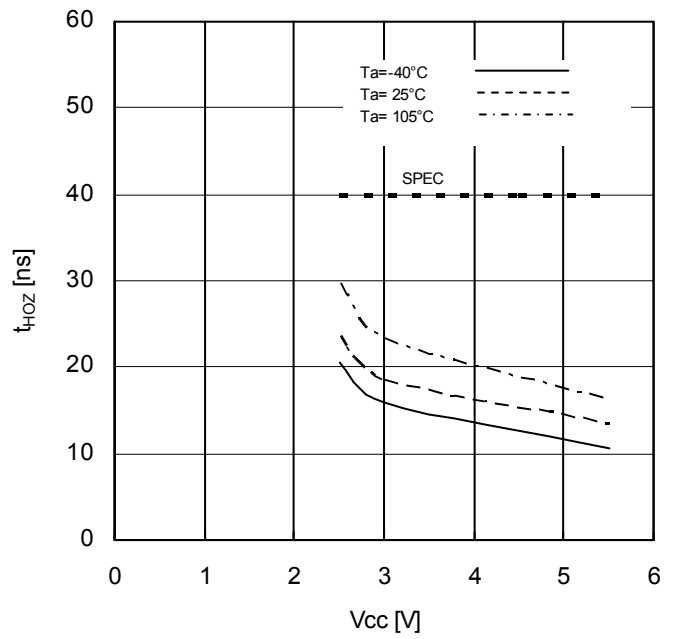


Figure 27. Time from HOLDB to Output High-Z vs Supply Voltage

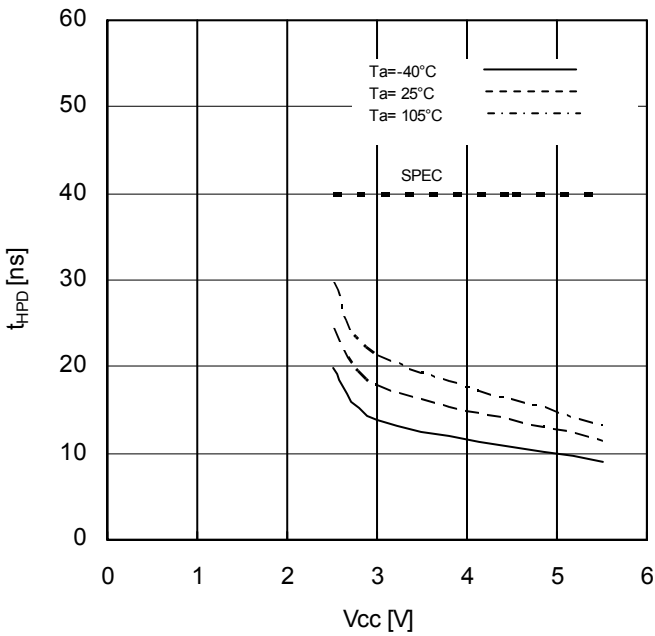


Figure 28. Time from HOLDB to Output change vs Supply Voltage

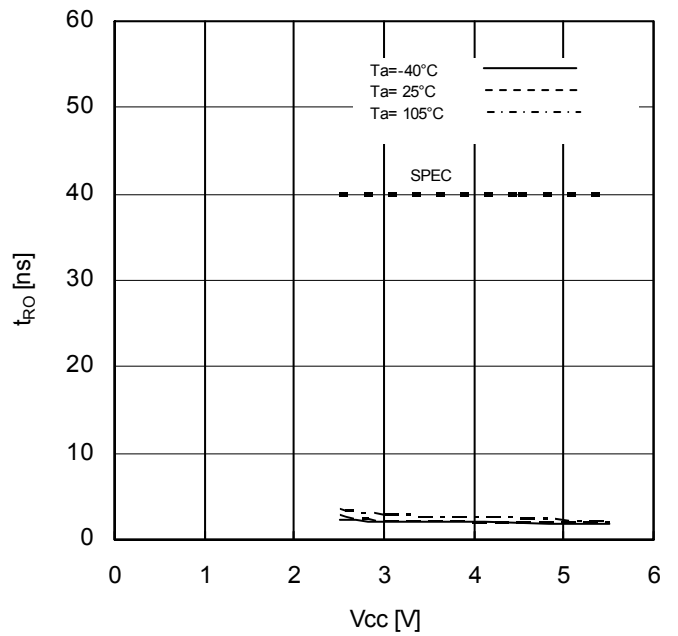


Figure 29. OUTPUT Rise Time vs Supply Voltage

## Typical Performance Curves - Continued

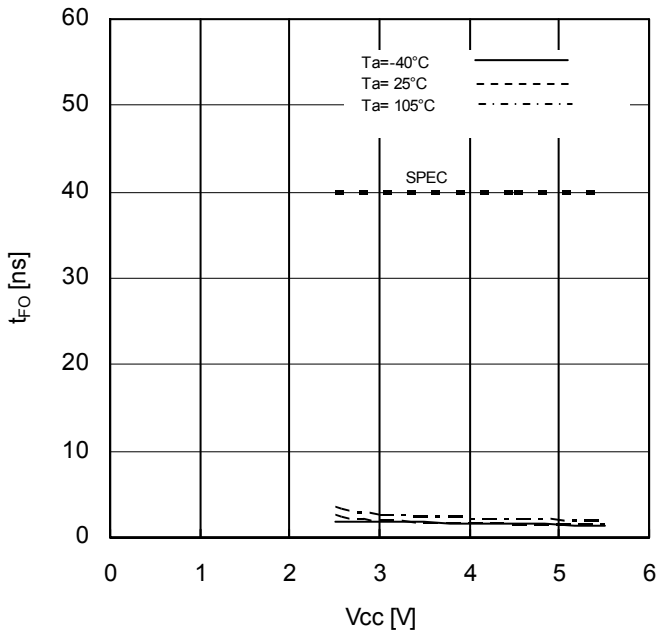


Figure 30. OUTPUT Fall Time vs Supply Voltage

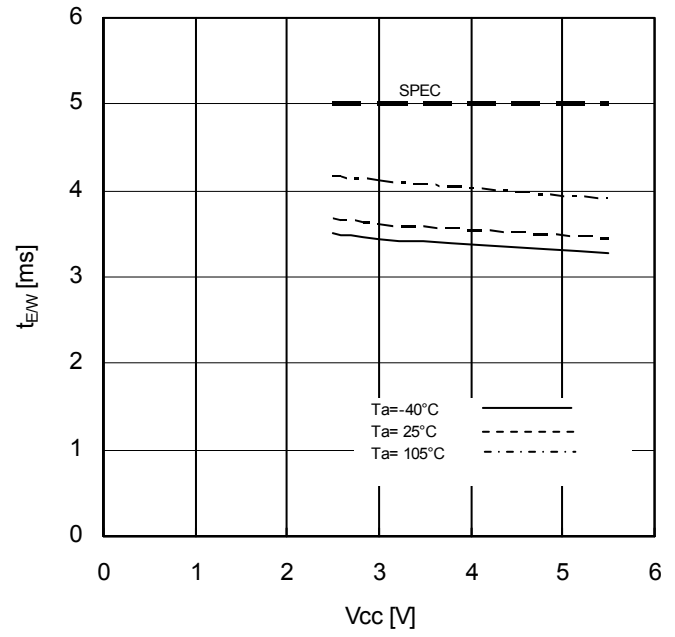


Figure 31. Write Cycle Time vs Supply Voltage

## Features

### 1. Status Registers

This IC has status register. The status register expresses the following parameters of 8 bits.

BP0 and BP1 can be set by write status register command. These 2 bits are memorized into the EEPROM, therefore are valid even when power source is turned off.

Rewrite characteristics and data hold time are same as characteristics of the EEPROM.

WEN can be set by write enable command and write disable command. WEN becomes write disable status when power source is turned off. R/B is for write confirmation, therefore cannot be set externally.

The value of status register can be read by read status register command.

#### (1) Contexture of Status Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WPEN	0	0	0	BP1	BP0	WEN	$\bar{R}/B$

bit	Memory location	Function
WPEN	EEPROM	WPB pin enable / disable designation bit WPEN=0=invalid WPEN=1=valid
BP1 BP0	EEPROM	EEPROM write disable block designation bit
WEN	registers	Write and write status register write enable / disable status confirmation bit WEN=0=prohibited WEN=1=permitted
$\bar{R}/B$	registers	Write cycle status (READY / BUSY) status confirmation bit $\bar{R}/B=0=READY$ $\bar{R}/B=1=BUSY$

#### (2) Write Disable Block Setting

BP1	BP0	Write disable block
0	0	None
0	1	C000h-FFFFh
1	0	8000h-FFFFh
1	1	0000h-FFFFh

### 2. WPB Pin

By setting WPB=LOW, write command is prohibited. And the write command to be disabled at this moment is WRSR. However, when write cycle is in execution, no interruption can be made.

WRSR	WRITE
Prohibition possible but WPEN bit "1"	Prohibition impossible

### 3. HOLDB Pin

By HOLDB pin, data transfer can be interrupted. When SCK="0", by making HOLDB from "1" into "0", data transfer to EEPROM is interrupted. When SCK = "0", by making HOLDB from "0" into "1", data transfer is restarted.

## Command Mode

Command	Contents	Ope code	
WREN	Write Enable Command	0000	0110
WRDI	Write Disable Command	0000	0100
READ	Read Command	0000	0011
WRITE	Write Command	0000	0010
RDSR	Read Status Register Command	0000	0101
WRSR	Write Status Register Command	0000	0001

## Timing Chart

### 1. Write Enable (WREN) / Disable (WRDI) Command

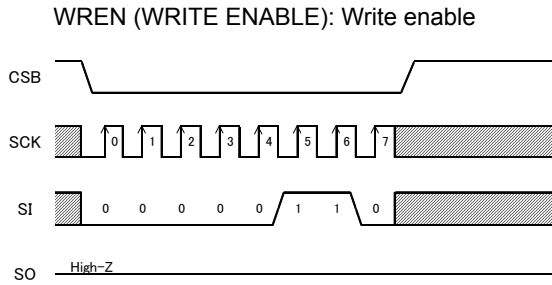


Figure 32. Write enable command

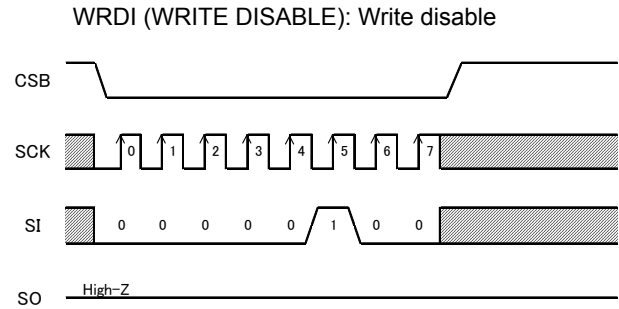


Figure 33. Write disable command

This IC has write enable status and write disable status. It is set to write enable status by write enable command, and it is set to write disable status by write disable command. As for these commands, set CSB LOW, and then input the respective commands. The respective commands are accepted at the 7-th clock rise. Even with input over 7 clocks, command becomes valid.

When to carry out write command, it is necessary to set write enable status by the write enable command. If write command is input in the write disable status, the command is cancelled. And even in the write enable status, once write command is executed, it gets in the write disable status. After power on, this IC is in write disable status.

### 2. Read Command (READ)

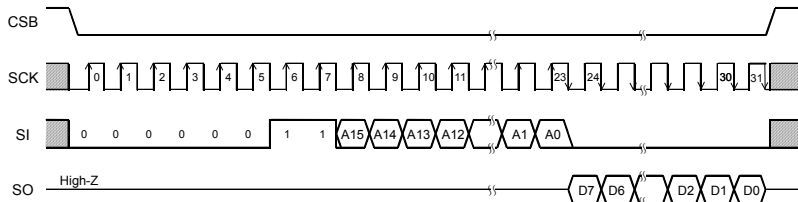


Figure 34. Read command

By read command, data of EEPROM can be read. As for this command, set CSB LOW, then input address after read ope code. EEPROM starts data output of the designated address. Data output is started from SCK fall of 23-th clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM. After reading data of the most significant address, by continuing increment read, data of the most insignificant address is read.



3. Write Command (WRITE)

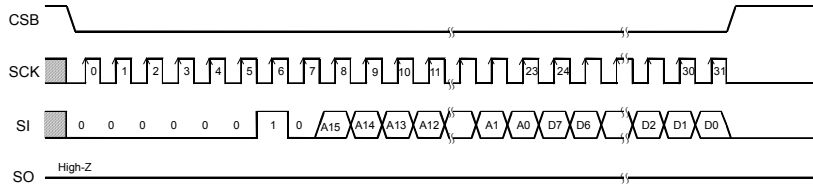


Figure 35. Write command

By write command, data of EEPROM can be written. As for this command, set CSB LOW, then input address and data after write ope code. Then, by making CSB HIGH, the EEPROM starts writing. The write time of EEPROM requires time of  $t_{EW}$  (Max 5ms). During  $t_{EW}$ , other than read status register command is not accepted. Set CSB HIGH between taking the last data (D0) and rising the next SCK clock. At the other timing, write command is not executed, and this write command is cancelled. This IC has page write function, and after input of data for 1 byte (8 bits), by continuing data input without setting CSB HIGH, 2byte or more data can be written for one  $t_{EW}$ . Up to 128 arbitrary bytes can be written. In page write, the insignificant 7 bit of the designated address is incremented internally at every time when data of 1 byte is input and data is written to respective addresses. When data of the maximum bytes or higher is input, address rolls over, and previously input data is overwritten.

4. Write Status Register, Read Status Register Command (WRSR/RDSR)

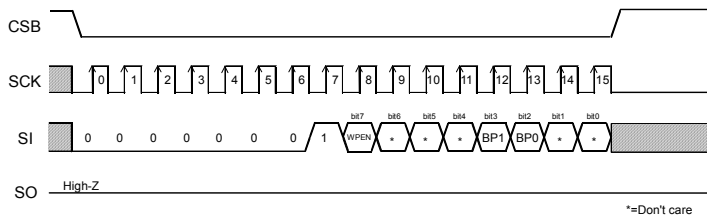


Figure 36. Write status register

Write status register command can write data of status register. The data can be written by this command are 3 bits, that is, WPEN (bit7), BP1 (bit3) and BP0 (bit2) among 8 bits of status register. By BP1 and BP0, write disable block of EEPROM can be set. As for this command, set CSB LOW, and input ope code of write status register, and input data. Then, by making CSB HIGH, EEPROM starts writing. Write time requires time of  $t_{EW}$  as same as write. As for CSB rise, set CSB HIGH between taking the last data bit (bit0) and the next SCK clock rising. At the other timing, command is cancelled. Write disable block is determined by BP1 BP0, and the block can be selected from 1/4, 1/2, and entire of memory array (Refer to the write disable block setting table.). To the write disabled block, write cannot be made, and only read can be made.

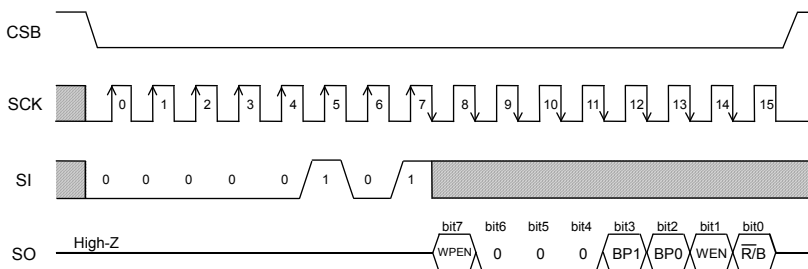


Figure 37. Read status register command

### WPB Cancel Valid Area

WPB is normally fixed to "H" or "L" for use, but when WPB is controlled so as to cancel write status register command, pay attention to the following WPB valid timing.

While write status register command is executed, by setting WPB = "L" in cancel valid area, command can be cancelled. The area from command ope code to CSB rise at internal automatic write start becomes the cancel valid area. However, once write is started, by any input write cycle cannot be cancelled. WPB input becomes Don't Care, and cancellation becomes invalid.

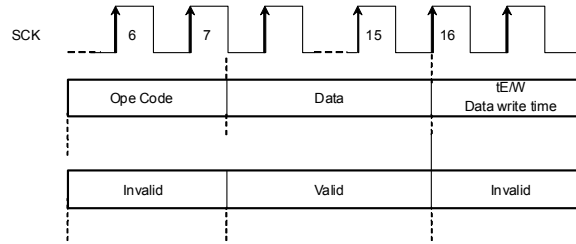


Figure 38. WPB valid timing (At inputting WRSR command)

### HOLDB Pin

By HOLDB pin, command communication can be stopped temporarily (HOLD status). The command communications are carried out when the HOLDB pin is HIGH. To get in HOLD status, at command communication, when SCK=LOW, set the HOLDB pin LOW. At HOLD status, SCK and SI become Don't Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the HOLDB pin HIGH when SCK=LOW. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at read, after release of HOLD status, by starting A4 address input, read can be restarted. When in HOLD status, keep CSB LOW. When it is set CSB=HIGH in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

**Method to Cancel Each Command**

**1. READ, RDSR**

• Method to cancel : cancel by CSB = "H".

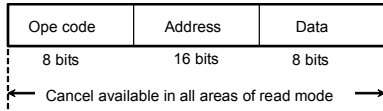


Figure 39. READ cancel valid timing

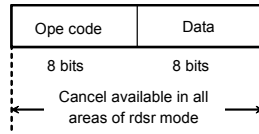


Figure 40. RDSR cancel valid timing

**2. WRITE, PAGE WRITE**

- a : Ope code or address input area  
Cancellation is available by CSB="H".
- b : Data input area (D7 to D1 input area)  
Cancellation is available by CSB="H".
- c : Data input area (D0 area)  
In this area, cancellation is not available.  
When CSB is set HIGH, write starts.
- d :  $t_{E/W}$  area  
In the area c, by rising CSB, write starts.  
While writing, by any input, cancellation cannot be made.

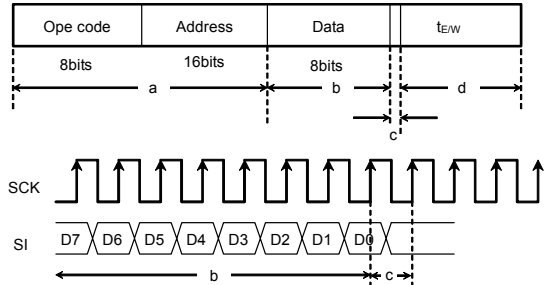


Figure 41. WRITE cancel valid timing

Note1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.  
 Note2) If CSB is risen at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to rise in SCK = "L" area. As for SCK rise, assure timing of  $t_{CSS}$  /  $t_{CSH}$  or more.

**3. WRSR**

- a : From ope code to 15-th clock rise  
Cancellation is available by CSB="H".
- b : From 15-th clock rise to 16-th clock rise (write enable area)  
In this area, cancellation is not available by CSB="H".  
When CSB is set HIGH, write starts using CSB.
- c : After 16-th clock rise.  
Cancellation is available by CSB="H".  
However, if write starts (CSB is risen)  
In the area b, cancellation cannot be made by any means.  
And, by inputting on SCK clock, cancellation cannot be made.

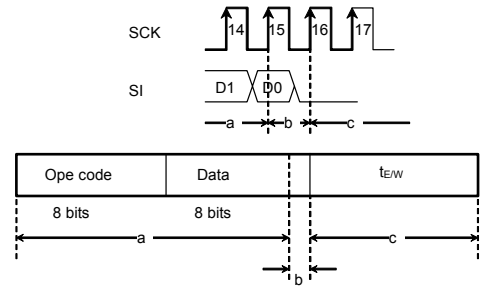


Figure 42. WRSR cancel valid timing

Note1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again  
 Note2) If CSB is risen at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to rise in SCK = "L" area. As for SCK rise, assure timing of  $t_{CSS}$  /  $t_{CSH}$  or more.

**4. WREN/WRDI**

- a : From ope code to 7-th clock rise, cancellation is available by CSB = "H".
- b : Cancellation is not available 7-th clock.

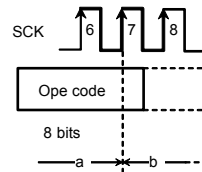


Figure 43. WREN/WRDI cancel valid timing

## I/O Peripheral Circuits

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

Input pin pull up, pull down resistance

When to attach pull up, pull down resistance to EEPROM input pin, select an appropriate value for the microcontroller  $V_{OL}$ ,  $I_{OL}$  with considering  $V_{IL}$  characteristics of this IC.

### 1. Pull Up Resistance

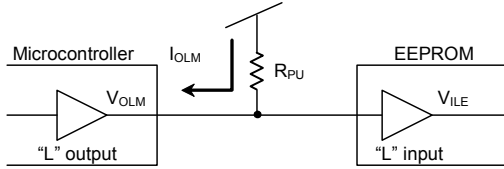


Figure 44. Pull up resistance

$$R_{PU} \geq \frac{V_{CC} - V_{OLM}}{I_{OLM}} \dots \textcircled{1}$$

$$V_{OLM} \leq V_{ILM} \dots \textcircled{2}$$

Example) When  $V_{CC}=5V$ ,  $V_{ILE}=1.5V$ ,  $V_{OLM}=0.4V$ ,  $I_{OLM}=2mA$ , from the equation  $\textcircled{1}$ ,

$$R_{PU} \geq \frac{5 - 0.4}{2 \times 10^{-3}}$$

$$\therefore R_{PU} \geq 2.3[k\Omega]$$

With the value of  $R_{PU}$  to satisfy the above equation,  $V_{OLM}$  becomes 0.4V or lower, and with  $V_{ILE} (=1.5V)$ , the equation  $\textcircled{2}$  is also satisfied.

- $V_{ILE}$  :EEPROM  $V_{IL}$  specifications
- $V_{OLM}$  :Microcontroller  $V_{OL}$  specifications
- $I_{OLM}$  :Microcontroller  $I_{OL}$  specifications

And, in order to prevent malfunction or erroneous write at power ON/OFF, be sure to make CSB pull up.

### 2. Pull Down Resistance

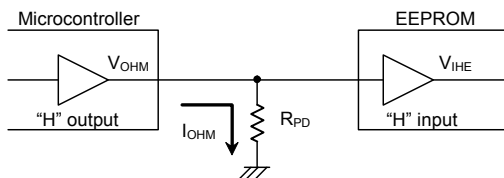


Figure 45. Pull down resistance

$$R_{PD} \geq \frac{V_{OHM}}{I_{OHM}} \dots \textcircled{3}$$

$$V_{OLM} \leq V_{IHM} \dots \textcircled{4}$$

Example) When  $V_{CC}=5V$ ,  $V_{OHM}=V_{CC}-0.5V$ ,  $I_{OHM}=0.4mA$ ,  $V_{IHE}=V_{CC} \times 0.7V$ , from the equation  $\textcircled{3}$ ,

$$R_{PD} \geq \frac{5 - 0.5}{0.4 \times 10^{-3}}$$

$$\therefore R_{PD} \geq 11.3[k\Omega]$$

Further, by amplitude  $V_{IHE}$ ,  $V_{ILE}$  of signal input to EEPROM, operation speed changes. By inputting  $V_{CC}/GND$  level amplitude of signal, more stable high speed operations can be realized. On the contrary, when amplitude of  $0.8V_{CC} / 0.2V_{CC}$  is input, operation speed becomes slow. (Note1)

In order to realize more stable high speed operation, it is recommended to make the values of  $R_{PU}$ ,  $R_{PD}$  as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of  $V_{CC} / GND$  level. (Note1) In this case, guaranteed value of operating timing is guaranteed.

### 3. SO Load Capacity Condition

Load capacity of SO output pin affects upon delay characteristic of SO output (Data output delay time, time from HOLDB to High-Z, Output rise time, Output fall time.). In order to make output delay characteristic into better, make SO load capacity small.

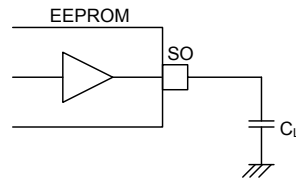


Figure 46. SO load capacity

### 4. Other cautions

Make the each wire length from the microcontroller to EEPROM input pin same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.

## I/O Equivalence Circuit

### 1. Output Circuit

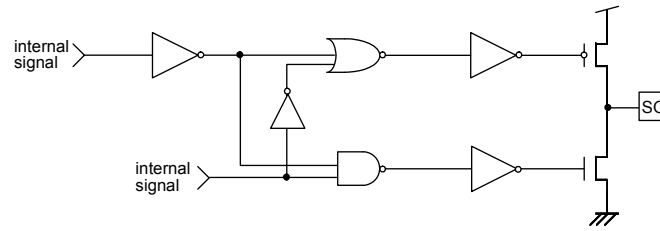


Figure 47. SO output equivalent circuit

### 2. Input Circuit

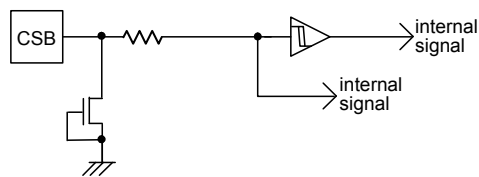


Figure 48. CSB input equivalent circuit

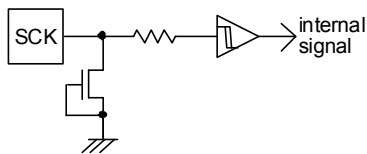


Figure 49. SCK input equivalent circuit

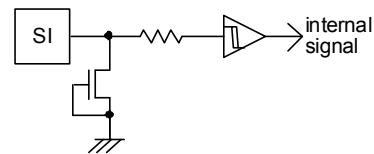


Figure 50. SI input equivalent circuit

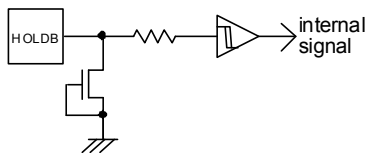


Figure 51. HOLDB input equivalent circuit

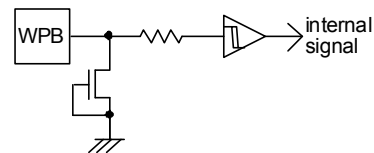


Figure 52. WPB input equivalent circuit

## Power-Up/Down Conditions

### 1. At Standby

Set CSB "H", and be sure to set SCK, SI input "L" or "H". Do not input intermediate electric potential.

### 2. At Power ON/OFF

When  $V_{cc}$  rise or fall, set CSB="H" (=V<sub>cc</sub>).

When CSB is "L", this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, erroneous write or so. To prevent these, at power ON, set CSB "H". (When CSB is in "H" status, all inputs are canceled.)

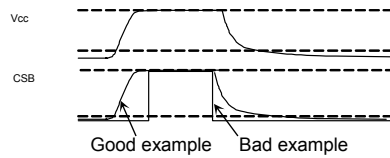


Figure 53. CSB timing at power ON/OFF

(Good example) CSB terminal is pulled up to  $V_{cc}$ .

At power OFF, take 10ms or more before supply. If power is turned on without observing this condition, the IC internal circuit may not be reset.

(Bad example) CSB terminal is "L" at power ON/OFF.

In this case, CSB always becomes "L" (active status), and EEPROM may have malfunction or erroneous write owing to noises and the likes.

Even when CSB input is High-Z, the status becomes like this case.

### 3. Operating Timing after Power ON

As shown in Figure 54, at standby, when SCK is "H", even if CSB is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB "H" status.

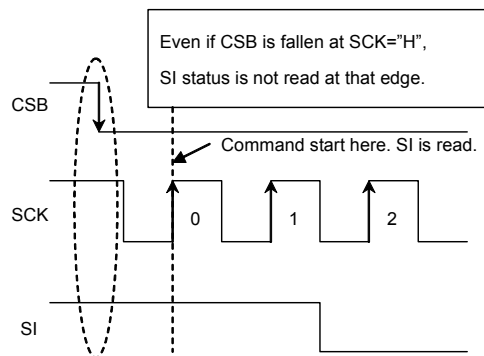


Figure 54. Operating timing

### 4. At Power on Malfunction Preventing Function

This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following  $t_R$ ,  $t_{OFF}$ , and  $V_{bot}$  are not satisfied, it may become write enable status owing to noises and the likes.

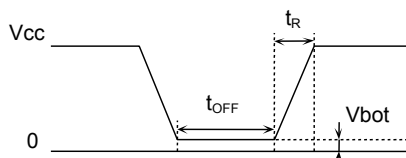


Figure 55. Rise waveform

Recommended conditions of  $t_R$ ,  $t_{OFF}$ ,  $V_{bot}$

$t_R$	$t_{OFF}$	$V_{bot}$
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

### 5. Low Voltage Malfunction Preventing Function

LVCC (V<sub>cc</sub>-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.

At LVCC voltage (Typ = 1.2V) or below, it prevent data rewrite.

## Noise Countermeasures

### 1. Vcc Noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1 $\mu$ F) between IC Vcc and GND. At that time, attach it as close to IC as possible.

And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

### 2. SCK Noise

When the rise time of SCK ( $t_{RC}$ ) is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SCK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time of SCK ( $t_{RC}$ ) 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

### 3. WPB Noise

During execution of write status register command, if there exist noises on WPB pin, mistake in recognition may occur and forcible cancellation may result. To avoid this, a Schmitt trigger circuit is built in WPB input. In the same manner, a Schmitt trigger circuit is built in CSB input, SI input and HOLDB input too.



## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

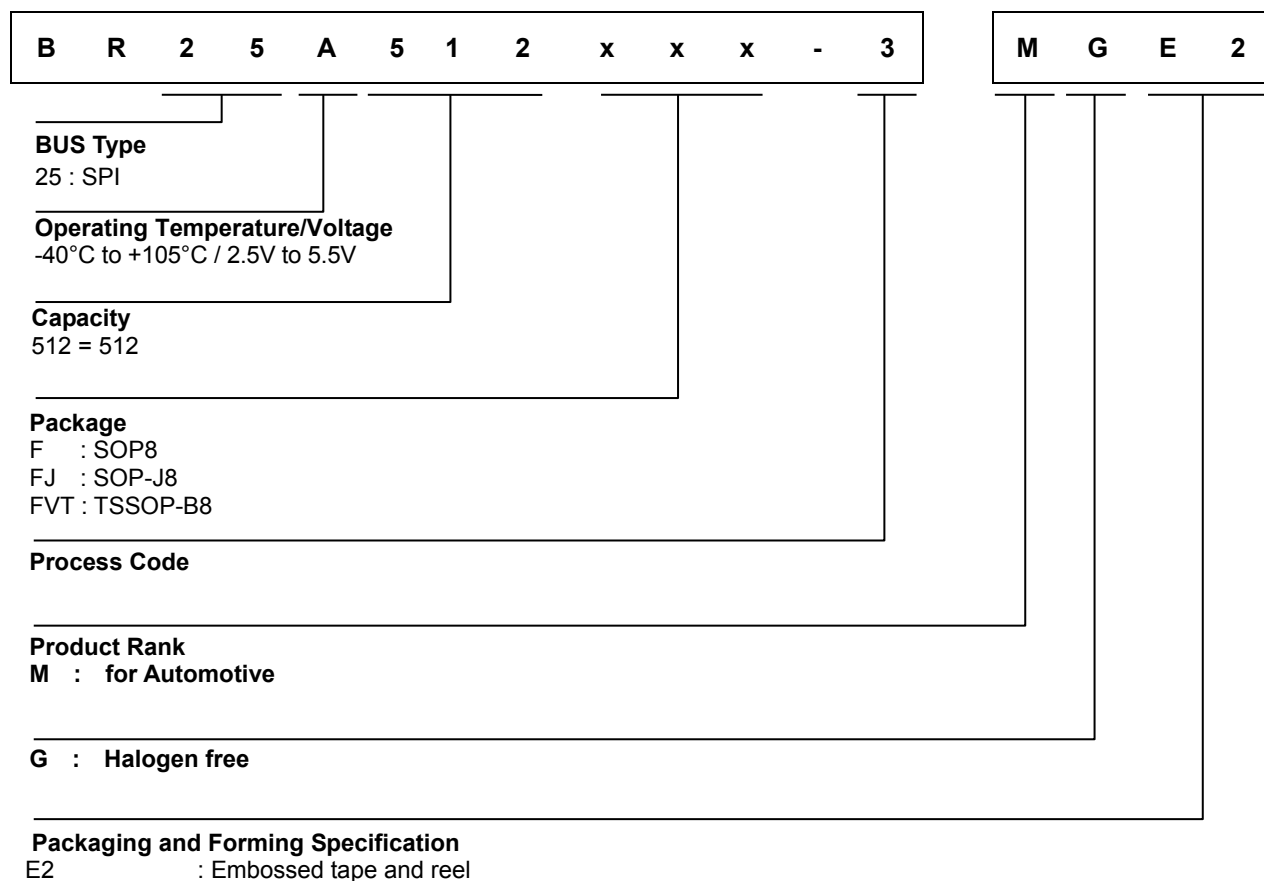
**Operational Notes – continued****11. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

**12. Regarding the Input Pin of the IC**

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

**Ordering Information**

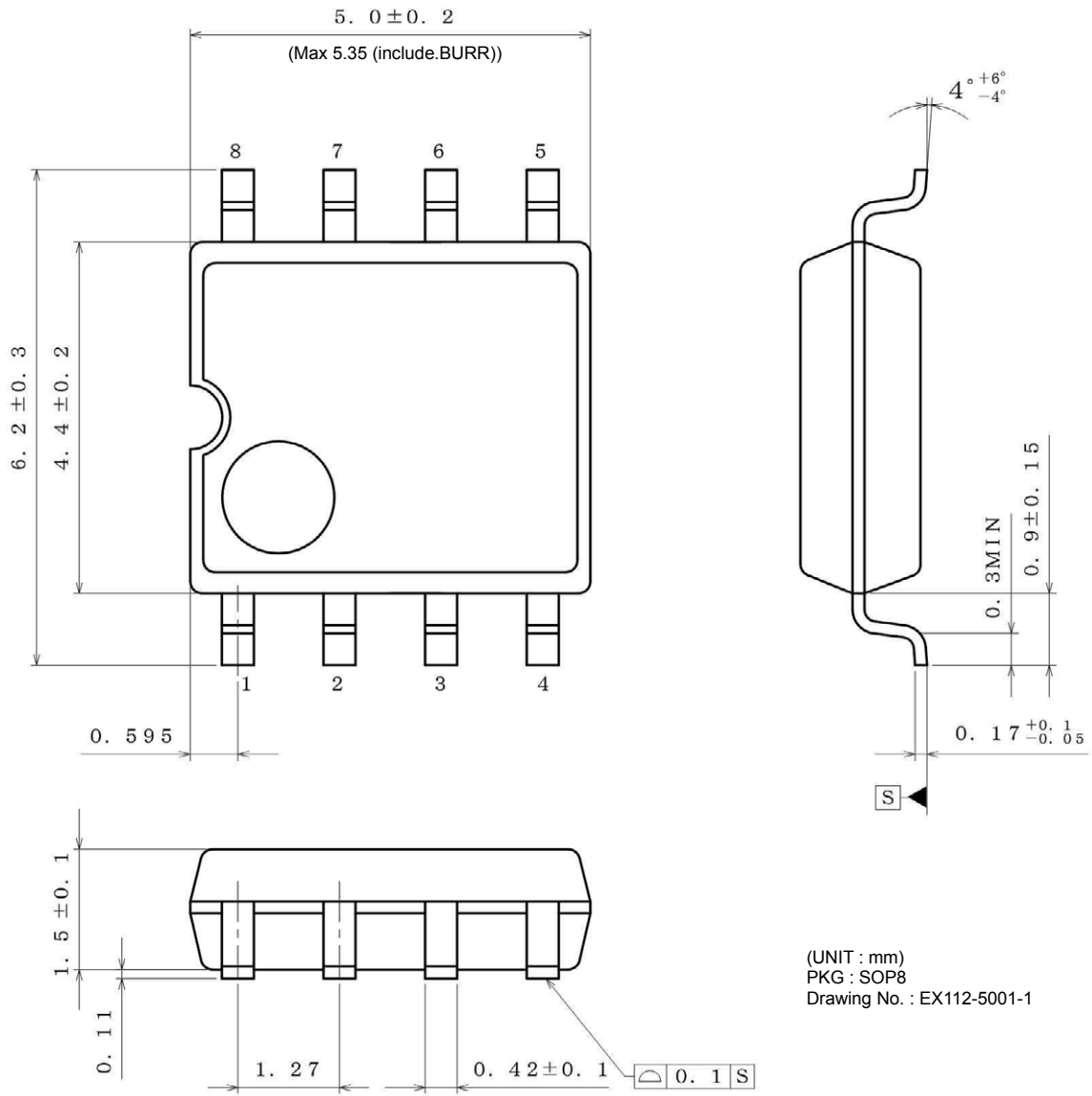


**Lineup**

Capacity	Package		Orderable Part Number
	Type	Quantity	
512K	SOP8	Reel of 2500	BR25A512F -3MGE2
	SOP-J8		BR25A512FJ -3MGE2
	TSSOP-B8	Reel of 3000	BR25A512FVT -3MGE2

Physical Dimension, Tape and Reel Information

Package Name	SOP8
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(UNIT : mm)  
 PKG : SOP8  
 Drawing No. : EX112-5001-1

