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Automotive Series Serial EEPROMs
125°C SPI BUS ICs BR25xxxxFamily

BR25Hxxx-WC Series
(1K 2K 4K 8K 16K 32K)

Description
BR25Hxxx-WC series is a serial EEPROM of SPI BUS interface method.

Features
- High Speed Clock Action Up to 5MHz (Max)
- Wait Function by HOLDB Terminal.
- Part or Whole of Memory Arrays Settable as Read Only Memory Area by Program.
- 2.5 to 5.5V single power source action most suitable for battery use.
- Page Write Mode Useful for Initial Value Write at Factory Shipment.
- Highly Reliable Connection by Au Pad and Au Wire.
- For SPI Bus Interface (CPOL, CPHA)=(0, 0), (1, 1)
- Auto Erase and Auto End Function at Data Rewrite.
- Low Current Consumption
  - At Write Action (5V) : 1.5mA (Typ)
  - At Read Action (5V) : 1.0mA (Typ)
  - At Standby Action (5V) : 0.1µA (Typ)
- Address Auto Increment Function at Read Action
- Write Mistake Prevention Function
  - Write Prohibition at Power on.
  - Write Prohibition by Command Code (WRDI).
  - Write Prohibition by WPB Pin.
  - Write Prohibition Block Setting by Status Registers (BP1, BP0)
  - Write Mistake Prevention Function at Low Voltage.
- Data at Shipment Memory Array: FFh, Status Register WPEN, BP1, BP0 : 0
- Data Kept for 40 Years.
- Data Rewrite Up to 1,000,000 Times.
- AEC-Q100 Qualified

Packages W(Typ) x D(Typ) x H(Max)

SOP8
5.00mm x 6.20mm x 1.71mm

SOP-J8
4.90mm x 6.00mm x 1.65mm

TSSOP-B8
3.00mm x 6.40mm x 1.20mm

Page Write

Number of pages	16 Byte	32 Byte
Product Number	BR25H010-WC BR25H020-WC BR25H040-WC	BR25H080-WC BR25H160-WC BR25H320-WC

BR25Hxxx-WC Series

Capacity	Bit Format	Type	Power Source Voltage	SOP8	SOP-J8	TSSOP-B8
1Kbit	128×8	BR25H010-WC	2.5 to 5.5V	●	●	●
2Kbit	256×8	BR25H020-WC	2.5 to 5.5V	●	●	●
4Kbit	512×8	BR25H040-WC	2.5 to 5.5V	●	●	●
8Kbit	1K×8	BR25H080-WC	2.5 to 5.5V	●	●	●
16Kbit	2K×8	BR25H160-WC	2.5 to 5.5V	●	●	●
32Kbit	4Kx8	BR25H320-WC	2.5 to 5.5V	●	●	

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit	Remarks
Impressed Voltage	V_{CC}	-0.3 to +6.5	V	
Permissible Dissipation	Pd	0.56 (SOP8)	W	When using at Ta=25°C or higher, 4.5mW to be reduced per 1°C
		0.56 (SOP-J8)		When using at Ta=25°C or higher, 4.5mW to be reduced per 1°C
		0.41 (TSSOP-B8)		When using at Ta=25°C or higher, 3.3mW to be reduced per 1°C
Storage Temperature Range	Tstg	-65 to +150	°C	
Operating Temperature Range	Topr	-40 to +125	°C	
Terminal Voltage	-	-0.3 to V_{CC}+0.3	V	

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Memory Cell Characteristics (V_{CC}=2.5V to 5.5V)

Parameter	Limits			Unit	Condition
	Min	Typ	Max		
Number of Data Rewrite Times (Note1)	1,000,000	-	-	Times	Ta≤85°C
	500,000	-	-	Times	Ta≤105°C
	300,000	-	-	Times	Ta≤125°C
Data Hold Years (Note1)	40	-	-	Years	Ta≤25°C
	20	-	-	Years	Ta≤125°C

(Note1) Not 100% TESTED

Recommended Operating Ratings

Parameter	Symbol	Limits	Unit
Power Source Voltage	V_{CC}	2.5 to 5.5	V
Input Voltage	V_{IN}	0 to V_{CC}	

Input / Output Capacity (Ta=25°C, Frequency=5MHz)

Parameter	Symbol	Min	Max	Unit	Conditions
Input Capacity (Note1)	C_{IN}	-	8	pF	V_{IN}=GND
Output Capacity (Note1)	C_{OUT}	-	8		V_{OUT}=GND

(Note1) Not 100% TESTED

Electrical Characteristics (Unless otherwise specified, Ta=-40°C to +125°C, V_{CC}=2.5V to 5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
"H" Input Voltage	V_{IH}	0.7xV_{CC}	-	V_{CC}+0.3	V	2.5V≤V_{CC}≤5.5V
"L" Input Voltage	V_{IL}	-0.3	-	0.3xV_{CC}	V	2.5V≤V_{CC}≤5.5V
"L" Output Voltage	V_{OL}	0	-	0.4	V	I_{OL}=2.1mA
"H" Output Voltage	V_{OH}	V_{CC}-0.5	-	V_{CC}	V	I_{OH}=-0.4mA
Input Leak Current	I_{LI}	-10	-	10	µA	V_{IN}=0 to V_{CC}
Output Leak Current	I_{LO}	-10	-	10	µA	V_{OUT}=0 to V_{CC}, CSB=V_{CC}
Current Consumption at Write Action	I_{CC1}	-	-	2.0	mA	V_{CC}=2.5V, f_{SCK}=5MHz, $t_{E/W}$=5ms V_{IH}/V_{IL}=0.9V_{CC}/0.1V_{CC}, SO=OPEN Byte write, Page write, Write status register
	I_{CC2}	-	-	3.0	mA	V_{CC}=5.5V, f_{SCK}=5MHz, $t_{E/W}$=5ms V_{IH}/V_{IL}=0.9V_{CC}/0.1V_{CC}, SO=OPEN Byte write, Page write, Write status register
Current Consumption at Read Action	I_{CC3}	-	-	1.5	mA	V_{CC}=2.5V, f_{SCK}=5MHz V_{IH}/V_{IL}=0.9V_{CC}/0.1V_{CC}, SO=OPEN Read, Read status register
	I_{CC4}	-	-	2.0	mA	V_{CC}=5.5V, f_{SCK}=5MHz V_{IH}/V_{IL}=0.9V_{CC}/0.1V_{CC}, SO=OPEN Read, Read status register
Standby Current	I_{SB}	-	-	10	µA	V_{CC}=5.5V CSB=HOLDB=WPB=V_{CC}, SCK=SI=V_{CC} or =GND, SO=OPEN

Operating Timing Characteristics

(Ta=-40°C to +125°C, unless otherwise specified, load capacity C_{L1}=100pF)

Parameter	Symbol	2.5≤V_{CC}≤5.5V			Unit
		Min	Typ	Max	
SCK Frequency	f_{SCK}	-	-	5	MHz
SCK High Time	t_{SCKWH}	85	-	-	ns
SCK Low Time	t_{SCKWL}	85	-	-	ns
CSB High Time	t_{CS}	85	-	-	ns
CSB Setup Time	t_{CSS}	90	-	-	ns
CSB Hold Time	t_{CSH}	85	-	-	ns
SCK Setup Time	t_{SCKS}	90	-	-	ns
SCK Hold Time	t_{SCKH}	90	-	-	ns
SI Setup Time	t_{DIS}	20	-	-	ns
SI Hold Time	t_{DIH}	30	-	-	ns
Data Output Delay Time1	t_{PD1}	-	-	70	ns
Data Output Delay Time2 (C_{L2}=30pF)	t_{PD2}	-	-	55	ns
Output Hold Time	t_{OH}	0	-	-	ns
Output Disable Time	t_{OZ}	-	-	100	ns
HOLDB Setting Setup Time	t_{HFS}	0	-	-	ns
HOLDB Setting Hold Time	t_{HFH}	40	-	-	ns
HOLDB Release Setup Time	t_{HRS}	0	-	-	ns
HOLDB Release Old Time	t_{HRH}	70	-	-	ns
Time from HOLDB to Output High-Z	t_{HOZ}	-	-	100	ns
Time from HOLDB To Output Change	t_{HPD}	-	-	70	ns
SCK Rise Time (Note1)	t_{RC}	-	-	1	µs
SCK Fall Time (Note1)	t_{FC}	-	-	1	µs
OUTPUT Rise Time (Note1)	t_{RO}	-	-	50	ns
OUTPUT Fall Time (Note1)	t_{FO}	-	-	50	ns
Write Time	$t_{E/W}$	-	-	5	ms

(Note1) NOT 100% TESTED

Sync Data Input / Output Timing

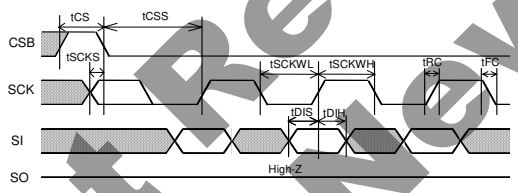


Figure 1. Input Timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the most significant bit MSB.

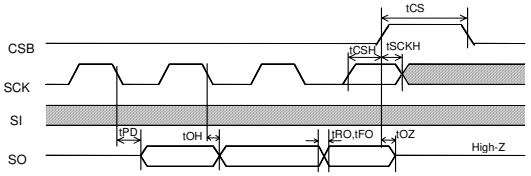


Figure 2. Input / Output Timing

SO is output in sync with data fall edge of SCK. Data is output from the most significant bit MSB.

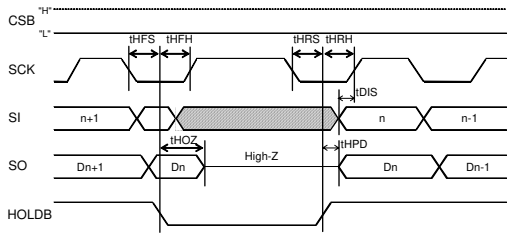


Figure 3. HOLD timing

AC Measurement Conditions

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Load Capacity 1	C_{L1}	-	-	100	pF
Load Capacity 2	C_{L2}	-	-	30	pF
Input Rise Time	-	-	-	50	ns
Input Fall Time	-	-	-	50	ns
Input Voltage	-	0.2V_{CC}/0.8V_{CC}			V
Input / Output Judgment Voltage	-	0.3V_{CC}/0.7V_{CC}			V

Block Diagram

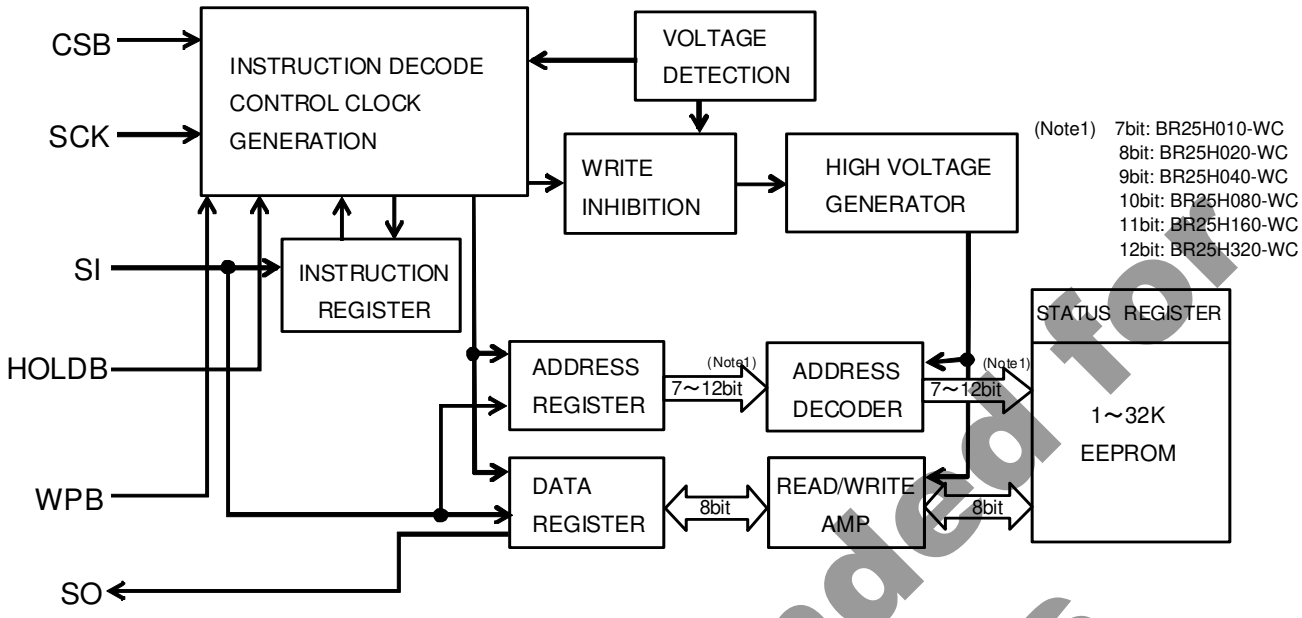


Figure 4. Block diagram

Pin Configuration

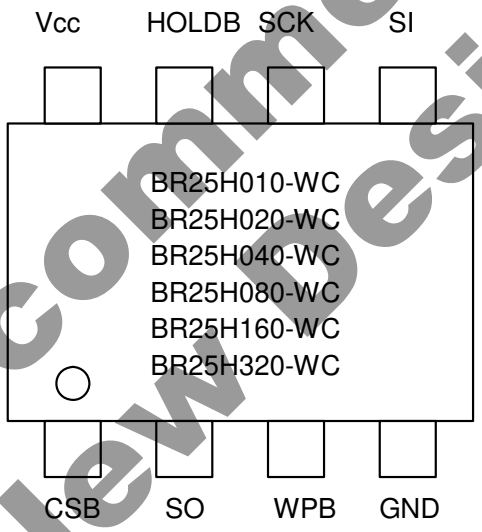


Figure 5. Pin Configuration

Pin Description

Terminal name	Input/Output	Function
V_{CC}	-	Power source to be connected
GND	-	All input / output reference voltage, 0V
CSB	Input	Chip select input
SCK	Input	Serial clock input
SI	Input	Start bit, ope code, address, and serial data input
SO	Output	Serial data output
HOLDB	Input	Hold input Command communications may be suspended temporarily (HOLD status)
WPB	Input	Write protect input Write command is prohibited (Note1) Write status register command is prohibited.

(Note1) BR25H010/020/040-WC

Typical Performance Curves

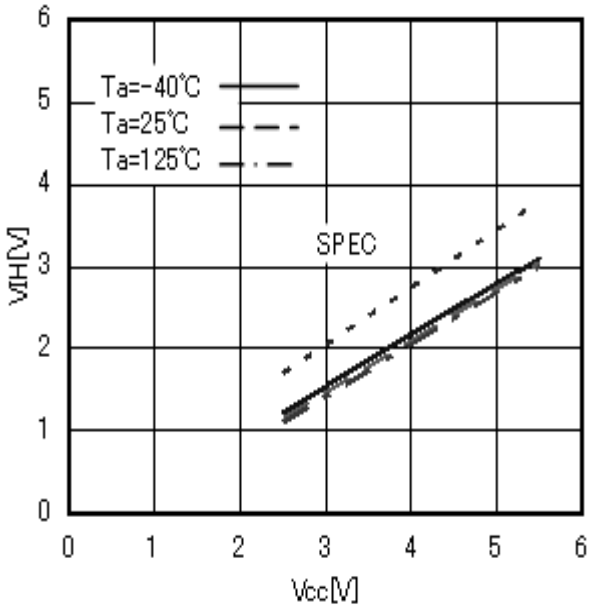


Figure 6. “H” Input Voltage vs Supply Voltage

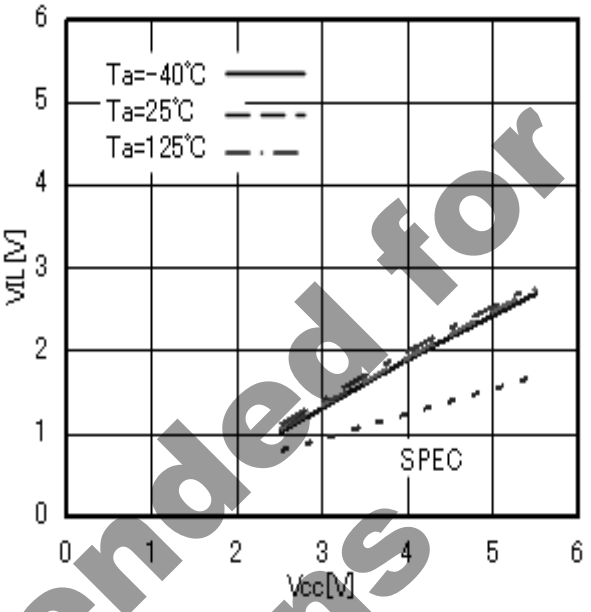


Figure 7. “L” Input Voltage vs Supply Voltage

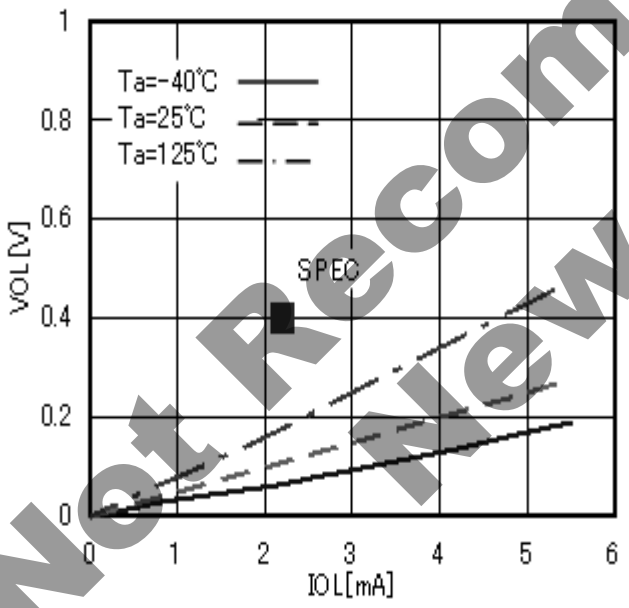


Figure 8. “L” Output Voltage vs Output Current (Vcc=2.5V)

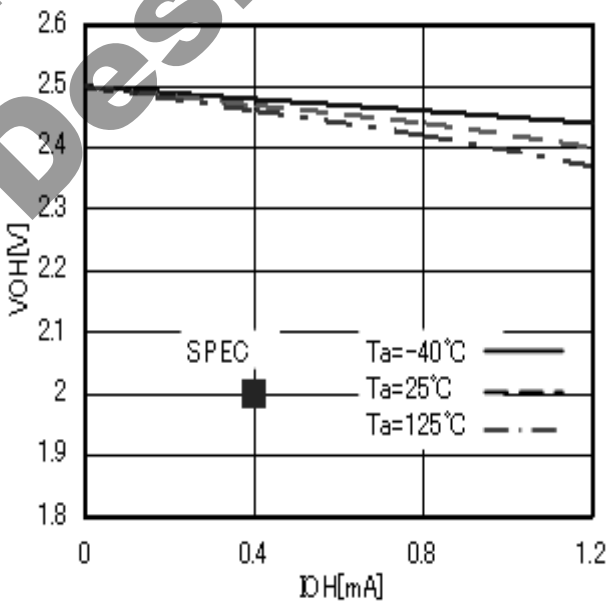


Figure 9. "H" Output Voltage vs Output Current (Vcc=2.5V)

Typical Performance Curves - continued

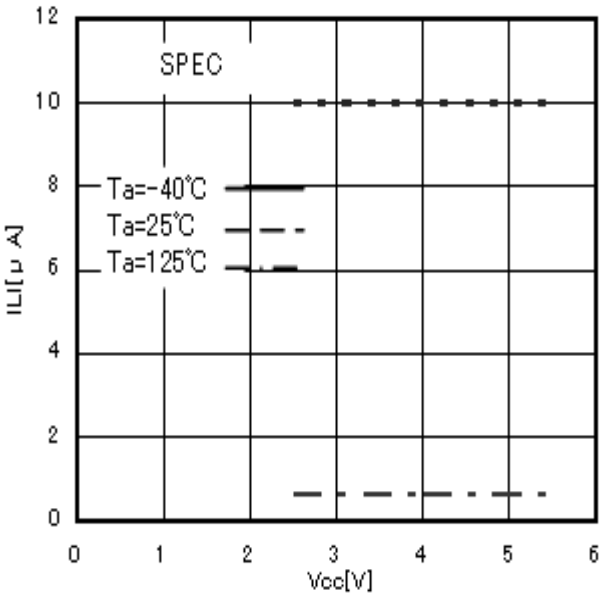


Figure 10. Input Leak Current vs Supply Voltage

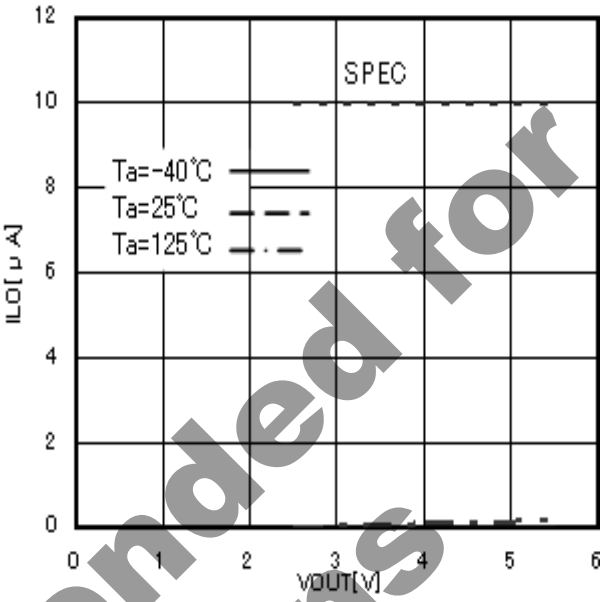


Figure 11. Output Leak Current vs Output Voltage (Vcc=5.5V)

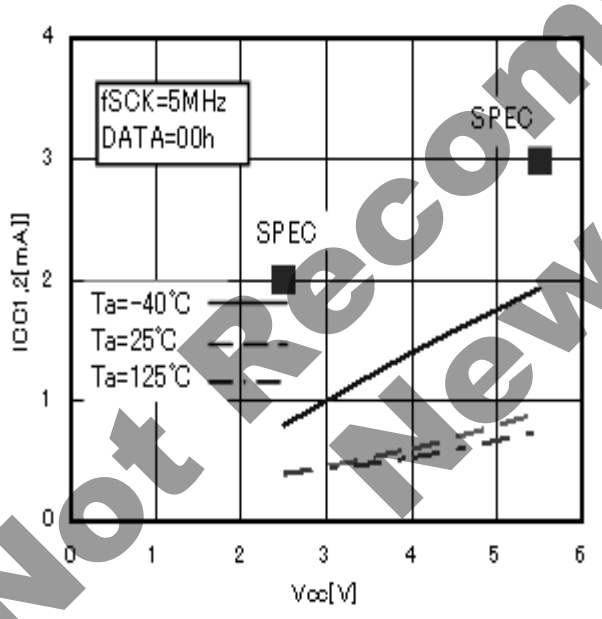


Figure 12. Current Consumption at WRITE Operation vs Supply Voltage

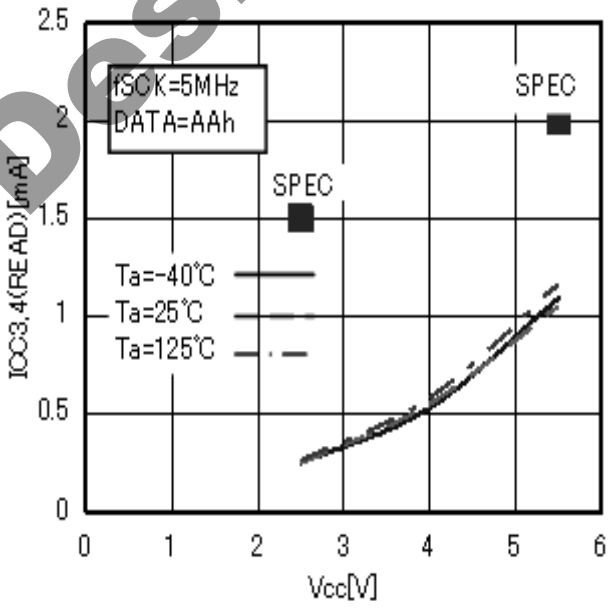


Figure 13. Consumption Current at READ Operation vs Supply Voltage

Typical Performance Curves - continued

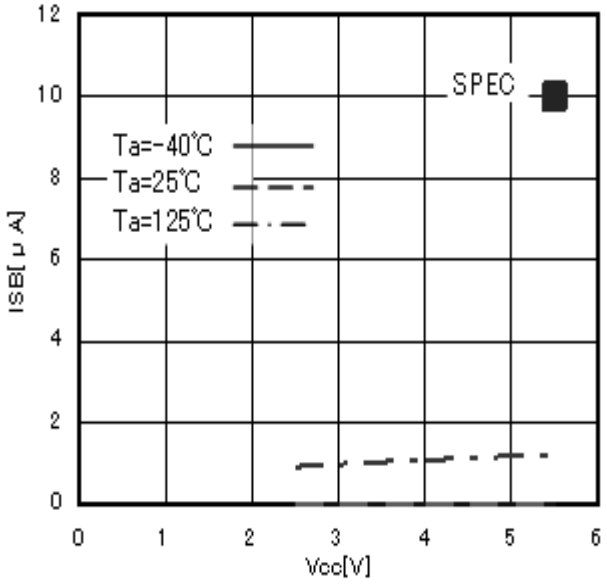


Figure 14. Standby Current vs Supply Voltage

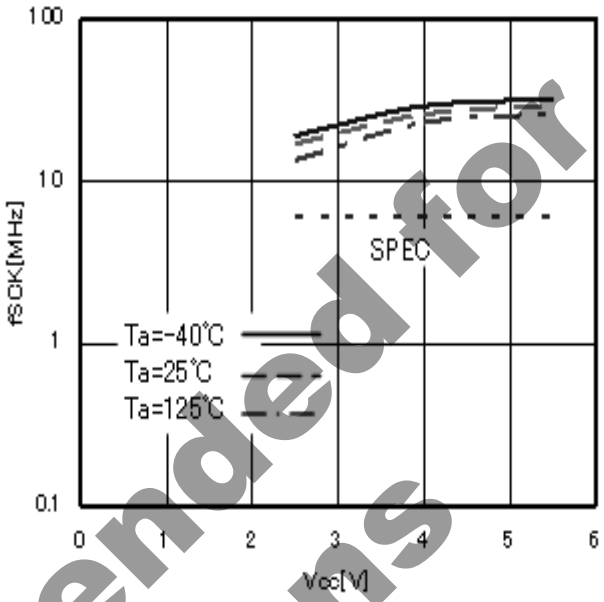


Figure 15. SCK Frequency vs Supply Voltage

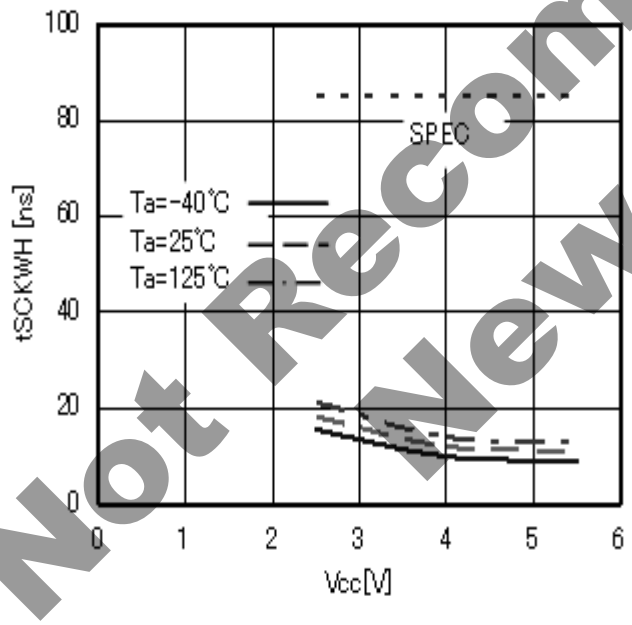


Figure 16. SCK High Time vs Supply Voltage

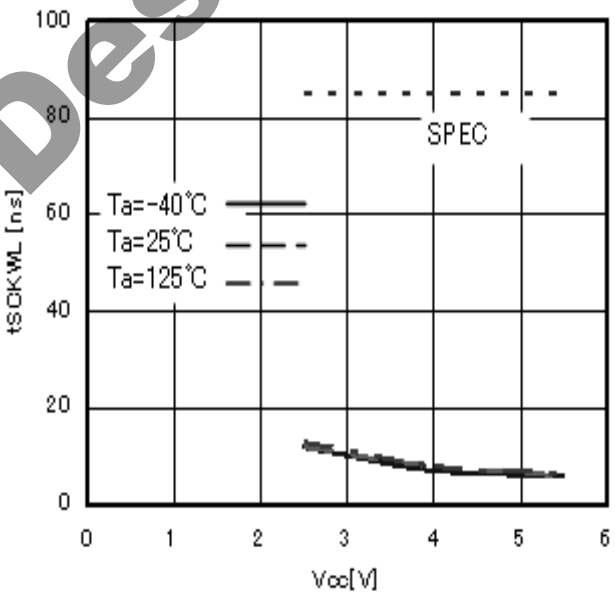


Figure 17. SCK Low Time vs Supply Voltage

Typical Performance Curves - continued

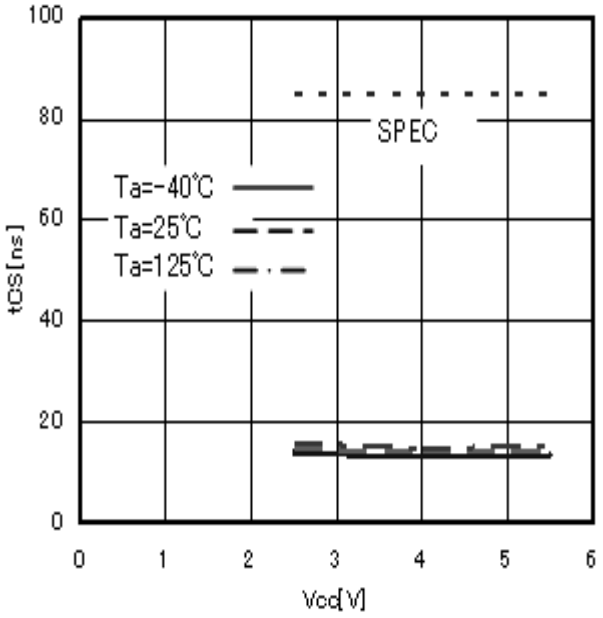


Figure 18. CSB High Time vs Supply Voltage

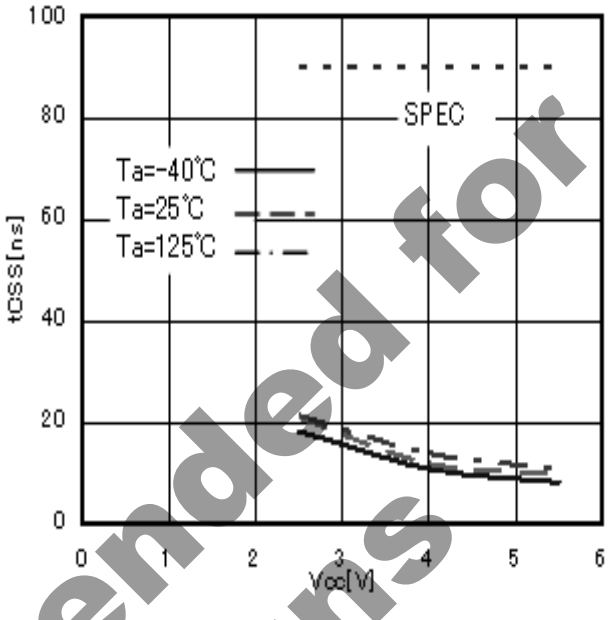


Figure 19. CSB Setup Time vs Supply Voltage

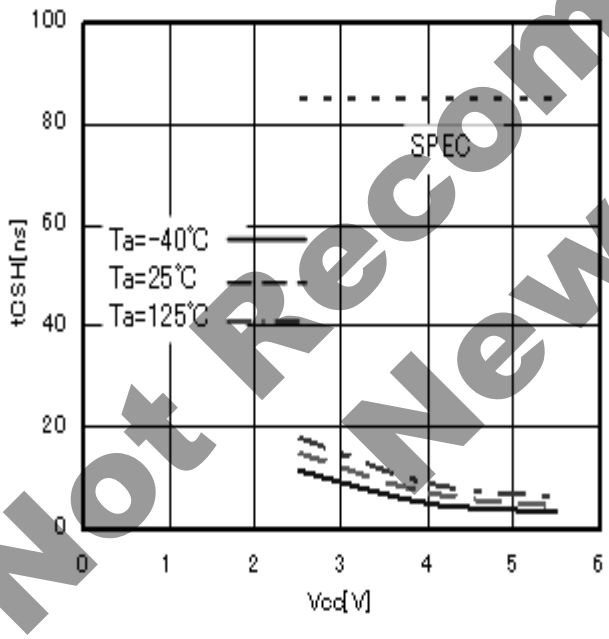


Figure 20. CSB Hold Time vs Supply Voltage

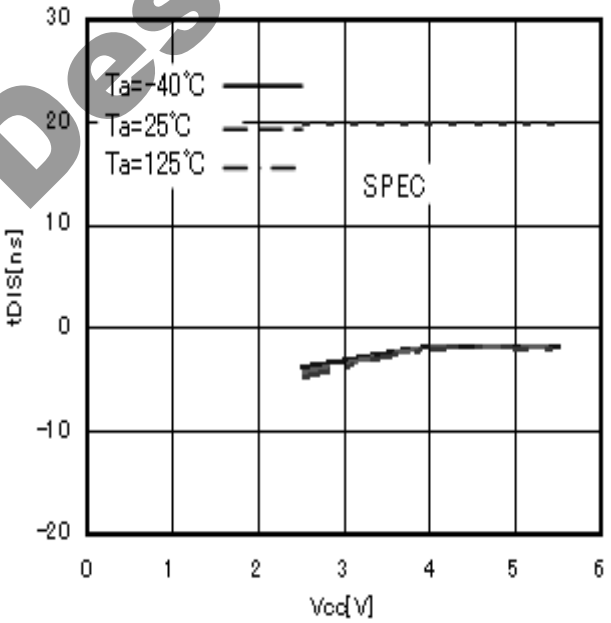


Figure 21. SI Setup Time vs Supply Voltage

Typical Performance Curves - continued

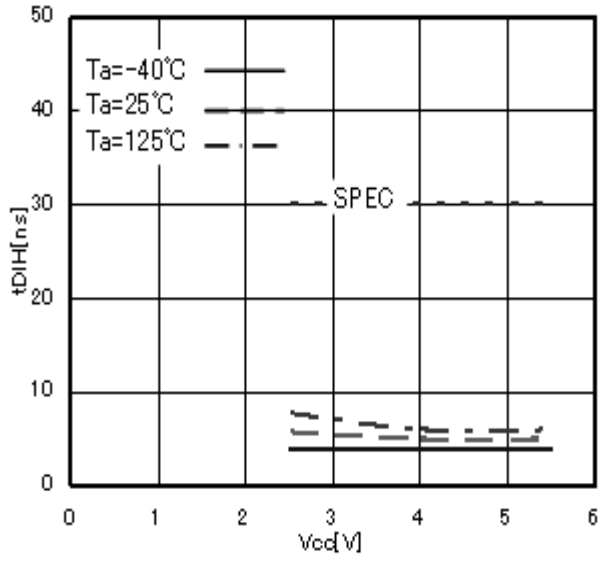


Figure 22. SI Hold Time vs Supply Voltage

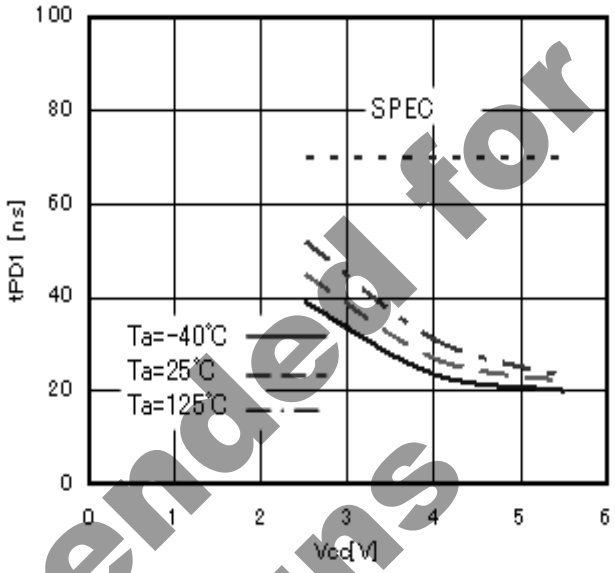


Figure 23. Data Output Delay Time vs Supply Voltage (C_{L1}=100pF)

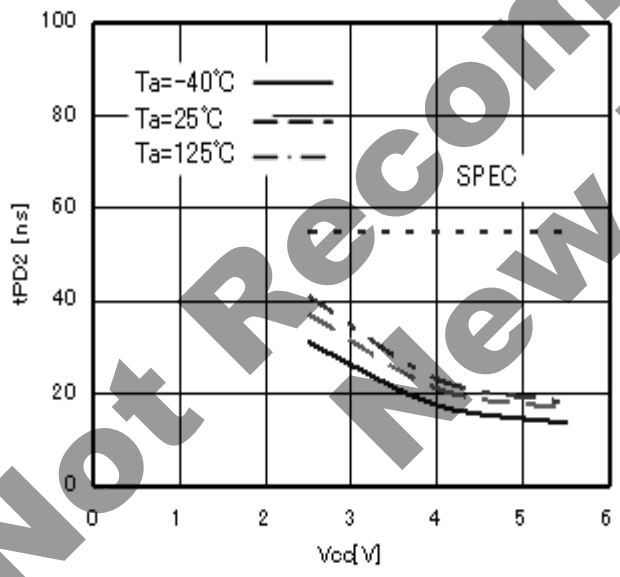


Figure 24. Data Output Delay Time vs Supply Voltage (C_{L2}=30pF)

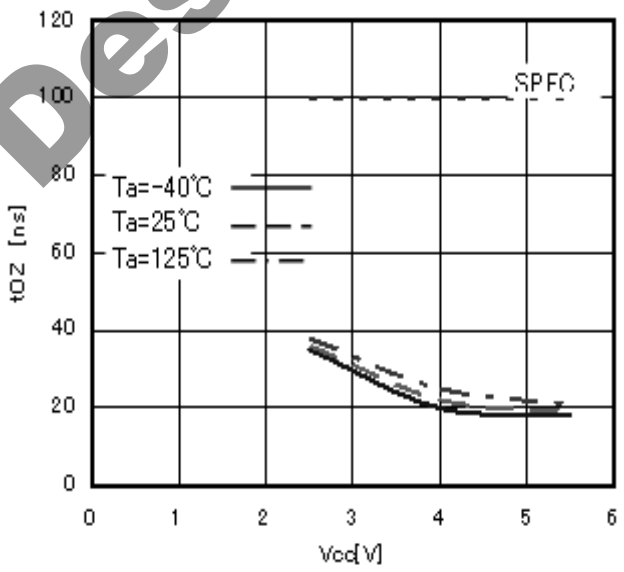


Figure 25. Output Disable Time vs Supply Voltage

Typical Performance Curves - continued

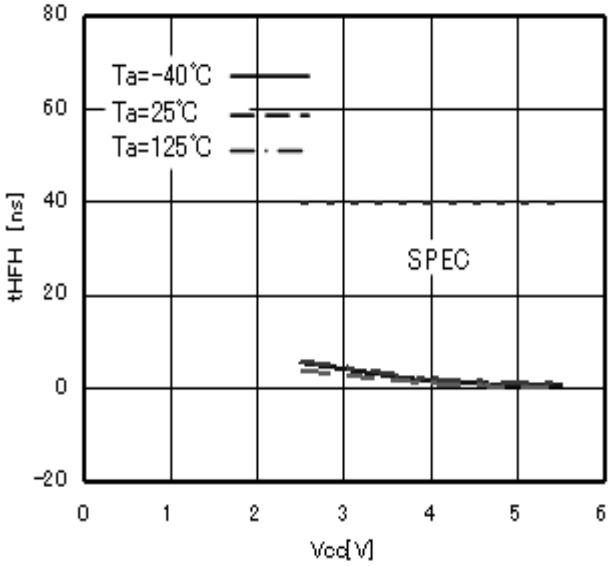


Figure 26. HOLDB Setting Hold Time vs Supply Voltage

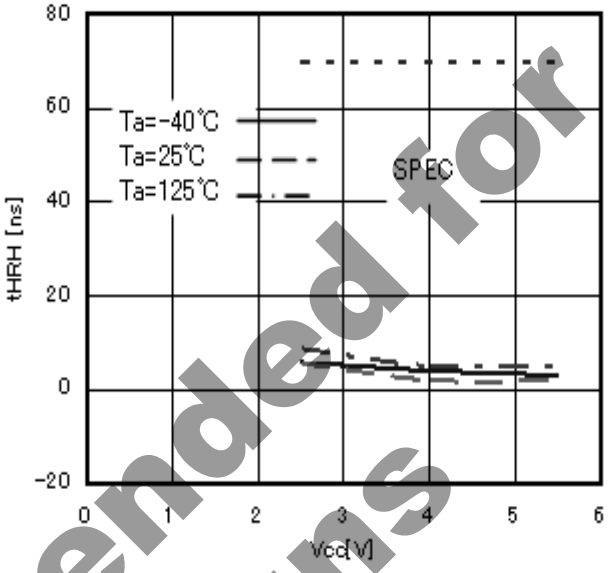


Figure 27. HOLDB Release Hold Time vs Supply Voltage

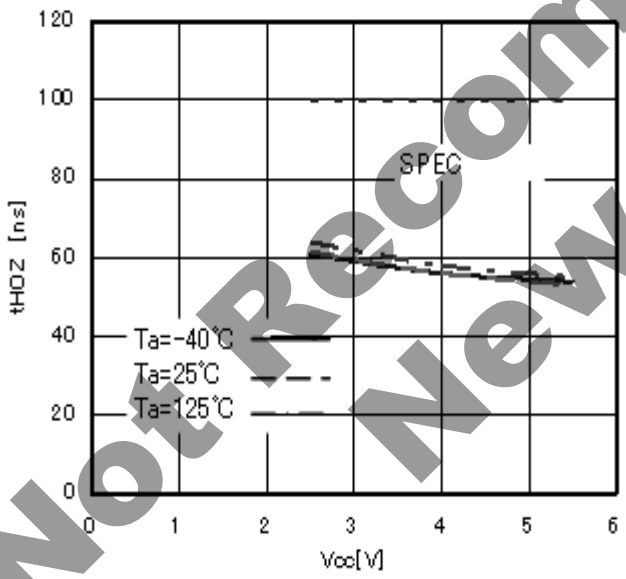


Figure 28. Time from HOLDB to Output High-Z vs Supply Voltage

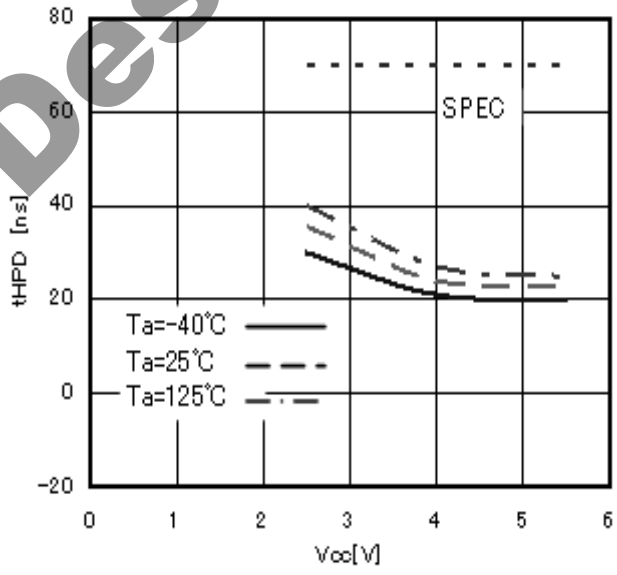


Figure 29. Time from HOLDB to Output Change vs Supply Voltage

Typical Performance Curves - continued

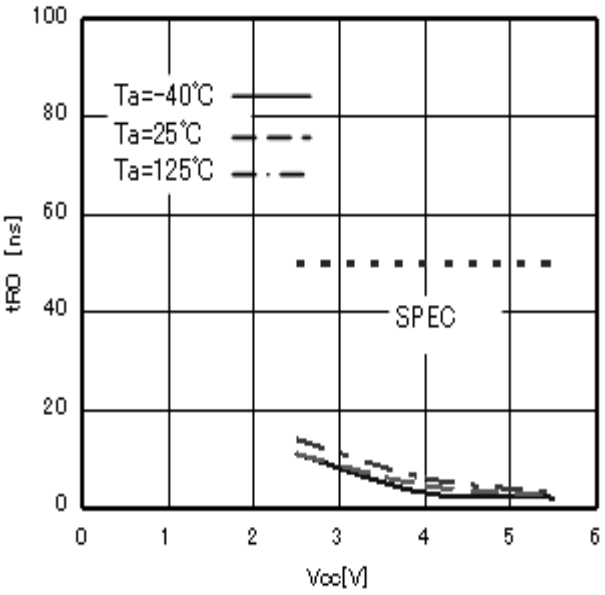


Figure 30. Output Rise Time vs Supply Voltage

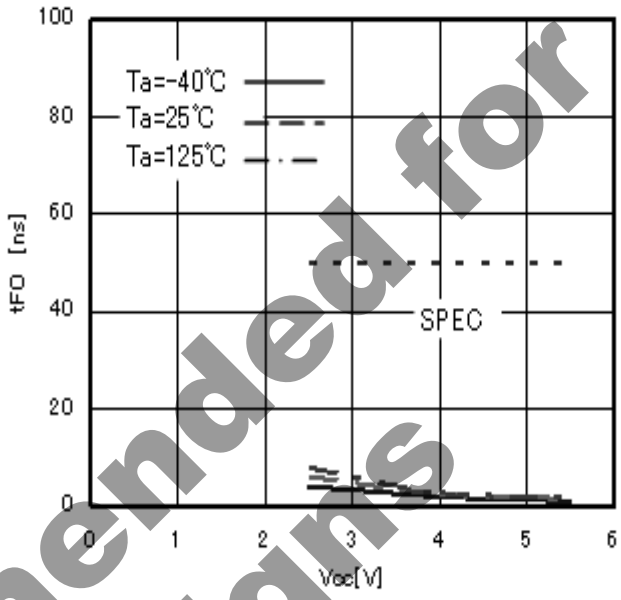


Figure 31. Output Fall Time vs Supply Voltage

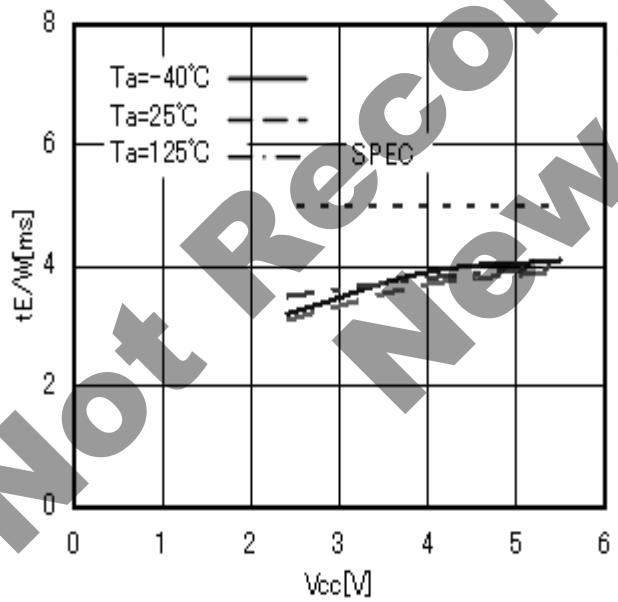


Figure 32. Write Cycle Time vs Supply Voltage

Features

1. Status Registers

This IC has status registers. The status registers are of 8 bits and express the following parameters.
BP0 and BP1 can be set by write status register command. These 2 bits are memorized into the EEPROM, therefore are valid even when power source is turned off.
Rewrite characteristics and data hold time are same as characteristics of the EEPROM.
WEN can be set by write enable command and write disable command. WEN becomes write disable status when power source is turned off. $\overline{R}$/B is for write confirmation, therefore cannot be set externally.
The value of status register can be read by read status command.

Status Registers

Product number	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR25H010-WC	1	1	1	1	BP1	BP0	WEN	$\overline{R}$/B
BR25H020-WC								
BR25H040-WC								
BR25H080-WC	WPEN	0	0	0	BP1	BP0	WEN	$\overline{R}$/B
BR25H160-WC								
BR25H320-WC								

bit	Memory location	Function	Contents
WPEN	EEPROM	WPB pin enable / disable designation bit WPEN=0=invalid WPEN=1=valid	This enables / disables the functions of WPB pin.
BP1 BP0	EEPROM	EEPROM write disable block designation bit	This designates the write disable area of EEPROM. Write designation areas of product numbers are shown below.
WEN	Register	Write and write status register write enable / disable status confirmation bit WEN=0=prohibited WEN=1=permitted	This confirms prohibited status or permitted status of the write and the write status register.
$\overline{R}$/B	Register	Write cycle status (READY / BUSY) status confirmation bit $\overline{R}$/B=0=READY $\overline{R}$/B=1=BUSY	This confirms READY status or BUSY status of the write cycle.

Write Disable Block Setting

BP1	BP0	Write disable block					
		BR25H010-WC	BR25H020-WC	BR25H040-WC	BR25H080-WC	BR25H160-WC	BR25H320-WC
0	0	None	None	None	None	None	None
0	1	60h-7Fh	C0h-FFh	180h-1FFh	300h-3FFh	600h-7FFh	C00h-FFFh
1	0	40h-7Fh	80h-FFh	100h-1FFh	200h-3FFh	400h-7FFh	800h-FFFh
1	1	00h-7Fh	00h-FFh	000h-1FFh	000h-3FFh	000h-7FFh	000h-FFFh

1. WPB Pin

By setting WPB=LOW, write command is prohibited. As for BR25H080/160/320-WC, only when WPEN bit is set “1”, the WPB pin functions become valid. And the write command to be disabled at this moment is WRSR. As for BR25H010/020/040-WC, both WRITE and WRSR commands are prohibited.
However, when write cycle is in execution, no interruption can be made.

Product number	WRSR	WRITE
BR25H010-WC	Prohibition possible	Prohibition possible
BR25H020-WC		
BR25H040-WC		
BR25H080-WC	Prohibition possible but WPEN bit “1”	Prohibition impossible
BR25H160-WC		
BR25H320-WC		

2. HOLDB Pin

By HOLDB pin, data transfer can be interrupted. When SCK=”0”, by making HOLDB from “1” into”0”, data transfer to EEPROM is interrupted. When SCK = “0”, by making HOLDB from “0” into “1”, data transfer is restarted.

Command Mode

Command		Contents	Ope Code					
			BR25H010-WC BR25H020-WC		BR25H040-WC		BR25H080-WC BR25H160-WC BR25H320-WC	
WREN	Write Enable	Write Enable Command	0000	*110	0000	*110	0000	0110
WRDI	Write Disable	Write Disable Command	0000	*100	0000	*100	0000	0100
READ	Read	Read Command	0000	*011	0000	A8011	0000	0011
WRITE	Write	Write Command	0000	*010	0000	A8010	0000	0010
RDSR	Read Status Register	Status Register Read Command	0000	*101	0000	*101	0000	0101
WRSR	Write Status Register	Status Register Write Command	0000	*001	0000	*001	0000	0001

*=Don't Care Bit.

Timing Chart

1. Write Enable (WREN) / Disable (WRDI) Cycle

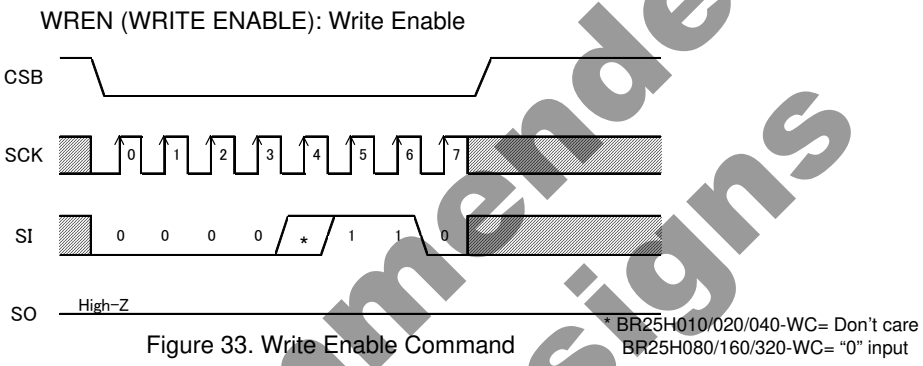


Figure 33. Write Enable Command

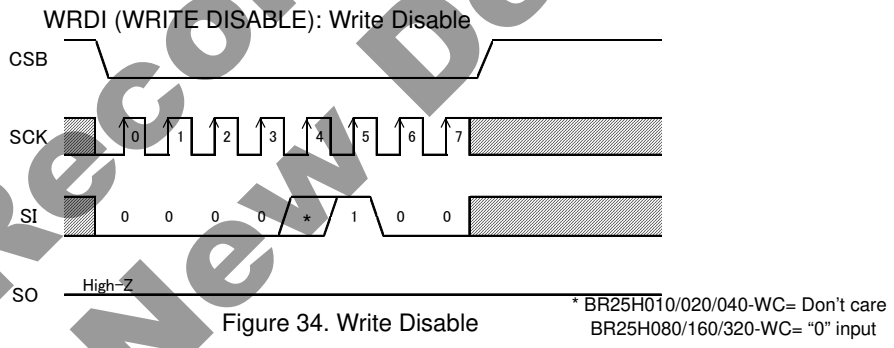
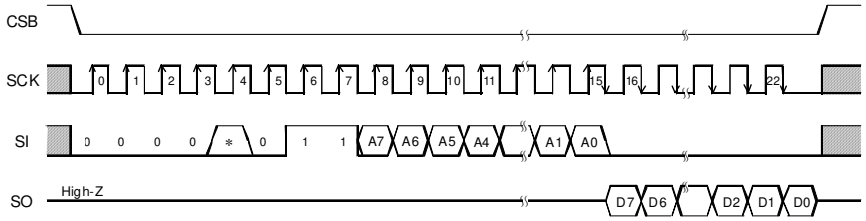


Figure 34. Write Disable

This IC has write enable status and write disable status. It is set to write enable status by write enable command, and it is set to write disable status by write disable command. As for these commands, set CSB LOW, and then input the respective ope codes. The respective commands accept command at the 7-th clock rise. Even with input over 7 clocks, command becomes valid.

When to carry out write and write status register command, it is necessary to set write enable status by the write enable command. If write or write status register command is input in the write disable status, commands are cancelled. And even in the write enable status, once write and write status register command is executed, it gets in the write disable status. After power on, this IC is in write disable status.

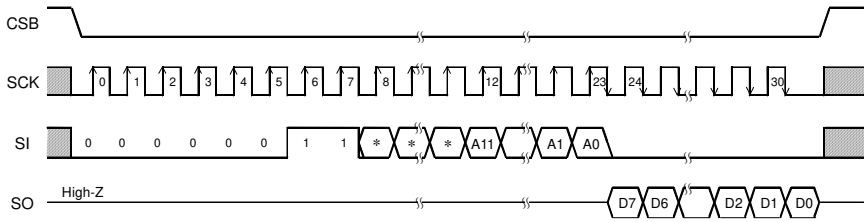
2. Read Command (READ)



Product number	Address length
BR25H010-WC	A6-A0
BR25H020-WC	A7-A0
BR25H040-WC	A8-A0

Figure 35. Read Command (BR25H010/020/040-WC)

* BR25H010/020-WC=Don't care
BR25H040-WC=A8



Product number	Address length
BR25H080-WC	A9-A0
BR25H160-WC	A10-A0
BR25H320-WC	A11-A0

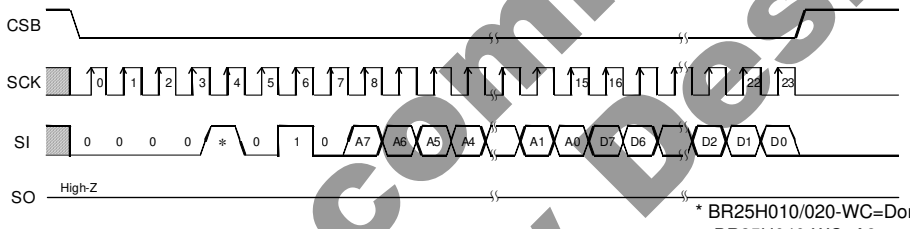
*=Don't Care

Figure 36. Read Command (BR25H080/160/320-WC)

By read command, data of EEPROM can be read. As for this command, set CSB LOW, then input address after read ope code. EEPROM starts data output of the designated address. Data output is started from SCK fall of 15/23(Note1) clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM. After reading data of the most significant address, by continuing increment read, data of the most insignificant address is read.

(Note1) BR25H010/020/040-WC=15 clocks
BR25H080/160/320-WC=23 clocks

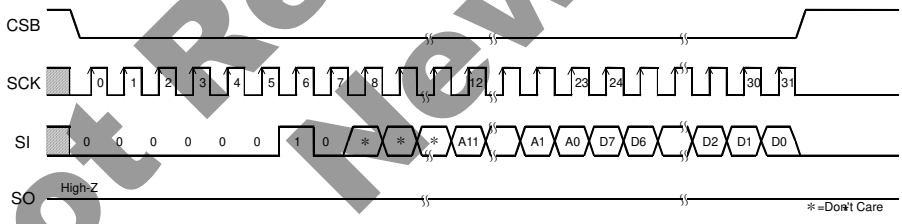
3. Write Command (WRITE)



Product number	Address length
BR25H010-WC	A6-A0
BR25H020-WC	A7-A0
BR25H040-WC	A8-A0

* BR25H010/020-WC=Don't care
BR25H040-WC=A8

Figure 37. Write Command (BR25H010/020/040-WC)



Product number	Address length
BR25H080-WC	A9-A0
BR25H160-WC	A10-A0
BR25H320-WC	A11-A0

*=Don't Care

Figure 38. Write Command (BR25H080/160/320-WC)

By write command, data of EEPROM can be written. As for this command, set CSB LOW, then input address and data after write ope code. Then, by making CSB HIGH, the EEPROM starts writing. The write time of EEPROM requires time of $t_{E/W}$ (Max 5ms). During $t_{E/W}$, other than status read command is not accepted. Start CSB after taking the last data (D0), and before the next SCK clock starts. At other timing, write command is not executed, and this write command is cancelled. This IC has page write function, and after input of data for 1 byte (8 bits), by continuing data input without starting CSB, data up to 16/32(Note1) bytes can be written for one $t_{E/W}$. In page write, the insignificant 4/5(Note2) bit of the designated address is incremented internally at every time when data of 1 byte is input and data is written to respective addresses. When data of the maximum bytes or higher is input, address rolls over, and previously input data is overwritten.

(Note1) BR25H010/020/040-WC=16 bytes at maximum
BR25H080/160/320-WC=32 bytes at maximum
(Note2) BR25H010/020/040-WC=Insignificant 4 bits
BR25H080/160/320-WC=Insignificant 5 bits

4. Status Register Write / Read Command

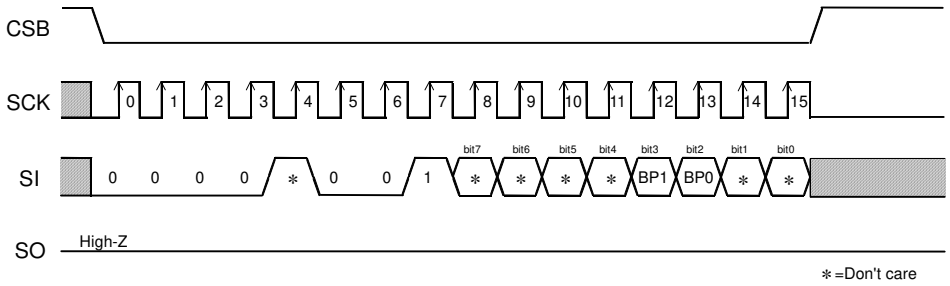


Figure 39. Status Register Write Command (BR25H010/020/040-WC)

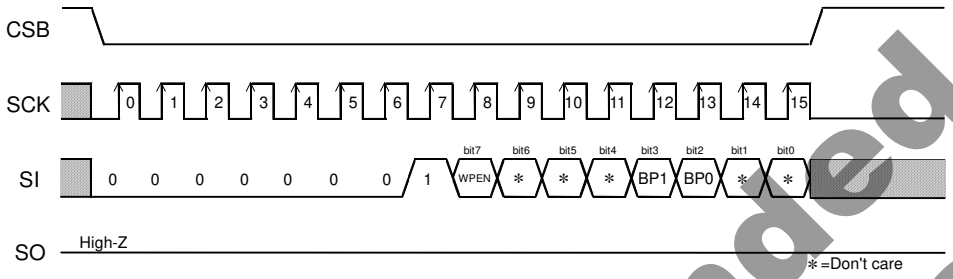


Figure 40. Status Register Write Command (BR25H080/160/320-WC)

Write status register command can write status register data. The data can be written by this command are 2 bits (Note1), that is, BP1 (bit3) and BP0 (bit2) among 8 bits of status register. By BP1 and BP0, write disable block of EEPROM can be set. As for this command, set CSB LOW, and input ope code of write status register, and input data. Then, by making CSB HIGH, EEPROM starts writing. Write time requires time of $t_{E/W}$ as same as write. As for CSB rise, start CSB after taking the last data bit (bit0), and before the next SCK clock starts. At other timing, command is cancelled. Write disable block is determined by BP1 and BP0, and the block can be selected from 1/4 of memory array, 1/2, and entire memory array. (Refer to the write disable block setting table.)
To the write disabled block, write cannot be made, and only read can be made.

(Note1) 3bits including BR25H080/160/320-WC WPEN (bit7)

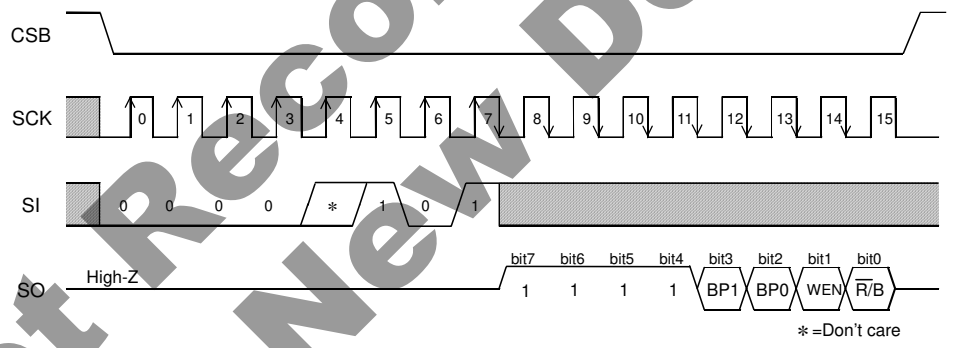


Figure 41. Status Register Read Command (BR25H010/020/040-WC)

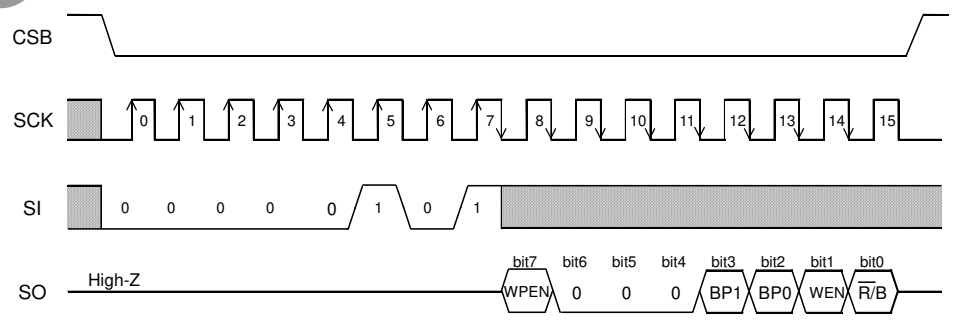


Figure 42. Status Register Read Command (BR25H080/160/320-WC)

At Standby

1. Current at Standby

Set CSB “H”, and be sure to set SCK, SI, WPB, HOLDB input “L” or “H”. Do not input intermediate electric potantial.

2. Timing

As shown in Figure 43., at standby, when SCK is “H”, even if CSB is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB “H” status.

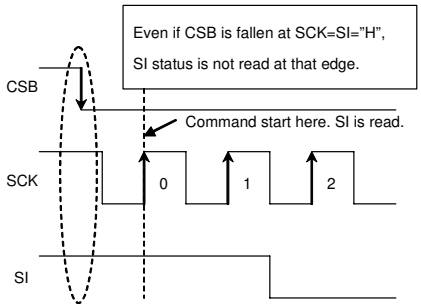


Figure 43. Operating Timing

WPB Cancel Valid Area

WPB is normally fixed to “H” or “L” for use, but when WPB is controlled so as to cancel write status register command and write command, pay attention to the following WPB valid timing.
While write or write status register command is executed, by setting WPB = “L” in cancel valid area, command can be cancelled. The area from command ope code before CSB rise at internal automatic write start becomes the cancel valid area. However, once write is started, any input cannot be cancelled. WPB input becomes Don’t Care, and cancellation becomes invalid.

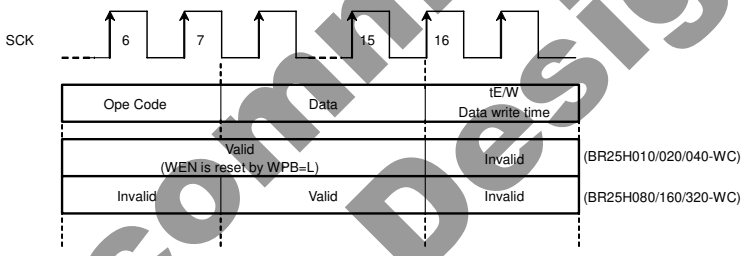
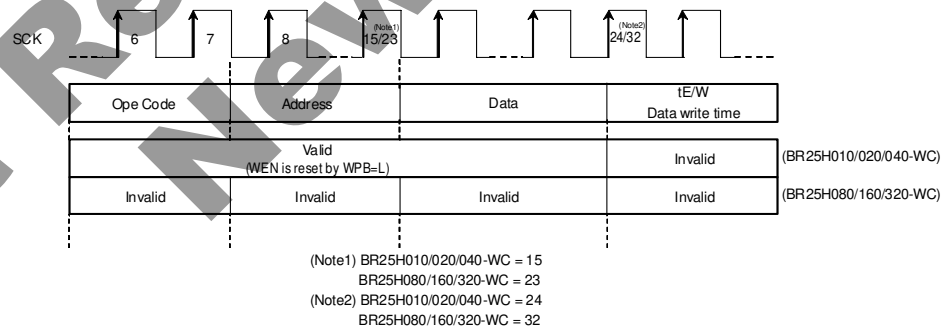


Figure 44. WPB Valid Timing (WRSR)



(Note1) BR25H010/020/040-WC = 15
BR25H080/160/320-WC = 23
(Note2) BR25H010/020/040-WC = 24
BR25H080/160/320-WC = 32

Figure 45. WPB Valid Timing (WRITE)

HOLDB Pin

By HOLDB pin, command communication can be stopped temporarily (HOLD status). The HOLDB pin carries out command communications normally when it is HIGH. To get in HOLD status, at command communication, when SCK=LOW, set the HOLDB pin LOW. At HOLD status, SCK and SI become Don’t Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the HOLDB pin HIGH when SCK=LOW. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at read, after release of HOLD status, by starting A4 address input, read can be restarted. When in HOLD status, leave CSB LOW. When it is set CSB=HIGH in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

Method to Cancel Each Command

1. READ, RDSR

・Method to cancel : cancel by CSB = “H”

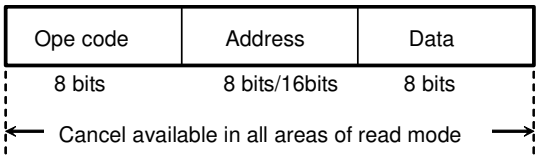


Figure .46 READ Cancel Valid Timing

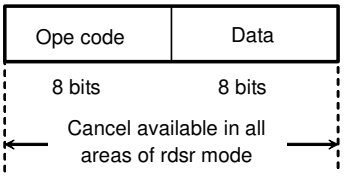


Figure .47 RDSR Cancel Valid Timing

2. WRITE, PAGE WRITE

a : Ope code, address input area.
Cancellation is available by CSB=”H”
b : Data input area (D7 to D1 input area)
Cancellation is available by CSB=”H”
c : Data input area (D0 area)
When CSB is started, write starts.
After CSB rise, cancellation cannot be made by any means.
d : $t_{E/W}$ area.
Cancellation is available by CSB = “H”. However, when write starts (CSB is started) in the area c, cancellation cannot be made by any means. And by inputting on SCK clock, cancellation cannot be made. In page write mode, there is write enable area at every 8 clocks.

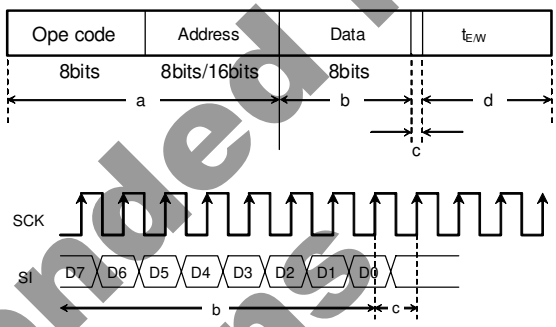


Figure 48. WRITE Cancel Valid Timing

Note 1) If V_{CC} is made OFF during write execution, designated address data is not guaranteed, therefore write it once again
Note 2) If CSB is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = “L” area. As for SCK rise, assure timing of t_{CSS} / t_{CSH} or higher.

3. WRSR

a : From ope code to 15 rise.
Cancel by CSB =”H”.
b : From 15 clock rise to 16 clock rise (write enable area).
When CSB is started, write starts.
After CSB rise, cancellation cannot be made by any means.
c : After 16 clock rise.
Cancel by CSB=”H”. However, when write starts (CSB is started) in the area b, cancellation cannot be made by any means.
And, by inputting on SCK clock, cancellation cannot be made.

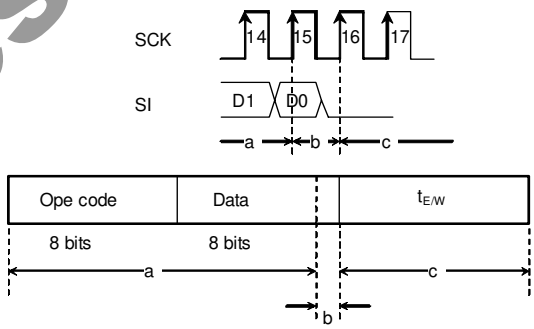


Figure 49. WRSR Cancel Valid Timing

Note 1) If V_{CC} is made OFF during write execution, designated address data is not guaranteed, therefore write it once again
Note 2) If CSB is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = “L” area. As for SCK rise, assure timing of t_{CSS} / t_{CSH} or higher.

4. WREN, WRDI

a : From ope code to 7-th clock rise, cancel by CSB = “H”.
b : Cancellation is not available when CSB is started after 7-th clock.

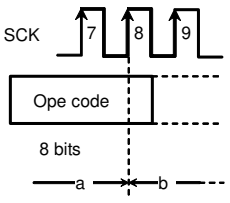


Figure 50. WREN/WRDI Cancel Valid Timing

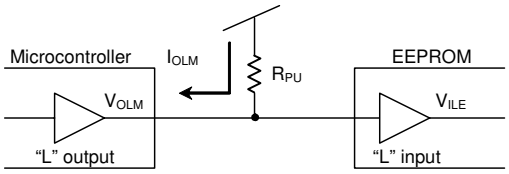
High Speed Operation

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

1. Input Pin pull up, pull down Resistance

When to attach pull up, pull down resistance to EEPROM input pin, select an appropriate value for the microcontroller V_{OL}, I_{OL} from V_{IL} characteristics of this IC.

2. Pull up Resistance



- V_{ILE} :EEPROM V_{IL} specifications
- V_{OLM} :Microcontroller V_{OL} specifications
- I_{OLM} :Microcontroller I_{OL} specifications

Figure 51. Pull up Resistance

$$R_{PU} \geq \frac{V_{CC} - V_{OLM}}{I_{OLM}} \quad \cdots ①$$

$$V_{OLM} \leq V_{ILE} \quad \cdots ②$$

Example) When Vcc=5V, V_{ILE}=1.5V, V_{OLM}=0.4V, I_{OLM}=2mA, from the equation ①,

$$R_{PU} \geq \frac{5 - 0.4}{2 \times 10^{-3}}$$

$$\therefore R_{PU} \geq 2.3 \quad [k\Omega]$$

With the value of R_{PU} to satisfy the above equation, V_{OLM} becomes 0.4V or lower, and with V_{ILE} (=1.5V), the equation ② is also satisfied.

And, in order to prevent malfunction, mistake write at power ON/OFF, be sure to make CSB pull up.

3. Pull down Resistance

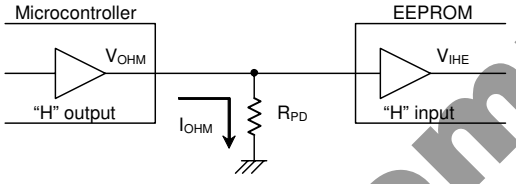


Figure 52. Pull down Resistance

$$R_{PD} \geq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ③$$

$$V_{OHM} \geq V_{IHE} \quad \cdots ④$$

Example) When V_{CC}=5V, V_{OHM}=V_{CC}-0.5V, I_{OHM}=0.4mA, V_{IHE}=V_{CC}×0.7V, from the equation③,

$$R_{PD} \geq \frac{5 - 0.5}{0.4 \times 10^{-3}}$$

$$\therefore R_{PU} \geq 11.3 \quad [k\Omega]$$

Further, by amplitude V_{IHE}, V_{ILE} of signal input to EEPROM, operation speed changes. By inputting signal of amplitude of V_{CC} / GND level to input, more stable high speed operations can be realized. On the contrary, when amplitude of $0.8V_{CC}$ / $0.2V_{CC}$ is input, operation speed becomes slow. (Note1)
In order to realize more stable high speed operation, it is recommended to make the values of R_{PU}, R_{PD} as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of V_{CC} / GND level.
(Note1) At this moment, operating timing guaranteed value is guaranteed.

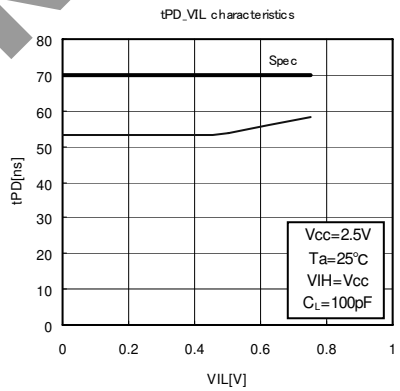


Figure 53. Data Output Delay Time vs "L" Input Voltage

4. SO Road Capacity Condition

Load capacity of SO output pin affects upon delay characteristic of SO output. (Data output delay time, time from HOLDB to High-Z) In order to make output delay characteristic into higher speed, make SO load capacity small. In concrete, “Do not connect many devices to SO bus”, “Make the wire between the controller and EEPROM short”, and so forth.

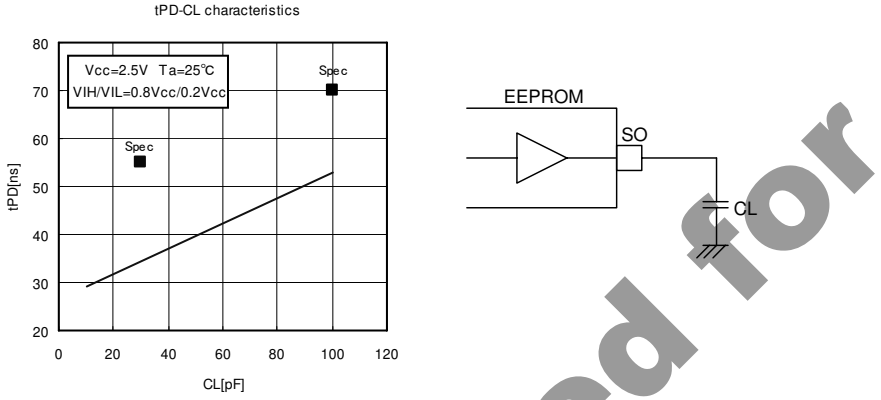


Figure 54. Data Output Delay Time vs SO Load

5. Other Cautions

Make the wire length from the microcontroller to EEPROM input signal same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.

Input / Output Circuit

1. Output Circuit

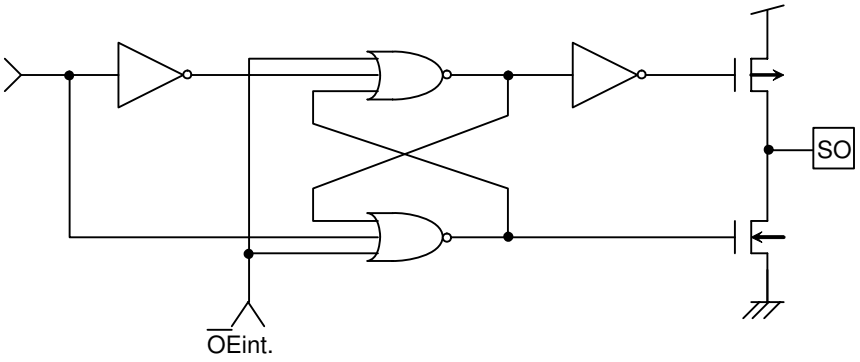


Figure 55. SO Output Equivalent Circuit

2. Input Circuit

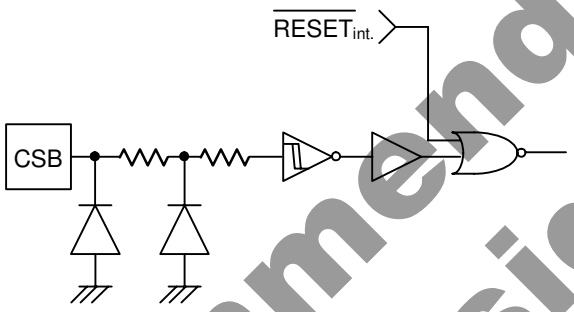


Figure 56. CSB Input Equivalent Circuit

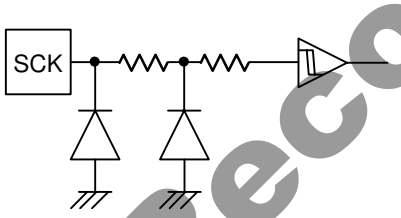


Figure 57. SCK Input Equivalent Circuit

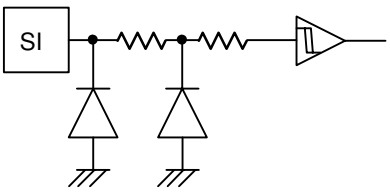


Figure 58. SI Input Equivalent Circuit

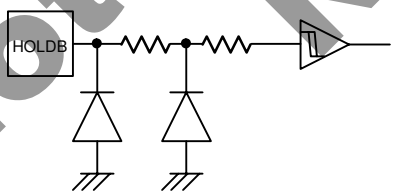


Figure 59. HOLDB Input Equivalent Circuit

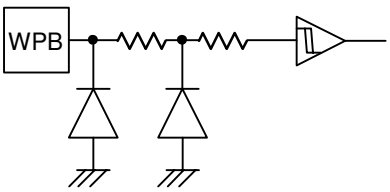
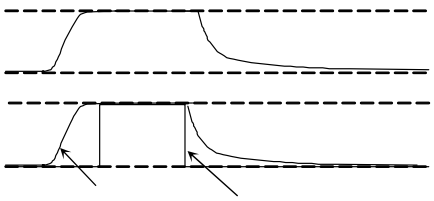


Figure 60. WPB Input Equivalent Circuit

Notes on Power ON/OFF

1. At Power ON/OFF, Set CSB "H" (=V_{CC}).

When CSB is "L", this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CSB "H". (When CSB is in "H" status, all inputs are canceled.)



(Good example) CSB terminal is pulled up to $V_{CC.}$

At power OFF, take 10ms or higher before supply. If power is turned on without observing this condition, the IC internal circuit may not be reset, which please note.

(Bad example) CSB terminal is "L" at power ON/OFF.

In this case, CSB always becomes "L" (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes.

Even when CSB input is High-Z, the status becomes like this case, which please note.

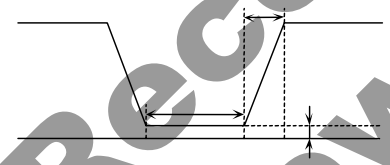
2. LVCC Circuit

LVCC (V_{CC}-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ =1.9V) or below, it prevent data rewrite.

3. P.O.R. Circuit

This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following t_R, t_{OFF}, and V_{bot} are not satisfied, it may become write enable status owing to noises and the likes.

Recommended conditions of t_R, t_{OFF}, V_{bot}



t_R	t_{OFF}	V_{bot}
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Noise Countermeasures

1. V_{CC} Noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1µF) between IC V_{CC} and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board V_{CC} and GND.

2. SCK Noise

When the rise time (t_R) of SCK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysterisis width of this circuit is set about 0.2V, if noises exist at SCK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time (t_R) of SCK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

3. WPB Noise

During execution of write status register command, if there exist noises on WPB pin, mistake in recognition may occur and forcible cancellation may result, which please note. To avoid this, a Schmitt trigger circuit is built in WPB input. In the same manner, a Schmitt trigger circuit is built in CSB input, SI input and HOLDB input too.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

12. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Ordering Information

B R 2 5 H x x x x - W C E 2

Bus type
25 : SPI

Operating Temperature
H : -40°C to +125°C

Capacity
010=1K 020=2K 040=4K
080=8K 160=16K 320=32K

Package
F :SOP8
FJ :SOP-J8
FVT :TSSOP-B8

W : Double Cell
C : For Automotive Application

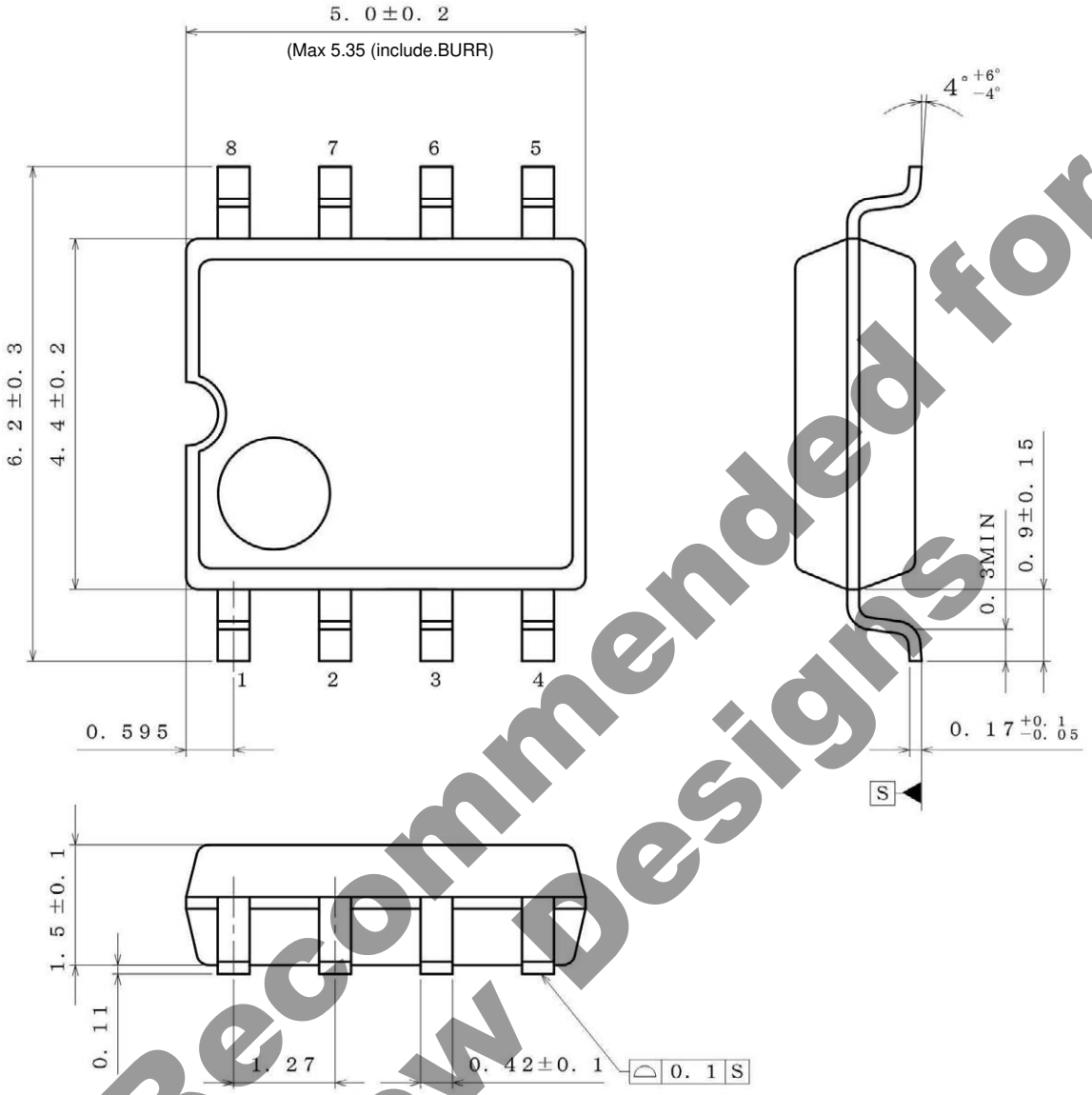
Packaging and forming specification
E2 :Embossed tape and reel

Lineup

Capacity	Package		Orderable Part Number
	Type	Quantity	
1K	SOP8	Reel of 2500	BR25H010F-WCE2
	SOP-J8	Reel of 2500	BR25H010FJ-WCE2
	TSSOP-B8	Reel of 3000	BR25H010FVT-WCE2
2K	SOP8	Reel of 2500	BR25H020F-WCE2
	SOP-J8	Reel of 2500	BR25H020FJ-WCE2
	TSSOP-B8	Reel of 3000	BR25H020FVT-WCE2
4K	SOP8	Reel of 2500	BR25H040F-WCE2
	SOP-J8	Reel of 2500	BR25H040FJ-WCE2
	TSSOP-B8	Reel of 3000	BR25H040FVT-WCE2
8K	SOP8	Reel of 2500	BR25H080F-WCE2
	SOP-J8	Reel of 2500	BR25H080FJ-WCE2
	TSSOP-B8	Reel of 3000	BR25H080FVT-WCE2
16K	SOP8	Reel of 2500	BR25H160F-WCE2
	SOP-J8	Reel of 2500	BR25H160FJ-WCE2
	TSSOP-B8	Reel of 3000	BR25H160FVT-WCE2
32K	SOP8	Reel of 2500	BR25H320F-WCE2
	SOP-J8	Reel of 2500	BR25H320FJ-WCE2

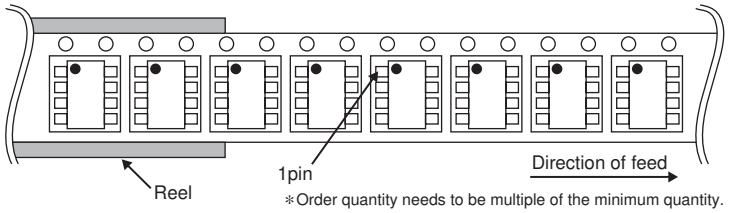
Physical Dimension, Tape and Reel Information

Package Name	SOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.