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Serial EEPROM Series Automotive EEPROM
125℃ Operation SPI BUS EEPROM

BR25H128-2C

●General Description

BR25H128-2C is a serial EEPROM of SPI BUS interface method.

●Features

- High speed clock action up to 10MHz (Max.)
- Wait function by HOLDB terminal.
- Part or whole of memory arrays settable as read only memory area by program.
- 2.5V to 5.5V single power source action most suitable for battery use.
- Page write mode useful for initial value write at factory shipment.
- For SPI bus interface (CPOL, CPHA)=(0, 0), (1, 1)
- Self-timed programming cycle.
- Low Supply Current
  At write operation (5V) : 1.2mA (Typ.)
  At read operation (5V) : 1.0mA (Typ.)
  At standby operation (5V) : 0.1μA (Typ.)
- Address auto increment function at read operation
- Prevention of write mistake
  Write prohibition at power on.
  Write prohibition by command code (WRDI).
  Write prohibition by WPB pin.
  Write prohibition block setting by status registers (BP1, BP0).
  Prevention of write mistake at low voltage.
- SOP8, SOP-J8 Package
- Data at shipment Memory array: FFh, status register WPEN, BP1, BP0 : 0
- More than 100 years data retention.
- More than 1 million write cycles.
- AEC-Q100 Qualified.

●Package

SOP8
5.00mm x 6.20mm x 1.71mm

SOP-J8
4.90mm x 6.00mm x 1.65mm

●Page write

Number of pages	64 Byte
Product Number	BR25H128-2C

●BR25H128-2C

Capacity	Bit Format	Product Number	Supply Voltage	SOP8	SOP-J8
128Kbit	16Kx8	BR25H128-2C	2.5V to 5.5V	●	●

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	VCC	-0.3 to +6.5	V
Permissible Dissipation	Pd	0.56(SOP8) *1	W
		0.56(SOP-J8) *2	
Storage Temperature Range	Tstg	-65 to +150	°C
Operating Temperature Range	Topr	-40 to +125	°C
Terminal Voltage	—	-0.3 to VCC+0.3	V
Electrostatic Discharge Voltage (Human Body Model)	V_{ESD}	-6000 to +6000	V

・When using at Ta=25℃ or higher, 4.5mW (*1,*2)to be reduced per 1℃

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

●Memory cell characteristics (VCC=2.5V to 5.5V)

Parameter	Limits			Unit	Condition
	Min.	Typ.	Max.		
Write Cycles *3	1,000,000	—	—	Cycles	Ta≦85°C
	500,000	—	—	Cycles	Ta≦105°C
	300,000	—	—	Cycles	Ta≦125°C
Data Retention *3	100	—	—	Years	Ta≦25°C
	60	—	—	Years	Ta≦105°C
	50	—	—	Years	Ta≦125°C

*3: Not 100% TESTED

●Recommended Operating Ratings

Parameter	Symbol	Limits	Unit
Supply Voltage	VCC	2.5 to 5.5	V
Input Voltage	Vin	0 to VCC	

●Input / output capacity (Ta=25°C, frequency=5MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Capacity *4	C_{IN}	V_{IN}=GND	—	8	pF
Output Capacity *4	C_{OUT}	V_{OUT}=GND	—	8	

*4: Not 100% TESTED

●DC characteristics (Unless otherwise specified, Ta=-40°C to +125°C, VCC=2.5V to 5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Input High Voltage	VIH	0.7xVCC	—	VCC +0.3	V	2.5V≦VCC≦5.5V
Input Low Voltage	VIL	-0.3	—	0.3x VCC	V	2.5V≦VCC≦5.5V
Output Low Voltage	VOL	0	—	0.4	V	IOL=2.1mA
Output High Voltage	VOH	VCC-0.5	—	VCC	V	IOH=-0.4mA
Input Leakage Current	ILI	-2	—	+2	μA	V_{IN}=0V to VCC
Output Leakage Current	ILO	-2	—	+2	μA	V_{OUT}=0V to VCC, CSB=VCC
Supply Current (WRITE)	ICC1	—	—	2.5	mA	VCC=2.5V,fSCK=5MHz, tE/W=4ms VIH/VIL=0.9VCC/0.1VCC, SO=OPEN Byte write, Page write, Write status register
	ICC2	—	—	5.5	mA	VCC=5.5V,fSCK=5 or 10 MHz, tE/W=4ms VIH/VIL=0.9VCC/0.1VCC, SO=OPEN Byte write, Page write, Write status register
Supply Current (READ)	ICC3	—	—	1.5	mA	VCC=2.5V,fSCK=5MHz VIH/VIL=0.9VCC/0.1VCC, SO=OPEN Read, Read status register
	ICC4	—	—	2.0	mA	VCC=5.5V,fSCK=5MHz VIH/VIL=0.9VCC/0.1VCC, SO=OPEN Read, Read status register
	ICC5	—	—	4.0	mA	VCC=5.5V,fSCK=10MHz VIH/VIL=0.9VCC/0.1VCC, SO=OPEN Read, Read status register
Standby Current	ISB	—	—	10	μA	VCC=5.5V CSB=HOLDB=WPB=VCC, SCK=SI=VCC or =GND, SO=OPEN

●AC characteristics (Ta=-40°C to +125°C, unless otherwise specified, load capacity C_{L1}=100pF)

Parameter	Symbol	2.5V≦VCC≦5.5V			4.5V≦VCC≦5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCK Frequency	fSCK	—	—	5	—	—	10	MHz
SCK High Time	tSCKWH	85	—	—	40	—	—	ns
SCK Low Time	tSCKWL	85	—	—	40	—	—	ns
CSB High Time	tCS	85	—	—	40	—	—	ns
CSB Setup Time	tCSS	90	—	—	30	—	—	ns
CSB Hold Time	tCSH	85	—	—	30	—	—	ns
SCK Setup Time	tSCKS	90	—	—	30	—	—	ns
SCK Hold Time	tSCKH	90	—	—	30	—	—	ns
SI Setup Time	tDIS	20	—	—	10	—	—	ns
SI Hold Time	tDIH	30	—	—	10	—	—	ns
Data Output Delay Time1	tPD1	—	—	60	—	—	40	ns
Data Output Delay Time2 (C_{L2}=30pF)	tPD2	—	—	50	—	—	30	ns
Output Hold Time	tOH	0	—	—	0	—	—	ns
Output Disable Time	tOZ	—	—	100	—	—	40	ns
HOLDB Setting Setup Time	tHFS	0	—	—	0	—	—	ns
HOLDB Setting Hold Time	tHFH	40	—	—	30	—	—	ns
HOLDB Release Setup Time	tHRS	0	—	—	0	—	—	ns
HOLDB Release Hold Time	tHRH	70	—	—	30	—	—	ns
Time from HOLDB to Output High-Z	tHOZ	—	—	100	—	—	40	ns
Time from HOLDB to Output Change	tHPD	—	—	70	—	—	40	ns
SCK Rise Time*1	tRC	—	—	1	—	—	1	µs
SCK Fall Time*1	tFC	—	—	1	—	—	1	µs
OUTPUT Rise Time*1	tRO	—	—	40	—	—	40	ns
OUTPUT Fall Time*1	tFO	—	—	40	—	—	40	ns
Write Time	tE/W	—	—	4	—	—	4	ms

*1 NOT 100% TESTED

●AC measurement conditions

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Load Capacity 1	C_{L1}	—	—	100	pF
Load Capacity 2	C_{L2}	—	—	30	pF
Input Rise Time	—	—	—	50	ns
Input Fall Time	—	—	—	50	ns
Input Voltage	—	0.2VCC/0.8VCC			V
Input / Output Judgment Voltage	—	0.3VCC/0.7VCC			V

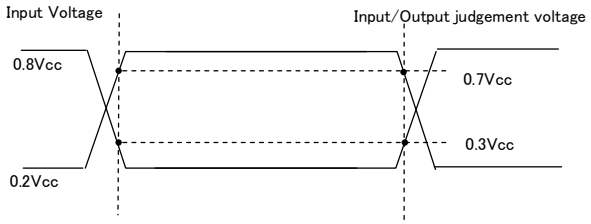


Figure 1. Input/Output judgment voltage

●Serial Input / Output Timing

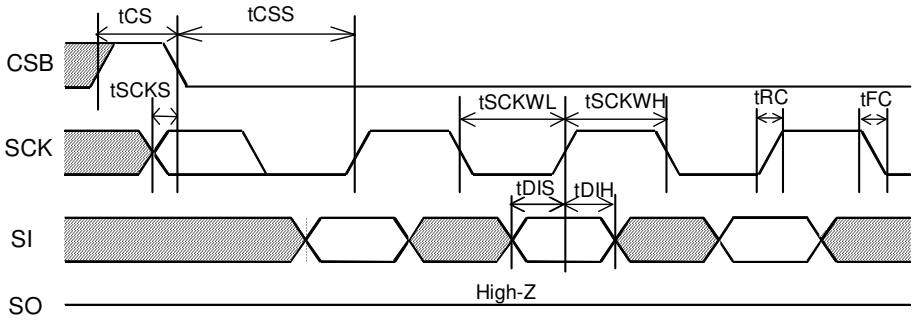


Figure 2. Input timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the most significant bit MSB.

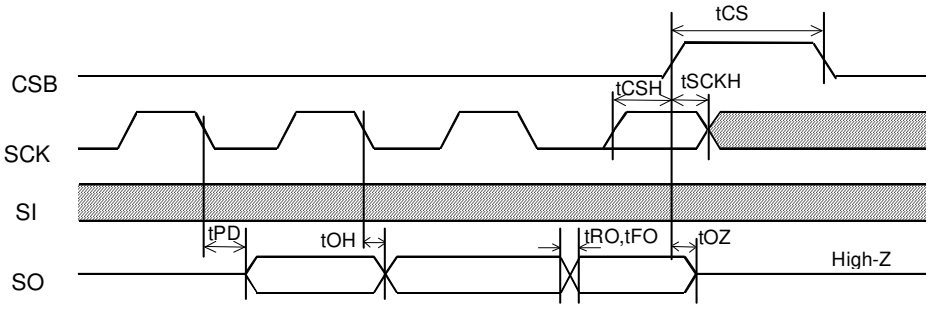


Figure 3. Input / Output timing

SO is output in sync with data fall edge of SCK. Data is output from the most significant bit MSB.

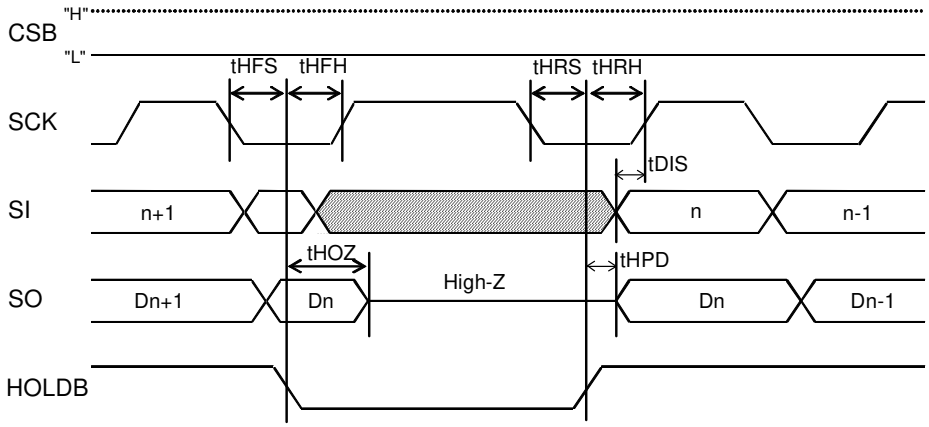


Figure 4. HOLD timing

●Block diagram

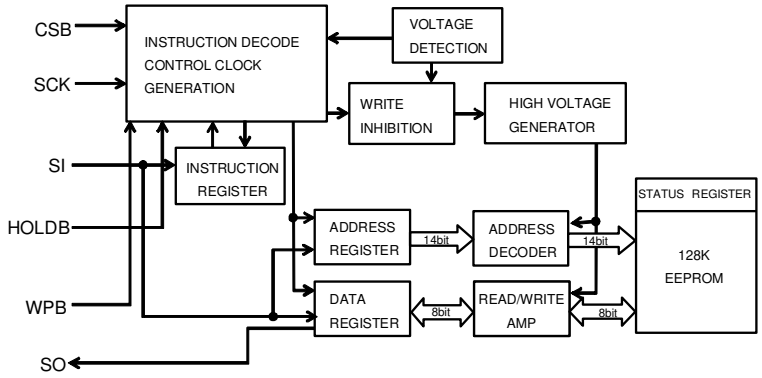


Figure 5. Block diagram

●Pin Configuration

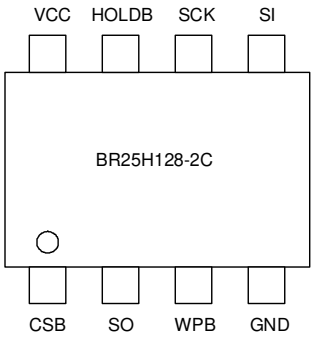


Figure 6. Pin assignment diagram

●Pin Descriptions

Terminal number	Terminal name	Input /Output	Function
1	CSB	Input	Chip select input
2	SO	Output	Serial data output
3	WPB	Input	Write protect input Write status register command is prohibited.
4	GND	—	All input / output reference voltage, 0V
5	SI	Input	Start bit, ope code, address, and serial data input
6	SCK	Input	Serial clock input
7	HOLDB	Input	Hold input Command communications may be suspended temporarily (HOLD status)
8	VCC	—	Power source to be connected

●Typical Performance Curves

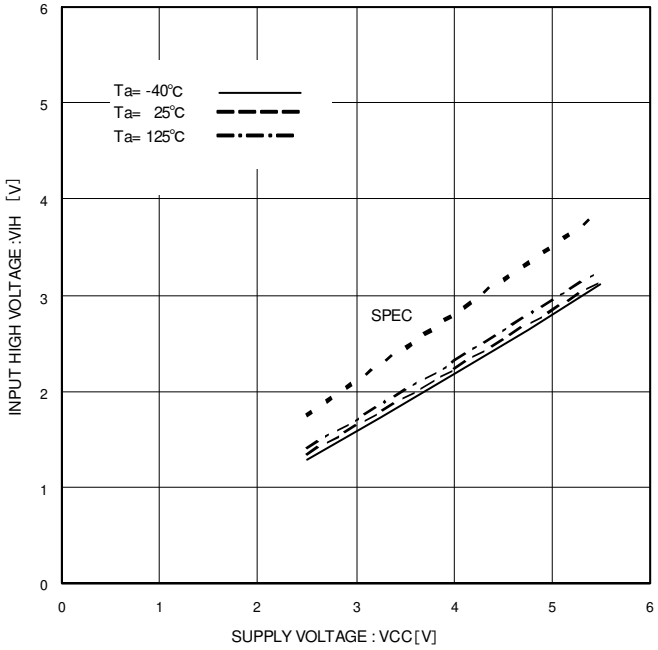


Figure 7. Input High Voltage VIH
(CSB,SCK,SI,HOLDB,WPB)

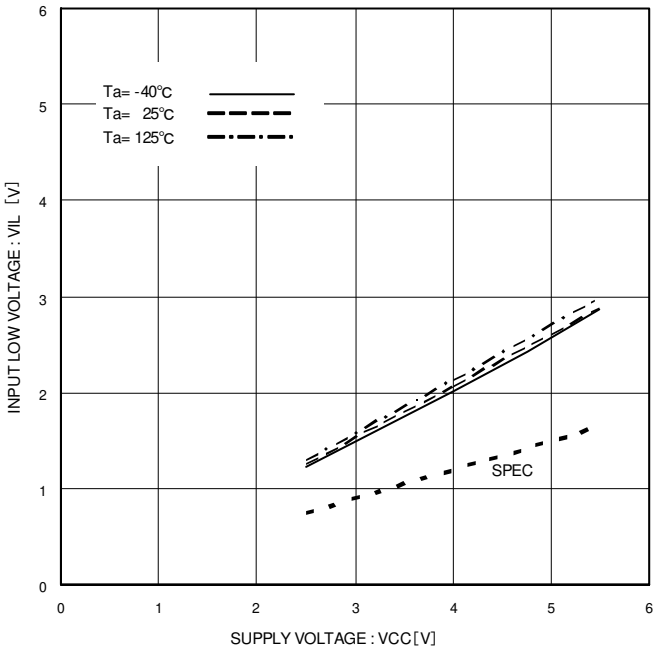


Figure 8. Input Low Voltage VIL
(CSB,SCK,SI,HOLDB,WPB)

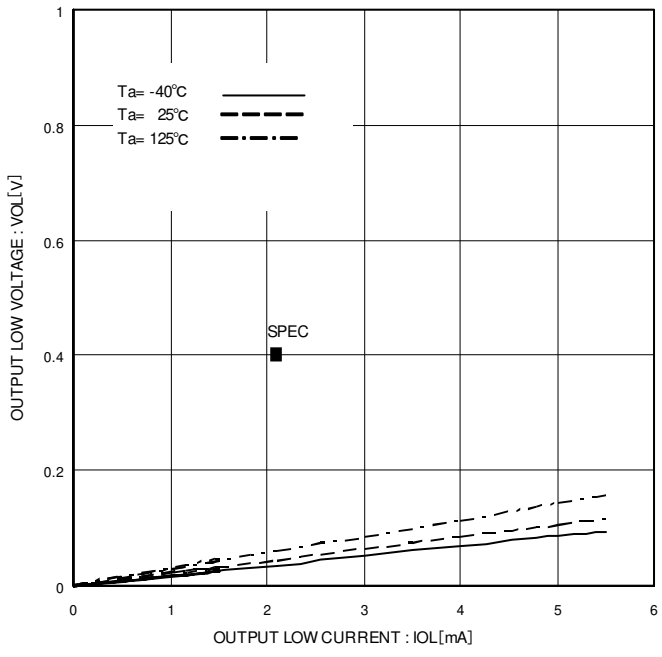


Figure 9. Output Low Voltage VOL, IOL (Vcc=2.5V)

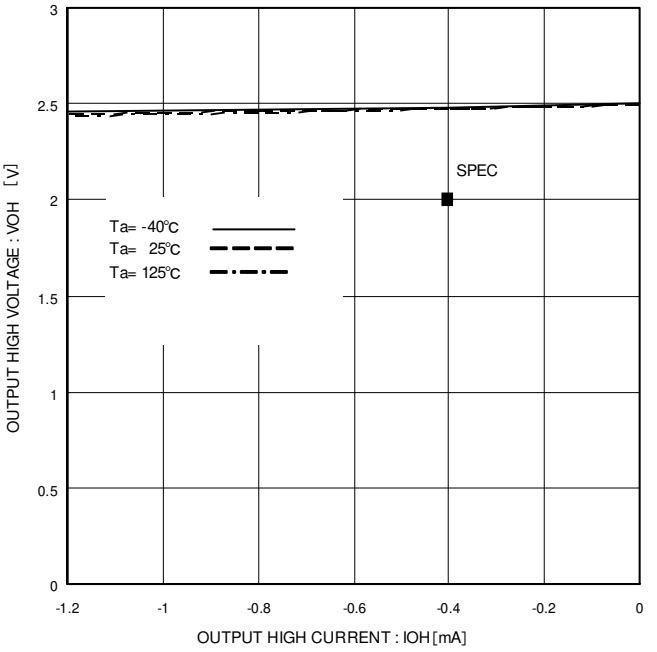


Figure 10. Output High Voltage VOH, IOH (Vcc=2.5V)

●Typical Performance Curves - Continued

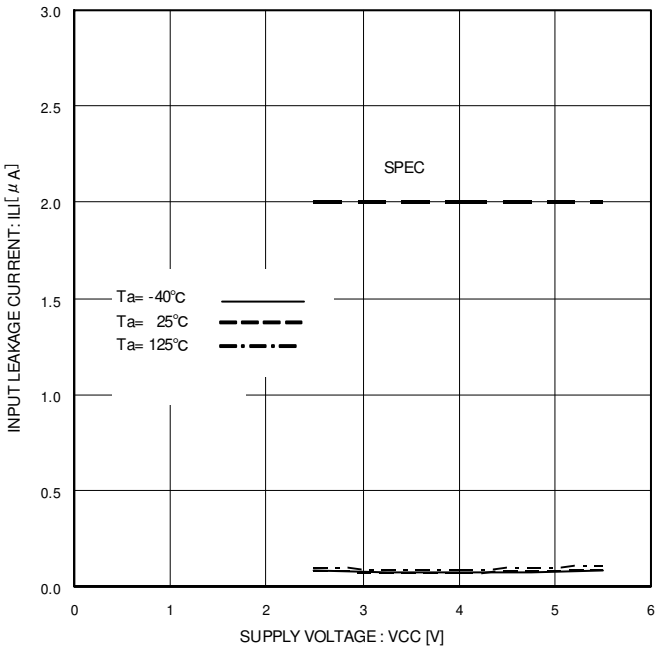


Figure 11. Input Leakage Current ILI (CSB,SCK,SI,HOLDB,WPB)

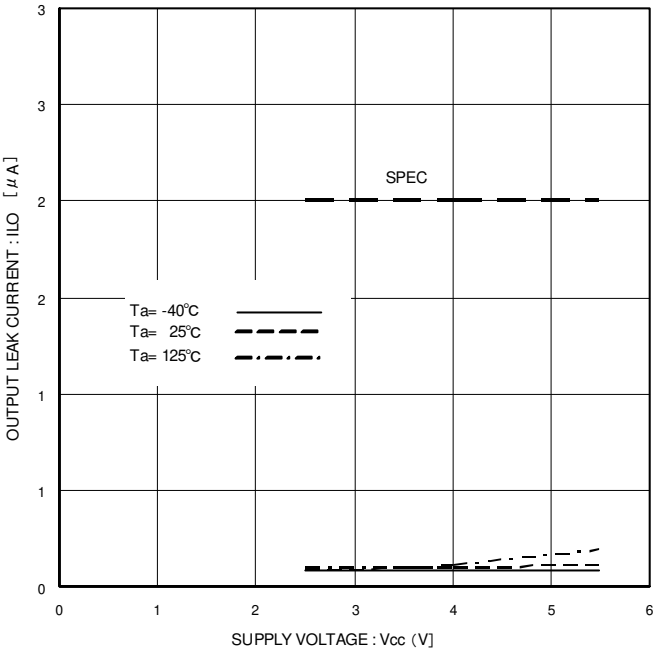


Figure 12. Output Leakage Current ILO(SO)(Vcc=5.5V)

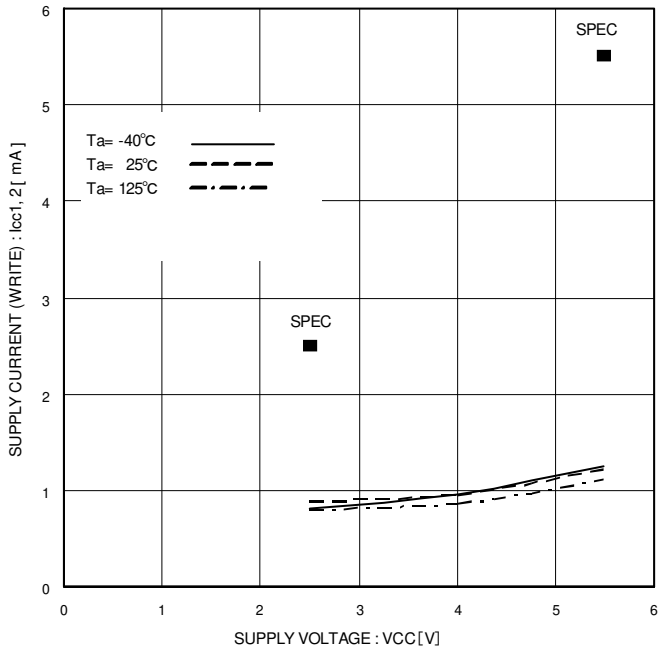


Figure 13. Supply Current (WRITE) ICC1,2

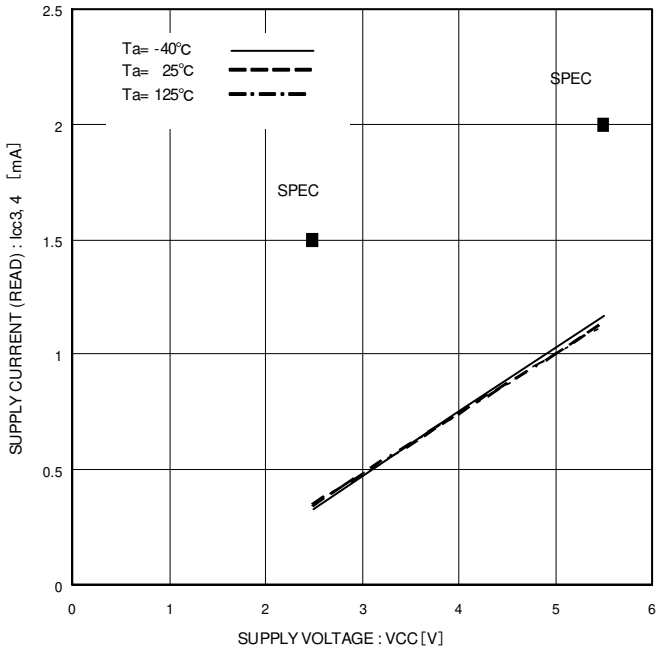


Figure 14. Supply Current (READ) ICC3,4

●Typical Performance Curves - Continued

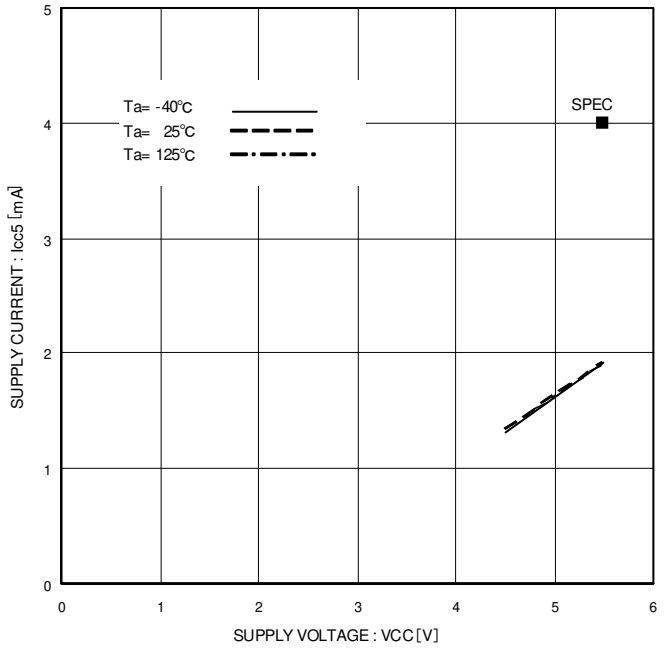


Figure 15. Supply Current (READ) ICC5

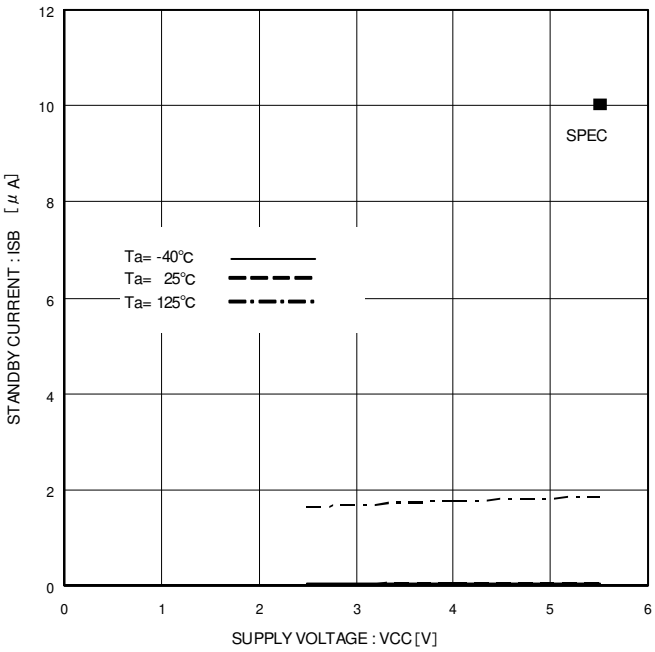


Figure.16 Standby Current ISB

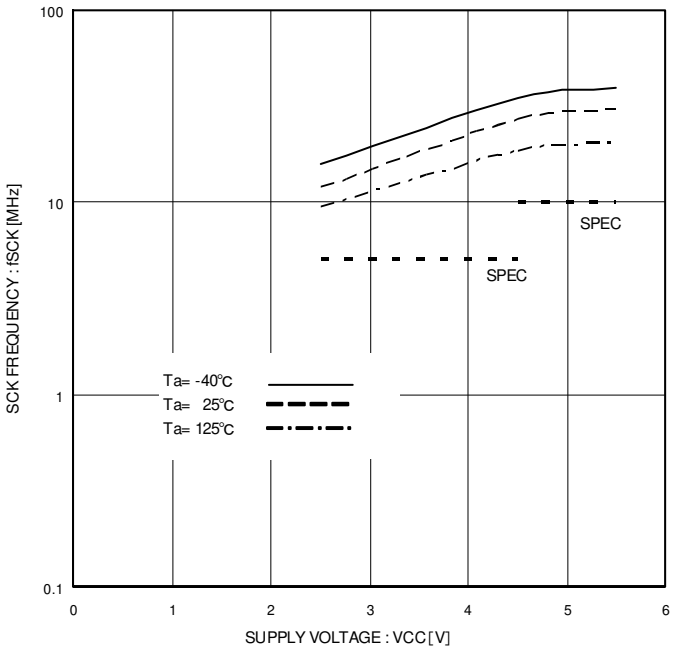


Figure 17. SCK Frequency fSCK

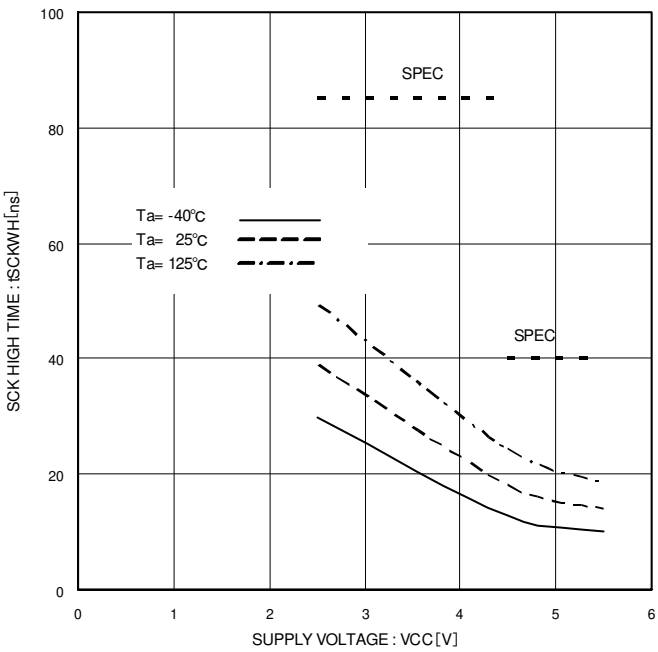


Figure 18. SCK High Time tSCKWH

●Typical Performance Curves - Continued

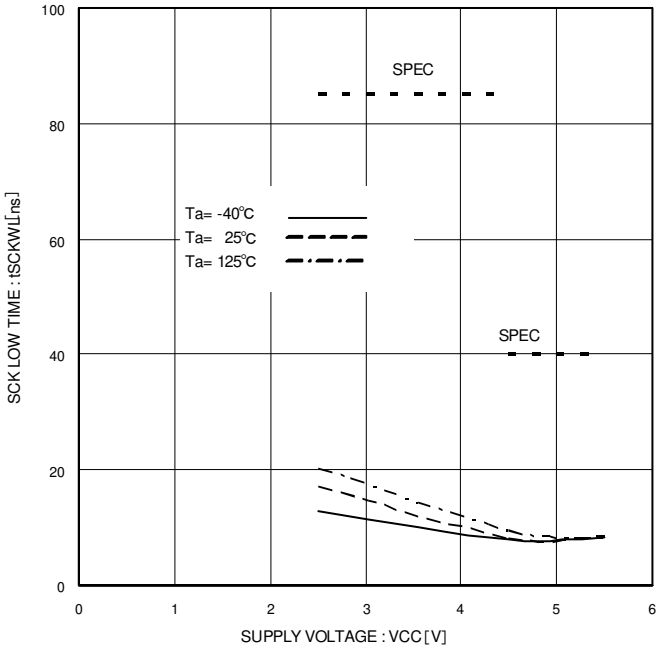


Figure 19. SCK Low Time tSCKWL

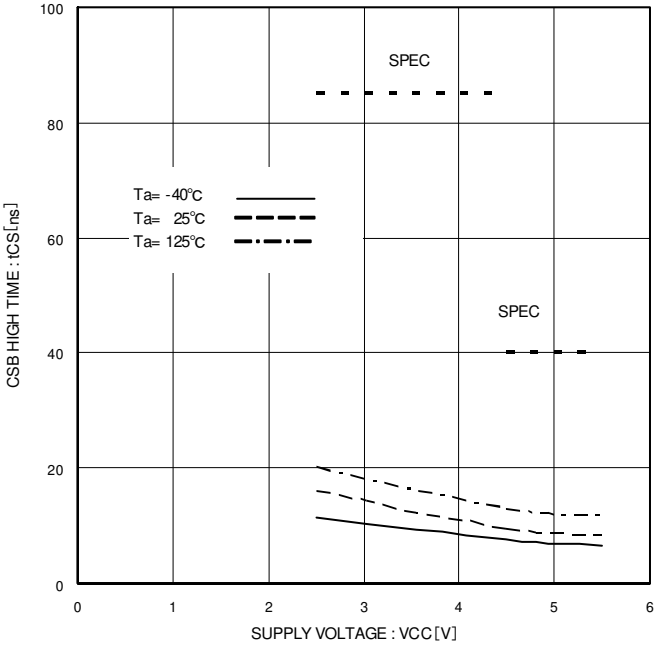


Figure 20. CSB High Time tCS

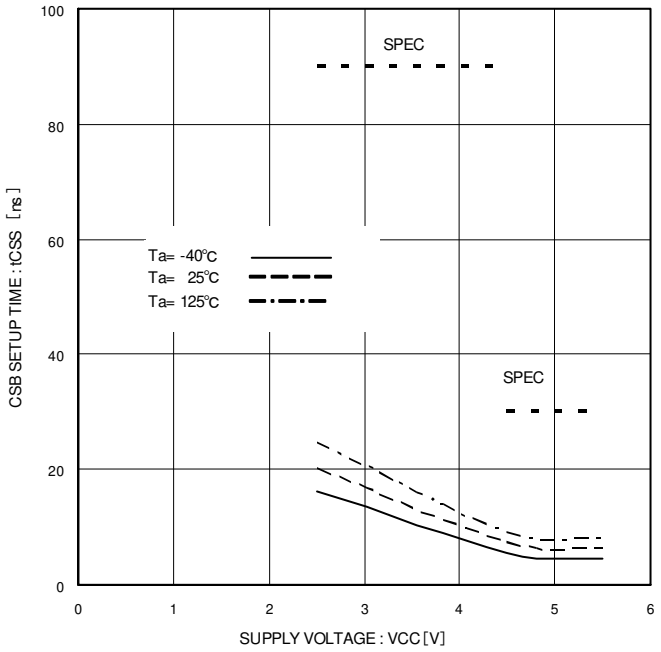


Figure 21. CSB Setup Time tCSS

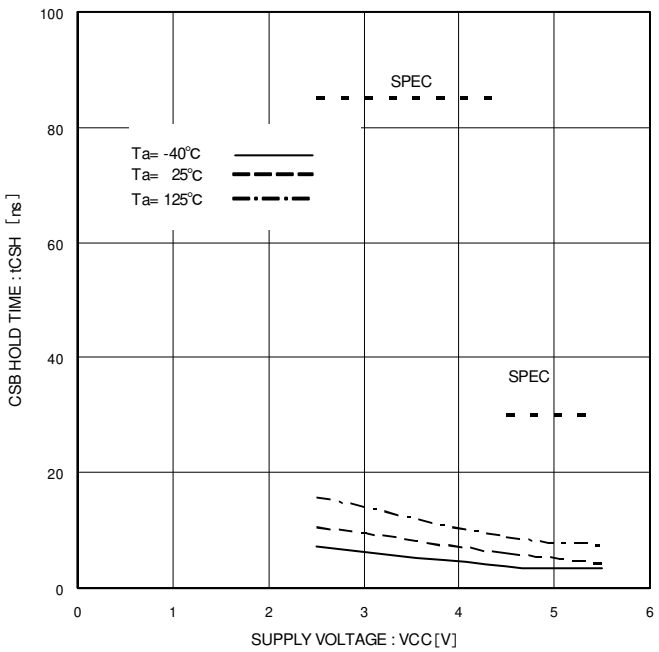


Figure 22. CSB Hold Time tCSH

●Typical Performance Curves - Continued

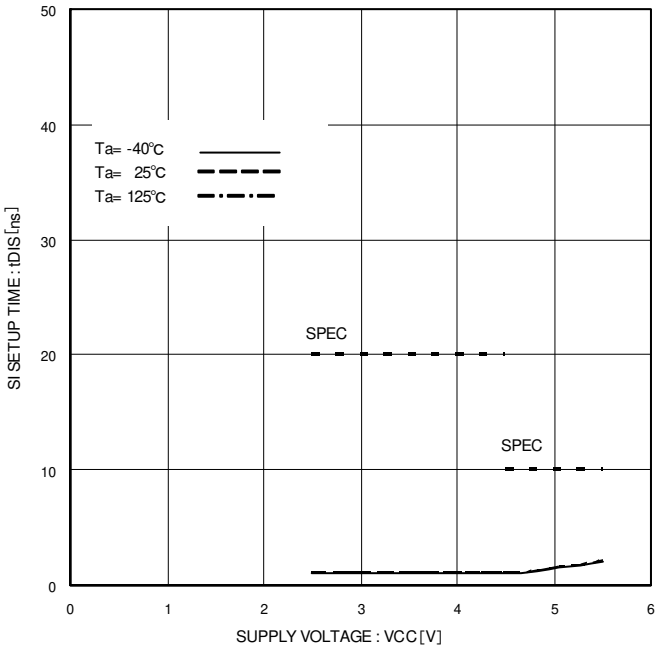


Figure 23. SI Setup Time tDIS

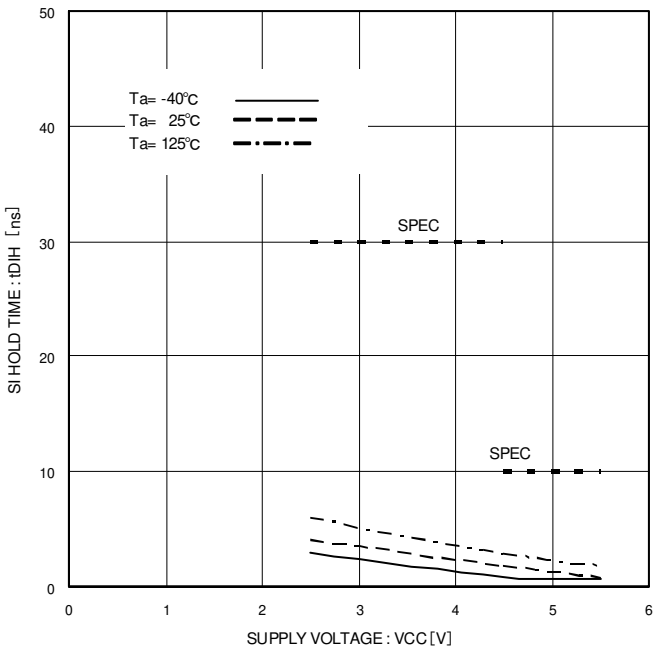


Figure 24. SI Hold Time tDIH

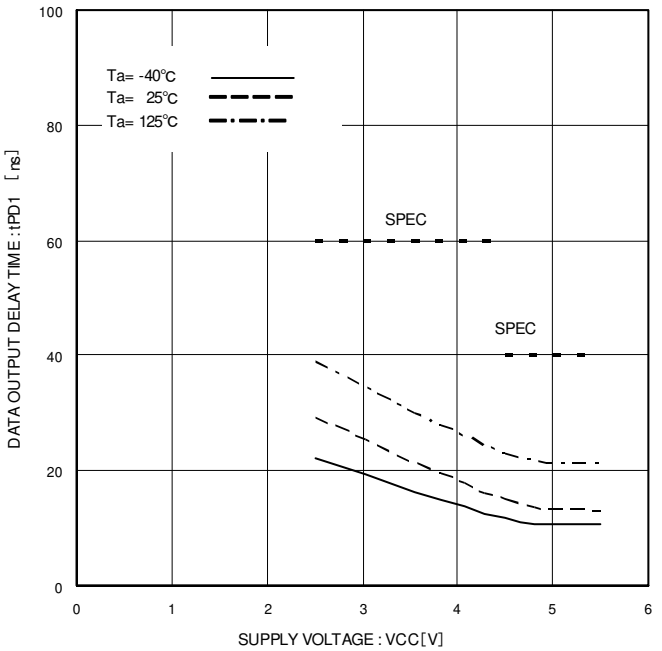


Figure 25. Data Output Delay Time tPD1 (CL=100pF)

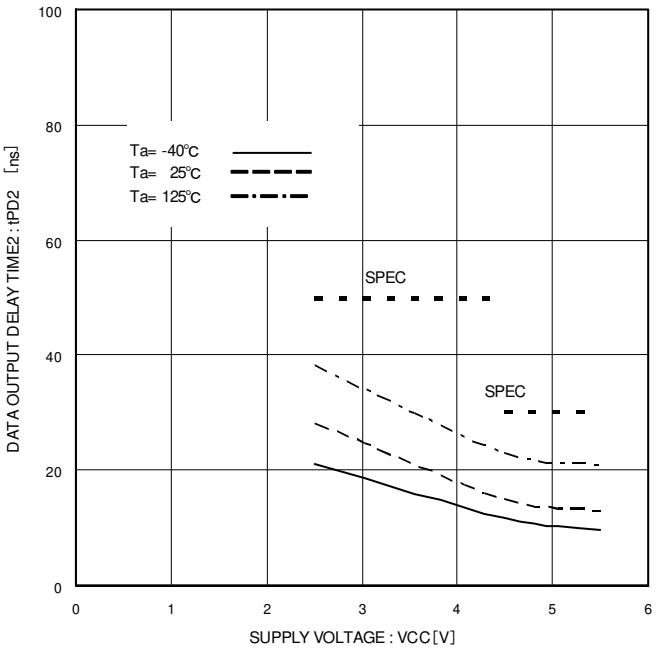


Figure 26. Data Output Delay Time tPD2 (CL=30pF)

●Typical Performance Curves - Continued

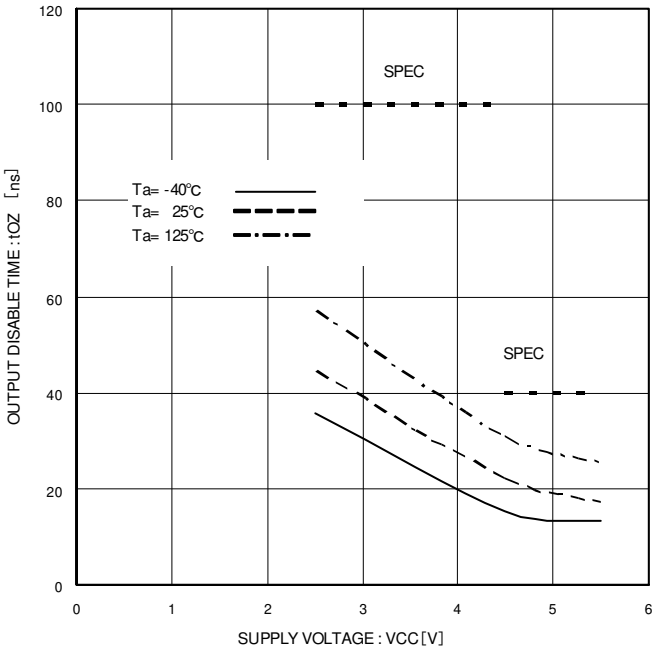


Figure 27.Output Disable Time tOZ

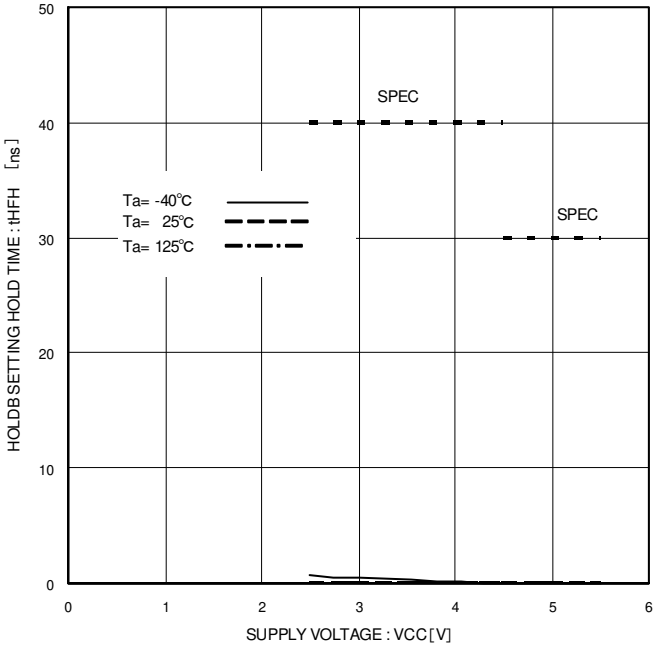


Figure 28. HOLDB Setting Hold Time tHFH

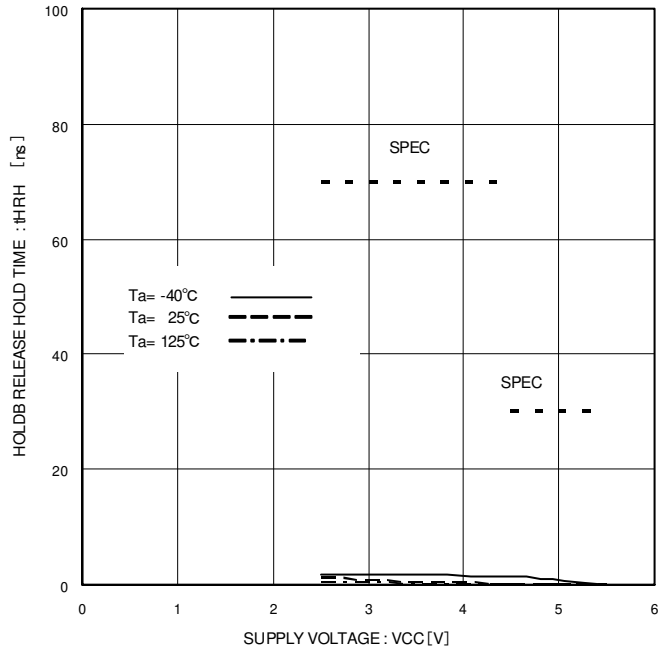


Figure 29. HOLDB Release Hold Time tHRH

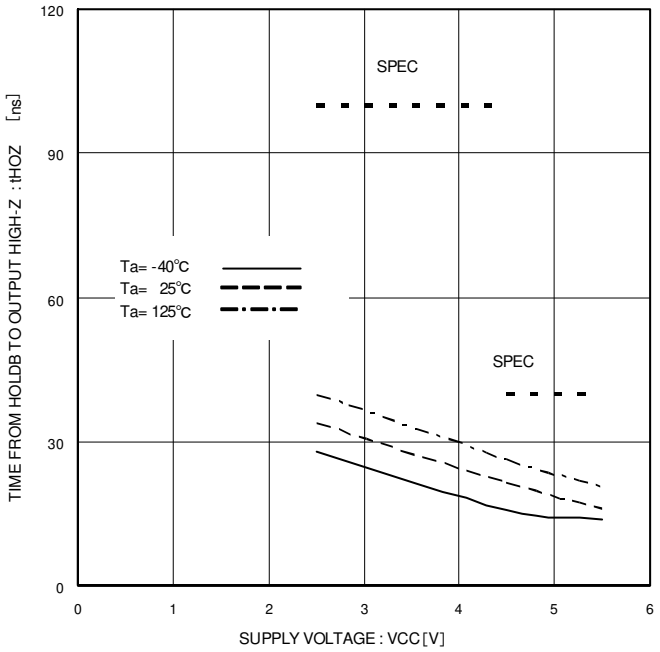


Figure 30. Time from HOLDB to Output High-Z tHOZ

●Typical Performance Curves - Continued

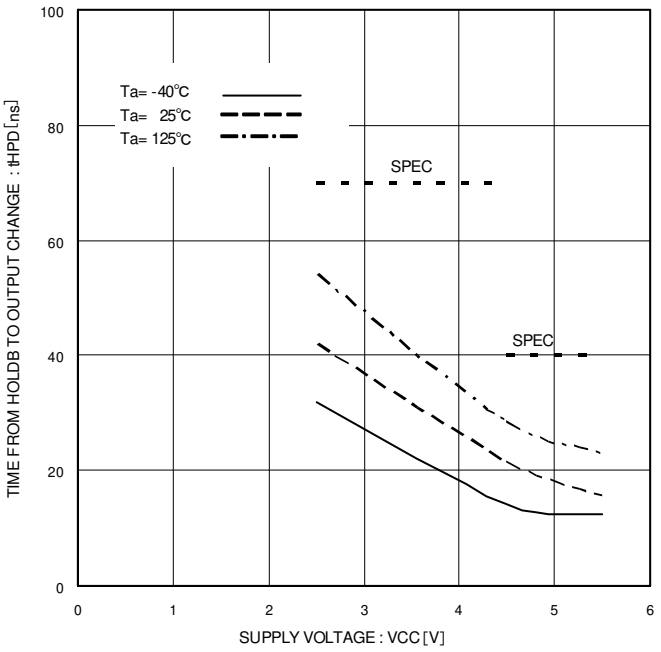


Figure 31. Time from HOLDB to Output Change tHPD

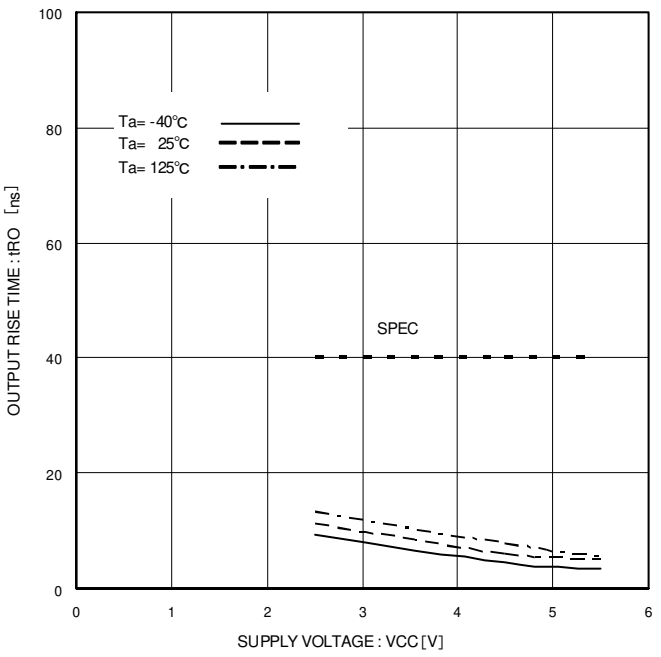


Figure 32. Output Rise Time tRO

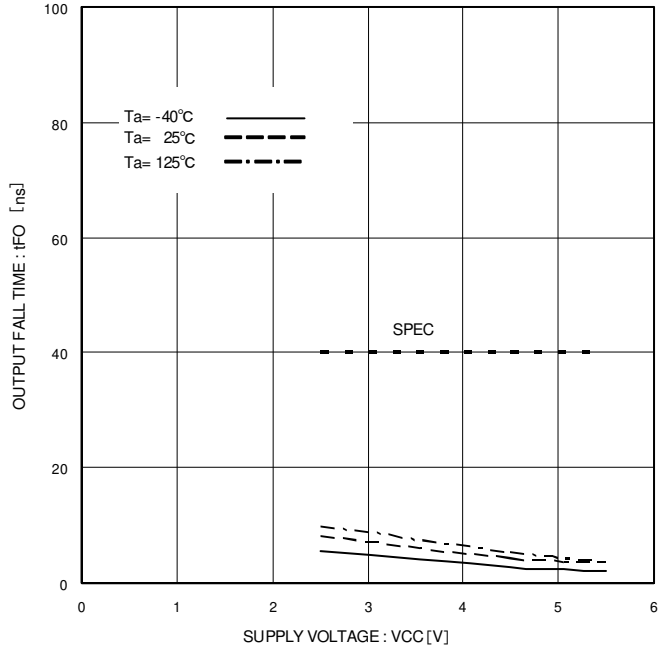


Figure 33. Output Fall Time tFO

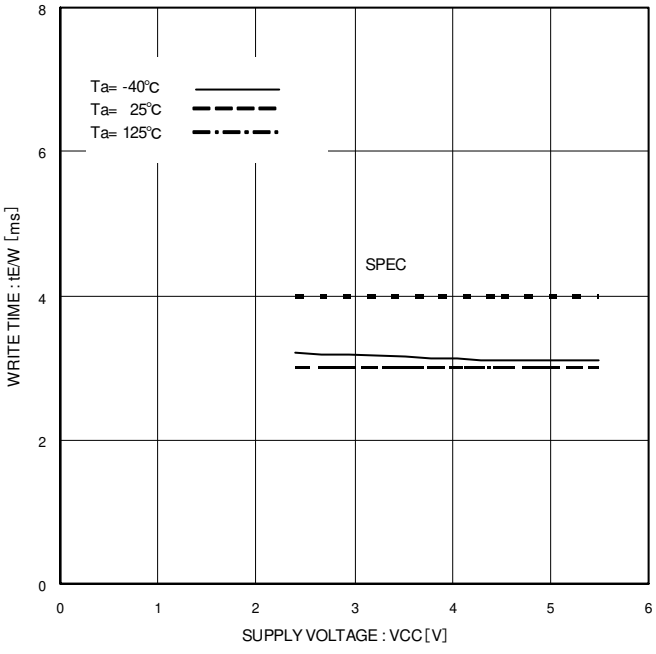


Figure 34. Write Cycle Time tE/W

●Features

○Status registers

This IC has status registers. The status registers are of 8 bits and express the following parameters.
BP0 and BP1 can be set by write status register command. These 2 bits are memorized into the EEPROM, therefore are valid even when power source is turned off.
Number of data rewrite times and data hold time are same as characteristics of the EEPROM.
WEN can be set by write enable command and write disable command. WEN becomes write disable status when power source is turned off. $\overline{R}$/B is for write confirmation, therefore cannot be set externally.
The value of status register can be read by read status command.

●Status registers

Product number	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR25H128-2C	WPEN	0	0	0	BP1	BP0	WEN	$\overline{R}$/B

bit	Memory location	Function	Contents
WPEN	EEPROM	WPB pin enable / disable designation bit WPEN=0=invalid , WPEN=1=valid	This enables / disables the functions of WPB pin.
BP1 BP0	EEPROM	EEPROM write disable block designation bit	This designates the write disable area of EEPROM. Write designation areas of product numbers are shown below.
WEN	Register	Write and write status register write enable / disable status confirmation bit WEN=0=prohibited , WEN=1=permitted	This confirms prohibited status or permitted status of the write and the write status register.
$\overline{R}$/B	Register	Write cycle status (READY / BUSY) confirmation bit $\overline{R}$/B=0=READY , $\overline{R}$/B=1=BUSY	This confirms READY status or BUSY status of the write cycle.

●Write disable block setting

BP1	BP0	BR25H128-2C
0	0	None
0	1	3000h-3FFFh
1	0	2000h-3FFFh
1	1	0000h-3FFFh

○WPB pin

By setting WPB=LOW, write command is prohibited. As for BR25H128-2C, only when WPEN bit is set “1”, the WPB pin functions become valid. And the write command to be disabled at this moment is WRSR. However, when write cycle is in execution, no interruption can be made.

Product number	WRSR	WRITE
BR25H128-2C	Prohibition possible but WPEN bit “1”	Prohibition impossible

○HOLDB pin

By HOLDB pin, data transfer can be interrupted. When SCK=”0”, by making HOLDB from “1” into”0”, data transfer to EEPROM is interrupted. When SCK = “0”, by making HOLDB from “0” into “1”, data transfer is restarted.

●Command mode

Command		Contents	Ope codes	
WREN	Write enable	Write enable command	0000	0110
WRDI	Write disable	Write disable command	0000	0100
READ	Read	Read command	0000	0011
WRITE	Write	Write command	0000	0010
RDSR	Read status register	Status register read command	0000	0101
WRSR	Write status register	Status register write command	0000	0001

●Timing Chart

1. Write enable (WREN) / disable (WRDI) cycle

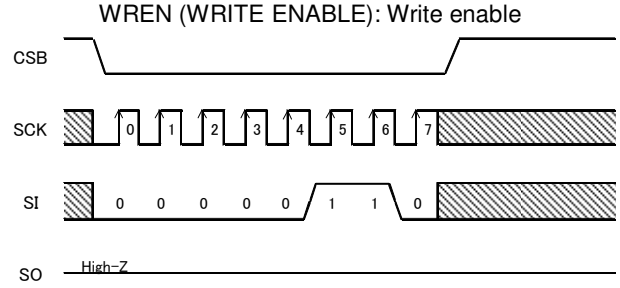


Figure 35. Write enable command

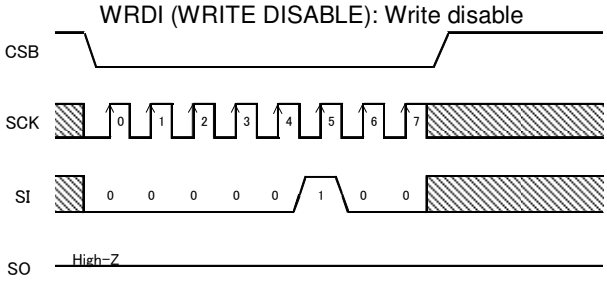


Figure 36. Write disable

○This IC has write enable status and write disable status. It is set to write enable status by write enable command, and it is set to write disable status by write disable command. As for these commands, set CSB LOW, and then input the respective ope codes. The respective commands accept command at the 7-th clock rise. Even with input over 7 clocks, command becomes valid.
When to carry out write and write status register command, it is necessary to set write enable status by the write enable command. If write or write status register command is input in the write disable status, commands are cancelled. And even in the write enable status, once write and write status register command is executed. It gets in the write disable status. After power on, this IC is in write disable status.

2. Read command (READ)

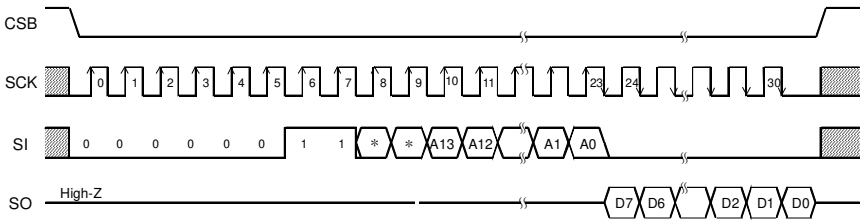


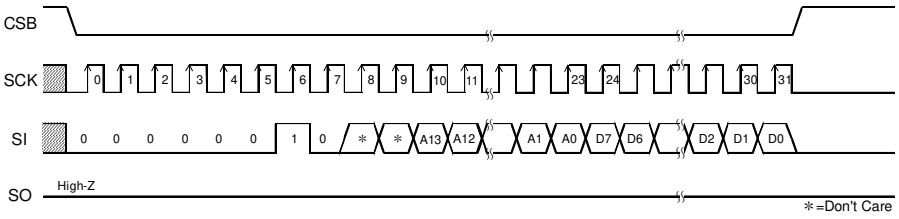
Figure 37. Read command

*=Don't Care

Product number	Address length
BR25H128-2C	A13-A0

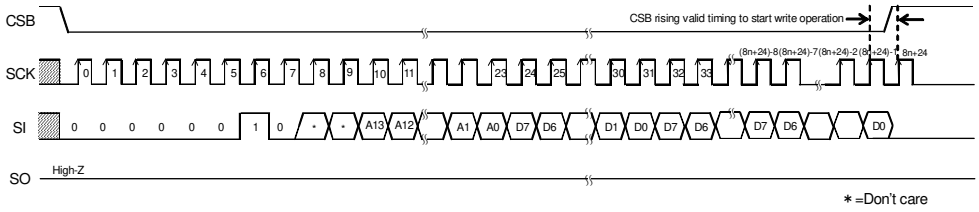
By read command, data of EEPROM can be read. As for this command, set CSB LOW, then input address after read ope code. EEPROM starts data output of the designated address. Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM. After reading data of the most significant address, by continuing increment read, data of the most insignificant address is read.

3. Write command (WRITE)



Product number	Address length
BR25H128-2C	A13-A0

Figure 38. Write command



n= up to 64 bytes

Figure 39. N Byte page write command

By write command, data of EEPROM can be written. As for this command, set CSB LOW, then input address and data after write ope code. Then, by making CSB HIGH, the EEPROM starts writing. The write time of EEPROM requires time of tE/W (Max 4ms). During tE/W, other than status read command is not accepted. Start CSB after taking the last data (D0), and before the next SCK clock starts. At other timing, write command is not executed, and this write command is cancelled. This IC has page write function, and after input of data for 1 byte (8 bits), by continuing data input without starting CSB, data up to 64 bytes can be written for one tE/W. In page write, the insignificant 6 bit of the designated address is incremented internally at every time when data of 1 byte is input and data is written to respective addresses. When data of the maximum bytes or higher is input, address rolls over, and previously input data is overwritten.

Write command is executed when CSB rises between the SCK clock rising edge to recognize the 8th bits of data input and the next SCK rising edge. At other timings the write command is not executed and cancelled (Figure.48 valid timing c). In page write, the CSB valid timing is every 8 bits. If CSB rises at other timings page write is cancelled together with the write command and the input data is reset.

This column addresses are Top address of this page

64byte

page0	0000h	0001h	0002h	・・・	003Eh	003Fh
page 1	0040h	0041h	0042h	・・・	007Eh	007Fh
page 2	0080h	0081h	0082h	・・・	00FEh	00FFh
・	・	・	・	・	・	・
・	・	・	・	・	・	・
・	・	・	・	・	・	・
page m-1	n-127	n-126	n-125	・・・	n-65	n-64
page *2 m	n-63	n-62	n-61	・・・	n-1	*1 n

This column addresses are the last address of this page

*1 n=16383d=3FFFh : BR25H128-2C
*2 m=255 : BR25H128-2C

Figure 40. EEPROM physical address for Page write command (64Byte)

○Example of Page write command

No.	Addresses of Page0	0000h	0001h	0002h	・・・・	003Eh	003Fh
①	Previous data	00h	01h	02h	・・・・	3Eh	3Fh
②	2 bytes input data	AAh	55h	-	・・・・	-	-
③	After No.②	AAh	55h	02h	・・・・	3Eh	3Fh
④	66 byte input data	AAh	55h	AAh	・・・・	AAh	55h
		FFh	00h	-	・・・・	-	-
⑤	After No.④	FFh	00h	AAh	・・・・	AAh	55h

a : In case of input the data of No.② which is 2 bytes page write command for the data of No.①, EEPROM data changes like No.③.

b : In case of input the data of No.④ which is 66 bytes page write command for the data of No.①, EEPROM data changes like No.⑤.

c : In case of a or b, when write command is cancelled, EEPROM data keep No.①.

In page write command, when data is set to the last address of a page (e.g. address “007Fh” of page 1), the next data will be set to the top address of the same page (e.g. address “0040h” of page 1). This is why page write address increment is available in the same page. As a reference, if of 64 bytes, page write command is executed for 2 bytes the data of the other 62 bytes without addresses will not be changed.

4. Status register write / read command

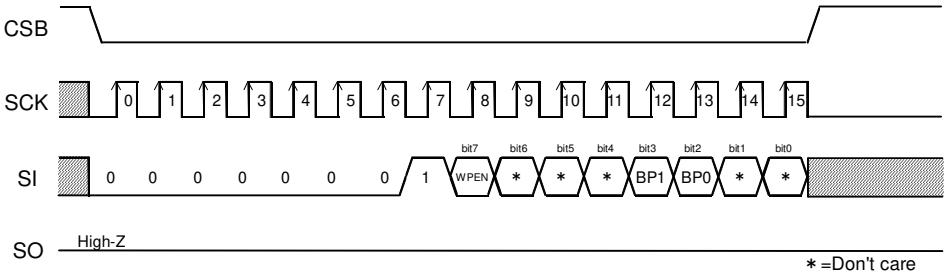


Figure 41. Status register write command

Write status register command can write status register data. The data can be written by this command are 3 bits, that is, WPEN (bit7), BP1 (bit3) and BP0 (bit2) among 8 bits of status register. By BP1 and BP0, write disable block of EEPROM can be set. As for this command, set CSB LOW, and input ope code of write status register, and input data. Then, by making CSB HIGH, EEPROM starts writing. Write time requires time of tE/W as same as write. As for CSB rise, start CSB after taking the last data bit (bit0), and before the next SCK clock starts. At other timing, command is cancelled. Write disable block is determined by BP1 and BP0, and the block can be selected from 1/4 of memory array, 1/2, and entire memory array. (Refer to the write disable block setting table.)
To the write disabled block, write cannot be made, and only read can be made.

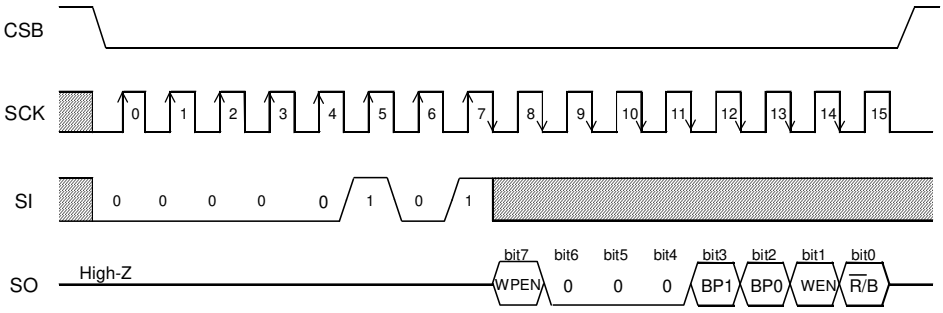


Figure 42. Status register read command

●At standby

○Current at standby

Set CSB “H”, and be sure to set SCK, SI, WPB, HOLDB input “L” or “H”. Do not input intermediate electric potential.

○Timing

As shown in Figure.43, at standby, when SCK is “H”, even if CSB is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB “H” status.

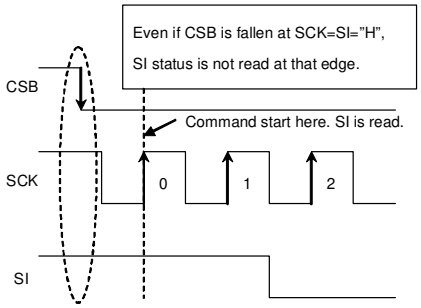


Figure 43. Operating timing

●WPB cancel valid area

WPB is normally fixed to “H” or “L” for use, but when WPB is controlled so as to cancel write status register command and write command, pay attention to the following WPB valid timing.

Write status register command is executed, by setting WPB = “L” in cancel valid area, command can be cancelled. The Data area (from 7clock fall to 16clock rise) becomes the cancel valid area. However, once write is started, any input cannot be cancelled. WPB input becomes Don’t Care, and cancellation becomes invalid.

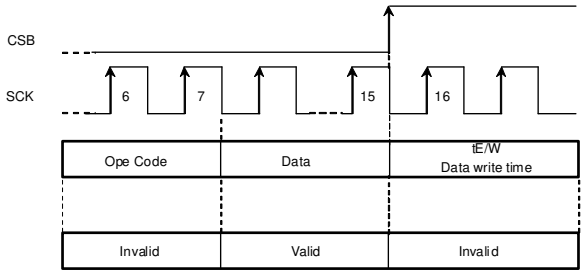


Figure 44. WPB valid timing (WRSR)

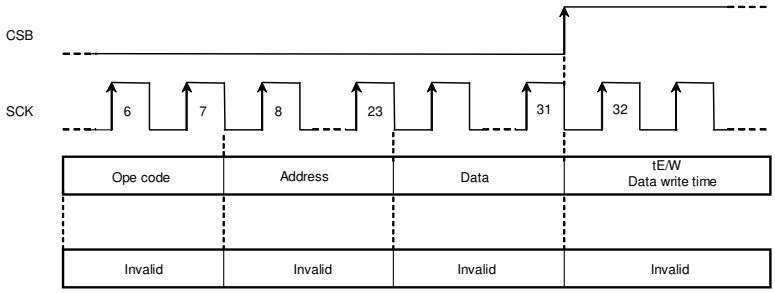


Figure 45. WPB valid timing (WRITE)

●HOLDB pin

By HOLDB pin, command communication can be stopped temporarily (HOLD status). The HOLDB pin carries out command communications normally when it is HIGH. To get in HOLD status, at command communication, when SCK=LOW, set the HOLDB pin LOW. At HOLD status, SCK and SI become Don’t Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the HOLDB pin HIGH when SCK=LOW. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at read, after release of HOLD status, by starting A4 address input, read can be restarted. When in HOLD status, leave CSB LOW. When it is set CSB=HIGH in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

●Method to cancel each command

○READ

・Method to cancel : cancel by CSB = “H”

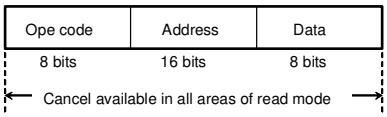


Figure 46 READ cancel valid timing

○RDSR

・Method to cancel : cancel by CSB = “H”

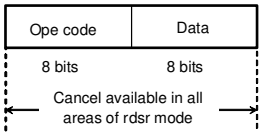


Figure 47 RDSR cancel valid timing

○WRITE,PAGE WRITE

a : Ope code, address input area.
Cancellation is available by CSB=”H”

b : Data input area (D7 to D1 input area)
Cancellation is available by CSB=”H”

c : Data input area (D0 area)
When CSB is started, write starts.
After CSB rise, cancellation cannot be made by any means.

d : tE/W area.
Cancellation is available by CSB = “H”. However, when write starts (CSB is started) in the area c, cancellation cannot be made by any means. And by inputting on SCK clock, cancellation cannot be made. In page write mode, there is write enable area at every 8 clocks.

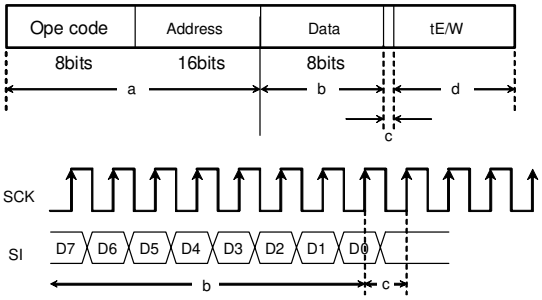


Figure 48. WRITE cancel valid timing

Note 1) If VCC is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
Note 2) If CSB is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = “L” area. As for SCK rise, assure timing of tCSS / tCSH or higher.

○WRSR

a : From ope code to 15 rise.
Cancel by CSB =”H”.

b : From 15 clock rise to 16 clock rise (write enable area).
When CSB is started, write starts.
After CSB rise, cancellation cannot be made by any means.

c : After 16 clock rise.
Cancel by CSB=”H”. However, when write starts (CSB is started) in the area b, cancellation cannot be made by any means.
And, by inputting on SCK clock, cancellation cannot be made.

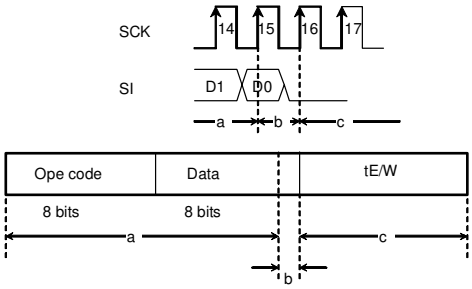


Figure 49. WRSR cancel valid timing

Note 1) If VCC is made OFF during write execution, designated address data is not guaranteed, therefore write it once again
Note 2) If CSB is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = “L” area. As for SCK rise, assure timing of tCSS / tCSH or higher.

○WREN/WRDI

a : From ope code to 7-th clock rise, cancel by CSB = “H”.

b : Cancellation is not available when CSB is started after 7-th clock.

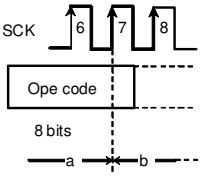


Figure 50. WREN/WRDI cancel valid timing

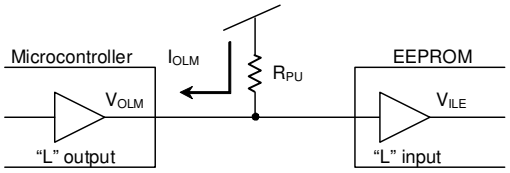
●High speed operation

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

○Input terminal pull up, pull down resistance

When to attach pull up, pull down resistance to EEPROM input terminal, select an appropriate value for the microcontroller VOL, IOL from VIL characteristics of this IC.

○Pull up resistance



- V_{ILE} :EEPROM V_{IL} specifications
- V_{OLM} :Microcontroller V_{OL} specifications
- I_{OLM} :Microcontroller I_{OL} specifications

Figure 51. Pull up resistance

$$R_{PU} \geqq \frac{V_{CC}-V_{OLM}}{I_{OLM}} \quad \cdots ①$$

$$V_{OLM} \leqq V_{ILE} \quad \cdots ②$$

Example) When Vcc=5V, V_{ILE}=1.5V, V_{OLM}=0.4V, I_{OLM}=2mA, from the equation ①,

$$R_{PU} \geqq \frac{5-0.4}{2\times10^{-3}}$$

$$\therefore R_{PU} \leqq 2.3[k\Omega]$$

With the value of Rpu to satisfy the above equation, V_{OLM} becomes 0.4V or lower, and with V_{ILE} (=1.5V), the equation ② is also satisfied.

And, in order to prevent malfunction, mistake write at power ON/OFF, be sure to make CSB pull up.

○Pull down resistance

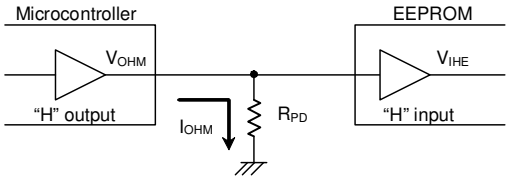


Figure 52. Pull down resistance

$$R_{PD} \geqq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ③$$

$$V_{OHM} \geqq V_{IHE} \quad \cdots ④$$

Example) When V_{CC}=5V, V_{OHM}=V_{CC}-0.5V, I_{OHM}=0.4mA, V_{IHE}=V_{CC}×0.7V, from the equation③

$$R_{PD} \geqq \frac{5-0.5}{0.4\times10^{-3}}$$

$$\therefore R_{PU} \geqq 11.3[k\Omega]$$

Further, by amplitude VIHE, VILE of signal input to EEPROM, operation speed changes. By inputting signal of amplitude of VCC / GND level to input, more stable high speed operations can be realized. On the contrary, when amplitude of 0.8VCC / 0.2VCC is input, operation speed becomes slow.*1

In order to realize more stable high speed operation, it is recommended to make the values of R_{PU}, R_{PD} as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of VCC / GND level.

(*1 At this moment, operating timing guaranteed value is guaranteed.)

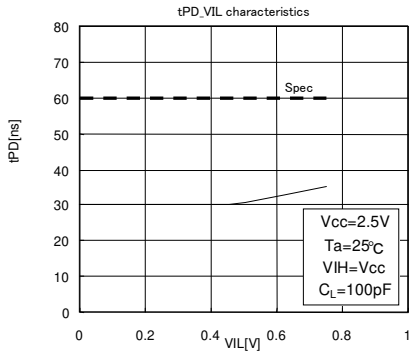


Figure 53. VIL dependency of data output delay time tPD

○SO load capacity condition

Load capacity of SO output terminal affects upon delay characteristic of SO output. (Data output delay time, time from HOLDB to High-Z) In order to make output delay characteristic into higher speed, make SO load capacity small. In concrete, "Do not connect many devices to SO bus", "Make the wire between the controller and EEPROM short", and so forth.

○Other cautions

Make the wire length from the microcontroller to EEPROM input signal same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.

●I/O equivalence circuit

○Output circuit

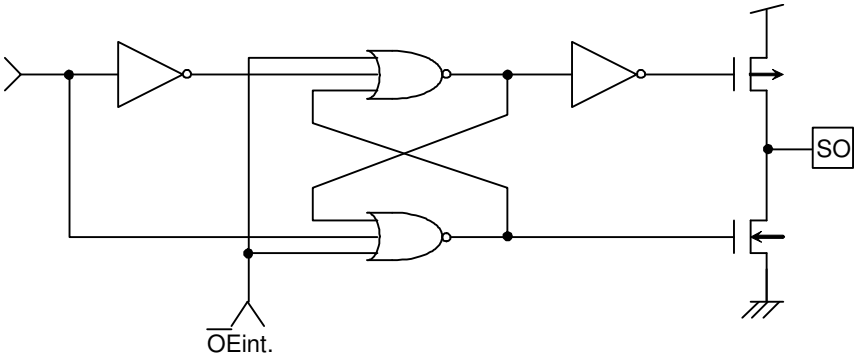


Figure 54. SO output equivalent circuit

○Input circuit

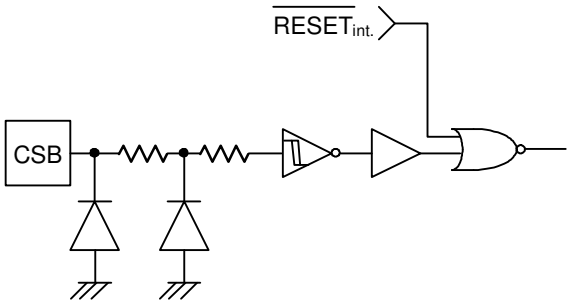


Figure 55. CSB input equivalent circuit

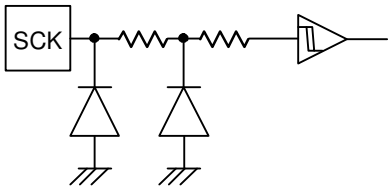


Figure 56. SCK input equivalent circuit

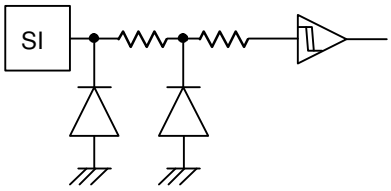


Figure 57. SI input equivalent circuit

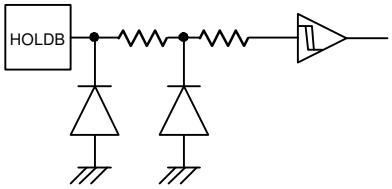


Figure 58. HOLDB input equivalent circuit

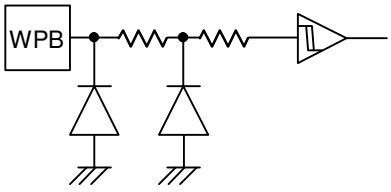


Figure 59. WPB input equivalent circuit

●Power-Up/Down conditions

○At power ON/OFF, set CSB “H” (=VCC).

When CSB is “L”, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CSB “H”. (When CSB is in “H” status, all inputs are canceled.)

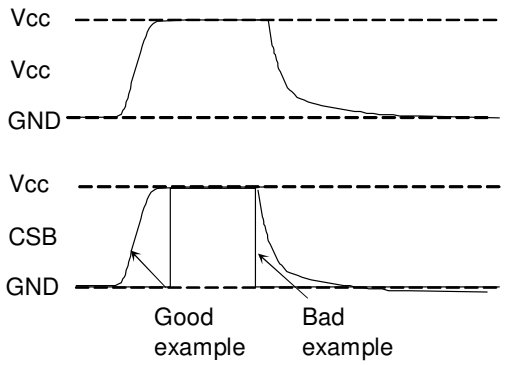


Figure 60. CSB timing at power ON/OFF

(Good example) CSB terminal is pulled up to VCC.

At power OFF, take 10ms or higher before supply. If power is turned on without observing this condition, the IC internal circuit may not be reset, which please note.

(Bad example) CSB terminal is “L” at power ON/OFF.

In this case, CSB always becomes “L” (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes.

Even when CSB input is High-Z, the status becomes like this case, which please note.

○LVCC circuit

LVCC (VCC-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.

At LVCC voltage (Typ. =1.9V) or below, it prevent data rewrite.

○P.O.R. circuit

This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following tR, tOFF, and Vbot are not satisfied, it may become write enable status owing to noises and the likes.

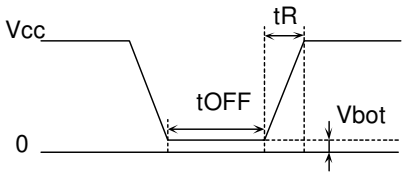


Figure 61. Rise waveform

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

●Noise countermeasures

○VCC noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1μF) between IC VCC and GND. At that moment, attach it as close to IC as possible.And, it is also recommended to attach a bypass capacitor between board VCC and GND.

○SCK noise

When the rise time (tR) of SCK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SCK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time (tR) of SCK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

○WPB noise

During execution of write status register command, if there exist noises on WPB pin, mistake in recognition may occur and forcible cancellation may result, which please note. To avoid this, a Schmitt trigger circuit is built in WPB input. In the same manner, a Schmitt trigger circuit is built in CSB input, SI input and HOLDB input too.

●Operational Notes

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) Application circuit
Although we can recommend the application circuits contained herein with a relatively high degree of confidence, we ask that you verify all characteristics and specifications of the circuit as well as its performance under actual conditions. Please note that we cannot be held responsible for problems that may arise due to patent infringements or noncompliance with any and all applicable laws and regulations.

(3) Absolute maximum ratings
Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

(4) Ground Voltage
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

(5) Thermal consideration
Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions. Consider Pc that does not exceed Pd in actual operating conditions (Pc≥Pd).

Package Power dissipation : $Pd\ (W)=(Tjmax-Ta)/\theta ja$

Power dissipation : $Pc\ (W)=(Vcc-Vo)\times Io+Vcc\times Ib$

(Tjmax : Maximum junction temperature=150℃, Ta : Peripheral temperature[℃] ,
θja : Thermal resistance of package-ambience[℃/W], Pd : Package Power dissipation [W],
Pc : Power dissipation [W], Vcc : Input Voltage, Vo : Output Voltage, Io : Load, Ib : Bias Current)

(6) Short between pins and mounting errors
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

(7) Operation under strong electromagnetic field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.