Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Datasheet

Serial EEPROM Series Automotive EEPROM

125°C Operation SPI BUS EEPROM

BR25H640-2AC

General Description

BR25H640-2AC is a 64Kbit Serial EEPROM of SPI BUS interface method.

Features

- SPI BUS interface (CPOL, CPHA)=(0,0), (1,1)
- Voltage Range : 2.5V to 5.5V
- Operating Range : -40°C to +125°C
- Clock Frequency : 10MHz(Max)
- Write Time : 4ms(Max)
- Page Size : 32bytes
- Bit Format : 8192 x 8bit
- 32bytes Write Lockable Identification Page (ID Page)
- Address Auto Increment Function at Read Operation
- Auto Erase and Auto End Function at Data Rewrite
- Write Protect Block Setting by Software
  Memory Array 1/4, 1/2, Whole
- HOLD Function by HOLDB Pin
- Low Supply Current
  Write Operation (5V) : 1.0mA (Typ)
  Read Operation (5V) : 1.2mA (Typ)
  Standby State(5V) : 0.1μA (Typ)
- Prevention of Write Mistake
  Write prohibition at Power On
  Write prohibition by WPB Pin
  Write prohibition Block Setting
  Prevention of Write Mistake at Low Voltage
- Write Cycles : 1,000,000 Write Cycles (Ta≤85°C)
  : 500,000 Write Cycles (Ta≤105°C)
  : 300,000 Write Cycles (Ta≤125°C)
- Data Retention : 100 Years (Ta≤25°C)
  : 60 Years (Ta≤105°C)
  : 50 Years (Ta≤125°C)
- Data at Shipment

Memory Array		: FFh
ID Page	First 3 Addresses	: 2Fh, 00h, 0Dh
	Other Addresses	: FFh
Status Register	WPEN, BP1, BP0	: 0, 0, 0
Lock Status	LS	: 0

- MSOP8, TSSOP-B8, SOP8, SOP-J8 Packages
- AEC-Q100 Qualified

Packages W(Typ) x D(Typ) x H(Max)

MSOP8
2.90mm x 4.00mm x 0.90mm

TSSOP-B8
3.00mm x 6.40mm x 1.20mm

SOP8
5.00mm x 6.20mm x 1.71mm

SOP-J8
4.90mm x 6.00mm x 1.65mm

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.3 to +6.5	V
Power Dissipation	Pd	0.38 (MSOP8) (Note1)	W
		0.41 (TSSOP-B8) (Note2)	
		0.56 (SOP8) (Note3)	
		0.56 (SOP-J8) (Note4)	
Storage Temperature Range	Tstg	-65 to +150	°C
Operating Temperature Range	Topr	-40 to +125	°C
Terminal Voltage	—	-0.3 to +6.5	V
Maximum Junction Temperature	Tjmax	150	°C
Electrostatic Discharge Voltage (Human Body Model)	V_{ESD}	-6000 to +6000	V

(Note1) Derate by 3.1mW/°C when operating above Ta=25°C
(Note2) Derate by 3.3mW/°C when operating above Ta=25°C.
(Note3) Derate by 4.5mW/°C when operating above Ta=25°C.
(Note4) Derate by 4.5mW/°C when operating above Ta=25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Memory Cell Characteristics (Vcc=2.5V to 5.5V)

Parameter	Limit			Unit	Condition
	Min	Typ	Max		
Write Cycles (Note5, 6)	1,000,000	—	—	Cycles	Ta≤85°C
	500,000	—	—	Cycles	Ta≤105°C
	300,000	—	—	Cycles	Ta≤125°C
Data Retention (Note5)	100	—	—	Years	Ta≤25°C
	60	—	—	Years	Ta≤105°C
	50	—	—	Years	Ta≤125°C

(Note5) Not 100% TESTED
(Note6) The Write Cycles is defined for unit of 4 data bytes with the same address bits of A12 to A2.

Recommended Operating Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply Voltage	Vcc	2.5	5.5	V
Input Voltage	V_{IN}	0	Vcc	V
Bypass Capacitor	C	0.1	—	μF

Input / Output Capacitance (Ta=25°C, Frequency=5MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Capacitance (Note7)	C_{IN}	V_{IN}=GND	—	8	pF
Output Capacitance (Note7)	C_{OUT}	V_{OUT}=GND	—	8	pF

(Note7) Not 100% TESTED

DC Characteristics (Unless otherwise specified, Ta=-40°C to +125°C, Vcc=2.5V to 5.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input High Voltage	V_{IH}	0.7 Vcc	—	Vcc+0.3	V	2.5V≤Vcc≤5.5V
Input Low Voltage	V_{IL}	-0.3	—	0.3 Vcc	V	2.5V≤Vcc≤5.5V
Output Low Voltage	V_{OL}	0	—	0.4	V	I_{OL}=2.1mA
Output High Voltage	V_{OH}	0.8 Vcc	—	Vcc	V	I_{OH}=-2.0mA
Input Leakage Current	I_{LI}	-2	—	+2	μA	V_{IN}=0V to Vcc
Output Leakage Current	I_{LO}	-2	—	+2	μA	V_{OUT}=0V to Vcc, CSB=Vcc
Supply Current (WRITE)	I_{CC1}	—	—	2.5	mA	Vcc=2.5V, f_{SCK}=5MHz, $t_{E/W}$=4ms V_{IH}/V_{IL}=0.9Vcc/0.1Vcc, SO=OPEN
	I_{CC2}	—	—	5.5	mA	Vcc=5.5V, f_{SCK}=5 or 10 MHz, $t_{E/W}$=4ms V_{IH}/V_{IL}=0.9Vcc/0.1Vcc, SO=OPEN
Supply Current (READ)	I_{CC3}	—	—	1.5	mA	Vcc=2.5V, f_{SCK}=5MHz V_{IH}/V_{IL}=0.9Vcc/0.1Vcc, SO=OPEN
	I_{CC4}	—	—	2.0	mA	Vcc=5.5V, f_{SCK}=5MHz V_{IH}/V_{IL}=0.9Vcc/0.1Vcc, SO=OPEN
	I_{CC5}	—	—	4.0	mA	Vcc=5.5V, f_{SCK}=10MHz V_{IH}/V_{IL}=0.9Vcc/0.1Vcc, SO=OPEN
Standby Current	I_{SB}	—	—	10	μA	Vcc=5.5V CSB=HOLDB=WPB=Vcc, SCK=SI=Vcc or 0V, SO=OPEN

AC Characteristics (Ta=-40°C to +125°C, unless otherwise specified, load capacitance C_{L1}=100pF)

Parameter	Symbol	2.5V≤Vcc≤5.5V			4.5V≤Vcc≤5.5V			Unit
		Min	Typ	Max	Min	Typ	Max	
SCK Frequency	f_{SCK}	0.01	—	5	0.01	—	10	MHz
SCK High Time	t_{SCKWH}	85	—	—	40	—	—	ns
SCK Low Time	t_{SCKWL}	85	—	—	40	—	—	ns
CSB High Time	t_{CS}	85	—	—	40	—	—	ns
CSB Setup Time	t_{CSS}	90	—	—	30	—	—	ns
CSB Hold Time	t_{CSH}	85	—	—	30	—	—	ns
SCK Setup Time	t_{SCKS}	90	—	—	30	—	—	ns
SCK Hold Time	t_{SCKH}	90	—	—	30	—	—	ns
SI Setup Time	t_{DIS}	20	—	—	10	—	—	ns
SI Hold Time	t_{DIH}	30	—	—	10	—	—	ns
Data Output Delay Time1	t_{PD1}	—	—	60	—	—	40	ns
Data Output Delay Time2 (C_{L2}=30pF)	t_{PD2}	—	—	50	—	—	30	ns
Output Hold Time	t_{OH}	0	—	—	0	—	—	ns
Output Disable Time	t_{OZ}	—	—	100	—	—	40	ns
HOLDB Setting Setup Time	t_{HFS}	0	—	—	0	—	—	ns
HOLDB Setting Hold Time	t_{HFH}	40	—	—	30	—	—	ns
HOLDB Release Setup Time	t_{HRS}	0	—	—	0	—	—	ns
HOLDB Release Hold Time	t_{HRH}	70	—	—	30	—	—	ns
Time from HOLDB to Output High-Z	t_{HOZ}	—	—	100	—	—	40	ns
Time from HOLDB to Output Change	t_{HPD}	—	—	60	—	—	40	ns
SCK Rise Time (Note1)	t_{RC}	—	—	2	—	—	2	µs
SCK Fall Time (Note1)	t_{FC}	—	—	2	—	—	2	µs
Output Rise Time (Note1)	t_{RO}	—	—	40	—	—	20	ns
Output Fall Time (Note1)	t_{FO}	—	—	40	—	—	20	ns
Write Time	$t_{E/W}$	—	—	4	—	—	4	ms

(Note1) NOT 100% TESTED

AC Measurement Conditions

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Load Capacitance1	C_{L1}	—	—	100	pF
Load Capacitance2	C_{L2}	—	—	30	pF
Input Rise Time	—	—	—	50	ns
Input Fall Time	—	—	—	50	ns
Input Voltage	—	0.2 Vcc / 0.8 Vcc			V
Input / Output Judgment Voltage	—	0.3 Vcc / 0.7 Vcc			V

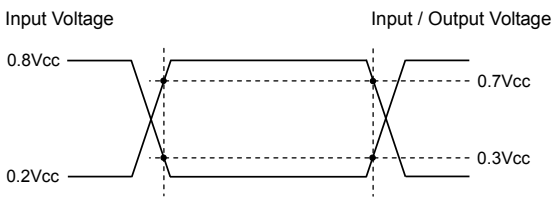


Figure 1. Input / Output Judgment Voltage

Serial Input / Output Timing

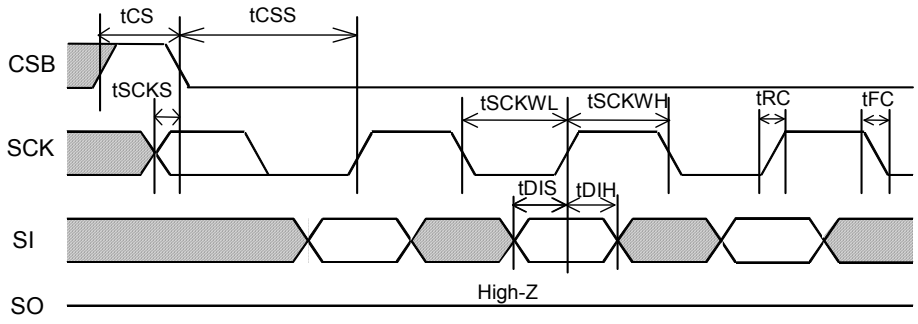


Figure 2. Input Timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the Most Significant Bit MSB.

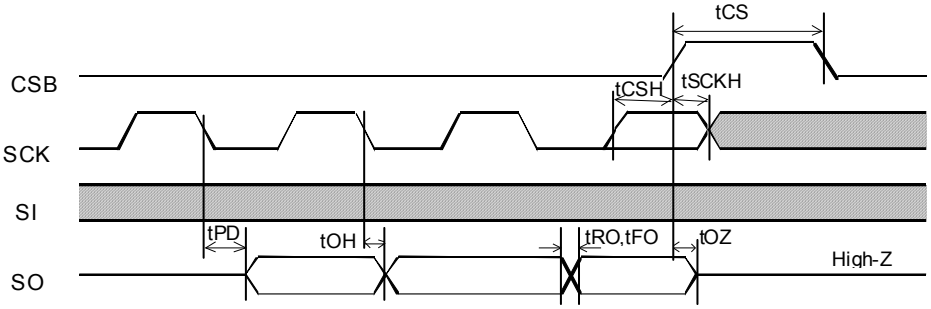


Figure 3. Input / Output Timing

SO is output in sync with data fall edge of SCK. Data is output from the Most Significant Bit MSB.

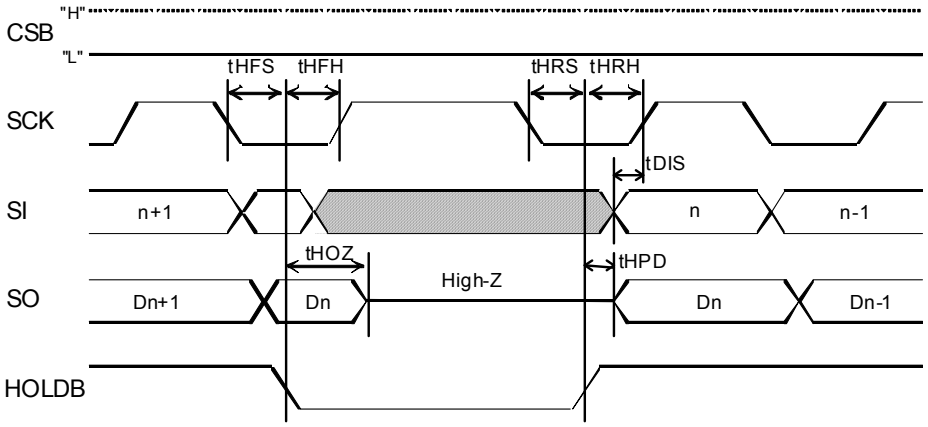


Figure 4. HOLD Timing

Block Diagram

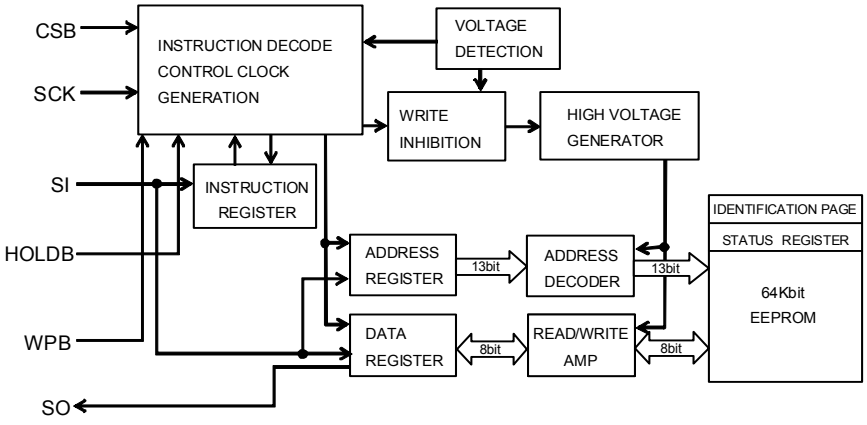


Figure 5. Block Diagram

Pin Configuration

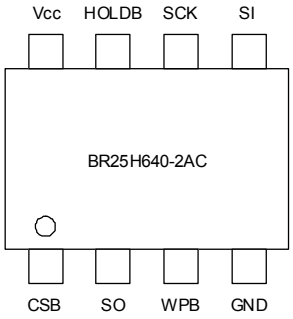


Figure 6. Pin Assignment Diagram

Pin Description

Pin Number	Pin Name	Input / Output	Function
1	CSB	Input	Chip Select Input
2	SO	Output	Serial Data Output
3	WPB	Input	Write Protect Input Write Status Register Command is prohibited.
4	GND	–	All Input / Output Reference Voltage, 0V
5	SI	Input	Serial Data Input Start Bit, Instruction Code, Address and Data Input
6	SCK	Input	Serial Clock Input
7	HOLDB	Input	Hold Input Serial Communications may be suspended temporarily (HOLD State).
8	Vcc	–	Supply Voltage

Typical Performance Curves

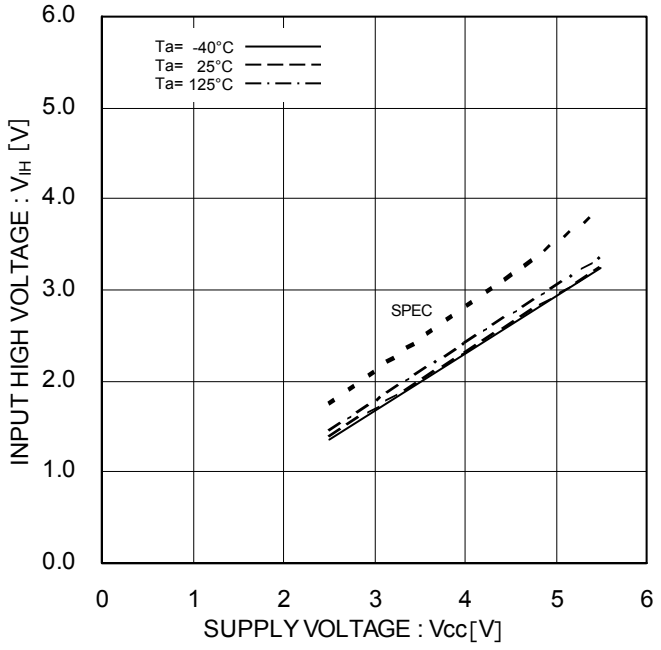


Figure 7. Input High Voltage V_{IH}
(CSB, SCK, SI, HOLDB, WPB)

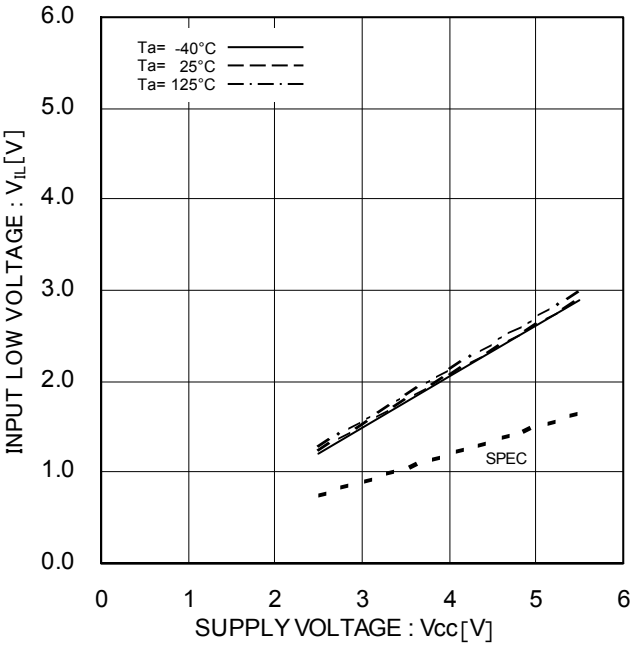


Figure 8. Input Low Voltage V_{IL}
(CSB, SCK, SI, HOLDB, WPB)

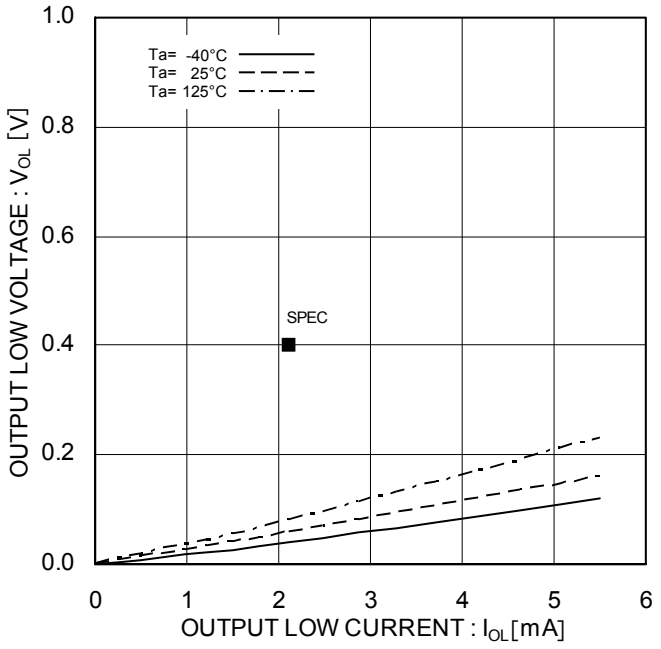


Figure 9. Output Low Voltage V_{OL}, I_{OL} (Vcc=2.5V)

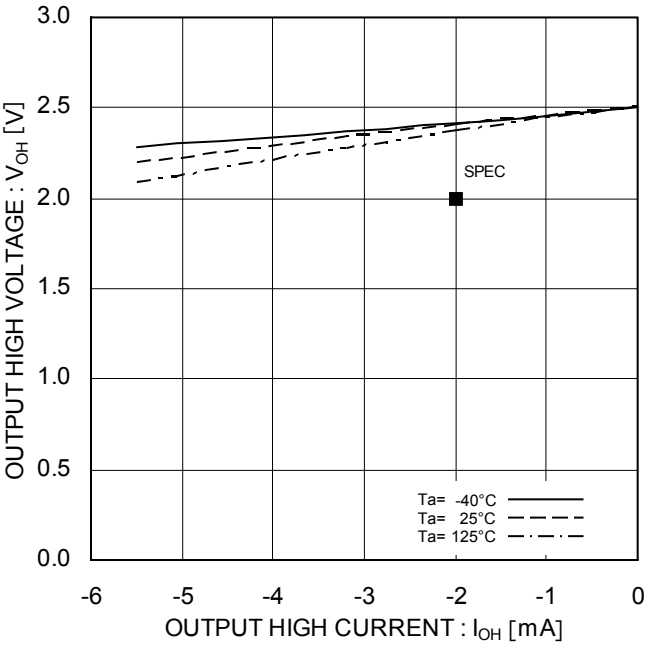


Figure 10. Output High Voltage V_{OH}, I_{OH} (Vcc=2.5V)

Typical Performance Curves - continued

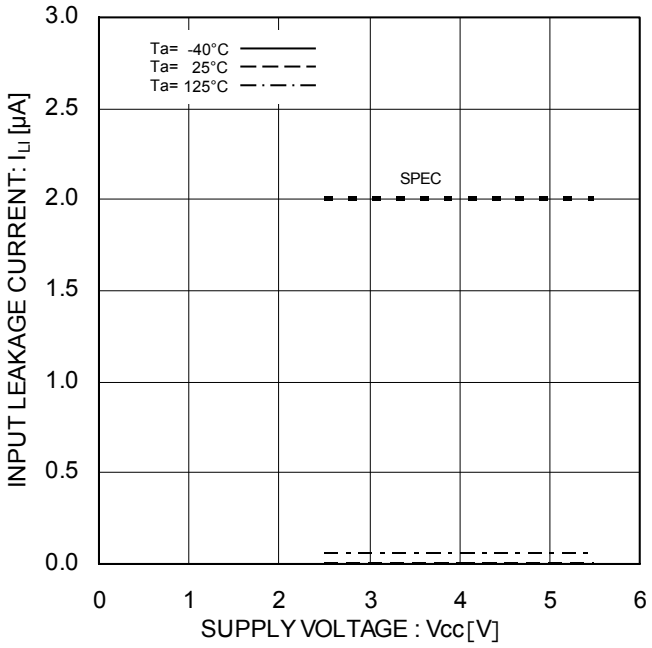


Figure 11. Input Leakage Current I_{LI}
(CSB, SCK, SI, HOLDB, WPB)

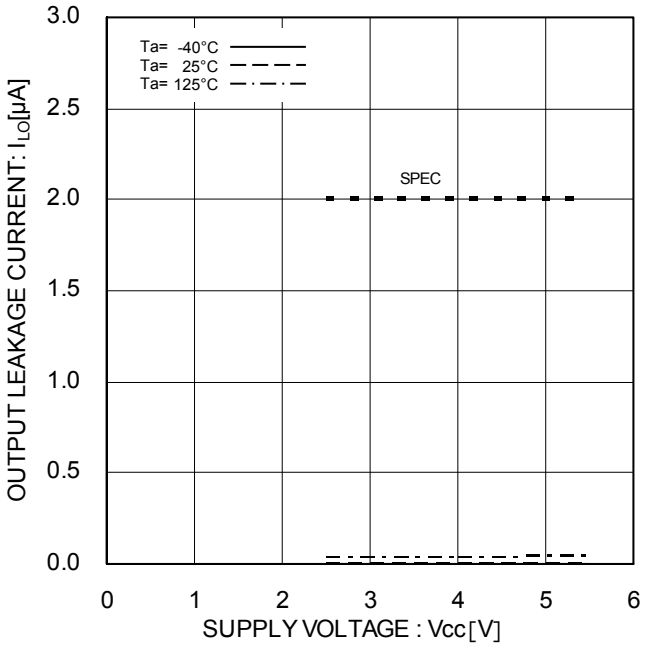


Figure 12. Output Leakage Current I_{LO}
(SO)

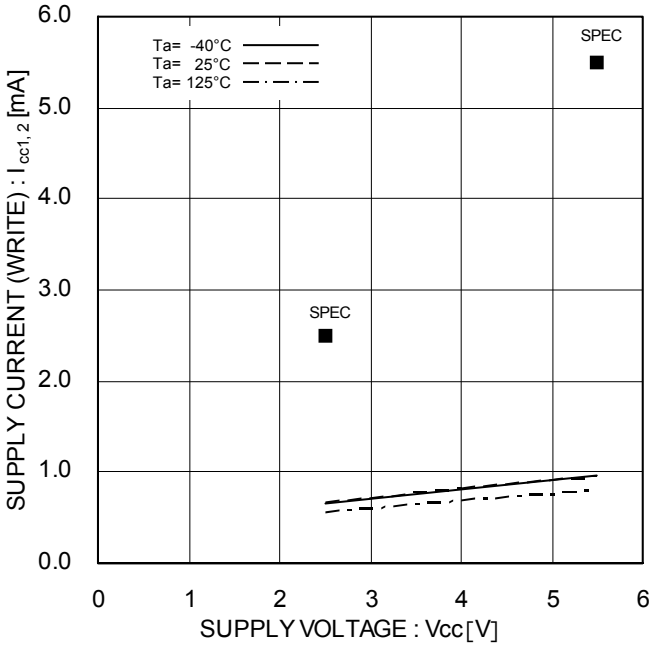


Figure 13. Supply Current (WRITE) $I_{CC1,2}$

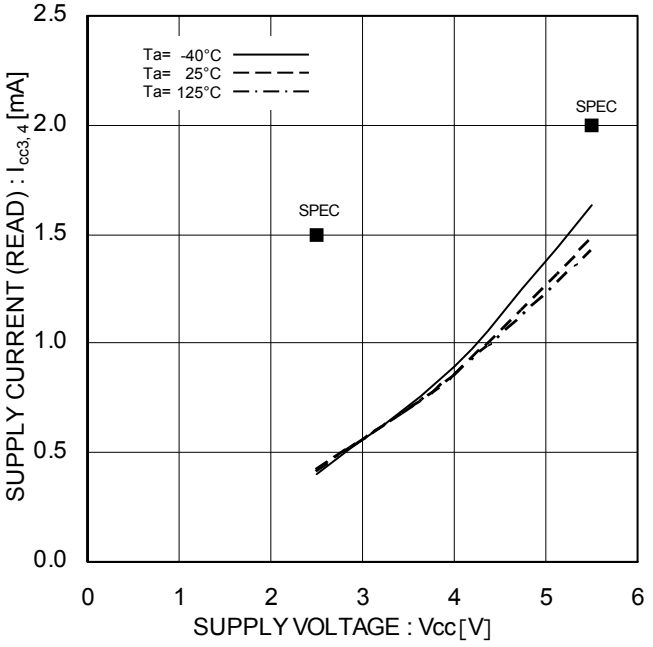


Figure 14. Supply Current (READ) $I_{CC3,4}$

Typical Performance Curves - continued

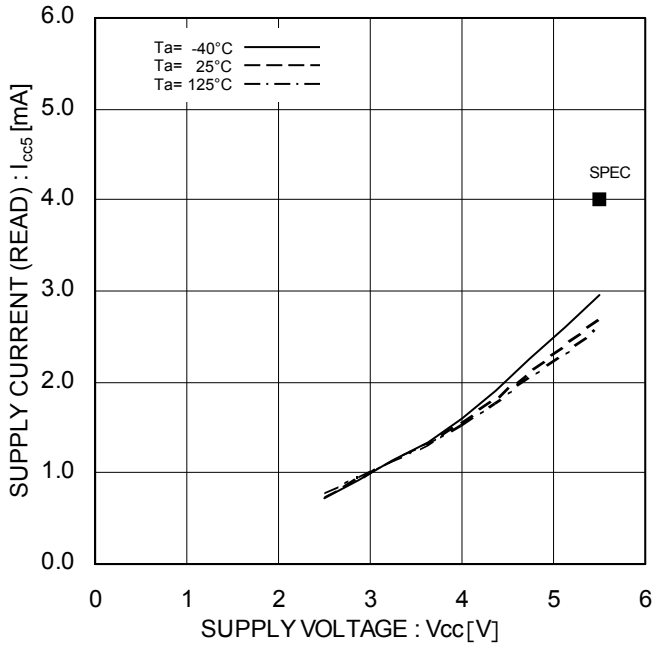


Figure 15. Supply Current (READ) I_{CC5}

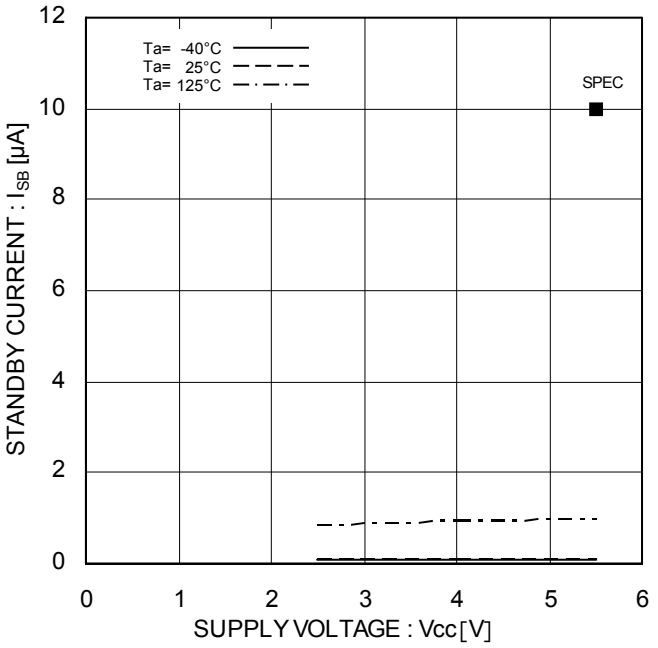


Figure 16. Standby Current I_{SB}

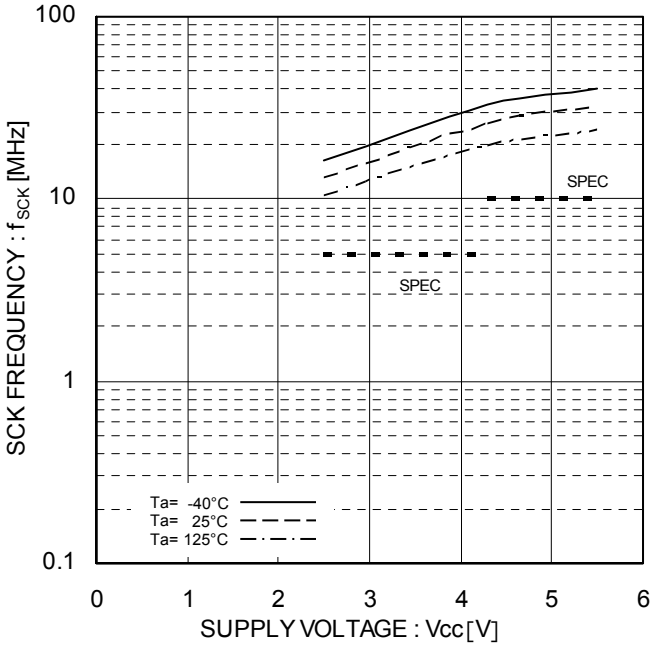


Figure 17. SCK Frequency f_{SCK}

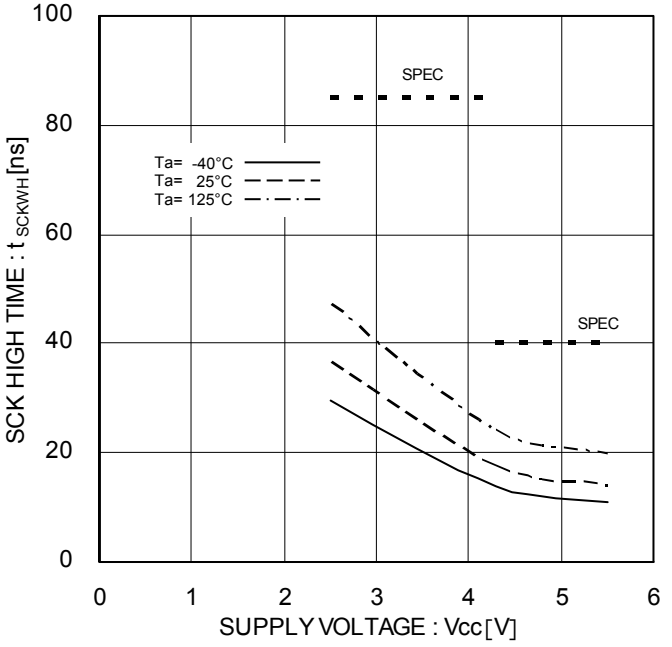


Figure 18. SCK High Time t_{SCKWH}

Typical Performance Curves - continued

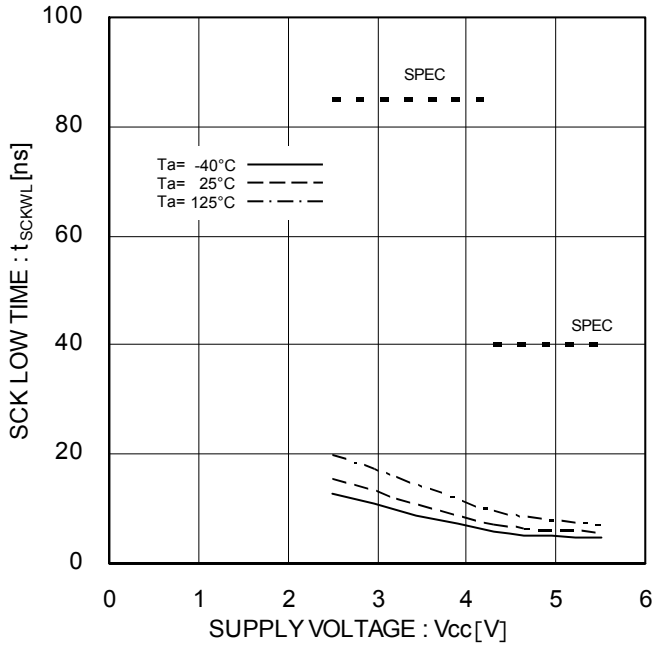


Figure 19. SCK Low Time t_{SCKWL}

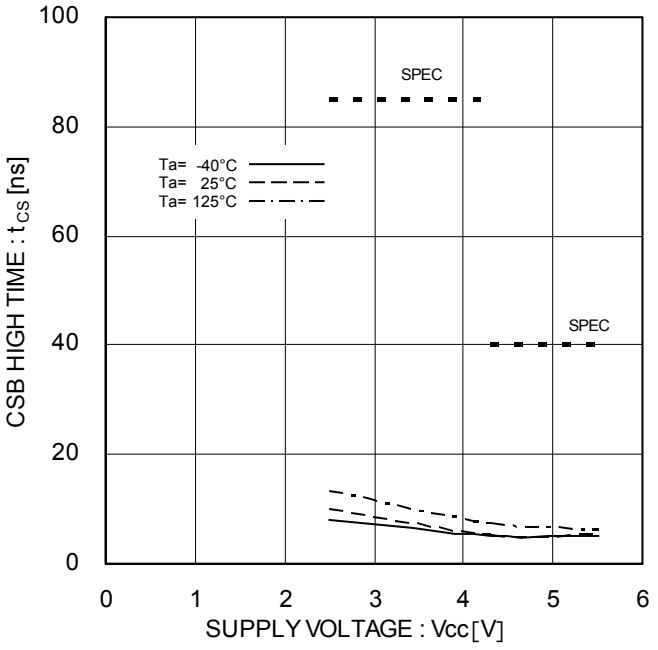


Figure 20. CSB High Time t_{CS}

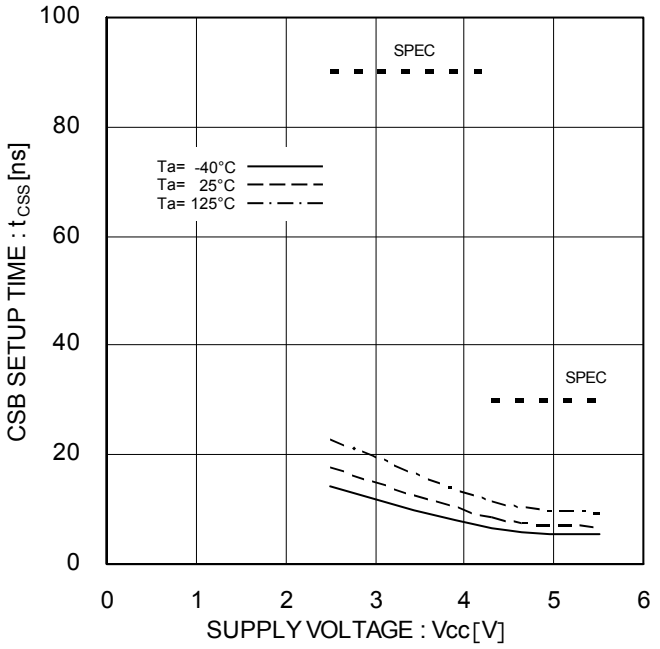


Figure 21. CSB Setup Time t_{CSS}

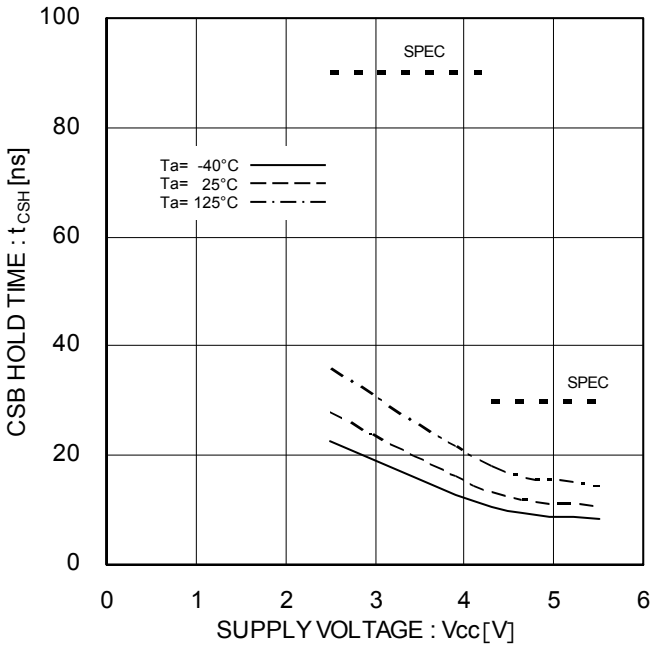


Figure 22. CSB Hold Time t_{CSH}

Typical Performance Curves - continued

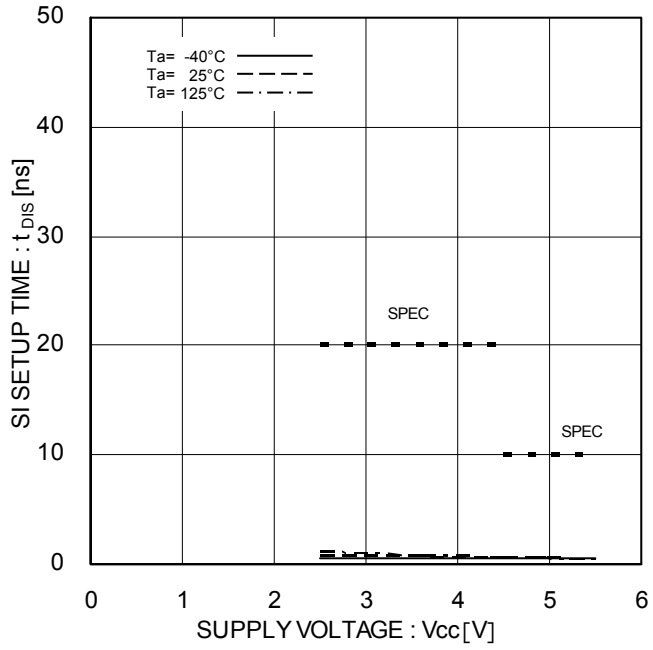


Figure 23. SI Setup Time t_{DIS}

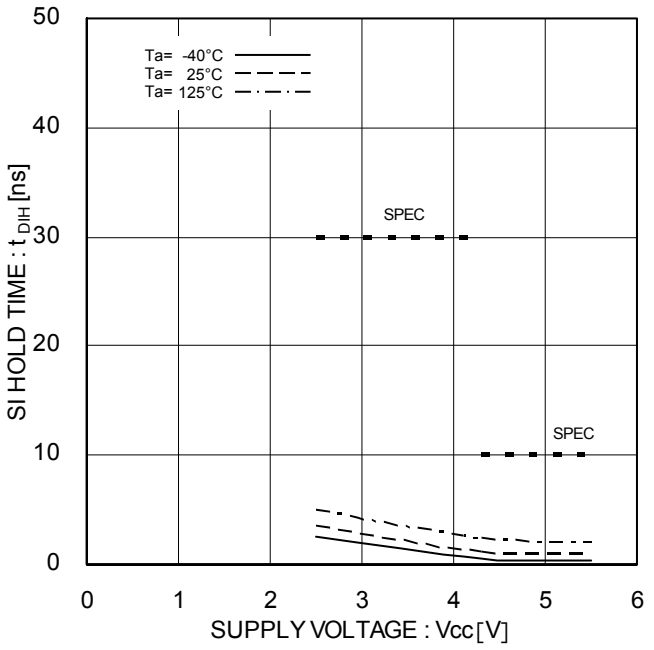


Figure 24. SI Hold Time t_{DIH}

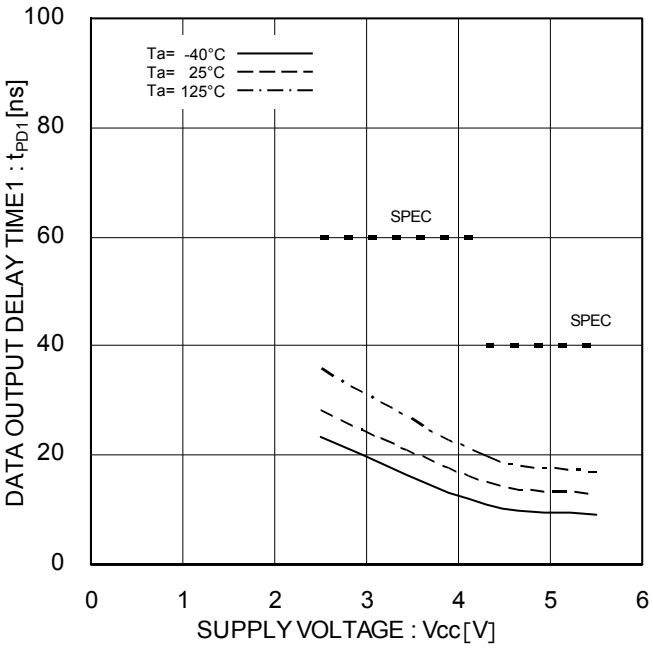


Figure 25. Data Output Delay Time1 t_{PD1} (C_{L1}=100pF)

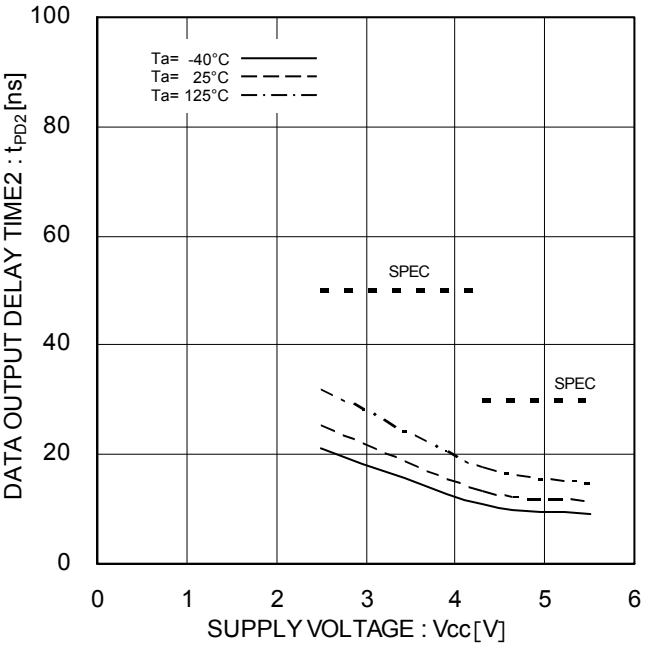


Figure 26. Data Output Delay Time2 t_{PD2} (C_{L2}=30pF)

Typical Performance Curves - continued

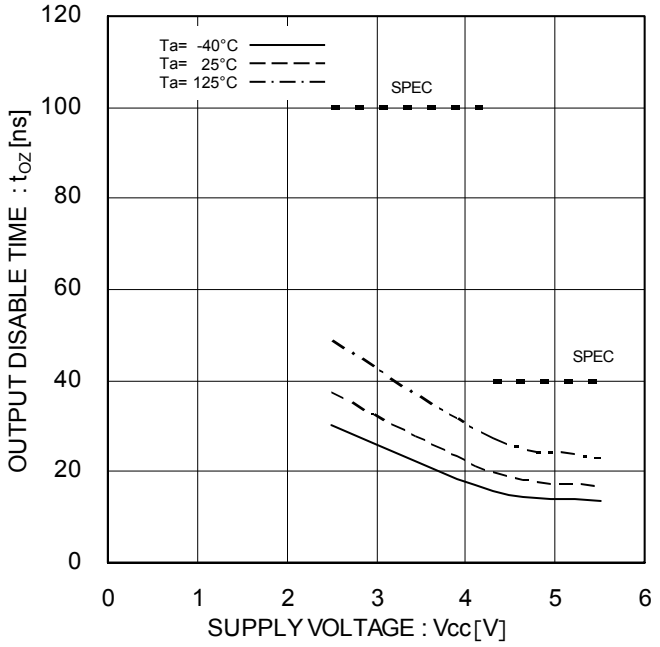


Figure 27. Output Disable Time t_{OZ}

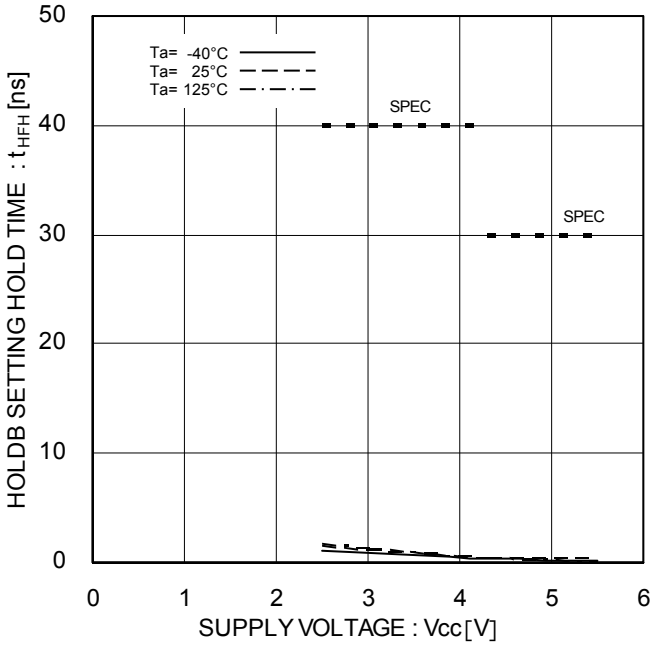


Figure 28. HOLDB Setting Hold Time t_{HFH}

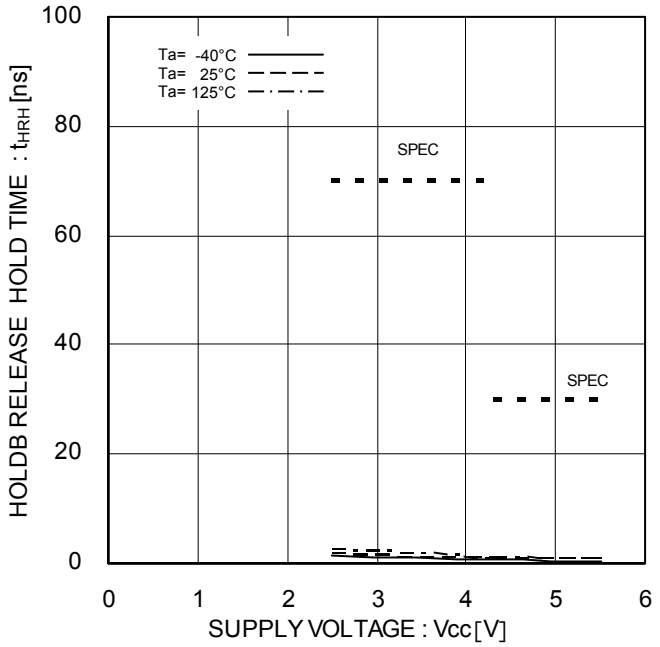


Figure 29. HOLDB Release Hold Time t_{HRH}

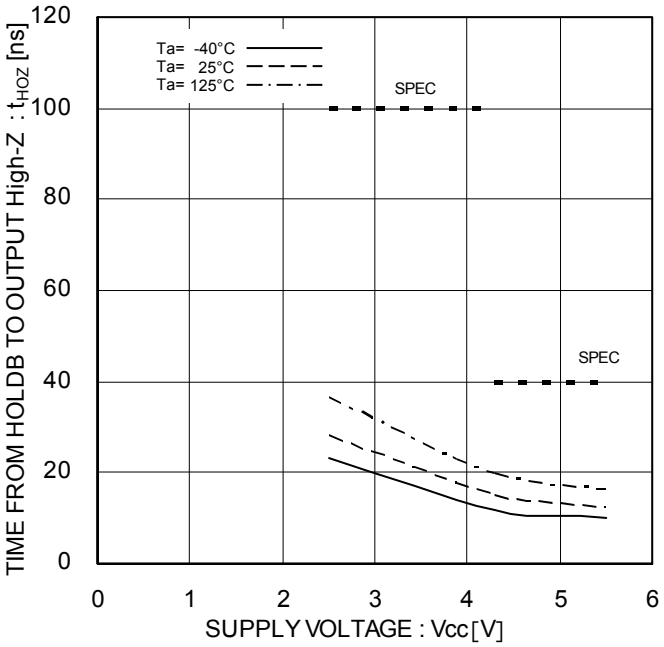


Figure 30. Time from HOLDB to Output High-Z t_{HOZ}

Typical Performance Curves - continued

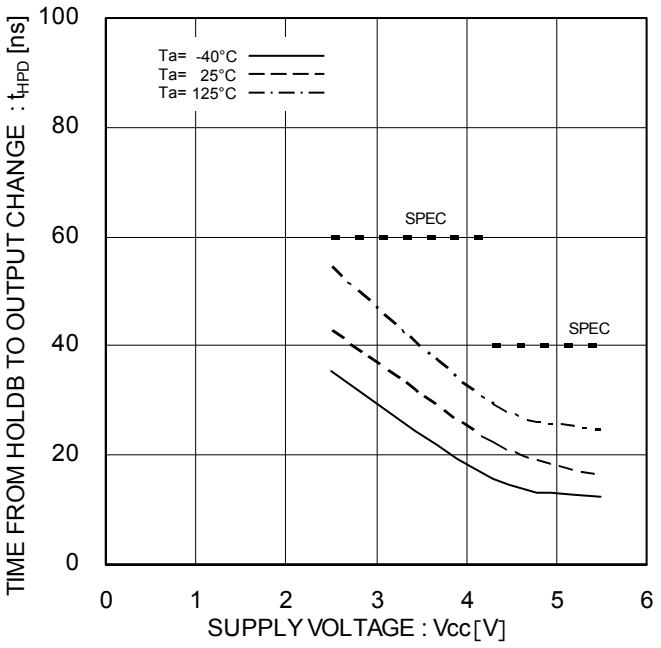


Figure 31. Time from HOLDB to Output Change t_{HPD}

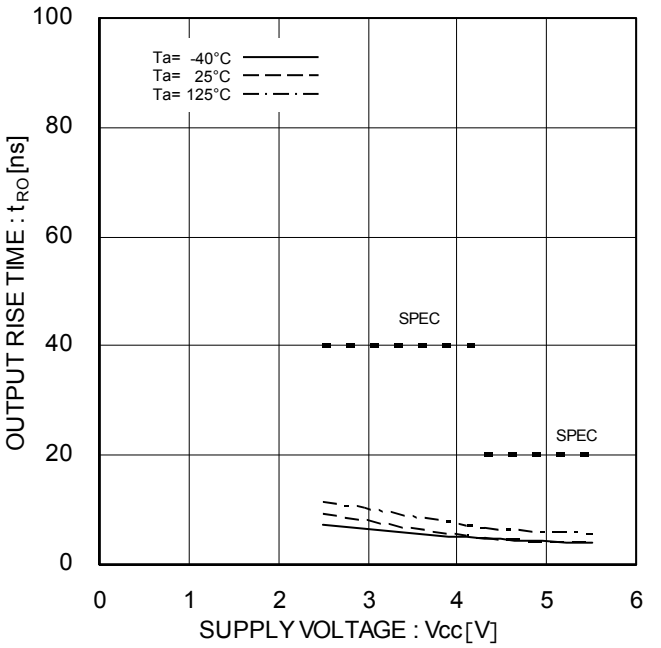


Figure 32. Output Rise Time t_{RO}

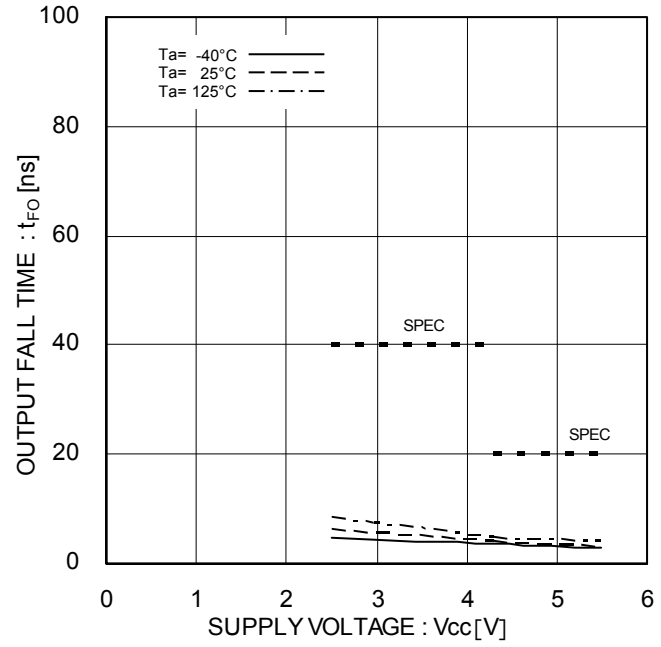


Figure 33. Output Fall Time t_{FO}

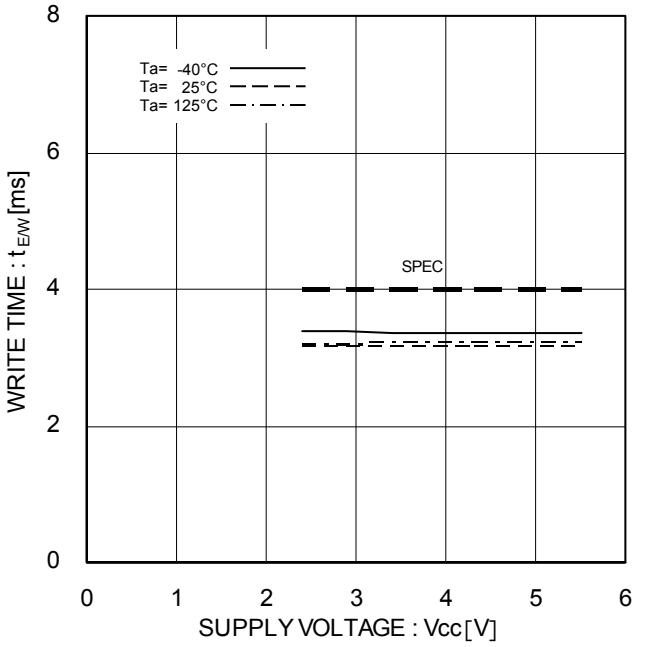


Figure 34. Write Time $t_{E/W}$

1. Features

(1) Status Register

This IC has the Status Registers. Status Registers are of 8 bits and express the following parameters.
WPEN, BP0 and BP1 can be set by Write Status Register command. These 3 bits are memorized into the EEPROM, therefore are valid even when supply voltage is turned off.
Write Cycles and Data Retention of Status Registers are same as characteristics of the EEPROM.
WEN can be set by Write Enable command and Write Disable command. WEN becomes write disable status when supply voltage is turned off. $\overline{R}$/B is for write confirmation, therefore cannot be set externally.
The values of Status Register can be read by Read Status Register command.

Table 1. Status Register

D7	D6	D5	D4	D3	D2	D1	D0
WPEN	0	0	0	BP1	BP0	WEN	$\overline{R}$/B

Table 2. Function of Status Register

bit	Memory Location	Function	Content
WPEN	EEPROM	Pin Enable / Disable designation bit for WPB pin WPEN=0=Invalid, WPEN=1=Valid	WPEN bit enables / disables the function of WPB pin.
BP1 BP0	EEPROM	EEPROM Write Disable Block designation bit	BP1 and BP0 bits designate the Write Disable Block of EEPROM. Refer Table 3. Write Disable Block Setting.
WEN	Register	Write Enable/Write Disable Confirmation bit for WRITE, WRSR, WRID and LID WEN=0=Prohibited, WEN=1=Permitted	WEN bit indicates the status of write enable or write disable for WRITE, WRSR, WRID, LID.
$\overline{R}$/B	Register	Write Cycle Status($\overline{READY}$/BUSY) Confirmation bit $\overline{R}$/B=0=READY , $\overline{R}$/B=1=BUSY	$\overline{R}$/B bit indicates the status of READY or BUSY of the write cycle.

Table 3. Write Disable Block Setting

Status Register		Protected Block	Protected Addresses
BP1	BP0		
0	0	None	None
0	1	Upper 1/4	1800h to 1FFFh
1	0	Upper 1/2	1000h to 1FFFh
1	1	Whole Memory	0000h to 1FFFh, ID Page

(2) Write Protect Mode by WPB pin

By setting WPB = Low with WPEN = 1, Write Status Register command is disabled. Only when WPEN bit is set “1”, the WPB pin functions become valid. However, when write cycle is in execution, no interruption can be made.

Table 4. Write Protect Mode

WPEN bit	WPB pin	Instruction	
		WRSR	WRITE/WRID/LID
0	X	Writable	Writable
1	1	Writable	Writable
1	0	Write Protected	Writable

WPB is normally fixed to High or Low for use, but when WPB is controlled so as to cancel Write Status Register command, pay attention to the following WPB Valid Timing.
Write Status Register command is executed, by setting WPB = Low in cancel valid area, command can be cancelled. The Data area (from 7th fall of SCK to 16th rise of SCK) becomes the cancel valid area. However, once write is started, any input cannot be cancelled. WPB input becomes Don’t Care, and cancellation becomes invalid.

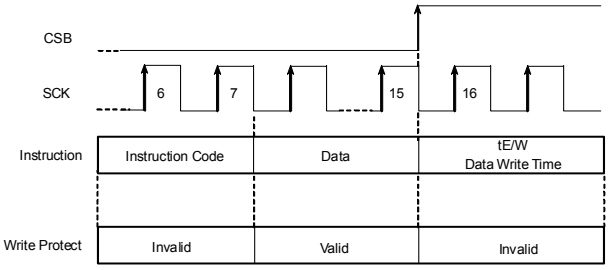


Figure 35. WPB Valid Timing (WRSR)

(3) Hold Mode by HOLDB pin

By the HOLDB pin, serial communication can be stopped temporarily (HOLD status). HOLDB pin carries out serial communications normally when it is High. To get in HOLD status, at serial communication, when SCK = Low, set the HOLDB pin Low. At HOLD status, SCK and SI become Don’t Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the HOLDB pin High when SCK = Low. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at Read command, after release of HOLD status, by starting A4 address input, Read command can be restarted. When in HOLD status, leave CSB = Low. When it is set CSB = High in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

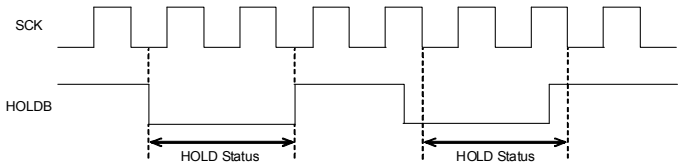


Figure 36. HOLD Status

(4) ID Page

This IC has 32 bytes Write lockable Identification Page (ID Page) in addition to Memory Array.
The data in the first 3 addresses are for device identification. These data are over written by Write ID Page command.

Table 5. Data in the first 3 addresses

ID Page Address	Data	Content
00h	2Fh	Manufacturer Code (ROHM)
01h	00h	Interface Method (SPI)
02h	0Dh	Memory Density (64Kbit)

By setting Lock Status (LS) bit to “1” with Lock ID Page command, it is prohibited to write to ID page permanently.
It is not reversible to set from ID Page Lock Status (LS=”1”) to ID Page Lock Release status (LS=”0”).

Table 6. Function of Lock Status

bit	Memory Location	Function	Content
LS	EEPROM	ID Page Lock/ Lock Release Status designation bit LS=0=ID Page Lock Release LS=1=ID Page Lock	LS bit can set Lock Status to ID Page.

(5) ECC Function

This IC has ECC bits for Error Correction to each 4 data bytes with the same address bits of A12 to A2. In the Read operation, even if there is 1 bit data error in the 4 bytes, IC corrects to correct data by ECC function and outputs data corrected. Even if write operation is started with only 1 byte data input, this IC rewrites the data of 4 bytes with the same address bits of A12 to A2 and the data of ECC bits added to these 4 bytes data. In order to maximize Write Cycles specified, it is recommended to write with data input of each 4 bytes with the same address bits of A12 to A2.

Table 7. Example of 4 data bytes with the same address bits of A12 to A2 (Address 0000h,0001h,0002h,0003h)

Same Address Bits from A12 to A2											Non-Common		Address
A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
0	0	0	0	0	0	0	0	0	0	0	0	1	0001h
0	0	0	0	0	0	0	0	0	0	0	1	0	0002h
0	0	0	0	0	0	0	0	0	0	0	1	1	0003h

2. Instruction Mode

After setting CSB pin from High to Low, to execute each command, input Instruction Code, Address and Data from the Most Significant Bit MSB.

Table 8. Instruction Mode

Instruction	Content	Instruction Code (8bit)	Address(MSB) / Data (8bit)	Address (LSB) (8bit)	Data (8bit)
WREN	Write Enable	0000 0110	-	-	-
WRDI	Write Disable	0000 0100	-	-	-
READ	Read	0000 0011	A15 to A8 (Note1)	A7 to A0	D7 to D0 Output
WRITE	Write	0000 0010	A15 to A8 (Note1)	A7 to A0	D7 to D0 Input
RDSR	Read Status Register	0000 0101	D7 to D0 Output (Note2)	-	-
WRSR	Write Status Register	0000 0001	D7 to D0 Input (Note2)	-	-
RDID	Read ID Page	1000 0011	0000 0000	00A4 to A0	D7 to D0 Output
WRID	Write ID Page	1000 0010	0000 0000	00A4 to A0	D7 to D0 Input
RDLS	Read Lock Status	1000 0011	0000 0100	0000 0000	D7 to D0 Output (Note3)
LID	Lock ID page	1000 0010	0000 0100	0000 0000	D7 to D0 Input (Note3)

(Note1) Address bit A15, A14, A13 = Don't Care
(Note2) Refer Figure 43. , Figure 44..
(Note3) Refer Figure 47. , Figure 48..

3. Timing Chart

(1) Write Enable Command (WREN)

It is set to write enable status by Write Enable command. As for this command, set CSB to Low, and then input the Instruction Code of Write Enable command. This command is accepted at the 7th rise of SCK. Even with input over 7 clocks, command becomes valid.

Before carrying out Write command, Write Status Register command, Write ID Page command and Lock ID Page command, it is necessary to set write enable status by the Write Enable command.

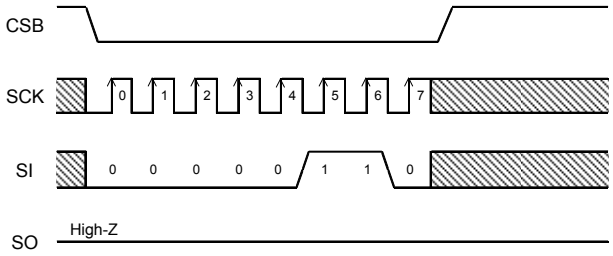


Figure 37. Write Enable Command

(2) Write Disable Command (WRDI)

It is set to write disable status, WEN bit becomes to “0”, by Write Disable command. As for this command, set CSB to Low, and then input the Instruction Code of Write Disable command. This command is accepted at the 7th rise of SCK. Even with input over 7 clocks, command becomes valid.

If Write command, Write Status Register command, Write ID Page command or Lock ID Page command is input in the write disable status, commands are cancelled. And even in the write enable status, once Write command, Write Status Register command, Write ID Page command or Lock ID Page is executed, it gets in the write disable status.

After power on, this IC is in write disable status.

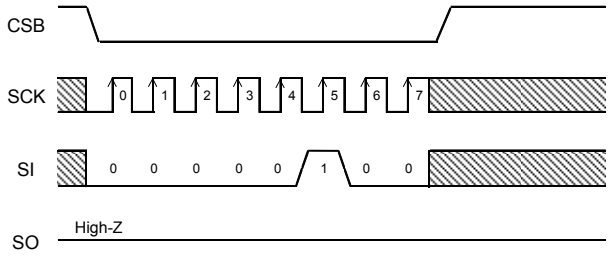


Figure 38. Write Disable Command

(3) Read Command (READ)

By Read command, data of EEPROM can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read command. This IC starts data output of the designated address. Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM Array. After reading data of the most significant address, by continuing increment read, data of the least significant address is read.

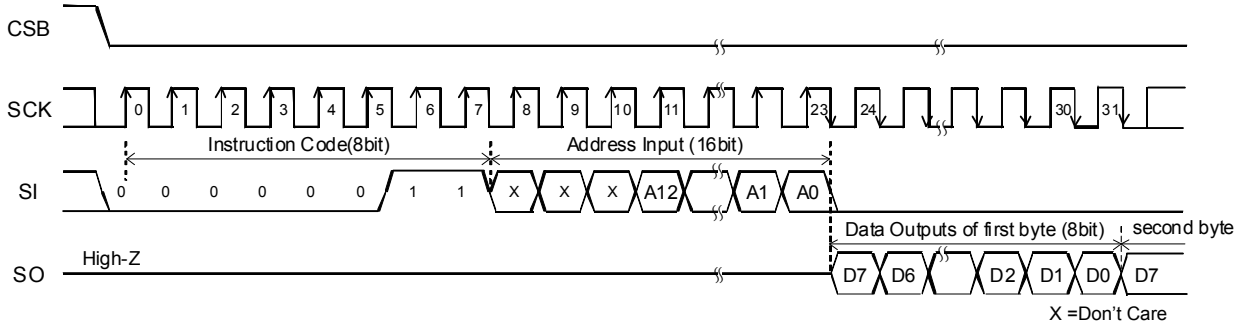


Figure 39. Read Command

(4) Write Command (WRITE)

By Write command, data of EEPROM can be written. As for this command, set CSB to Low, then input address and data after Instruction Code of Write command. Then, by making CSB to High, the IC starts write operation. The write time of EEPROM requires time of $t_{E/W}$ (Max 4ms). To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Write command is not executed, and this Write command is cancelled.

During write operation, other than Read Status Register command is not accepted.

This IC has Page Write function, and after input of data for 1 byte (8bits), by continuing data input without setting CSB Low to High, data up to 32 bytes can be written for one $t_{E/W}$. In Page Write, the addressed lower 5 address bits are incremented internally at every time when data of 1 byte is inputted and data is written to respective addresses. When the data input exceeds the last address byte of the page, address rolls over to the first address byte of the same page. It is not recommended to input data over 32 bytes, it is recommended to input data in 32 bytes. In case of the data input over 32 bytes, it is explained in Table 10.

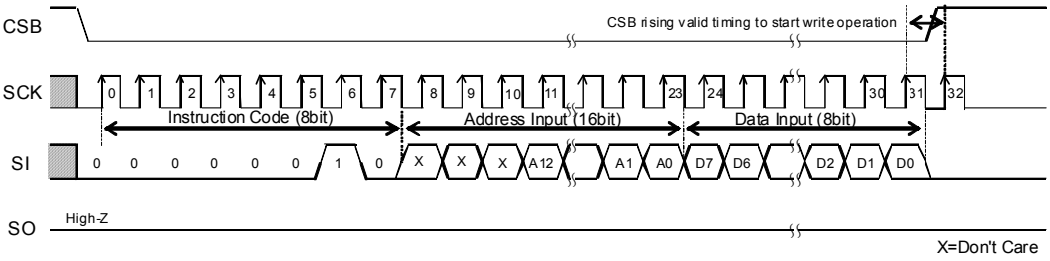


Figure 40. Write Command (Byte Write)

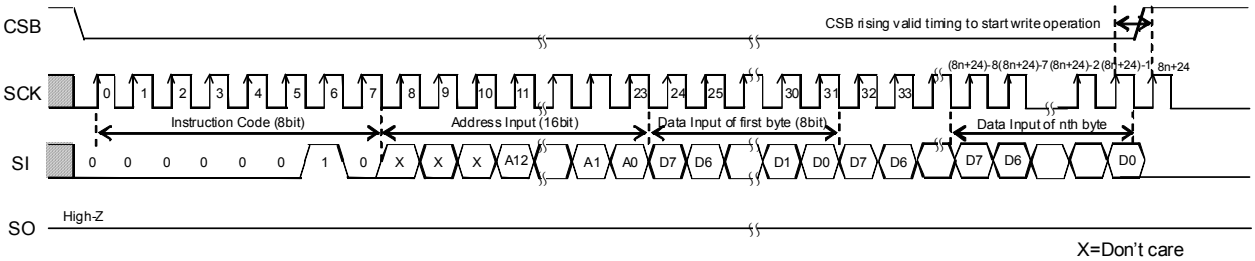


Figure 41. Write Command (Page Write)

(a) Page Write Function

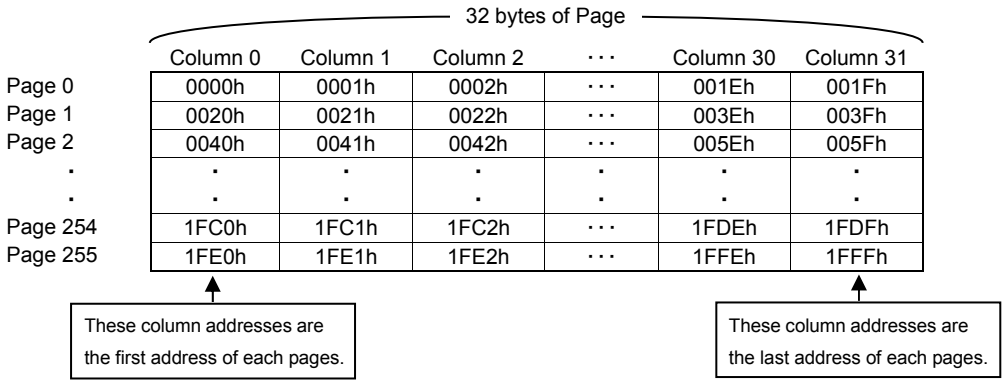


Figure 42. EEPROM physical address for Page Write command (32Byte)

● In case of Page Write command with lower than 32 bytes data input

Table 9. Example of Page Write with 2 bytes data input

No.	4 bytes group	Group 0				・・・	・・・	Group 7			
	Addresses of Page 0	0000h	0001h	0002h	0003h	0004h	・・・	001Ch	001Dh	001Eh	001Fh
①	Previous Data	00h	01h	02h	03h	04h	・・・	1Ch	1Dh	1Eh	1Fh
②	Input data for Page Write (2 bytes)	AAh	55h	-	-	-	・・・	-	-	-	-
③	The Data after Write operation	AAh	55h	02h	03h	04h	・・・	1Ch	1Dh	1Eh	1Fh

No.① : These data are EEPROM data before Write operation.
No.② : Inputted 2 bytes data AAh, 55h from address 0000h.
No.③ : If Write operation is executed with the data of No.②, the data are changed from the data of No.① to the data of No.③.
The data of address 0000h, 0001h are changed to data AAh, 55h, the data of address 0002h, 0003h, the 4 bytes group of Group 0, are over-written to data 02h, 03h.
When Write command is cancelled, EEPROM data keep No.①.

● In case of Page Write command with more than 32 bytes data input

Table 10. Example of Page Write with 34 bytes data input

No.	4 bytes group	Group 0				・・・	・・・	Group 7			
	Addresses of Page 0	0000h	0001h	0002h	0003h	0004h	・・・	001Ch	001Dh	001Eh	001Fh
①	Previous Data	00h	01h	02h	03h	04h	・・・	1Ch	1Dh	1Eh	1Fh
②	Input data for Page Write (34 bytes)	55h	AAh	55h	AAh	55h	・・・	55h	AAh	55h	AAh
		FFh	00h	-	-	-	・・・	-	-	-	-
③	The Data after Write operation	FFh	00h	02h	03h	55h	・・・	55h	AAh	55h	AAh

No.① : These data are EEPROM data before Write operation.
No.② : Inputted 34 bytes data 55h, AAh, ・・・・, 55h, AAh, FFh, 00h from address 0000h.
The data of address 0000h, 0001h are set to data 55h, AAh first. The data of address 0002h, 0003h are set to data 55h, AAh. After inputting data to Maximum byte (001Fh), the data address 0000h, 0001h are set to data FFh, 00h again. No data input to address 0002h, 0003h again.
No.③ : If Write operation is executed with the data of No.②, the data are changed from the data of No.① to the data of No.③.
The data of address 0000h, 0001h are changed to FFh, 00h inputted data later, not to 55h, AAh inputted data first. The data of address 0002h, 0003h, the 4 bytes group of Group 0, are over-written to 02h, 03h of Previous Data, not to 55h, AAh inputted data first. The data of other addresses are changed to 55h, AAh・・・・, 55h, AAh.
When Write command is cancelled, EEPROM data keep No.①.

● Roll Over
In Page Write command, when data is set to the last address of a page (e.g. address “001Fh” of page 0), the next data will be set to the first address of the same page (e.g. address “0000h” of page 0). This is why Page Write address increment is available in the same page.

(5) Read Status Register Command (RDSR)

By Read Status register command, data of status register can be read. As for this command, set CSB to Low, then input Instruction Code of Read Status Register command. This IC starts data output of the status register. Data output is started from SCK fall of 7 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, this IC repeats to output data of the status register.
Even if in write operation, Read Status Register command can be executed.

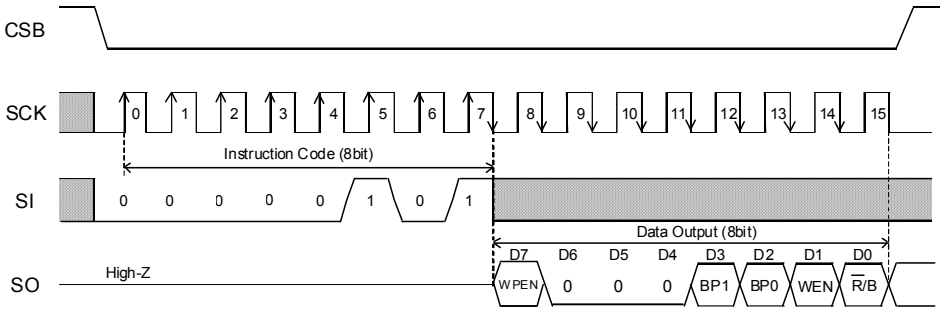


Figure 43. Read Status Register Command

(6) Write Status Register Command (WRSR)

Write Status Register command can write status register data. The data can be written by this command are 3 bits, that is, WPEN (D7), BP1 (D3) and BP0 (D2) among 8 bits of status register. As for this command, set CSB to Low, and input Instruction Code of Write Status Register command, and input data. Then, by making CSB to High, this IC starts write operation. Write Time requires time of $t_{E/W}$ as same as Write command. As for CSB rise, start CSB after taking the last data bit (D0), and before the next SCK clock starts. At other timing, command is cancelled.
To the write disabled block, write cannot be made, and only read can be made.
During write operation, other than Read Status Register command is not accepted.

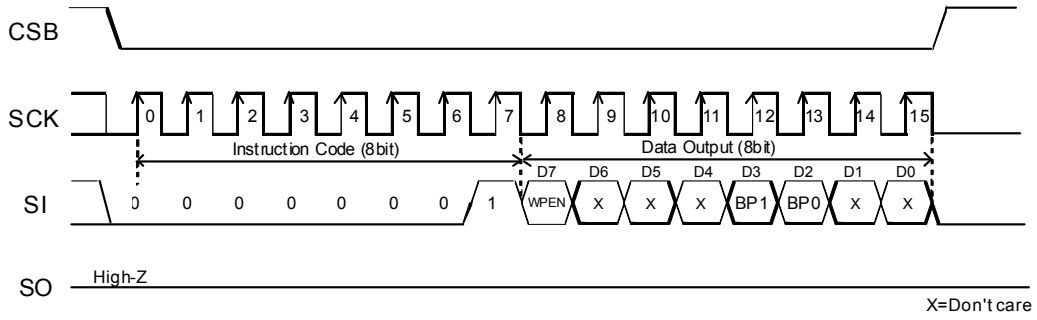


Figure 44. Write Status Register Command

(7) Read ID Page Command (RDID)

By Read ID Page command, data of ID Page can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read ID Page command. Input address bit A10 as “0”, other upper address bits A12 to A6 as “0”. By inputting lower address bits A4 to A0, it is possible to address to 32 bytes ID Page. Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. After reading data of the most significant address of ID Page, by continuing increment read, data of the least significant address of ID Page is read.

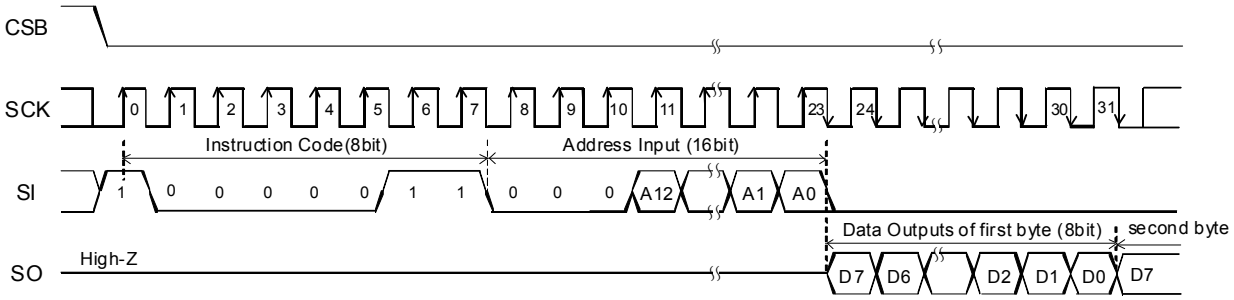


Figure 45. Read ID Page Command

(8) Write ID Page Command (WRID)

By Write ID Page command, data of ID Page can be written. As for this command, set CSB to Low, then input address and data after Instruction Code of Write ID Page command. Input address bit A10 as “0”, other upper address bits A12 to A6 as “0”. By inputting lower address bits A4 to A0, it is possible to address to 32 bytes ID Page. Then, by making CSB to High, the IC starts write operation. To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Write ID Page command is not executed, and this Write ID Page command is cancelled. The write time of EEPROM requires time of $t_{E/W}$ (Max 4ms).

During write operation, other than Read Status Register command is not accepted.

In case of Lock Status (LS) bit “1”, Write ID Page command can’t be executed.

Write ID Page command has Page Write Function same as Write command.

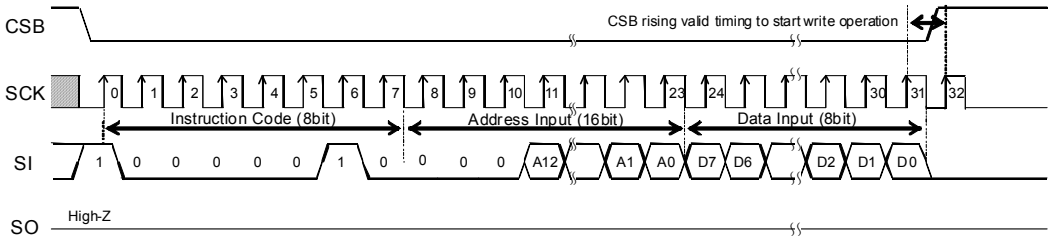


Figure 46. Write ID Page Command

(9) Read Lock Status Command (RDLS)

By Read Lock Status command, data of Lock Status can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read Lock Status command. Input address bit A10 as “1”, other address bits A12 to A0 as “0”. Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. The data D0 indicates Lock Status bit. The data D7 to D1 are Don’t Care. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, this IC repeats to output data of the Lock Status byte. In case of Lock Status (LS) bit “1”, ID Page is locked, Write ID Page command can’t be executed. In case of LS bit “0”, ID Page is released to lock, Write ID Page command can be executed.

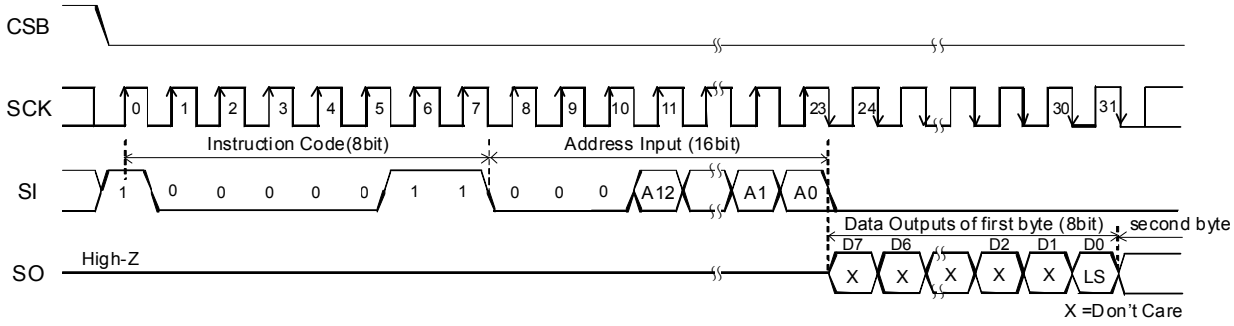


Figure 47. Read Lock Status Command

(10) Lock ID Page Command (LID)

By Lock ID Page command, data of Lock Status can be written. In case of Lock Status (LS) bit “1”, Lock ID Page command can’t be executed permanently. As for this command, set CSB to Low, then input address and data after Instruction Code of Lock ID Page command. Input address bit A10 as “1”, other address bits A12 to A0 as “0”. The data D1 is for LS bit, other data bits are Don’t Care. Then, by making CSB to High, the IC starts write operation. To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Lock ID Page command is not executed, and this Lock ID Page command is cancelled. The write time of EEPROM requires time of $t_{E/W}$ (Max 4ms).

During write operation, other than Read Status Register command is not accepted.

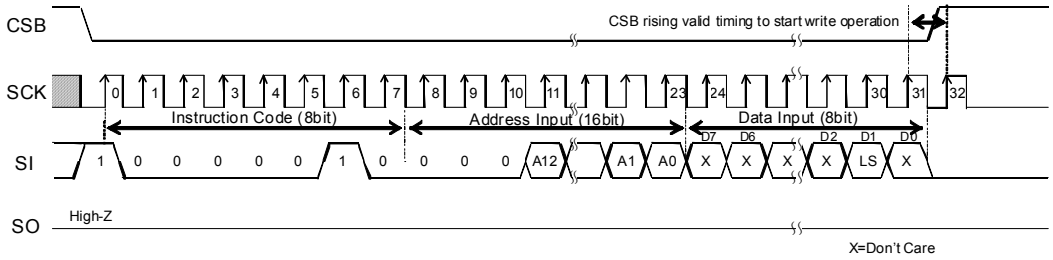


Figure 48. Lock ID Page Command

At Standby State

1. Standby Current

Set CSB = High, and be sure to set SCK, SI, WPB and HOLDB inputs = Low or High. Do not input intermediate electric potential.

2. Timing

As shown in Figure.49, at standby, when SCK is High, even if CSB is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB = High status.

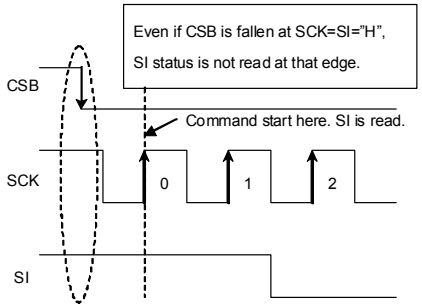


Figure 49. Operating Timing

Method to cancel each command

1. READ, RDID, RDLS

・Method to cancel : cancel by CSB = High

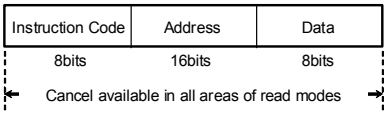


Figure 50. READ, RDID, RDLS Cancel Valid Timing

2. RDSR

・Method to cancel : cancel by CSB = High

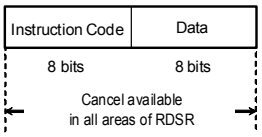


Figure 51. RDSR Cancel Valid Timing

3. WRITE, WRID, LID

a : Instruction Code, Address Input Area
Cancellation is available by CSB = High.

b : Data Input Area (D7 to D1 input area)
Cancellation is available by CSB = High.

c : Data Input Area (D0 area)
When CSB is started, write starts.
After CSB rise, cancellation cannot be made by any means.

d : $t_{E/W}$ Area
Cancellation is available by CSB = High. However, when write starts (CSB is started) in the area c, cancellation cannot be made by any means.
And by inputting on SCK clock, cancellation cannot be made.
In page write mode, there is write enable area at every 8 clocks

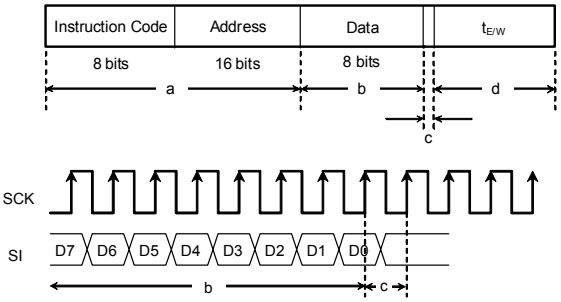


Figure 52. WRITE, WRID, LID Cancel Valid Timing

Note 1) If V_{CC} is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
Note 2) If CSB is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = Low area. As for SCK rise, assure timing of t_{CSS} / t_{CSH} or higher.

4. WRSR

a : From Instruction code to 15th rising of SCK
Cancel by CSB = High.

b : From 15th rising of SCK to 16th rising of SCK (write enable area)
When CSB is started, write starts.

c : After 16th rising of SCK
Cancel by CSB = High.
However, when write starts (CSB is started) in the area b, cancellation cannot be made by any means.
And, by inputting on SCK clock, cancellation cannot be made.

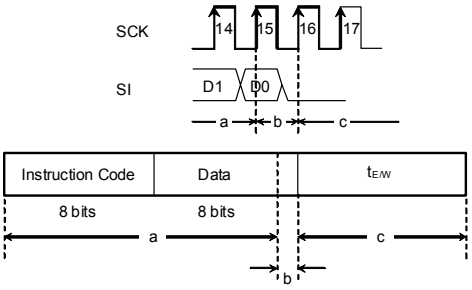


Figure 53. WRSR Cancel Valid Timing

Note 1) If V_{CC} is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
Note 2) If CSB is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = Low area. As for SCK rise, assure timing of t_{CSS} / t_{CSH} or higher.

5. WREN/WRDI

a : From instruction code to 7th rising of SCK
Cancel by CSB = High.

b : Cancellation is not available when CSB is started after 7th clock.

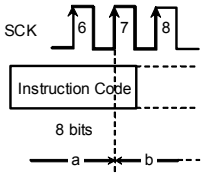


Figure 54. WREN/WRDI Cancel Valid Timing

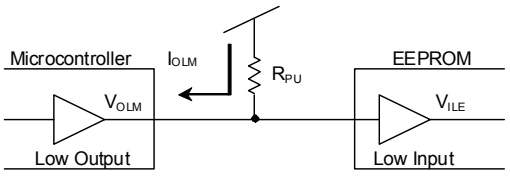
High speed operation

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

1. Pull Up, Pull Down Resistance for Input Pins

When to attach pull up, pull down resistance to EEPROM input pins, select an appropriate value for the microcontroller V_{OL}, I_{OL} from V_{IL} characteristics of this IC.

2. Pull Up Resistance



・V_{ILE} : V_{IL} specifications of EEPROM
・V_{OLM} : V_{OL} specifications of Microcontroller
・I_{OLM} : I_{OL} specifications of Microcontroller

Figure 55. Pull Up Resistance

$$R_{PU} \geq \frac{V_{CC} - V_{OLM}}{I_{OLM}} \quad \cdots ①$$

$$V_{OLM} \leq V_{ILE} \quad \cdots ②$$

Example) When Vcc=5V, V_{ILE}=1.5V, V_{OLM}=0.4V, I_{OLM}=2mA, from the equation ①,

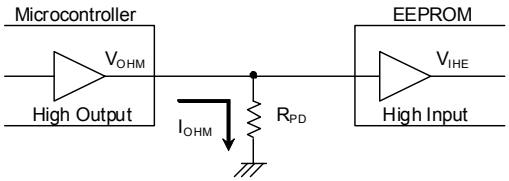
$$R_{PU} \geq \frac{5 - 0.4}{2 \times 10^{-3}}$$

$$\therefore R_{PU} \leq 2.3 \quad [k\Omega]$$

With the value of R_{PU} to satisfy the above equation, V_{OLM} becomes 0.4V or lower, and with V_{ILE} (=1.5V), the equation ② is also satisfied.

And, in order to prevent malfunction, mistake write at power ON/OFF, be sure to make CSB pull up.

3. Pull Down Resistance



・V_{IHE} : V_{IH} specifications of EEPROM
・V_{OHM} : V_{OH} specifications of Microcontroller
・I_{OHM} : I_{OH} specifications of Microcontroller

Figure 56. Pull Down Resistance

$$R_{PD} \geq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ③$$

$$V_{OHM} \geq V_{IHE} \quad \cdots ④$$

Example) When V_{CC}=5V, V_{OHM}=V_{CC}-0.5V, I_{OHM}=0.4mA, V_{IHE}=V_{CC}×0.7V, from the equation ③,

$$R_{PD} \geq \frac{5 - 0.5}{0.4 \times 10^{-3}}$$

$$\therefore R_{PU} \geq 11.3 \quad [k\Omega]$$

Further, by amplitude V_{IHE}, V_{ILE} of signal input to EEPROM, operation speed changes. By inputting signal of amplitude of Vcc / GND level to input, more stable high speed operations can be realized. On the contrary, when amplitude of 0.8Vcc / 0.2Vcc is input, operation speed becomes slow.(Note1)

In order to realize more stable high speed operation, it is recommended to make the values of R_{PU}, R_{PD} as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of Vcc / GND level.

(Note1) At this moment, operating timing guaranteed value is guaranteed.

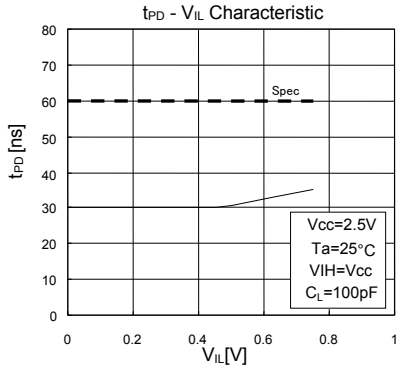


Figure 57. V_{IL} dependency of Data Output Delay Time t_{PD}

4. SO Load Capacitance Condition

Load capacitance of SO Pin affects upon delay characteristic of SO output. (Data Output Delay Time, Time from HOLDB to High-Z) In order to make output delay characteristic into higher speed, make SO load capacitance small. In concrete, “Do not connect many devices to SO bus”, “Make the wire between the controller and EEPROM short”, and so forth.

5. Other cautions

Make the wire length from the Microcontroller to EEPROM input signal same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.