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## Serial EEPROM Series Standard EEPROM

## SPI BUS EEPROM

# BR25Lxxx-W Series

# (1K 2K 4K 8K 16K 32K 64K)

### ●General Description

BR25Lxxx-W series is a serial EEPROM of SPI BUS interface method.

### ●Features

- High speed clock action up to 5MHz (Max.)
- Wait function by HOLD terminal
- Part or whole of memory arrays settable as read only memory area by program
- 1.8V to 5.5V single power source action most suitable for battery use
- Page write mode useful for initial value write at factory shipment
- Highly reliable connection by Au pad and Au wire
- For SPI bus interface
  (CPOL, CPHA) = (0, 0), (1, 1)
- Auto erase and auto end function at data rewrite
- Low current consumption
  - At write action (5V) : 1.5mA (Typ.)
  - At read action (5V) : 1.0mA (Typ.)
  - At standby action (5V) : 0.1μA (Typ.)
- Address auto increment function at read action
- Write mistake prevention function
  - Write prohibition at power on
  - Write prohibition by command code (WRDI)
  - Write prohibition by $\overline{WP}$ pin
  - Write prohibition block setting by status registers (BP1, BP0)
  - Write mistake prevention function at low voltage
- Data at shipment Memory array : FFh, status register WPEN, BP1, BP0 : 0
- Data kept for 40 years
- Data rewrite up to 1,000,000 times

### ●Packages W(Typ.) x D(Typ.) x H(Max.)

**DIP-T8**
9.30mm x 6.50mm x 7.10mm

**TSSOP-B8**
3.00mm x 6.40mm x 1.20mm

**SOP8**
5.00mm x 6.20mm x 1.71mm

**TSSOP-B8J**
3.00mm x 4.90mm x 1.10mm

**SOP- J8**
4.90mm x 6.00mm x 1.65mm

**MSOP8**
2.90mm x 4.00mm x 0.90mm

**SSOP-B8**
3.00mm x 6.40mm x 1.35mm

### ●Page write

| Number of pages | 16Byte | 32Byte |
|---|---|---|
| Product number | BR25L010-W<br>BR25L020-W<br>BR25L040-W | BR25L080-W<br>BR25L160-W<br>BR25L320-W<br>BR25L640-W |

### ●BR25L Series

| Capacity | Bit format | Type | Power source voltage | DIP-T8 | SOP8 | SOP-J8 | SSOP-B8 | TSSOP-B8 | MSOP8 | TSSOP-B8J |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | F | FJ | FV | FVT | FVM | FVJ |
| 1Kbit | 128 X 8 | BR25L010-W | 1.8 ~ 5.5V | | ● | ● | ● | ● | ● | ● |
| 2Kbit | 256 X 8 | BR25L020-W | 1.8 ~ 5.5V | | ● | ● | ● | ● | ● | ● |
| 4Kbit | 512 X 8 | BR25L040-W | 1.8 ~ 5.5V | ● | ● | ● | ● | ● | ● | ● |
| 8Kbit | 1K X 8 | BR25L080-W | 1.8 ~ 5.5V | ● | ● | ● | ● | ● | | |
| 16Kbit | 2K X 8 | BR25L160-W | 1.8 ~ 5.5V | ● | ● | ● | ● | ● | | |
| 32Kbit | 4K X 8 | BR25L320-W | 1.8 ~ 5.5V | ● | ● | ● | | | | |
| 64Kbit | 8K X 8 | BR25L640-W | 1.8 ~ 5.5V | ● | ● | ● | | | | |

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

●**Absolute Maximum Ratings** (Ta=25℃)

| Parameter | Symbol | Limits | Unit | Remarks |
|---|---|---|---|---|
| Impressed voltage | $V_{CC}$ | -0.3 to +6.5 | V | |
| Permissible dissipation | Pd | 800 (DIP-T8) | mW | When using at Ta=25℃ or higher, 8.0mW to be reduced per 1℃. |
| | | 450 (SOP8) | | When using at Ta=25℃ or higher, 4.5mW to be reduced per 1℃. |
| | | 450 (SOP-J8) | | When using at Ta=25℃ or higher, 4.5mW to be reduced per 1℃. |
| | | 300 (SSOP-B8) | | When using at Ta=25℃ or higher, 3.0mW to be reduced per 1℃. |
| | | 330 (TSSOP-B8) | | When using at Ta=25℃ or higher, 3.3mW to be reduced per 1℃. |
| | | 310 (MSOP8) | | When using at Ta=25℃ or higher, 3.1mW to be reduced per 1℃. |
| | | 310 (TSSOP-B8J) | | When using at Ta=25℃ or higher, 3.1mW to be reduced per 1℃. |
| Storage temperature range | Tstg | −65 to +125 | ℃ | |
| Operating temperature range | Topr | −40 to +85 | ℃ | |
| Terminal Voltage | - | -0.3 to Vcc+0.3 | V | |

●**Memory cell characteristics (Ta=25°C , Vcc=1.8V to 5.5V)**

| Parameter | Limits | | | Unit |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| Number of data rewrite times *1 | 1,000,000 | - | - | Times |
| Data hold years *1 | 40 | - | - | Years |

*1 Not 100% TESTED

●**Recommended Operating Ratings**

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power source voltage | Vcc | 1.8 to 5.5 | V |
| Input voltage | Vin | 0 to Vcc | |

●**Input / output capacity** (Ta=25°C, frequency=5MHz)

| Parameter | Symbol | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Input capacity *1 | $C_{IN}$ | − | 8 | pF | $V_{IN}$=GND |
| Output capacity *1 | $C_{OUT}$ | − | 8 | | $V_{OUT}$=GND |

*1 Not 100% TESTED.

●**Electrical Characteristics** (Unless otherwise specified, Ta=-40°C to +85°C, Vcc=1.8V to 5.5V)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| “H” input voltage1 | VIH | 0.7Vcc | − | Vcc+0.3 | V | 1.8V≦Vcc≦5.5V |
| “L” input voltage1 | VIL | -0.3 | − | 0.3Vcc | V | 1.8V≦Vcc≦5.5V |
| “L” output voltage1 | VOL1 | 0 | − | 0.4 | V | IOL=2.1mA(Vcc=2.5V to 5.5V) |
| “L” output voltage2 | VOL2 | 0 | − | 0.2 | V | IOL=150μA(Vcc=1.8V to 2.5V) |
| “H” output voltage1 | VOH1 | Vcc-0.5 | − | Vcc | V | IOH=-0.4mA(Vcc=2.5V to 5.5V) |
| “H” output voltage2 | VOH2 | Vcc-0.2 | − | Vcc | V | IOH=-100μA(Vcc=1.8V to 2.5V) |
| Input leak current | ILI | -1 | − | 1 | μA | $V_{IN}$=0 to Vcc |
| Output leak current | ILO | -1 | − | 1 | μA | VOUT=0 to Vcc, $\overline{CS}$=Vcc |
| Current consumption at write action | Icc1 | − | − | 1.0 | mA | Vcc=1.8V, fSCK=2MHz, tE/W=5ms<br>Byte write, Page write, Write status register |
| | Icc2 | − | − | 2.0 | mA | Vcc=2.5V, fSCK=5MHz, tE/W=5ms<br>Byte write, Page write, Write status register |
| | Icc3 | − | − | 3.0 | mA | Vcc=5.5V, fSCK=5MHz, tE/W=5ms<br>Byte write, Page write, Write status register |
| Current consumption at read action | Icc4 | − | − | 1.5 | mA | Vcc=2.5V, fSCK=5MHz<br>Read, Read status register |
| | Icc5 | − | − | 2.0 | mA | Vcc=5.5V, fSCK=5MHz<br>Read, Read status register |
| Standby current | ISB | − | − | 2 | μA | Vcc=5.5V,SO=OPEN<br>$\overline{CS}$=$\overline{HOLD}$=$\overline{WP}$=Vcc, SCK=SI=Vcc or =GND |

●**Operating timing characteristics (Ta=-40°C to +85°C, unless otherwise specified, load capacity $C_{L1}$ 100pF)**

| Parameter | Symbol | 1.8V≦Vcc<2.5V | | | 2.5V≦Vcc<5.5V | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| SCK frequency | fSCK | - | - | 2 | - | - | 5 | MHz |
| SCK high time | tSCKWH | 200 | - | - | 85 | - | - | ns |
| SCK low time | tSCKWL | 200 | - | - | 85 | - | - | ns |
| $\overline{CS}$ high time | tCS | 200 | - | - | 85 | - | - | ns |
| $\overline{CS}$ setup time | tCSS | 200 | - | - | 90 | - | - | ns |
| $\overline{CS}$ hold time | tCSH | 200 | - | - | 85 | - | - | ns |
| SCK setup time | tSCKS | 200 | - | - | 90 | - | - | ns |
| SCK hold time | tSCKH | 200 | - | - | 90 | - | - | ns |
| SI setup time | tDIS | 40 | - | - | 20 | - | - | ns |
| SI hold time | tDIH | 50 | - | - | 40 | - | - | ns |
| Data output delay time 1 | tPD1 | - | - | 150 | - | - | 70 | ns |
| Data output delay time 2 ($CL_2$=30pF) | tPD2 | - | - | 145 | - | - | 55 | ns |
| Output hold time | tOH | 0 | - | - | 0 | - | - | ns |
| Output disable time | tOZ | - | - | 250 | - | - | 100 | ns |
| $\overline{HOLD}$ setting setup time | tHFS | 120 | - | - | 60 | - | - | ns |
| $\overline{HOLD}$ setting hold time | tHFH | 90 | - | - | 40 | - | - | ns |
| $\overline{HOLD}$ release setup time | tHRS | 120 | - | - | 60 | - | - | ns |
| $\overline{HOLD}$ release hold time | tHRH | 140 | - | - | 70 | - | - | ns |
| Time from $\overline{HOLD}$ to output High-Z | tHOZ | - | - | 250 | - | - | 100 | ns |
| Time from $\overline{HOLD}$ to output change | tHPD | - | - | 150 | - | - | 70 | ns |
| SCK rise time *1 | tRC | - | - | 1 | - | - | 1 | µs |
| SCK fall time *1 | tFC | - | - | 1 | - | - | 1 | µs |
| OUTPUT rise time *1 | tRO | - | - | 100 | - | - | 50 | ns |
| OUTPUT fall time *1 | tFO | - | - | 100 | - | - | 50 | ns |
| Write time | tE/W | - | - | 5 | - | - | 5 | ms |

*1 NOT 100% TESTED

●**AC measurement conditions**

| Parameter | Symbol | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Load capacity 1 | $C_{L1}$ | - | - | 100 | pF |
| Load capacity 2 | $C_{L2}$ | | | 30 | pF |
| Input rise time | - | - | - | 50 | ns |
| Input fall time | - | - | - | 50 | ns |
| Input voltage | - | 0.2Vcc/0.8Vcc | | | V |
| Input / output judgment voltage | - | 0.3Vcc/0.7Vcc | | | V |

**●Sync data input / output timing**

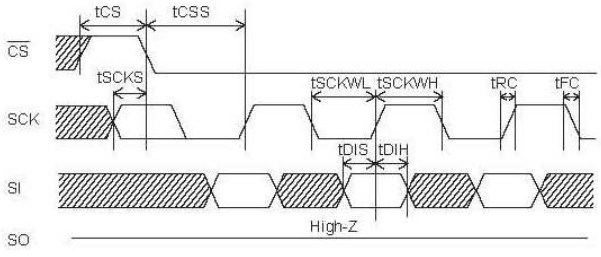



Figure 1. Input timing

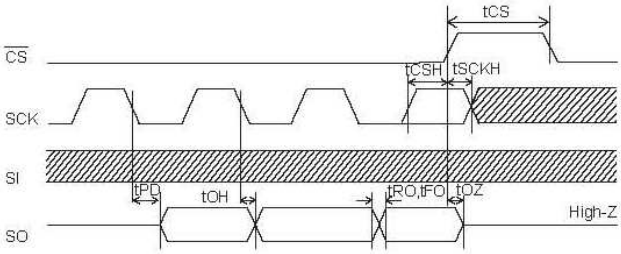



Figure 2. Input / output timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the most significant bit MSB.

SO is output in sync with data fall edge of SCK. Data is output from the most significant bit MSB.

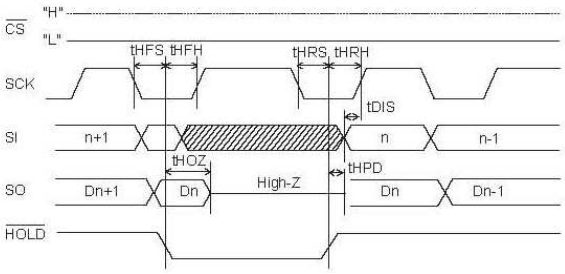
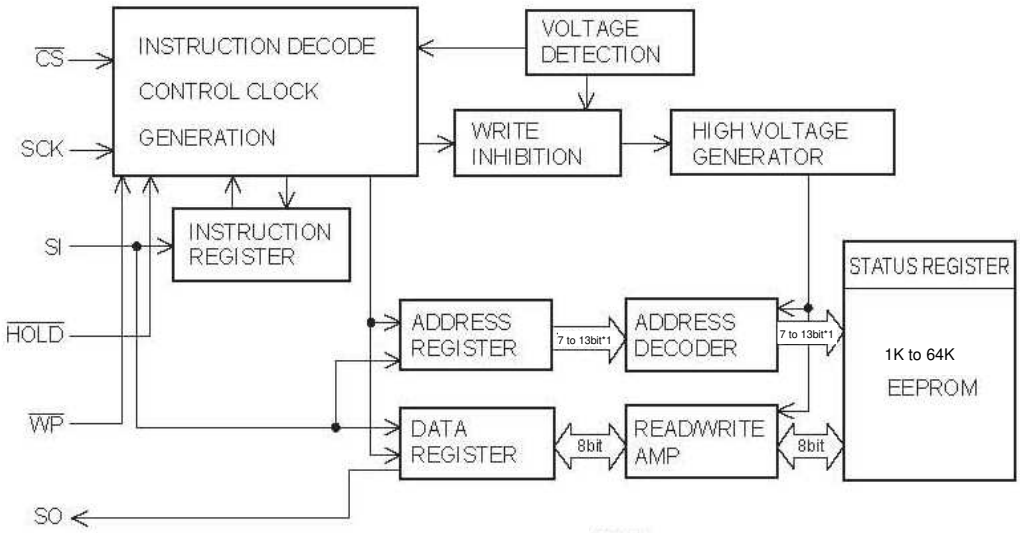



Figure 3. $\overline{\text{HOLD}}$ timing

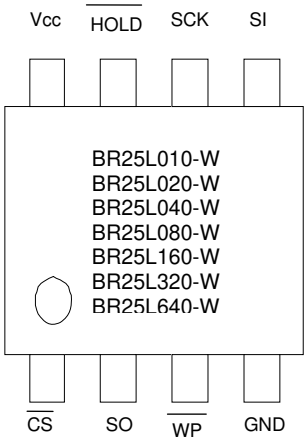
## ●Block Diagram




*1 7bit: BR25L010-W
8bit: BR25L020-W
9bit: BR25L040-W
10bit: BR25L080-W
11bit: BR25L160-W
12bit: BR25L320-W
13bit: BR25L640-W

## ●Pin Configuration

(TOP VIEW)




## ●Pin Descriptions

| Terminal name | Input /output | Function |
|---|---|---|
| Vcc | - | Power source to be connected |
| GND | - | All input / output reference voltage, 0V |
| $\overline{CS}$ | Input | Chip select input |
| SCK | Input | Serial clock input |
| SI | Input | Start bit, ope code, address, and serial data input |
| SO | Output | Serial data output |
| $\overline{HOLD}$ | Input | Hold input<br>Command communications may be suspended temporarily (HOLD status). |
| $\overline{WP}$ | Input | Write protect input<br>Write command is prohibited. *1<br>Write status register command is prohibited. |

*1:BR25L010/020/040-W

**●Typical Performance Curves**

(The following characteristic data are Typ. Values.)

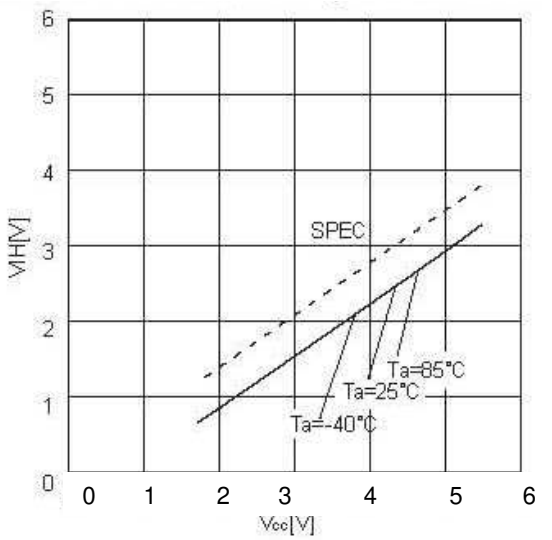



Figure 4. "H" input voltage VIH

($\overline{CS}$,SCK,SI,$\overline{HOLD}$,$\overline{WP}$)

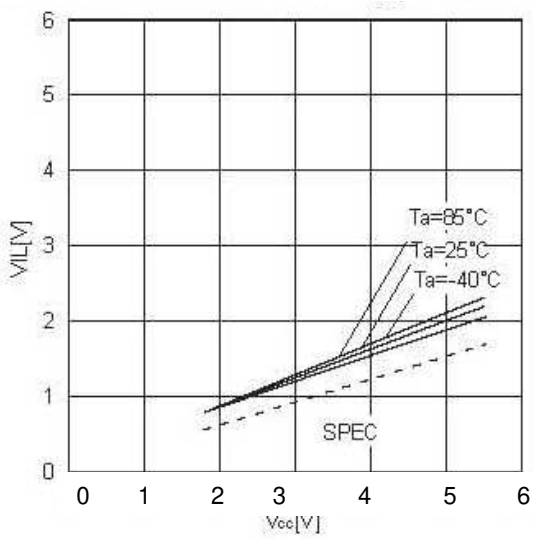



Figure 5. "L" input voltage VIL

($\overline{CS}$,SCK,SI,$\overline{HOLD}$,$\overline{WP}$)

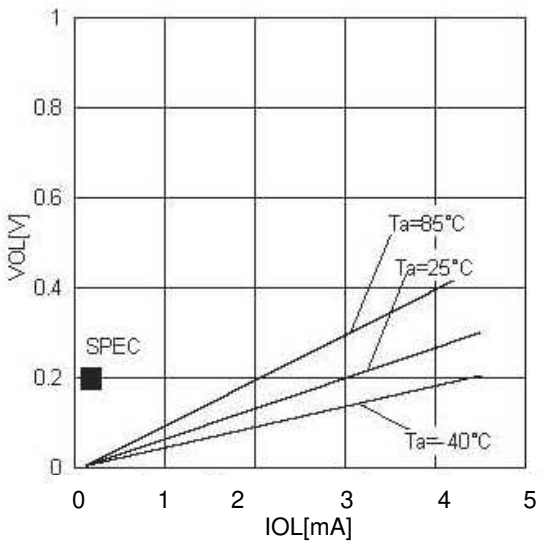



Figure 6. "L" output voltage VOL-IOL(Vcc=1.8V)

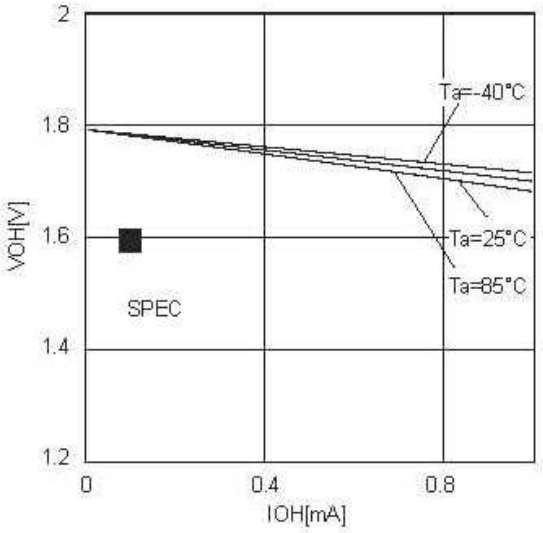



Figure 7. "H" output voltage VOH-IOH (Vcc=1.8V)

**●Typical Performance Curves - Continued**

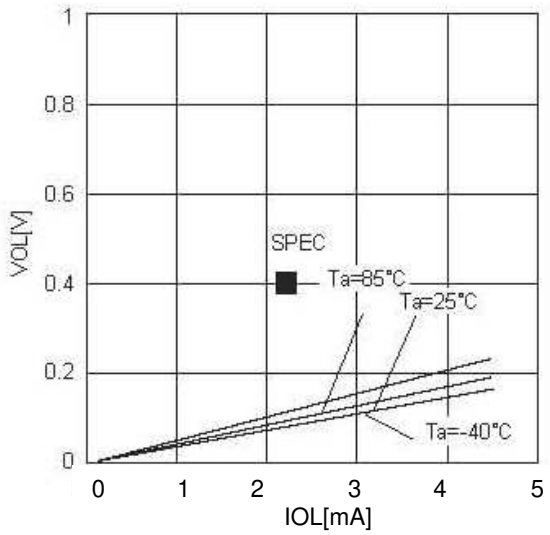



Figure 8. "L" output voltage VOL-IOL(Vcc=2.5V)

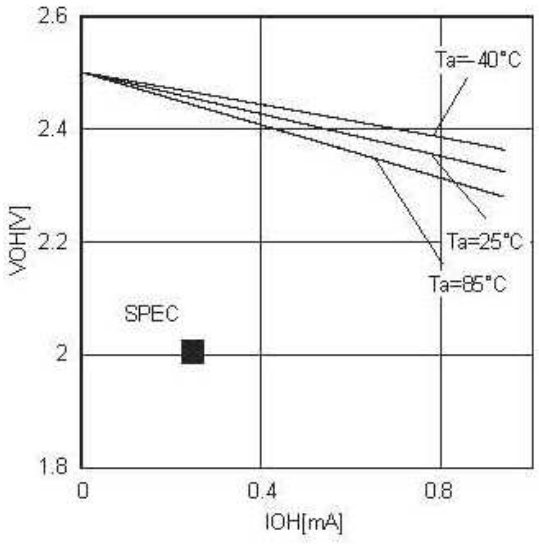



Figure 9. "H" output voltage VOH-IOH(Vcc=2.5V)

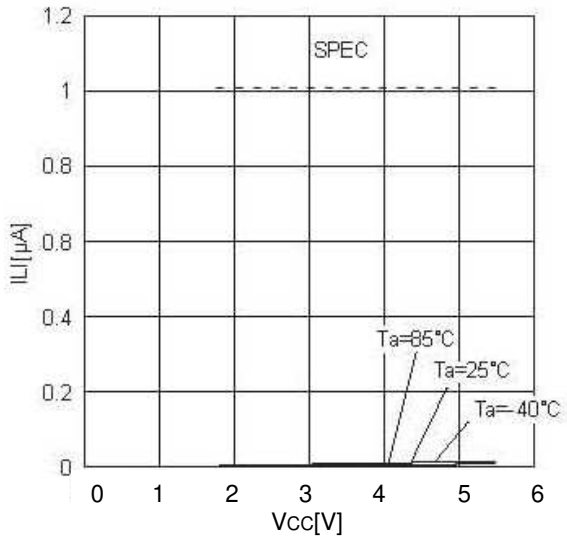



Figure 10. Input leak current ILI

($\overline{CS}$,SCK,SI,$\overline{WP}$,$\overline{HOLD}$)

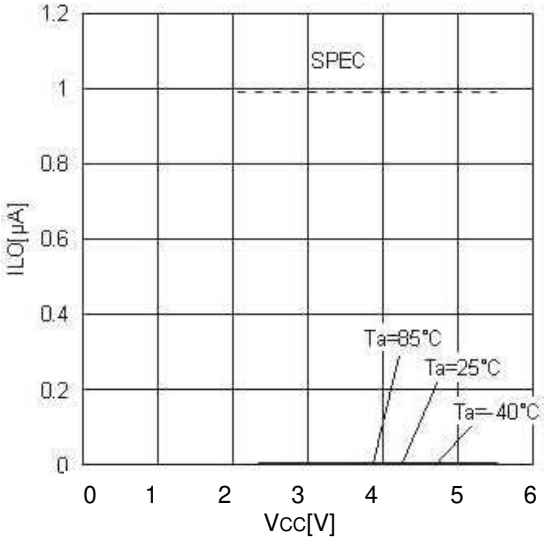



Figure 11. Output leak current ILO(SO)

●**Typical Performance Curves - Continued**

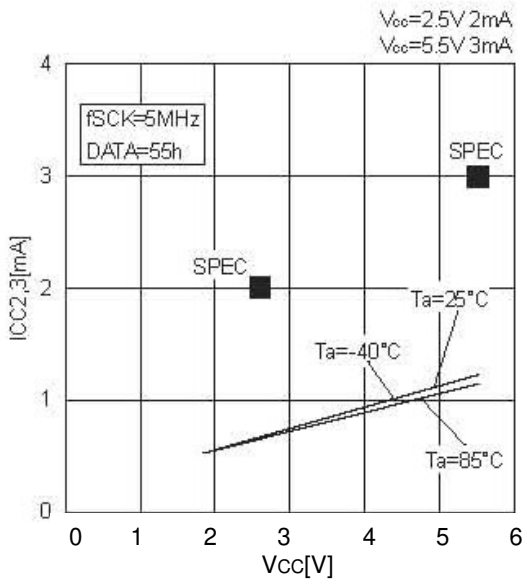



Figure 12. Current consumption at WRITE operation ICC1,2,3 (WRITE,PAGE WRITE,WRSR,fSCK=5MHz) BR25L010-W,BR25L020-W,BR25L040-W

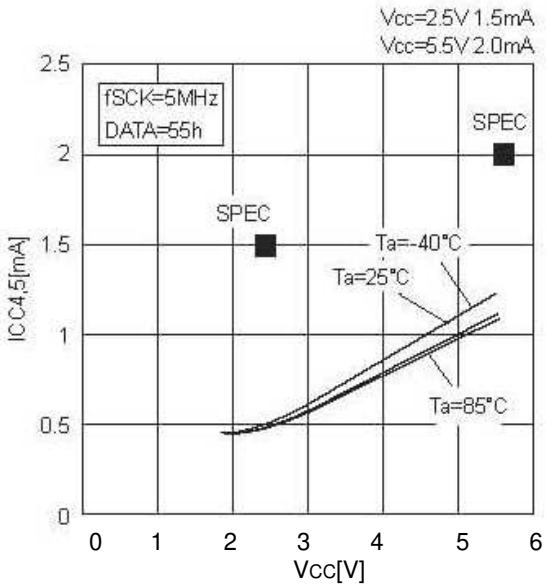



Figure 13. Consumption current at READ operation ICC4,5 (READ, WRSR,fSK=5MHz)

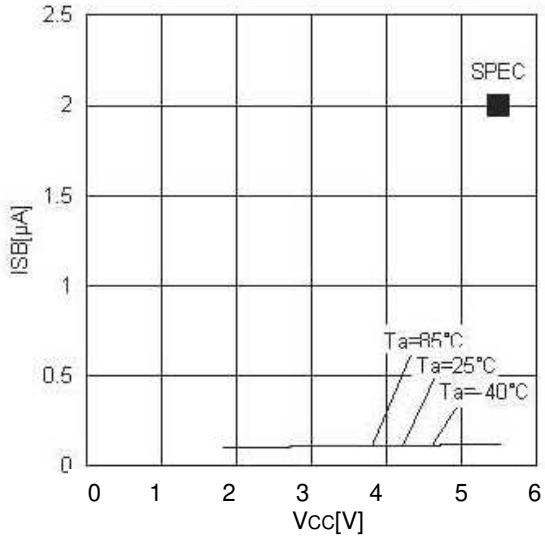



Figure 14. Consumption current at standby operation ISB

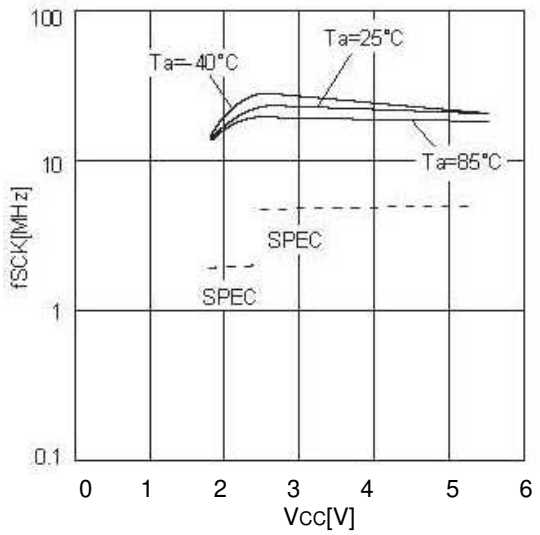



Figure 15. SCK frequency tSCK

**●Typical Performance Curves - Continued**

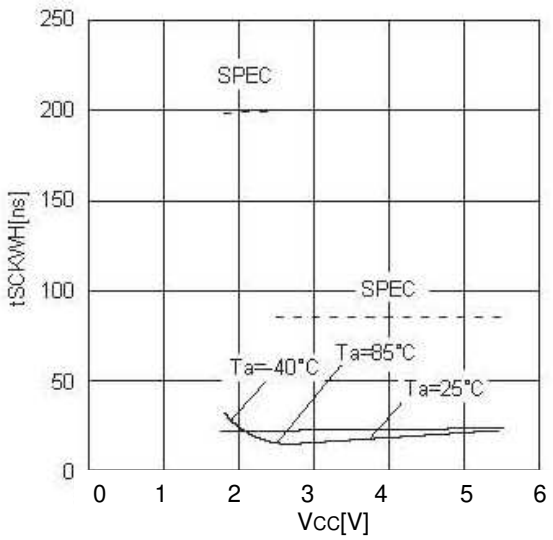



Figure 16. tSCK high time tSCKWH

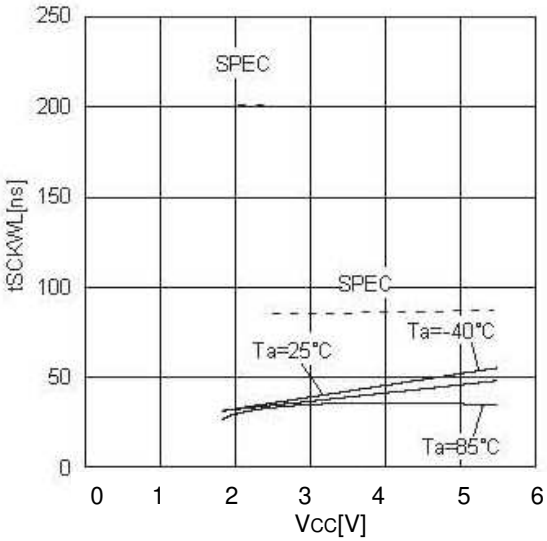



Figure 17. SCK low time tSCKWL

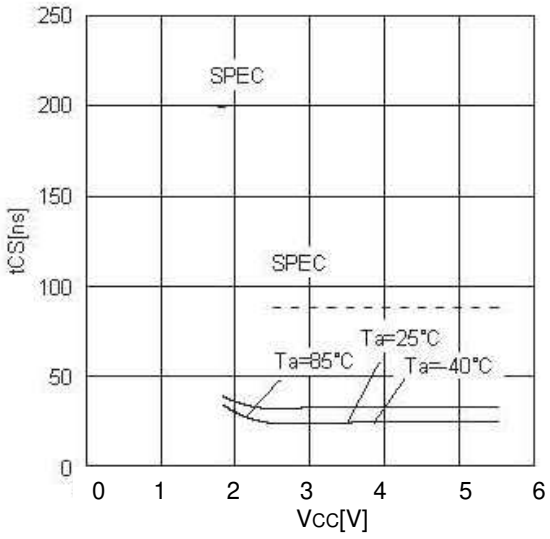



Figure 18. $\overline{CS}$ high time tCS

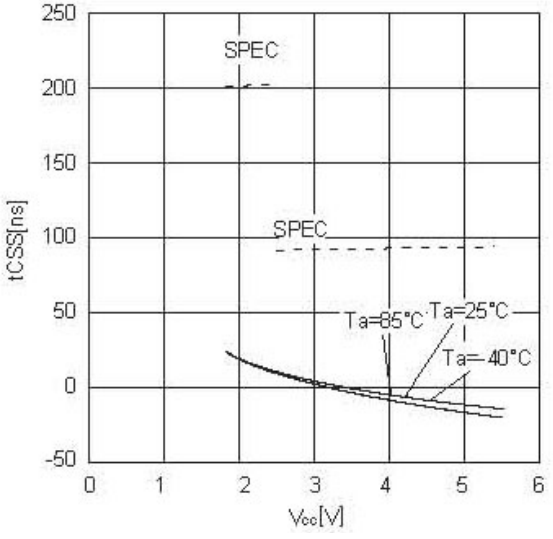



Figure 19. $\overline{CS}$ setup time tCSS

●**Typical Performance Curves - Continued**

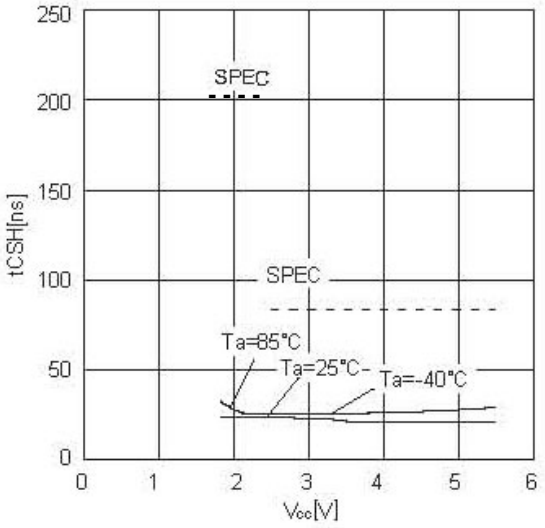



Figure 20. $\overline{CS}$ hold time tCSH

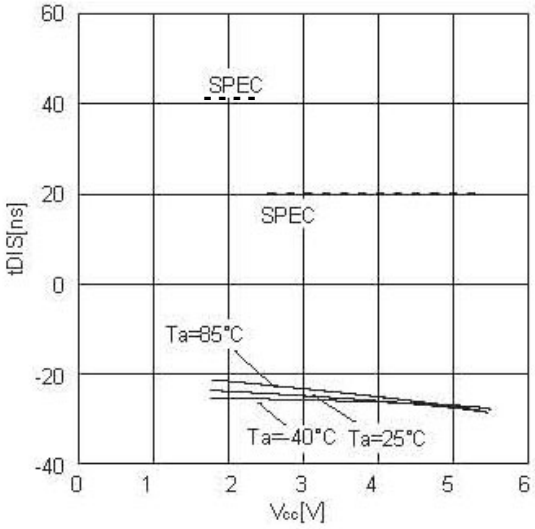



Figure 21. SI setup time tDIS

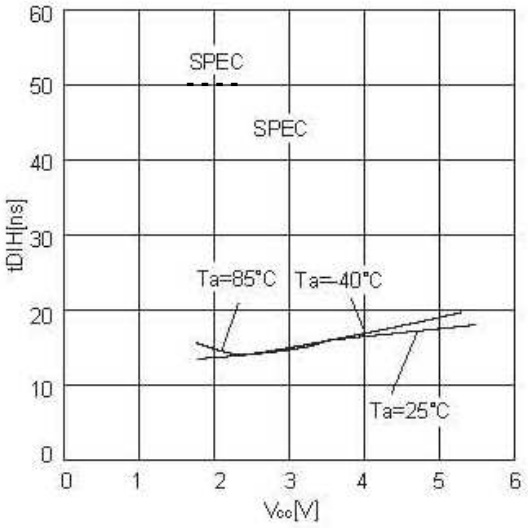



Figure 22. SI hold time tDIH

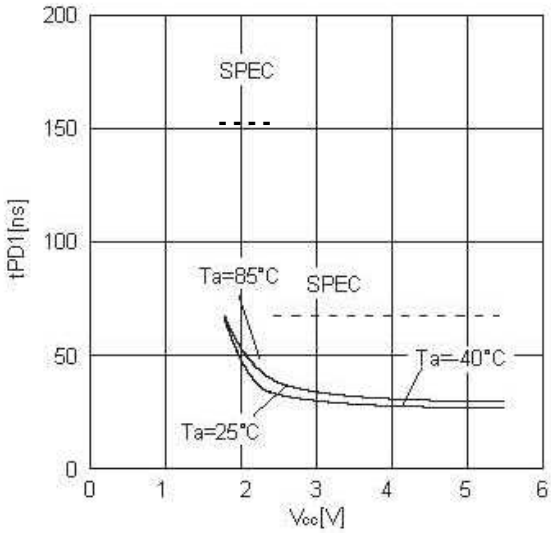



Figure 23. Data output delay time tPD1(CL=100pF)

●**Typical Performance Curves - Continued**

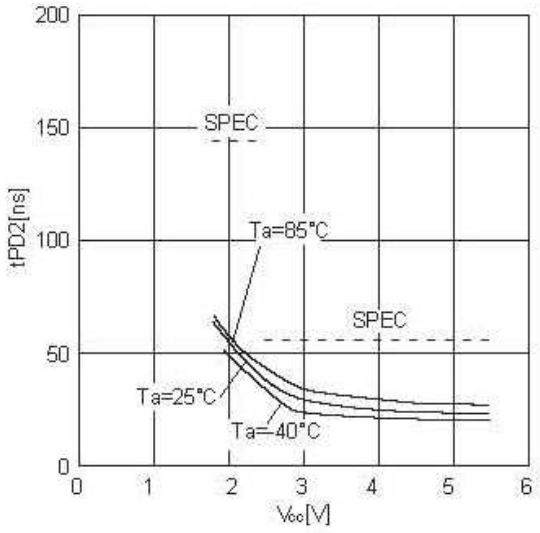



Figure 24. Data output delay time tPD2(CL=30pF)

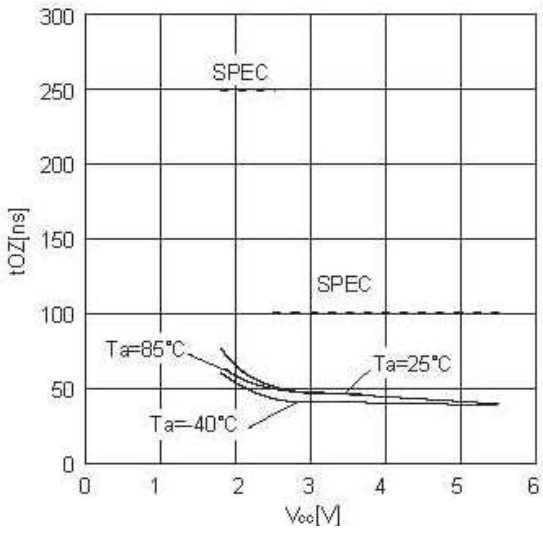



Figure 25. Output disable time tOZ

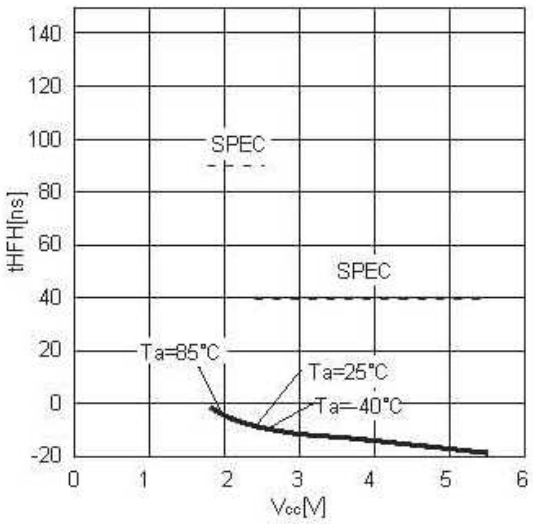



Figure 26. $\overline{\text{HOLD}}$ setting hold time tHFH

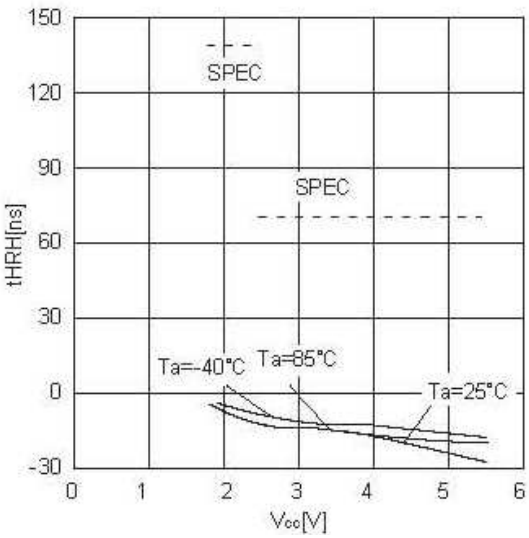



Figure 27. $\overline{\text{HOLD}}$ release hold time tHRH

**●Typical Performance Curves - Continued**

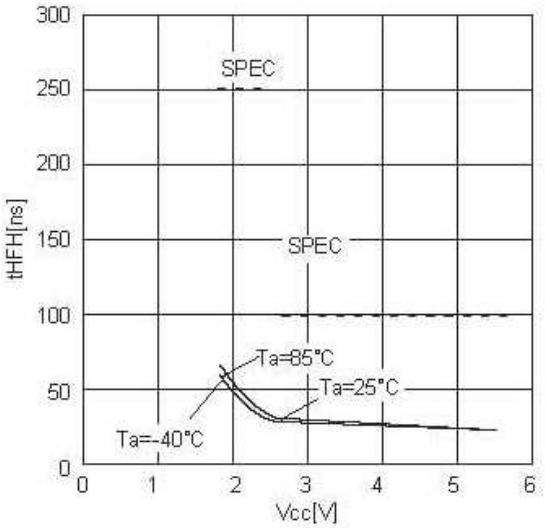



Figure 28. Time from $\overline{HOLD}$ to output High-Z tHOZ

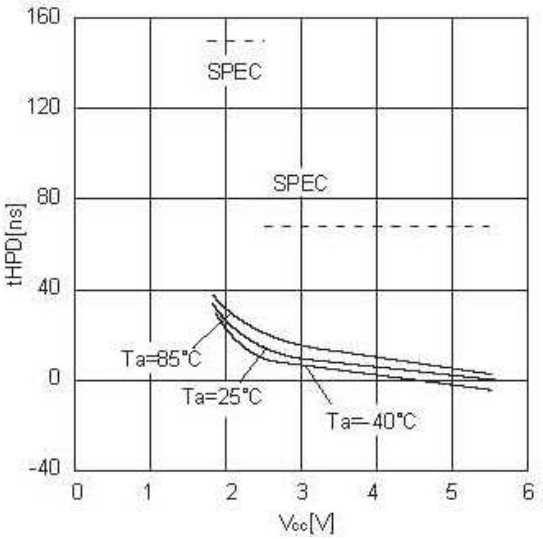



Figure 29. Time from $\overline{HOLD}$ to output change tHPO

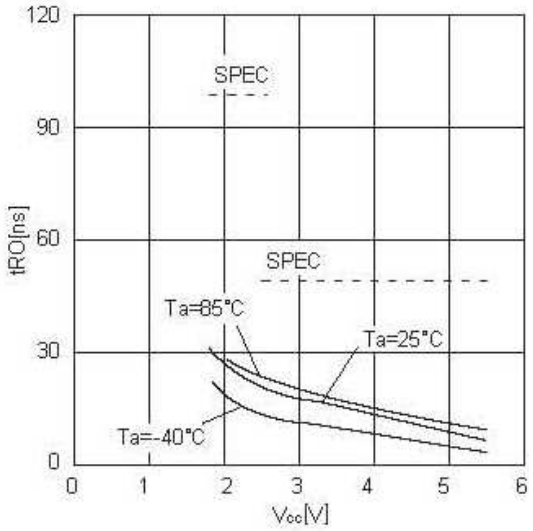



Figure 30. Output rise time tRO

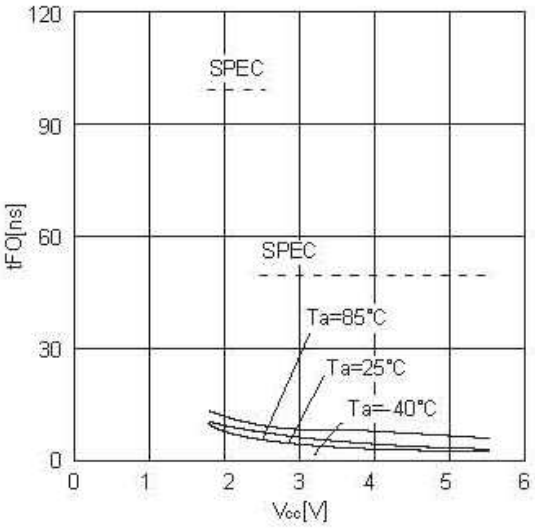



Figure 31. Output fall time

●**Typical Performance Curves - Continued**

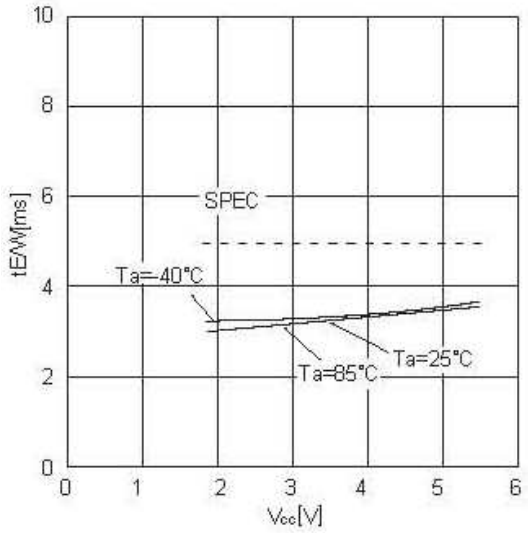



Figure 32. Write cycle time tE/W

## ●Features

○Status registers

This IC has status registers. The status registers are of 8 bits and express the following parameters.
BP0 and BP1 can be set by write status register command. These 2 bits are memorized into the EEPROM, therefore are valid even when power source is turned off.
Rewrite characteristics and data hold time are same as characteristics of the EEPROM.
WEN can be set by write enable command and write disable command. WEN becomes write disable status when power source is turned off. R/B is for write confirmation, therefore cannot be set externally.
The value of status register can be read by read status command.

## ●Status registers

| Product number | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| BR25L010-W | 1 | 1 | 1 | 1 | BP1 | BP0 | WEN | R/B |
| BR25L020-W | | | | | | | | |
| BR25L040-W | | | | | | | | |
| BR25L080-W | WPEN | 0 | 0 | 0 | BP1 | BP0 | WEN | R/B |
| BR25L160-W | | | | | | | | |
| BR25L320-W | | | | | | | | |
| BR25L640-W | | | | | | | | |

| bit | Memory location | Function | Contents |
|---|---|---|---|
| WPEN | EEPROM | WP pin enable / disable designation bit<br>WPEN=0=invalid<br>WPEN=1=valid | This enables / disables the functions of WP pin. |
| BP1<br>BP0 | EEPROM | EEPROM write disable block designation bit | This designates the write disable area of EEPROM. Write designation areas of product numbers are shown below. |
| WEN | Register | Write and write status register write enable / disable status confirmation bit<br>WEN=0=prohibited<br>WEN=1=permitted | |
| R/B | Register | Write cycle status (READY / BUSY) status confirmation bit<br>R/B=0=READY<br>R/B=1=BUSY | |

## ●Write disable block setting

| BP1 | BP0 | Write disable block | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | BR25L010-W | BR25L020-W | BR25L040-W | BR25L080-W | BR25L160-W | BR25L320-W | BR25L640-W |
| 0 | 0 | None | None | None | None | None | None | None |
| 0 | 1 | 60h-7Fh | C0h-FFh | 180h-1FFh | 300h-3FFh | 600h-7FFh | C00h-FFFh | 1800h-1FFFh |
| 1 | 0 | 40h-7Fh | 80h-FFh | 100h-1FFh | 200h-3FFh | 400h-7FFh | 800h-FFFh | 1000h-1FFFh |
| 1 | 1 | 00h-7Fh | 00h-FFh | 000h-1FFh | 000h-3FFh | 000h-7FFh | 000h-FFFh | 0000h-1FFFh |

○WP pin

By setting WP=LOW, write command is prohibited. As for BR25L080, 160, 320, 640-W, only when WPEN bit is set "1", the WP pin functions become valid. And the write command to be disabled at this moment is WRSR. As for BR25L010, 020, 040-W, both WRITE and WRSR commands are prohibited.
However, when write cycle is in execution, no interruption can be made.

| Product number | WRSR | WRITE |
|---|---|---|
| BR25L010-W | Prohibition possible | Prohibition possible |
| BR25L020-W | | |
| BR25L040-W | | |
| BR25L080-W | Prohibition possible but WPEN bit "1" | Prohibition impossible |
| BR25L160-W | | |
| BR25L320-W | | |
| BR25L640-W | | |

○HOLD pin

By HOLD pin, data transfer can be interrupted. When SCK="1", by making HOLD from "1" into"0", data transfer to EEPROM is interrupted. When SCK = "0", by making HOLD from "0" into "1", data transfer is restarted.

●**Command mode**

| Command | | Contents | Ope code | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | BR25L010-W BR25L020-W | | BR25L040-W | | BR25L080-W BR25L160-W BR25L320-W BR25L640-W | |
| WREN | Write enable | Write enable command | 0000 | * 110 | 0000 | * 110 | 0000 | 0110 |
| WRDI | Write disable | Write disable command | 0000 | * 100 | 0000 | * 100 | 0000 | 0100 |
| READ | Read | Read command | 0000 | * 011 | 0000 | A8011 | 0000 | 0011 |
| WRITE | Write | Write command | 0000 | * 010 | 0000 | A8010 | 0000 | 0010 |
| RDSR | Read status register | Status register read command | 0000 | * 101 | 0000 | * 101 | 0000 | 0101 |
| WRSR | Write status register | Status register write command | 0000 | * 001 | 0000 | * 001 | 0000 | 0001 |

●**Timing chart**

1. Write enable (WREN) / disable (WRDI) cycle

WREN (WRITE ENABLE): Write enable

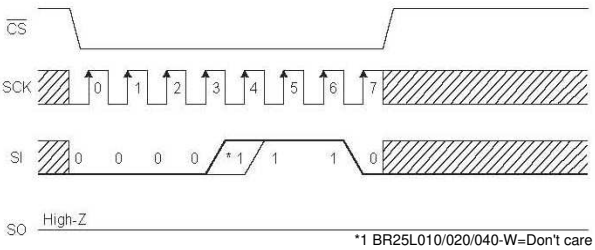



Figure 33. Write enable command

WRDI (WRIDE DISABLE): Write disable

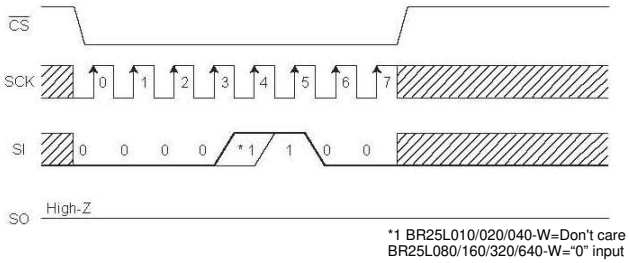



Figure 34. Write disable

○This IC has write enable status and write disable status. It is set to write enable status by write enable command, and it is set to write disable status by write disable command. As for these commands, set CS LOW, and then input the respective ope codes. The respective commands accept command at the 7-th clock rise. Even with input over 7 clocks, command becomes valid. When to carry out write and write status register command, it is necessary to set write enable status by the write enable command. If write or write status register command is input in the write disable status, commands are cancelled. And even in the write enable status, once write and write status register command is executed once, it gets in the write disable status. After power on, this IC is in write disable status.

2. Read command (READ)

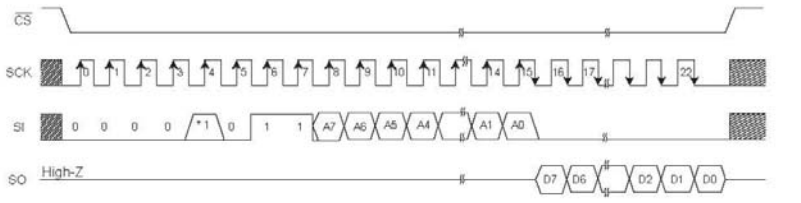



Figure 35. Read command (BR25L010/020/040-W)

| Product number | Address length |
|---|---|
| BR25L010-W | A6-A0 |
| BR25L020-W | A7-A0 |
| BR25L040-W | A8-A0 |

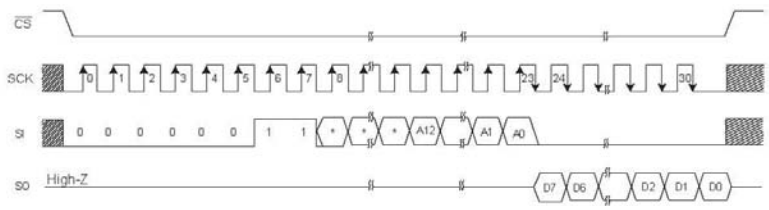


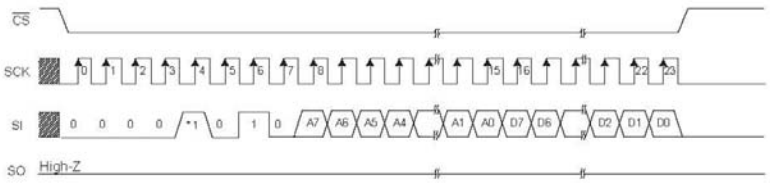

Figure 36. Read command (BR25L080/160/320/640-W)

| Product number | Address length |
|---|---|
| BR25L080-W | A9-A0 |
| BR25L160-W | A10-A0 |
| BR25L320-W | A11-A0 |
| BR25L640-W | A12-A0 |

By read command, data of EEPROM can be read. As for this command, set $\overline{CS}$ LOW, then input address after read ope code. EEPROM starts data output of the designated address. Data output is started from SCK fall of 15/23*1 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8 bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM. After reading data of the most significant address, by continuing increment read, data of the most insignificant address is read.

*1 BR25L010/020/040-W=15 clocks
BR25L080/160/320/640-W=23 clocks

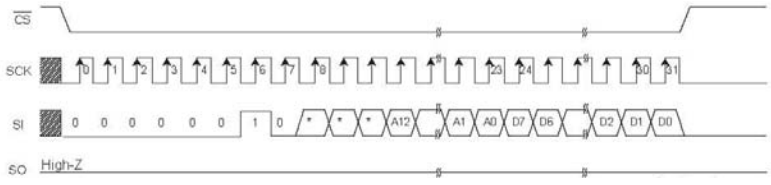
3. Write command (WRITE)




*1 BR25L010/020-W=Don't care
BR25L040-W=A8

Figure 37. Write command (BR25L010/020/040-W)

| Product number | Address length |
|---|---|
| BR25L010-W | A6-A0 |
| BR25L020-W | A7-A0 |
| BR25L040-W | A8-A0 |




* =Don't care

Figure 38. Write command (BR25L080/160/320/640-W)

| Product number | Address length |
|---|---|
| BR25L080-W | A9-A0 |
| BR25L160-W | A10-A0 |
| BR25L320-W | A11-A0 |
| BR25L640-W | A12-A0 |

By write command, data of EEPROM can be written. As for this command, set $\overline{CS}$ LOW, then input address and data after write ope code. Then, by making $\overline{CS}$ HIGH, the EEPROM starts writing. The write time of EEPROM requires time of tE/W (Max 5ms). During tE/W, other than status read command is not accepted. Start $\overline{CS}$ after taking the last data (D0), and before the next SCL clock starts. At other timing, write command is not executed, and this write command is cancelled. This IC has page write function, and after input of data for 1 byte (8 bits), by continuing data input without starting $\overline{CS}$, data up to 16/32*1 bytes can be written for one tE/W. In page write, the insignificant 4/5*2 bit of the designated address is incremented internally at every time when data of 1 byte is input, and data is written to respective addresses. When data of the maximum bytes or higher is input, address rolls over, and previously input data is overwritten.

*1 BR25L010/020/040-W=16 bytes at maximum
BR25L080/160/320/640-W=32 bytes at maximum

*2 BR25L010/020/040-W=Insignificant 4 bits
BR25L080/160/320/640-W=Insignificant 5 bits

4. Status register write / read command

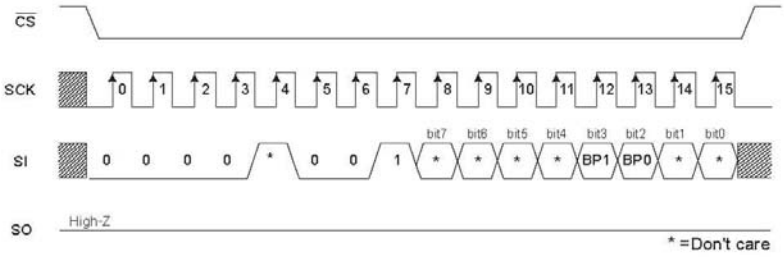



Figure 39. Status register write command (BR25L010/020/040-W)

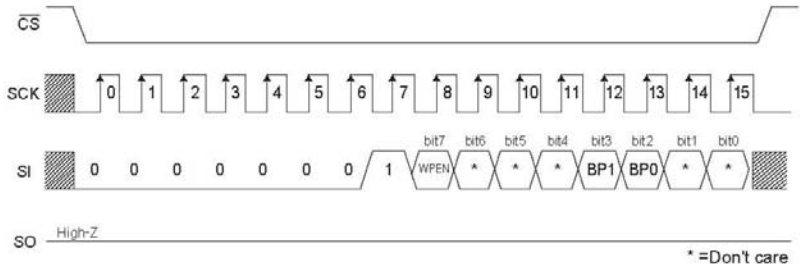



Figure 40. Status register write command (BR25L080/160/320/640-W)

Write status register command can write status register data. The data the can be written by this command are 2 bits *1, that is, BP1 (bit3) and BP0 (bit2) among 8 bits of status register. By BP1 and BP0, write disable block of EEPROM can be set. As for this command, set $\overline{CS}$ LOW, and input ope code of write status register, and input data. Then, by making $\overline{CS}$ HIGH, EEPROM starts writing. Write time requires time of tE/W as same as write. As for $\overline{CS}$ rise, start $\overline{CS}$ after taking the last data bit (bit0), and before the next SCK clock starts. At other timing, command is cancelled. Write disable block is determined by BP1 and BP0, and the block can be selected from 1/4 of memory array, 1/2, and entire memory array. (Refer to the write disable block setting table.) To the write disabled block, write cannot be made, and only read can be made.

* 3 bits including BR25L080, 160, 320, 640-W WPEN (bit7)

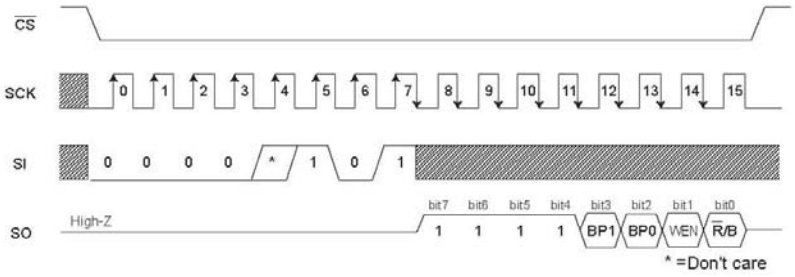



Figure 41. Status register read command (BR25L010/020/040-W)

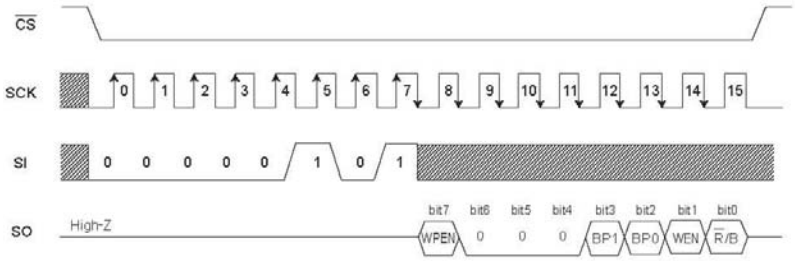



Figure 42. Status register read command (BR25L080/160/320/640-W)

**●At standby**

○ Current at standby

Set $\overline{CS}$ "H", and be sure to set SCK, SI, $\overline{WP}$, $\overline{HOLD}$ input "L" or "H". Do not input intermediate electric potential.

○ Timing

As shown in Figure 43, at standby, when SCK is "H", even if $\overline{CS}$ is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of $\overline{CS}$. At standby and at power ON/OFF, set $\overline{CS}$ "H" status.

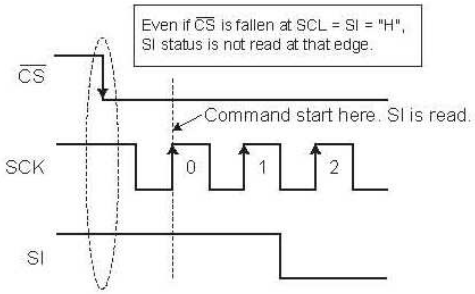



Figure 43. Operating timing

**●$\overline{WP}$ cancel valid area**

WP is normally fixed to “H” or “L” for use, but when $\overline{WP}$ is controlled so as to cancel write status register command and write command, pay attention to the following $\overline{WP}$ valid timing.

While write or write status register command is executed, by setting $\overline{WP}$ = "L" in cancel valid area, command can be cancelled. The area from command ope code before $\overline{CS}$ rise at internal automatic write start becomes the cancel valid area. However, once write is started, any input cannot be cancelled. $\overline{WP}$ input becomes Don't Care, and cancellation becomes invalid.

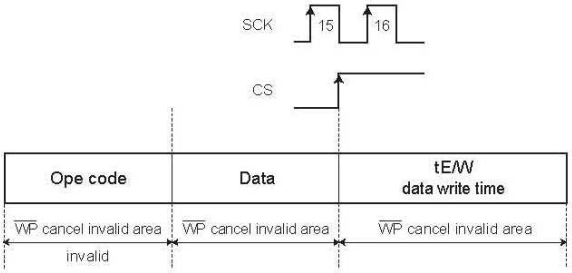



Figure 44. $\overline{WP}$ valid timing (WRSR)

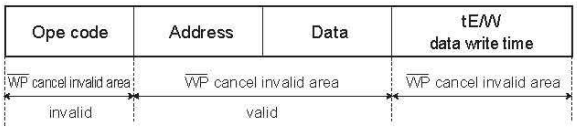



Figure 45. $\overline{WP}$ valid timing (WRITE)

**●$\overline{HOLD}$ pin**

By $\overline{HOLD}$ pin, command communication can be stopped temporarily. (HOLD status) The $\overline{HOLD}$ pin carries out command communications normally when it is HIGH. To get in HOLD status, at command communication, when SCK = LOW, set the $\overline{HOLD}$ pin LOW. At HOLD status, SCK and SI become Don't Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the $\overline{HOLD}$ pin HIGH when SCK = LOW. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at read, after release of $\overline{HOLD}$ status, by starting A4 address input, read can be restarted. When in HOLD status, leave $\overline{CS}$ LOW. When it is set $\overline{CS}$ = HIGH in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

**●Method to cancel each command**

○READ, RDSR

・Method to cancel : cancel by $\overline{CS}$ = “H”.

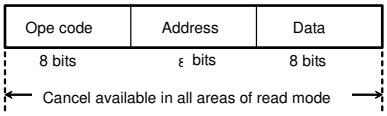



Figure 46. READ cancel valid timing

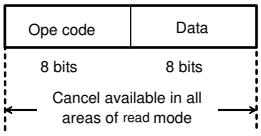



Figure 47. RDSR cancel valid timing

○WRITE、PAGE WRITE

a : Ope code, address input area.
Cancellation is available by $\overline{CS}$=”H”.

b : Data input area (D7 to D1 input area)
Cancellation is available by $\overline{CS}$=”H”.

c : Data input area (D0 area)
When $\overline{CS}$ is started, write starts.
After $\overline{CS}$ rise, cancellation cannot be made by any means.

d : tE/W area
Cancellation is available by $\overline{CS}$ = "H". However, when write starts ($\overline{CS}$ is started) in the area c, cancellation cannot be made by any means. And, by inputting on SCK clock, cancellation cannot be made. In page write mode, there is write enable area at every 8 clocks.

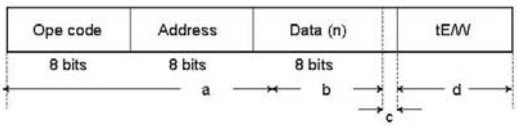
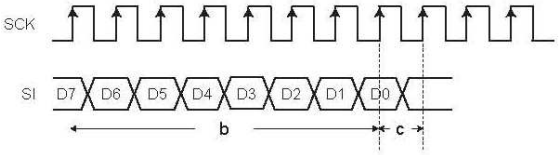



Figure 48. WRITE cancel valid timing




Note1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
Note2) If $\overline{CS}$ is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = "L" area. As for SCK rise, assure timing of tCSS / tCSH or higher.

○WRSR

a : From ope code to 15 clock rise
Cancel by $\overline{CS}$=”H”.

b : From 15 clock rise to 16 clock rise (write enable area)
When $\overline{CS}$ is started, write starts.
After $\overline{CS}$ rise, cancellation cannot be made by any means.

c : After 16 clock rise.
Cancel by $\overline{CS}$=”H”. However, when write starts ($\overline{CS}$ is started) in the area b, cancellation cannot be made by any means. And, by inputting on SCK clock, cancellation cannot be made.

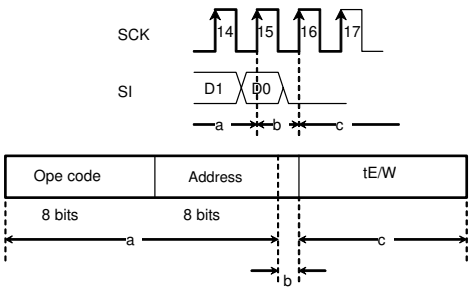



Figure 49. WRSR cancel valid timing

Note1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
Note2) If CS is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = "L" area. As for SCK rise, assure timing of tCSS/tCSH or higher.

○WREN/WRDI

a : From ope code to clock rise, cancel by $\overline{CS}$ = “H”.

b : Cancellation is not available when $\overline{CS}$ is started after 7 clock.

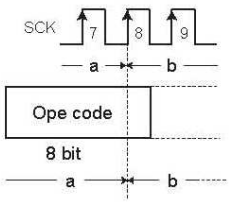



Figure 50. WREN/WRDI cancel valid timing

## ●High speed operation

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

○Input pin pull up, pull down resistance

When to attach pull up, pull down resistance to EEPROM input pin, select an appropriate value for the microcontroller VOL, IOL from VIL characteristics of this IC.

○Pull up resistance

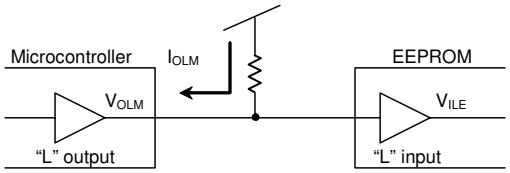



Figure 51. Pull up resistance

$$R_{PU} \geqq \frac{V_{CC}-V_{OLM}}{I_{OLM}} \quad \cdots ①$$

$$V_{OLM} \leqq V_{ILE} \quad \cdots ②$$

Example) When Vcc=5V, $V_{ILM}$=1.5V, $V_{OLM}$=0.4V, $I_{OLM}$=2mA, from the equation ①,

$$R_{PU} \geqq \frac{5-0.4}{2\times10^{-3}}$$

$$\therefore R_{PU} \geqq 2.3[k\Omega]$$

With the value of Rpu to satisfy the above equation, $V_{OLM}$ becomes 0.4V or higher, and with $V_{ILE}$ (=1.5V), the equation ② is also satisfied.

- $V_{ILM}$ :EEPROM $V_{IH}$ specifications
- $V_{OLM}$ :Microcontroller $V_{OL}$ specifications
- $I_{OLM}$ :Microcontroller $I_{OL}$ specifications

And, in order to prevent malfunction, mistake write at power ON/OFF, be sure to make $\overline{CS}$ pull up.

○Pull down resistance

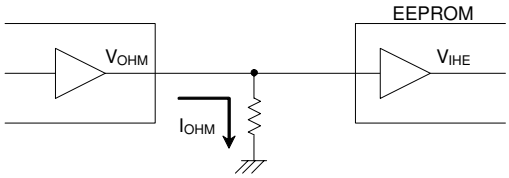



Figure 52. Pull down resistance

$$R_{PD} \geqq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ③$$

$$V_{OHM} \geqq V_{IHE} \quad \cdots ④$$

Example) When $V_{CC}$=5V, $V_{OHM}$=$V_{CC}$-0.5V, $I_{OHM}$=0.4mA, $V_{IHM}$=$V_{CC}$×0.7V, from the equation③,

$$R_{PD} \geqq \frac{5-0.5}{0.4\times10^{-3}}$$

$$\therefore R_{PD} \geqq 11.3[k\Omega]$$

Further, by amplitude VIHE, VILE of signal input to EEPROM, operation speed changes. By inputting signal of amplitude of VCC / GND level to input, more stable high speed operations can be realized. On the contrary, when amplitude of 0.8VCC / 0.2VCC is input, operation speed becomes slow.

In order to realize more stable high speed operation, it is recommended to make the values of RPU, RPD as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of VCC / GND level.
(*1 At this moment, operating timing guaranteed value is guaranteed.)

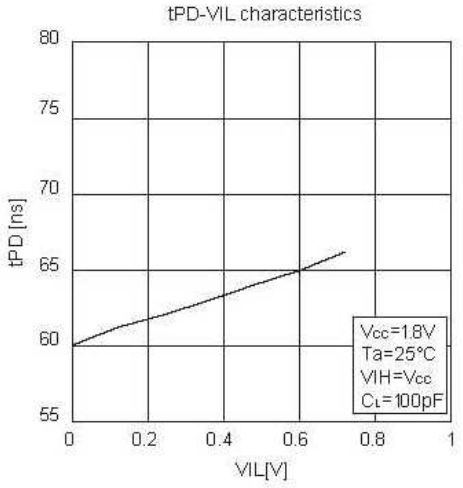



Figure 53. VIL dependency of data output delay time

○SO load capacity condition

Load capacity of SO output pin affects upon delay characteristic of SO output. (Data output delay time, time from $\overline{\text{HOLD}}$ to High-Z) In order to make output delay characteristic into higher speed, make SO load capacity small. In concrete, "Do not connect many devices to SO bus", "Make the wire between the controller and EEPROM short", and so forth.

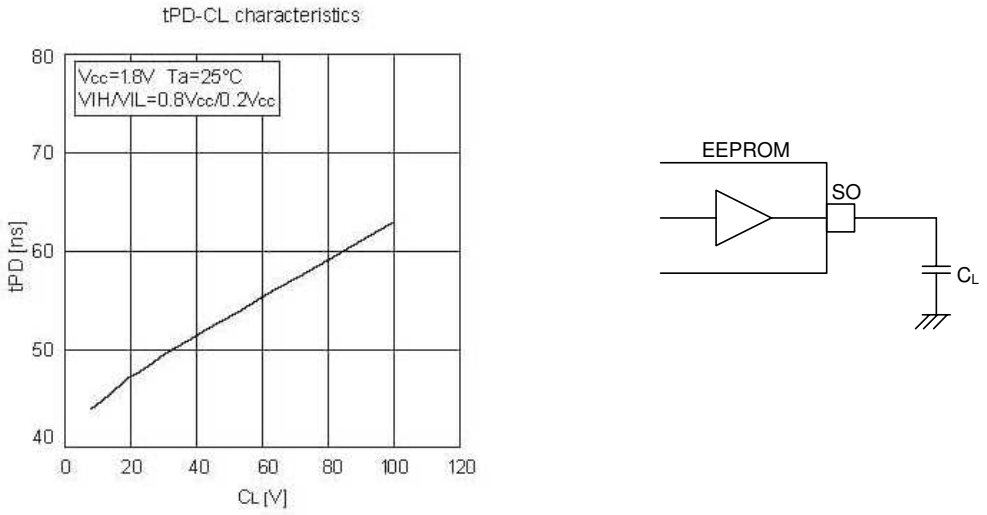



Figure 54. SO load dependency of data output delay time

○Other cautions

Make the wire length from the microcontroller to EEPROM input signal same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.

## ●Equivalent circuit

○Output circuit

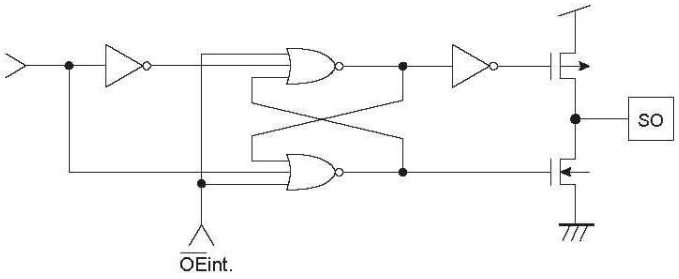



Figure 55. SO output equivalent circuit

○Input circuit

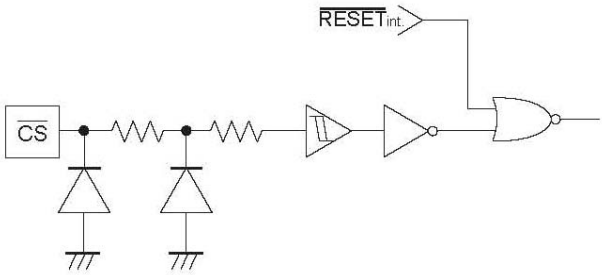



Figure 56. $\overline{CS}$ input equivalent circuit

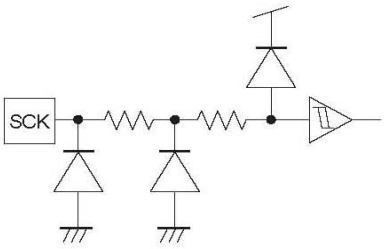



Figure 57. SCK input equivalent circuit

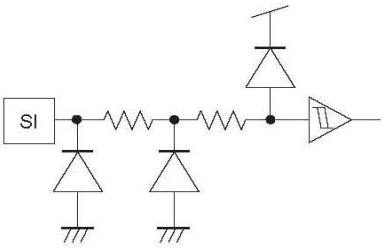



Figure 58. SI input equivalent circuit

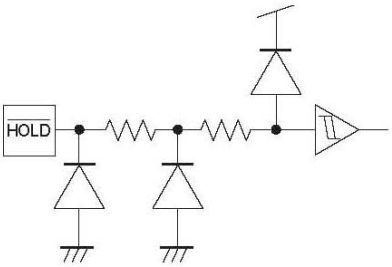



Figure 59. $\overline{HOLD}$ input equivalent circuit

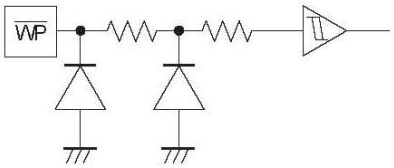



Figure 60. $\overline{WP}$ input equivalent circuit

## ●Notes on power ON/OFF

○At power ON/OFF, set $\overline{CS}$ "H" (= Vcc).

When $\overline{CS}$ is "L", this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set $\overline{CS}$ "H". (When $\overline{CS}$ is in "H" status, all inputs are canceled.)

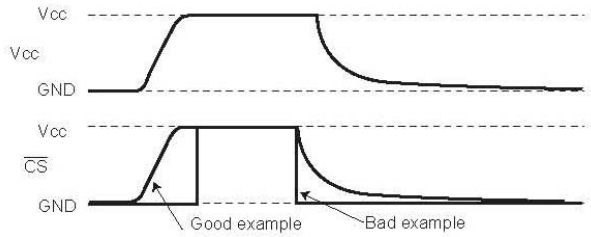



Figure 61. $\overline{CS}$ timing at power ON/OFF

(Good example) $\overline{CS}$ terminal is pulled up to Vcc.
At power OFF, take 10ms or higher before re supply. If power is turned on without observing this condition, the IC internal circuit may not be reset, which please note.

(Bad example) CS terminal is "L" at power ON/OFF.
In this case, CS always becomes "L" (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes.
Even when $\overline{CS}$ input is High-Z, the status becomes like this case, which please note.

○POR circuit

This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following tR, tOFF, and Vbot are not satisfied, it may become write enable status owing to noises and the likes.

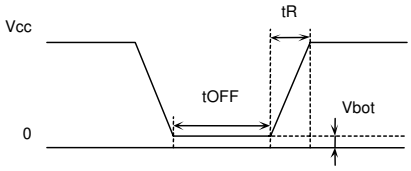



Figure 62. Rise waveform

Recommended conditions of $t_R$, $t_{OFF}$, Vbot

| tR | tOFF | Vbot |
|---|---|---|
| 10ms or below | 10ms or higher | 0.3V or below |
| 100ms or below | 10ms or higher | 0.2V or below |

## ●Noise countermeasures

○Vcc noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible.
And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

○SCK noise

When the rise time (tR) of SCK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement.
To avoid this, a Schmitt trigger circuit is built in SCK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SCK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time (tR) of SCK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

○$\overline{WP}$ noise

During execution of write status register command, if there exist noises on $\overline{WP}$ pin, mistake in recognition may occur and forcible cancellation may result, which please note. To avoid this, a Schmitt trigger circuit is built in $\overline{WP}$ input. In the same manner, a Schmitt trigger circuit is built in SI input and HOLD input too.

## ●Cautions on use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and operating temperature range and so forth are exceeded, LSI may be destructed.
Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5) Heat design
In consideration of permissible dissipation in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal short circuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of short circuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

## ●Ordering Information

**Product Code Description**

B R 2 5 L x x x x x x - W x x

**BUS type**
25 : SPI

**Operating temperature**
-40℃ to+85℃

**Capacity**

010=1K 080=8K 640=64K
020=2K 160=16K
040=4K 320=32K

**Package**

Blank : DIP-T8
F : SOP8
FJ : SOP-J8
FV : SSOP-B8
FVT : TSSOP-B8
FVJ : TSSOP-B8J
FVM : MSOP8

**Double Cell**

**Package specifications**

E2 : reel shape emboss taping (SOP8,SOP-J8,SSOP-B8,TSSOP-B8,TSSOP-B8J)
TR : reel shape emboss taping (MSOP8)
None : Tube (DIP-T8)

## ●Lineup

| Capacity | Package | |
|---|---|---|
| | Type | Quantity |
| 1K | SOP8 | Reel of 2500 |
| | SOP-J8 | |
| | SSOP-B8 | |
| | TSSOP-B8J | |
| | TSSOP-B8 | Reel of 3000 |
| | MSOP8 | |
| 2K | SOP8 | Reel of 2500 |
| | SOP-J8 | |
| | SSOP-B8 | |
| | TSSOP-B8J | |
| | TSSOP-B8 | Reel of 3000 |
| | MSOP8 | |
| 4K | DIP-T8 | Tube of 2000 |
| | SOP8 | Reel of 2500 |
| | SOP-J8 | |
| | SSOP-B8 | |
| | TSSOP-B8J | |
| | TSSOP-B8 | Reel of 3000 |
| | MSOP8 | |

| Capacity | Package | |
|---|---|---|
| | Type | Quantity |
| 8K | DIP-T8 | Tube of 2000 |
| | SOP8 | Reel of 2500 |
| | SOP-J8 | |
| | SSOP-B8 | |
| | TSSOP-B8 | Reel of 3000 |
| 16K | DIP-T8 | Tube of 2000 |
| | SOP8 | Reel of 2500 |
| | SOP-J8 | |
| | SSOP-B8 | |
| | TSSOP-B8 | Reel of 3000 |
| 32K | DIP-T8 | Tube of 2000 |
| | SOP8 | Reel of 2500 |
| | SOP-J8 | |
| 64K | DIP-T8 | Tube of 2000 |
| | SOP8 | Reel of 2500 |
| | SOP-J8 | |