Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Serial EEPROM Series Standard EEPROM

Plug & Play EEPROM

BR34E02-3

General Description

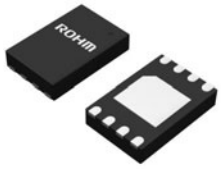
BR34E02-3 is 256×8 bit Electrically Erasable PROM (Based on Serial Presence Detect)

Features

- 256×8 bit Architecture Serial EEPROM
- Wide Operating Voltage Range: 1.7V to 5.5V
- Two-Wire Serial Interface
- Self-Timed Erase and Write Cycle
- Page Write Function (16byte)
- Write Protect Mode
  - Settable Reversible Write Protect Function : 00h-7Fh
  - Write Protect 1 (Onetime Rom) : 00h-7Fh
  - Write Protect 2 (Hardwire WP PIN) : 00h-FFh
- Low Power consumption
  - Write (at 1.7V) : 0.4mA (typ)
  - Read (at 1.7V) : 0.1mA (typ)
  - Standby (at 1.7V) : 0.1μA (typ)
- Prevention of Write Mistake
  - Write Protect Feature (WP pin)
  - Prevention of Write Mistake at Low Voltage
- High Reliability Fine Pattern CMOS Technology
- More than 1 million write cycles
- More than 40 years data retention
- Noise Reduction Filtered Inputs in SCL / SDA
- Initial delivery state FFh

Packages W(Typ) x D(Typ) x H(Max)

TSSOP-B8
3.00mm x 6.40mm x 1.20mm



VSON008X2030
2.00mm x 3.00mm x 0.60mm

BR34E02-3

Capacity	Bit Format	Type	Power Source Voltage	Package
2Kbit	256x8	BR34E02FVT-3	1.7V to 5.5V	TSSOP-B8
		BR34E02NUX-3		VSON008X2030

Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	V_{CC}	-0.3 to +6.5	V	
Power Dissipation	Pd	330 (TSSOP-B8)	mW	Derate by 3.3mW/°C when operating above Ta=25°C
		300 (VSON008X2030)		Derate by 3.0mW/°C when operating above Ta=25°C
Storage Temperature	Tstg	-65 to +125	℃	
Operating Temperature	Topr	-40 to +85	℃	
Input Voltage / Output Voltage (A0)	-	-0.3 to 10.0	V	
Input Voltage / Output Voltage (others)	-	-0.3 to V_{CC}+1.0	V	
Electrostatic discharge voltage (human body model)	V_{ESD}	-4000 to +4000	V	

Memory Cell Characteristics (Ta=25℃, V_{CC}=1.7V to 5.5V)

Parameter	Limit			Unit
	Min	Typ	Max	
Write / Erase Cycle (1)	1,000,000	-	-	Times
Data Retention(1)	40	-	-	Years

(1) Not 100% TESTED

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Recommended Operating Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	1.7 to 5.5	V
Input Voltage	V_{IN}	0 to V_{CC}	V

DC Characteristics (Unless otherwise specified Ta=-40℃ to +85℃, V_{CC} =1.7V to 5.5V)

Parameter	Symbol	Limit			Unit	Test Conditions
		Min	Typ	Max		
Input High Voltage	V_{IH}	0.7 Vcc	-	Vcc+1.0	V	
Input Low Voltage	V_{IL}	-0.3	-	0.3 Vcc	V	
Output Low Voltage 1	V_{OL1}	-	-	0.4	V	I_{OL}=2.1mA, 2.5V≦V_{CC}≦5.5V(SDA)
Output Low Voltage 2	V_{OL2}	-	-	0.2	V	I_{OL}=0.7mA, 1.7V≦V_{CC}＜2.5V(SDA)
Input Leakage Current 1	I_{LI1}	-1	-	1	μA	V_{IN}=0V to V_{CC} (A0, A1, A2, SCL)
Input Leakage Current 2	I_{LI2}	-1	-	15	μA	V_{IN}=0V to V_{CC} (WP)
Input Leakage Current 3	I_{LI3}	-1	-	20	μA	V_{IN}=V_{HV}(A0)
Output Leakage Current	I_{LO}	-1	-	1	μA	V_{OUT}=0V to V_{CC}
Supply Current (Write)	I_{CC1}	-	-	2.0	mA	V_{CC} =5.5V, f_{SCL}=400kHz, t_{WR}=5ms Byte Write Page Write Write Protect
Supply Current (Read)	I_{CC2}	-	-	0.5	mA	V_{CC} =5.5V, f_{SCL}=400kHz Random Read Current Read Sequential Read
Standby Current	I_{SB}	-	-	2.0	μA	V_{CC} =5.5V, SDA, SCL= V_{CC} A0, A1, A2=GND, WP=GND
A0 HV Voltage	V_{HV}	7	-	10	V	V_{HV}-V_{CC}≧4.8V

AC Characteristics (Unless otherwise specified Ta=-40℃ to +85℃, V_{CC} =1.7V to 5.5V)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Clock Frequency	f_{SCL}	-	-	400	kHz
Data Clock High Period	t_{HIGH}	0.6	-	-	μs
Data Clock Low Period	t_{LOW}	1.2	-	-	μs
SDA and SCL Rise Time(1)	t_R	-	-	0.3	μs
SDA and SCL Fall Time(1)	t_F	-	-	0.3	μs
Start Condition Hold Time	$t_{HD:STA}$	0.6	-	-	μs
Start Condition Setup Time	$t_{SU:STA}$	0.6	-	-	μs
Input Data Hold Time	$t_{HD:DAT}$	0	-	-	ns
Input Data Setup Time	$t_{SU:DAT}$	100	-	-	ns
Output Data Delay Time	t_{PD}	0.1	-	0.9	μs
Output Data Hold Time	t_{DH}	0.1	-	-	μs
Stop Condition Setup Time	$t_{SU:STO}$	0.6	-	-	μs
Bus Free Time	t_{BUF}	1.2	-	-	μs
Write Cycle Time	t_{WR}	-	-	5	ms
Noise Spike Width (SDA and SCL)	t_I	-	-	0.1	μs
WP Hold Time	$t_{HD:WP}$	0	-	-	μs
WP Setup Time	$t_{SU:WP}$	0.1	-	-	μs
WP High Period	$t_{HIGH:WP}$	1.0	-	-	μs

(1) Not 100% TESTED

Serial Input / Output Timing

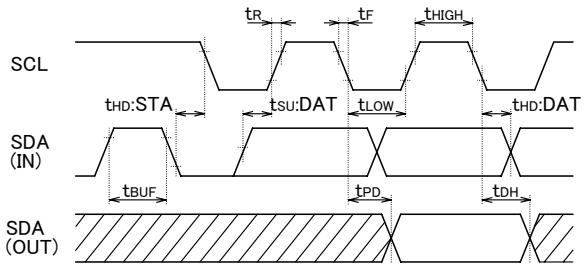


Figure 1-(a). Serial Input / Output Timing

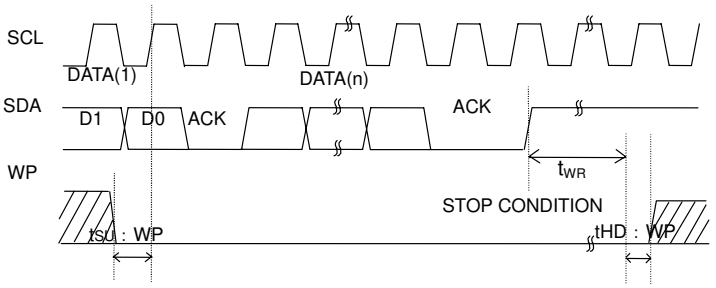


Figure 1-(d). WP Timing of the Write Operation

○SDA data is latched into the chip at the rising edge of SCL clock.
○Output data toggles at the falling edge of SCL clock.

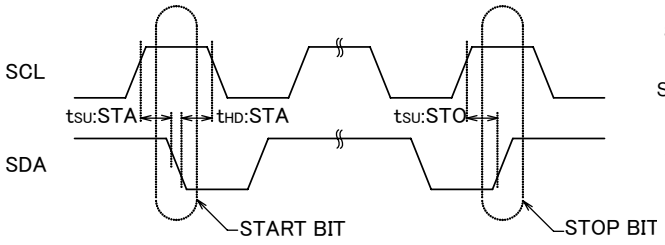


Figure 1-(b). Start/Stop Bit Timing

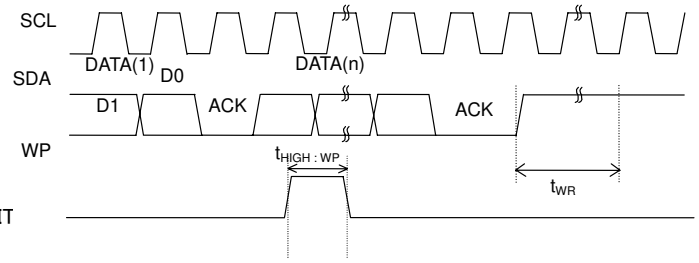


Figure 1-(e). WP Timing of the Write Cancel Operation

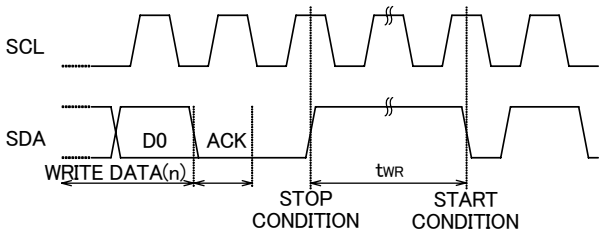
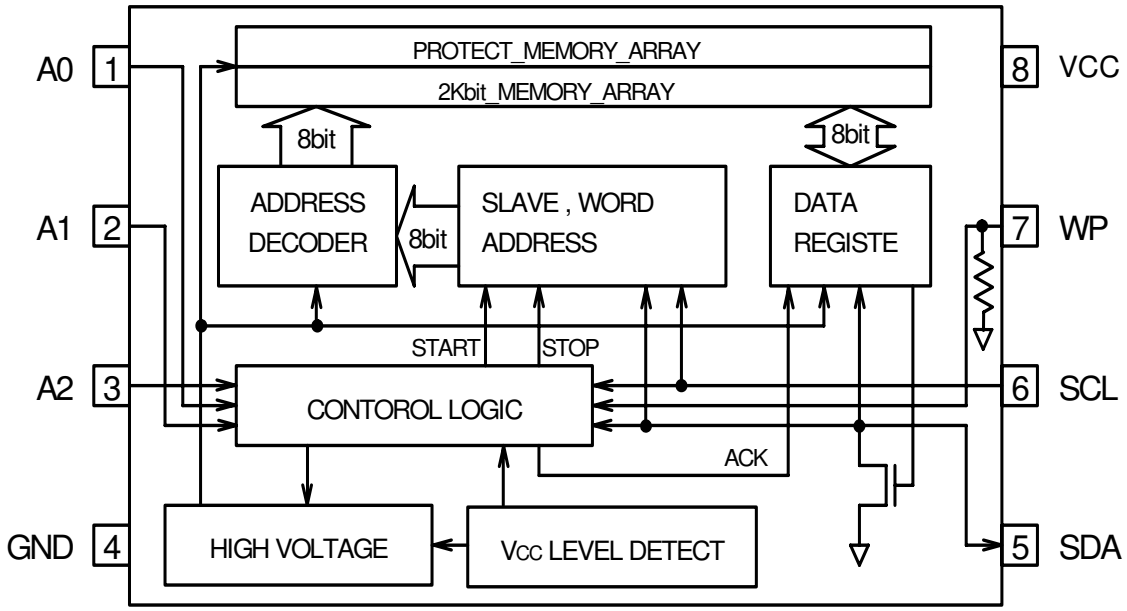


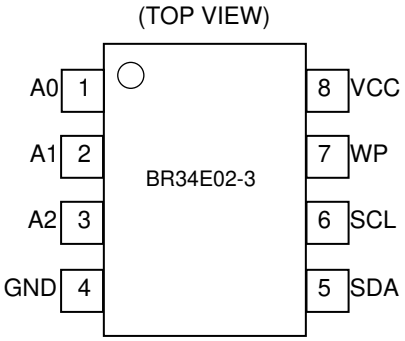
Figure 1-(c). Write Cycle Timing

○For WRITE operation, WP must be "Low" from the rising edge of the clock (which takes in D0 of first byte) until the end of t_{WR}. (See Figure 1-(d)) During this period, WRITE operation can be canceled by setting WP "High".（See Figure 1-(e)）
○When WP is set to "High" during t_{WR}, WRITE operation is immediately ceased, making the data unreliable. It must then be re-written.

Block Diagram



Pin Configuration



Pin Descriptions

Pin Name	Input/Output	Descriptions
VCC	-	Power supply
GND	-	Ground 0V
A0, A1, A2	IN	Slave address set(1)
SCL	IN	Serial clock input
SDA	IN / OUT	Slave and word address(2) Serial data input, serial data output
WP	IN	Write protect input(3)

(1) A0, A1 and A2 are not allowed to use as open.
(2) Open drain output requires a pull-up resistor.
(3) WP Pin has a Pull-Down resistor. Please leave unconnected or connect to GND when not in use.

Typical Performance Curves

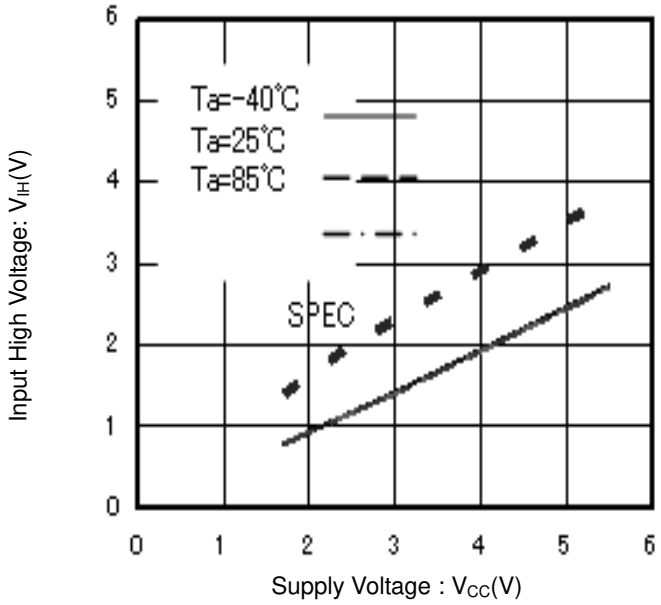


Figure 2. Input High Voltage vs Supply Voltage
(A0, A1, A2, SCL, SDA, WP)

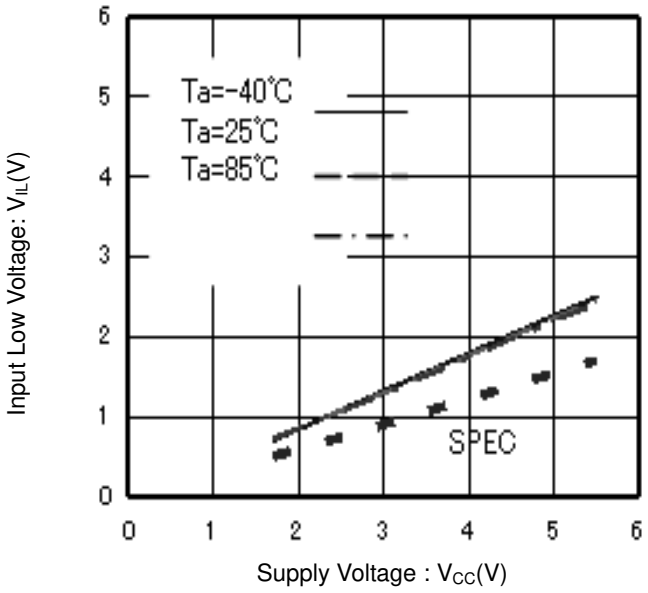


Figure 3. Input Low Voltage vs Supply Voltage
(A0, A1, A2, SCL, SDA, WP)

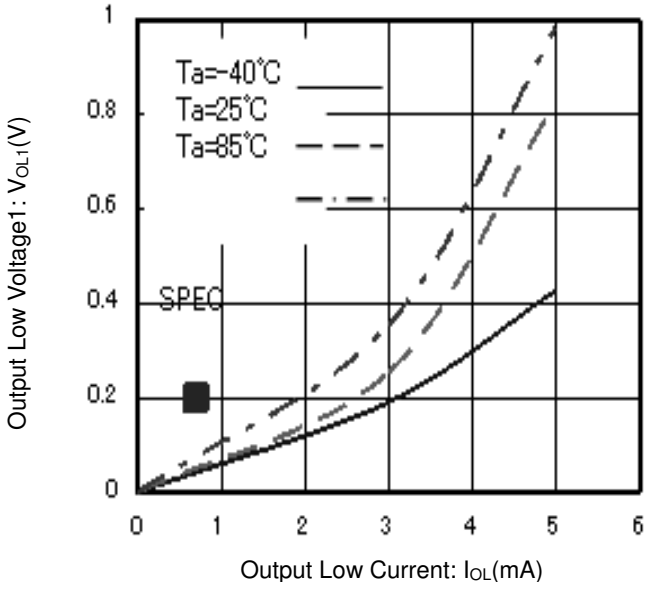


Figure 4. Output Low Voltage1 vs Output Low Current
(Vcc=2.5V)

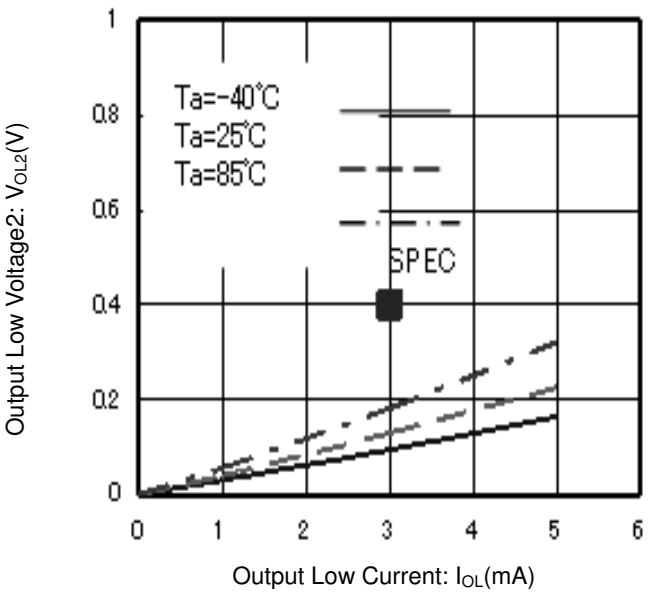


Figure 5. Output Low Voltage2 vs Output Low Current
(Vcc=1.7V)

Typical Performance Curves - Continued

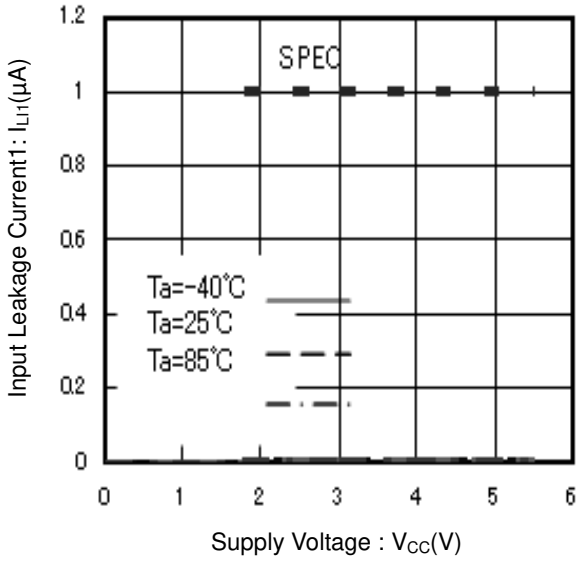


Figure 6. Input Leakage Current1 vs Supply Voltage (A0, A1, A2, SCL)

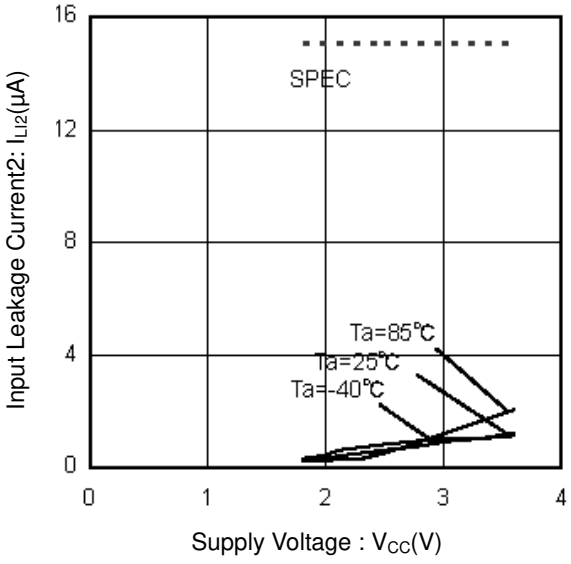


Figure 7. Input Leakage Current2 vs Supply Voltage (WP)

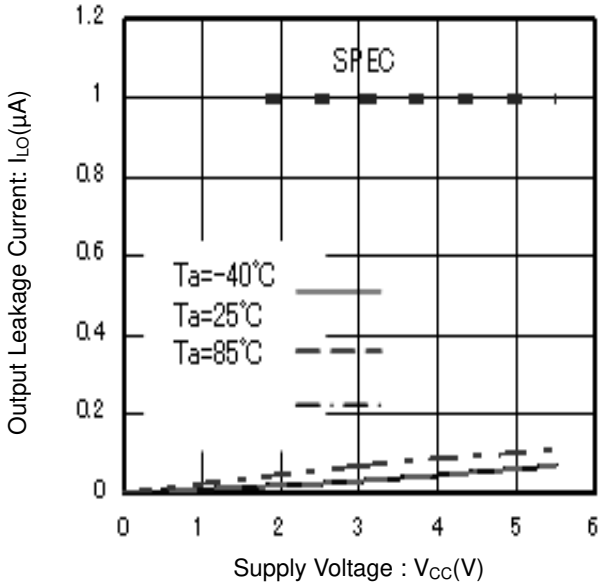


Figure 8. Output Leakage Current vs Supply Voltage (SDA)

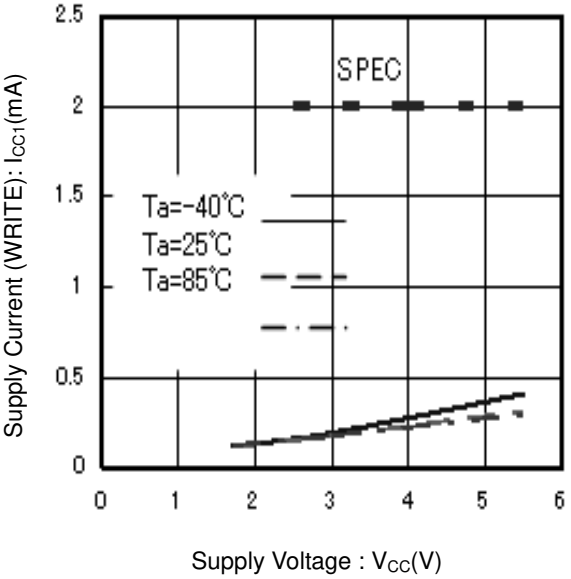


Figure 9. Supply Current (WRITE) vs Supply Voltage (f_{SCL}=400kHz)

Typical Performance Curves - Continued

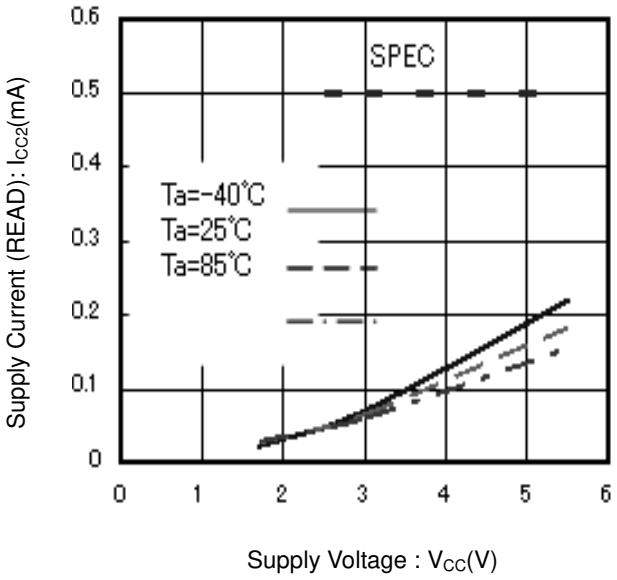


Figure 10. Supply Current (READ) vs Supply Voltage (f_{SCL}=400kHz)

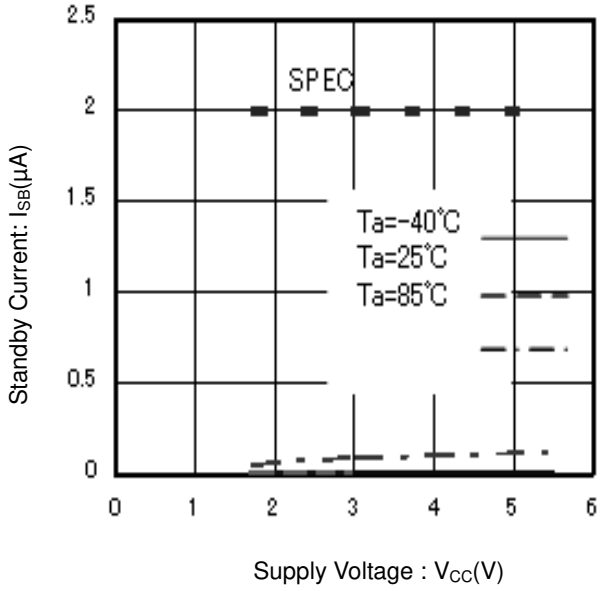


Figure 11. Standby Current vs Supply Voltage

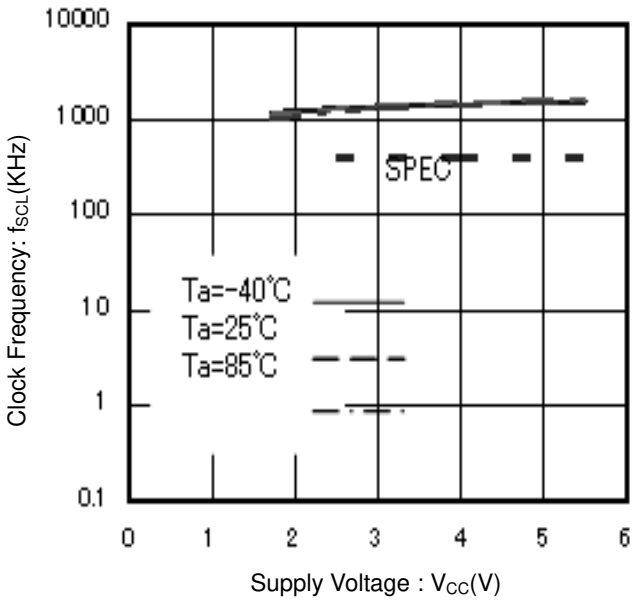


Figure 12. Clock Frequency vs Supply Voltage

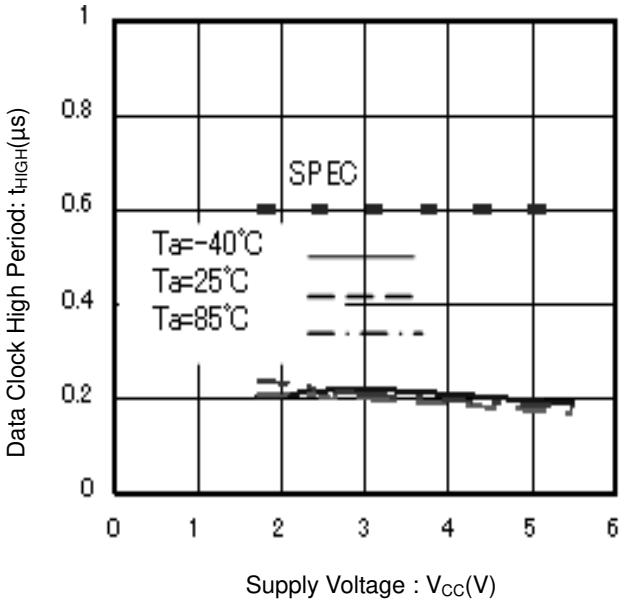


Figure 13. Data Clock High Period vs Supply Voltage

Typical Performance Curves - Continued

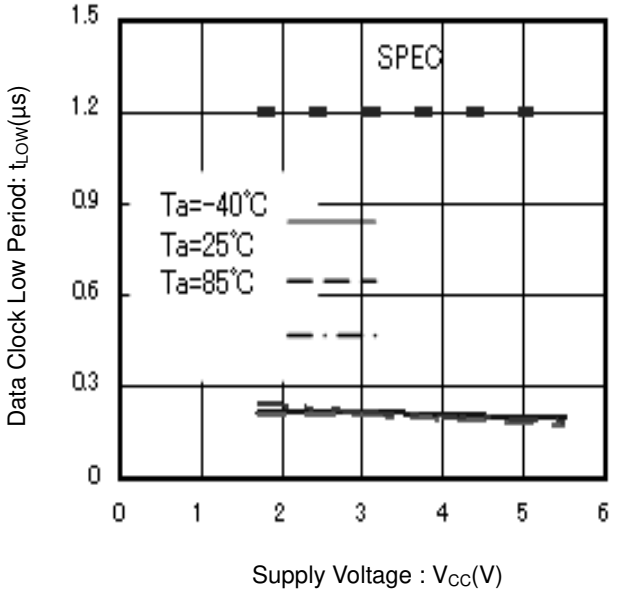


Figure 14. Data Clock Low Period vs Supply Voltage

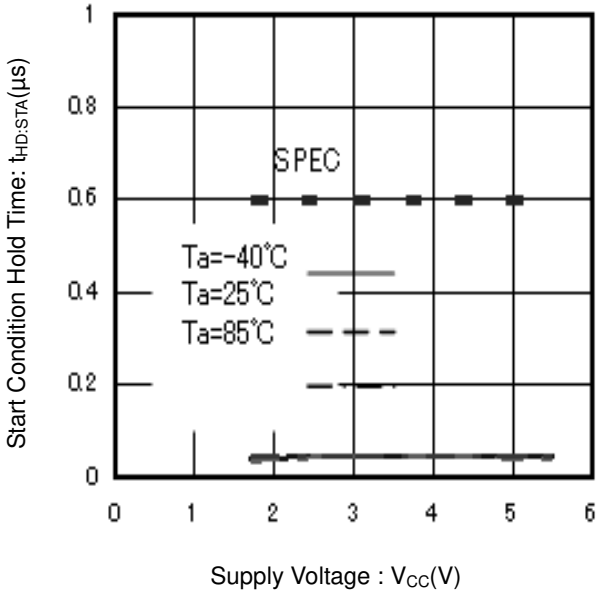


Figure 15. Start Condition Hold Time vs Supply Voltage

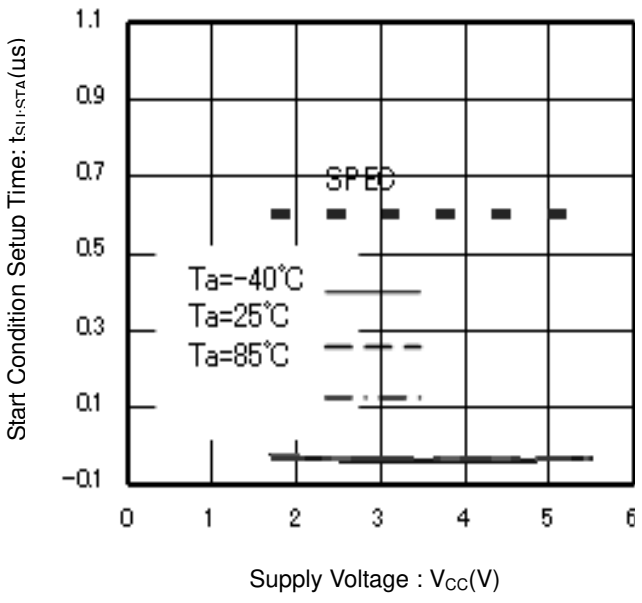


Figure 16. Start Condition Setup Time vs Supply Voltage

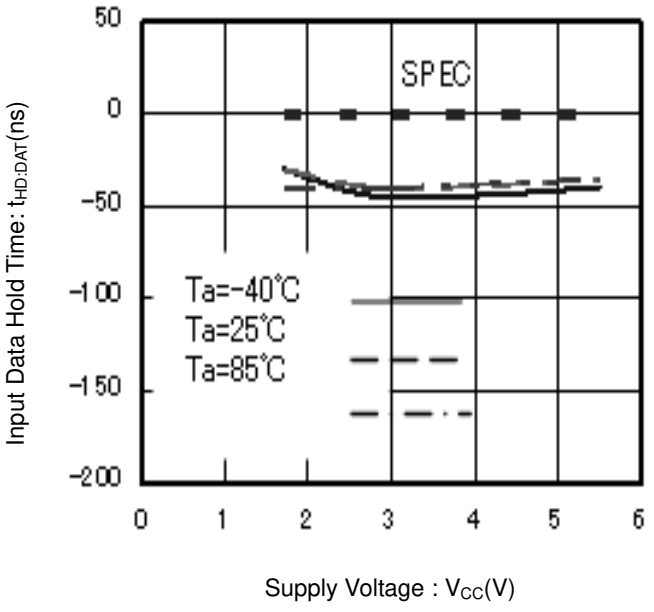


Figure 17. Input Data Hold Time vs Supply Voltage (HIGH)

Typical Performance Curves - Continued

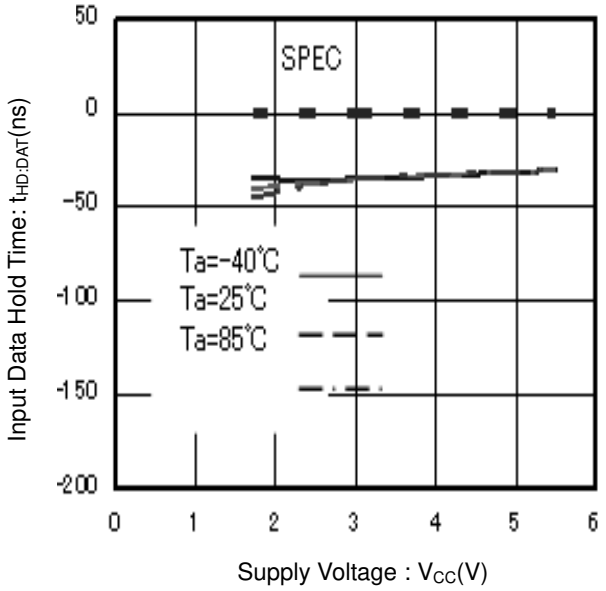


Figure 18. Input Data Hold Time vs Supply Voltage (LOW)

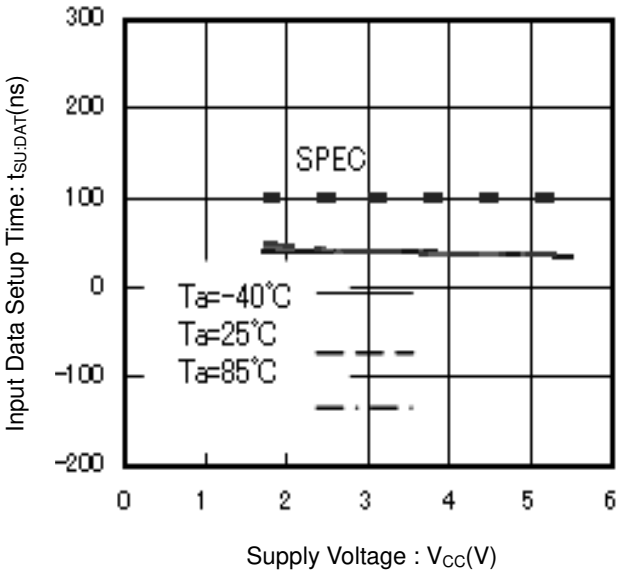


Figure 19. Input Data Setup Time vs Supply Voltage (HIGH)

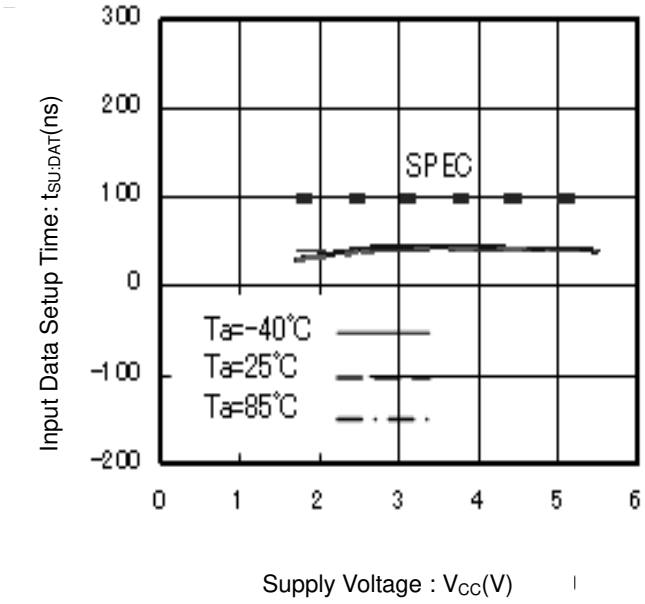


Figure 20. Input Data Setup Time vs Supply Voltage (LOW)

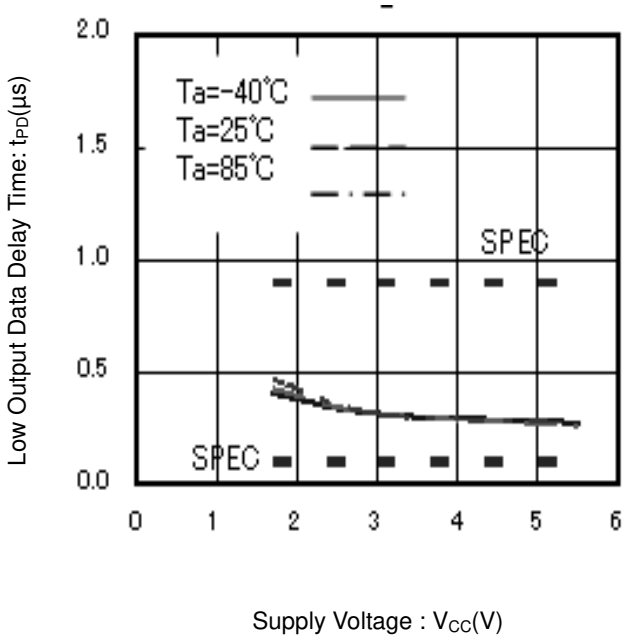


Figure 21. Low Output Data Delay Time vs Supply Voltage

Typical Performance Curves - Continued

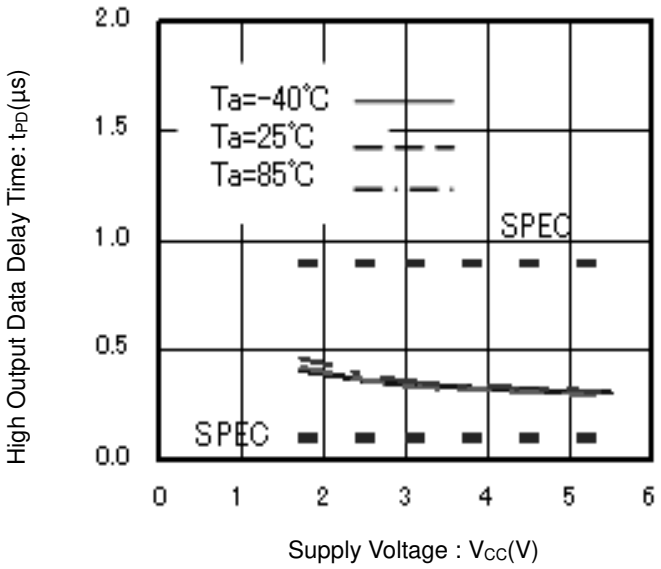


Figure 22. High Output Data Delay Time vs Supply Voltage

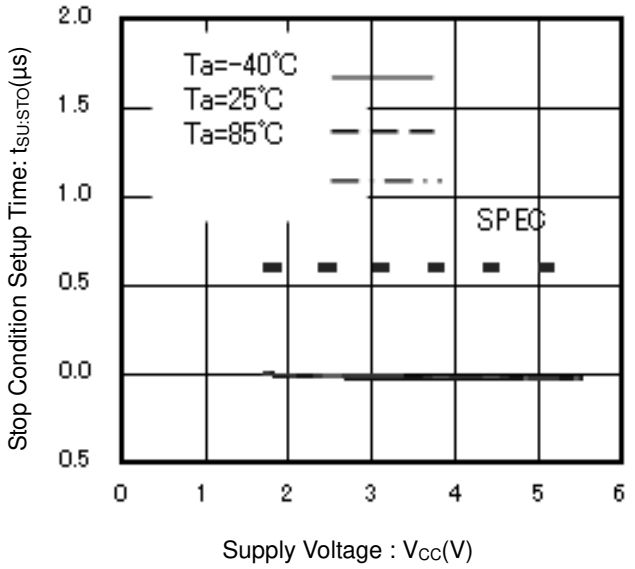


Figure 23. Stop Condition Setup Time vs Supply Voltage

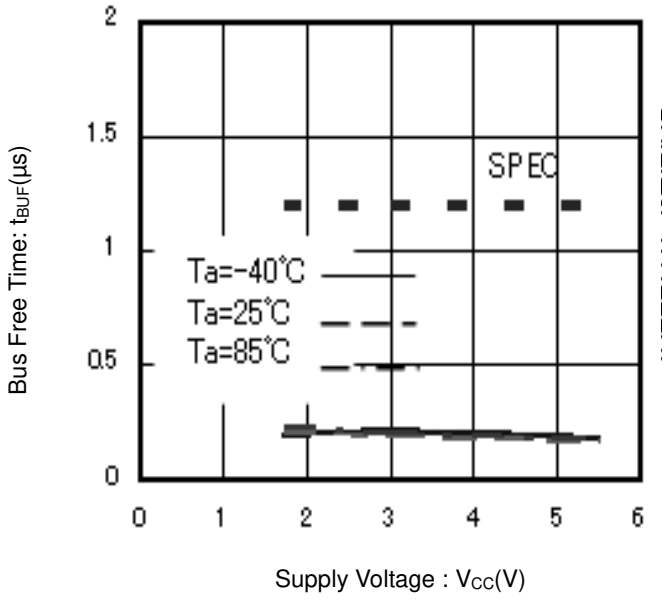


Figure 24. Bus Free Time vs Supply Voltage

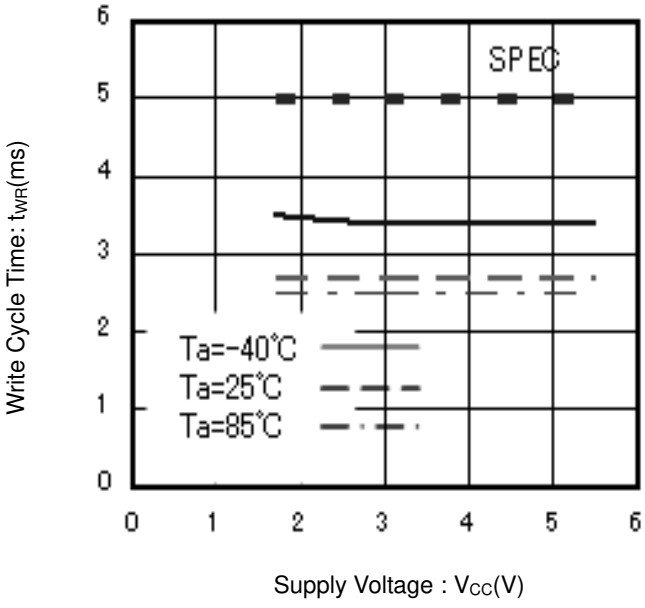


Figure 25. Write Cycle Time vs Supply Voltage

Typical Performance Curves - Continued

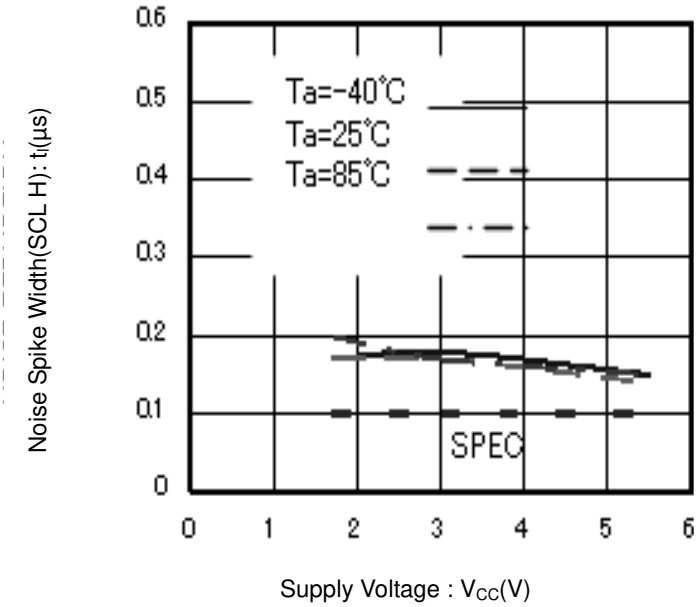


Figure 26. Noise Spike Width vs Supply Voltage (SCL H)

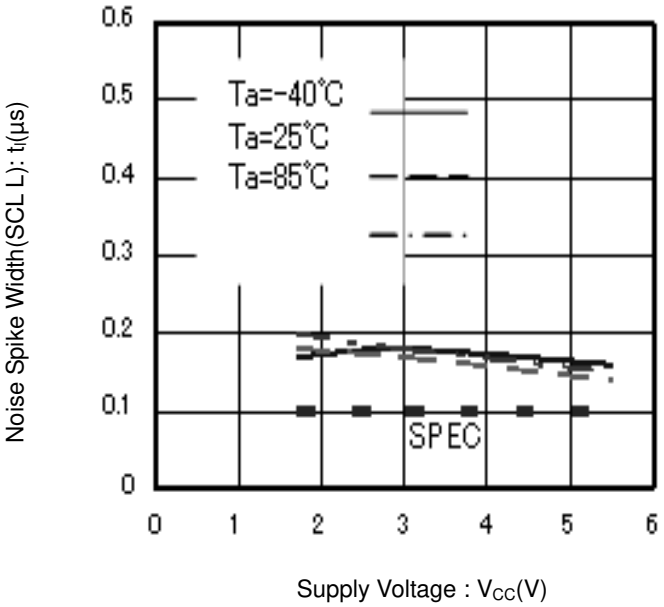


Figure 27. Noise Spike Width vs Supply Voltage (SCL L)

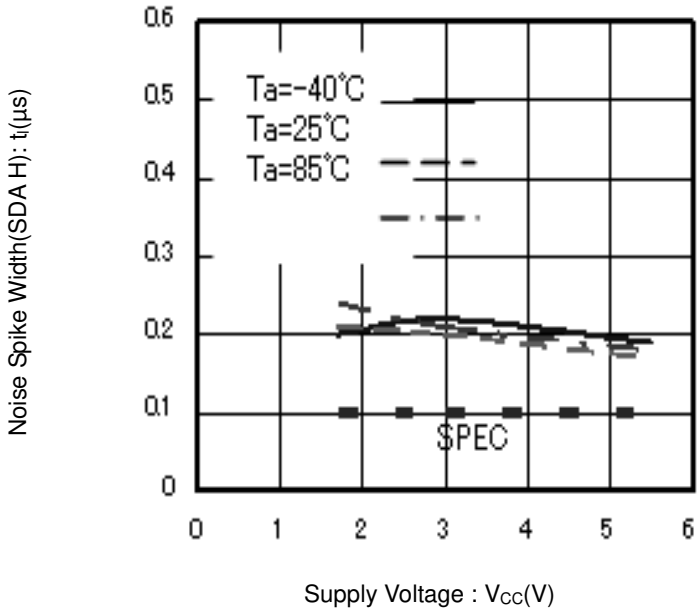


Figure 28. Noise Spike Width vs Supply Voltage (SDA H)

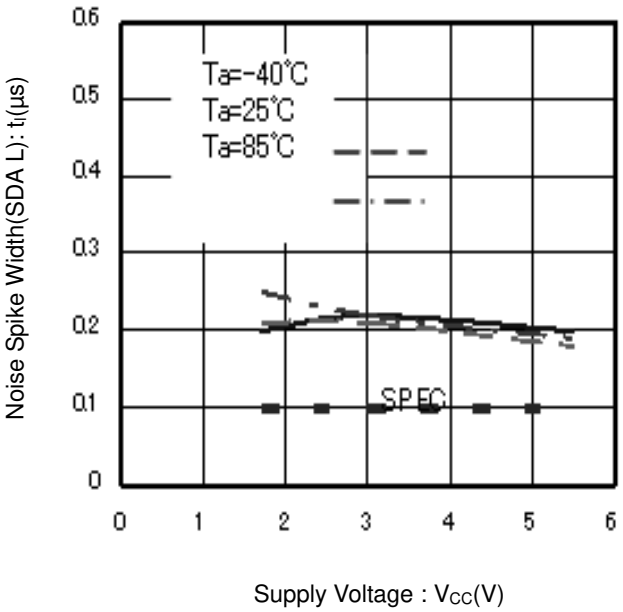


Figure 29. Noise Spike Width vs Supply Voltage (SDA L)

Typical Performance Curves - Continued

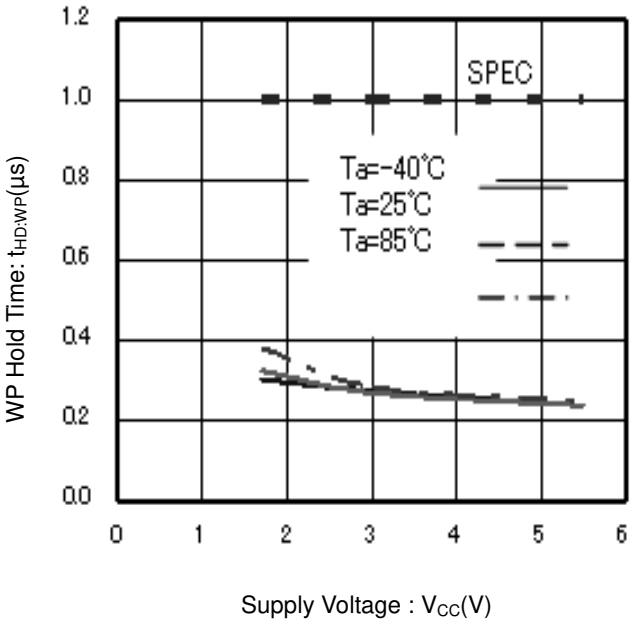


Figure 30. WP Hold Time vs Supply Voltage

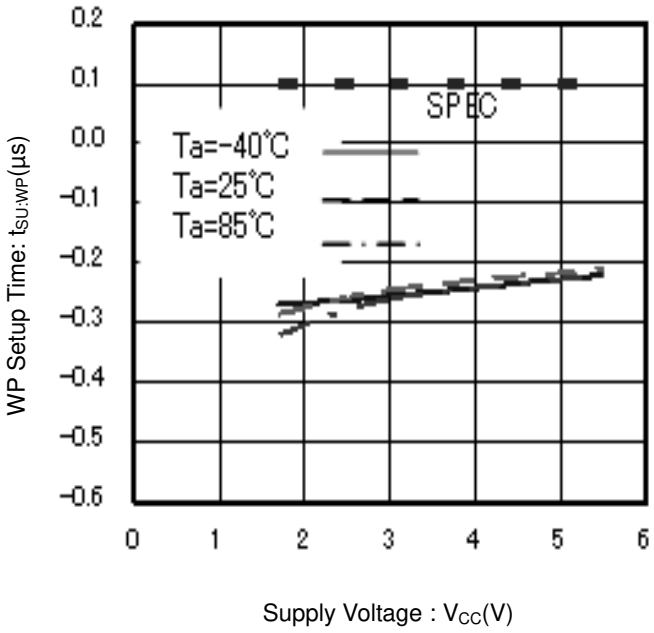


Figure 31. WP Setup Time vs Supply Voltage

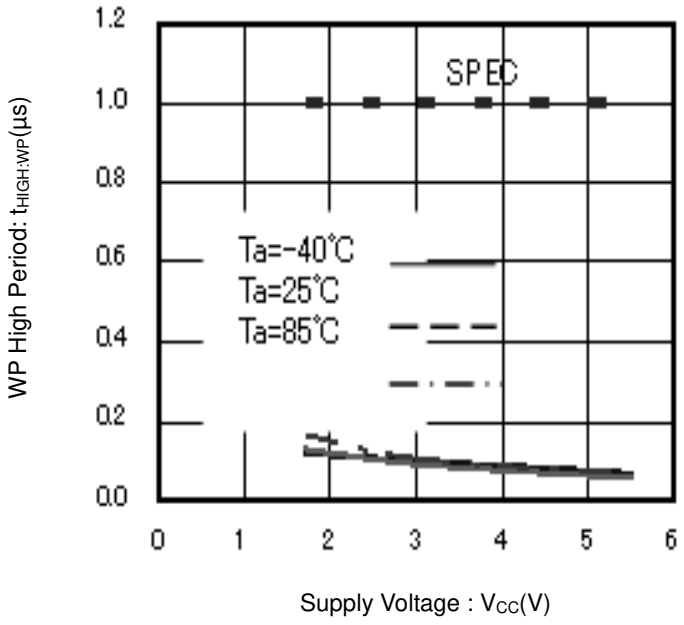


Figure 32. WP High Period vs Supply Voltage

Timing Chart

1. I²C BUS Data Communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS data communication with several devices is possible by connecting with 2 communication lines: serial data (SDA) and serial clock (SCL).

Among the devices, there should be a “master” that generates clock and control communication start and end. The rest become “slave” which are controlled by an address peculiar to each device, like this EEPROM. The device that outputs data to the bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

2. START Condition (START bit Recognition)

(1) Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is ‘HIGH' is necessary.
(2) This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command cannot be executed.

3. STOP Condition (STOP bit Recognition)

(1) Each command can be ended by a stop condition (stop bit) where SDA goes from 'LOW' to 'HIGH' while SCL is 'HIGH'. (See Figure 1-(b) START/STOP Bit Timing)

4. Write Protect By Soft Ware

(1) Set Write Protect command and permanent set Write Protect command set data of 00h to 7Fh in 256 words write protection block. Clear Write Protect command can cancel write protection block which is set by set write Protect command. Cancel of write protection block which is set by permanent set Write Protect command at once is impossibility. When these commands are carried out, WP pin must be OPEN or GND.

5. Acknowledge

(1) Acknowledge is a software used to indicate successful data transfers. The Transmitter device will release the BUS after transmitting eight bits. When inputting the slave address during write or read operation, the Transmitter is the µ-COM. When outputting the data during read operation, the Transmitter is the EEPROM.
(2) During the ninth clock cycle the Receiver will pull the SDA line Low to verify that the eight bits of data have been received. (When inputting the slave address during write or read operation, EEPROM is the receiver. When outputting the data during read operation the receiver is the µ-COM.)
(3) The device will respond with an Acknowledge after recognition of a START condition and its slave address (8bit).
(4) In WRITE mode, the device will respond with an Acknowledge after the receipt of each subsequent 8-bit word (word address and write data).
(5) In READ mode, the device will transmit eight bits of data, release the SDA line, and monitor the line for an Acknowledge.
(6) If an Acknowledge is detected and no STOP condition is generated by the Master, the device will continue to transmit the data. If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to standby mode.

6. Device Addressing

Following a START condition, the Master outputs the Slave address to be accessed. The most significant four bits of the slave address are the “device type indentifier.” For this EEPROM it is “1010.” (For WP register access this code is "0110".) The next three bits identify the specified device on the BUS (device address). The device address is defined by the state of the A0,A1 and A2 input pins. This IC works only when the device address input from the SDA pin corresponds to the status of the A0,A1 and A2 input pins. Using this address scheme allows up to eight devices to be connected to the BUS. The last bit of the stream (R/$\overline{W}$···READ/$\overline{WRITE}$) determines the operation to be performed.

R/$\overline{W}$=0 ···· WRITE (including word address input of Random Read)
R/$\overline{W}$=1 ···· READ

Slave Address Set Pin			Device Type	Device Address			Read Write Mode	Access Area
A2	A1	A0	1010	A2	A1	A0	R / $\overline{W}$	2kbit Access to Memory
A2	A1	A0	0110	A2	A1	A0	R / $\overline{W}$	Access to Permanent Set Write Protect Memory
GND	GND	VHV		0	0	1	R / $\overline{W}$	Access to Set Write Protect Memroy
GND	VCC	VHV		0	1	1	R / $\overline{W}$	Access to Clear Write Protect Memory

7. Write Protect Pin (WP)

When WP pin set to Vcc (H level), write protect is set for 256 words (all address). When WP pin set to GND (L level), it is enable to write 256 words (all address).
If permanent protection is done by Write Protect command, lower half area (00 to 7Fh address) is inhibited writing regardless of WP pin state.
WP pin has a Pull-Down resistor. Please be left unconnected or connect to GND when WP feature is not in use.

8. Confirm Write Protect Resistor by ACK

According to state of Write Protect Resistor, ACK is as follows.

State of Write Protect Register	WP Input	Input Command	ACK	Address	ACK	Data	ACK	Write Cycle(t_{WR})
In case, protect by PSWP	-	PSWP,SWP,CWP	No ACK	-	No ACK	-	No ACK	No
		Page or Byte Write (00 to 7Fh)	ACK	WA7 to WA0	ACK	D7 to D0	No ACK	No
In case,protect by SWP	0	SWP	No ACK	-	No ACK	-	No ACK	No
		CWP	ACK	-	ACK	-	ACK	Yes
		PSWP	ACK	-	ACK	-	ACK	Yes
		Page or Byte Write (00 to 7Fh)	ACK	WA7 to WA0	ACK	D7 to D0	No ACK	No
	1	SWP	No ACK	-	No ACK	-	No ACK	No
		CSP	ACK	-	ACK	-	No ACK	No
		PSWP	ACK	-	ACK	-	No ACK	No
		Page or Byte Write	ACK	WA7 to WA0	ACK	D7 to D0	No ACK	No
In case, Not protect	0	PSWP, SWP, CWP	ACK	-	ACK	-	ACK	Yes
		Page or Byte Write	ACK	WA7 to WA0	ACK	D7 to D0	ACK	Yes
	1	PSWP, SWP, CWP	ACK	-	ACK	-	No ACK	No
		Page or Byte Write	ACK	WA7 to WA0	ACK	D7 to D0	No ACK	No

Acknowledge when writing data or defining the write-protection (instructions with R/$\overline{W}$ bit=0) - is Don't Care

State of Write Protect Register	Command	ACK	Address	ACK	Data	ACK
In case, protect by PSWP	PSWP, SWP, CWP	No ACK	-	No ACK	-	No ACK
In case, protect by SWP	SWP	No ACK	-	No ACK	-	No ACK
	CWP	ACK	-	No ACK	-	No ACK
	PSWP	ACK	-	No ACK	-	No ACK
Case, Not protect	PSWP, SWP, CWP	ACK	-	No ACK	-	No ACK

Acknowledge when reading data the write-protection (instructions with R/$\overline{W}$ bit=1)

Command

1. Write Cycle

During WRITE CYCLE operation data is written in the EEPROM. The Byte Write Cycle is used to write only one byte. In the case of writing continuous data consisting of more than one byte, Page Write is used. The maximum bytes that can be written at one time is 16 bytes.

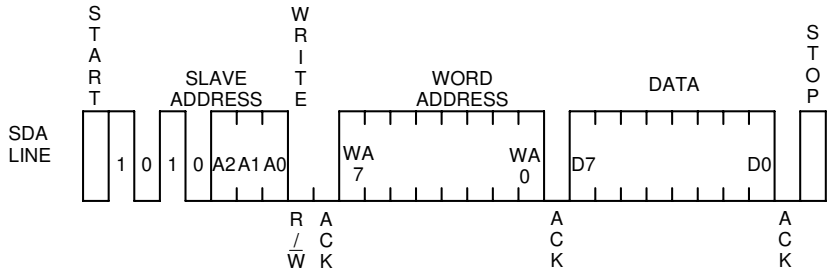


Figure 33. Byte Write Cycle Timing

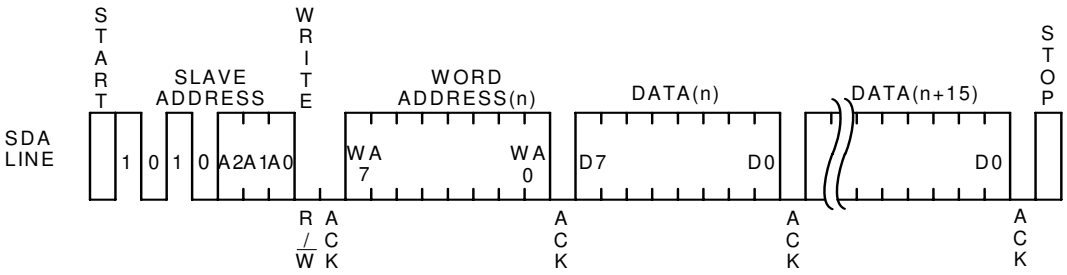


Figure 34. Page Write Cycle Timing

(1) With this command the data is programmed into the indicated word address.
(2) When the Master generates a STOP condition, the device begins the internal write cycle to the nonvolatile memory array.
(3) Once programming is started no commands are accepted for t_{WR} (5ms max).
(4) This device is capable of 16-byte Page Write operations.
(5) If the Master transmits more than 16 words prior to generating the STOP condition, the address counter will “roll over” and the previously transmitted data will be overwritten. When two or more byte of data are input, the four low order address bits are internally incremented by one after the receipt of each word, while the four higher order bits of the address (WA7 to WA4) remain constant.

2. Read Cycle

During Read Cycle operation data is read from the EEPROM. The Read Cycle is composed of Random Read Cycle and Current Read Cycle. The Random Read Cycle reads the data in the indicated address.
The Current Read Cycle reads the data in the internally indicated address and verifies the data immediately after the Write Operation. The Sequential Read operation can be performed with both Current Read and Random Read. With the Sequential Read Cycle it is possible to continuously read the next data.

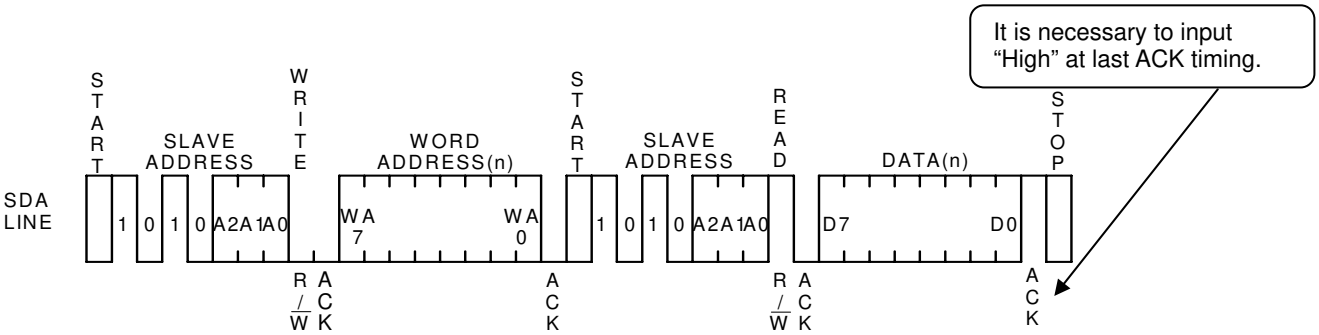


Figure 35. Random Read Cycle Timing

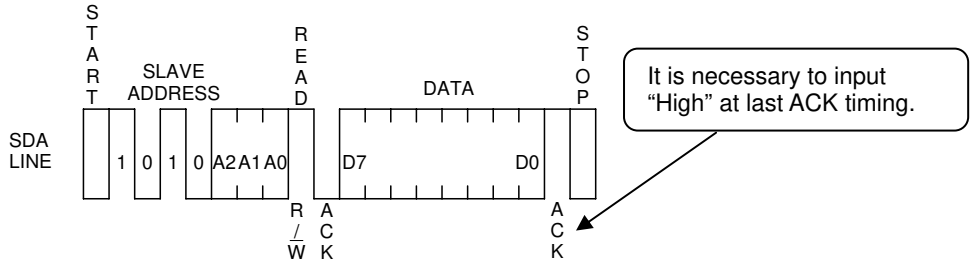


Figure 36. Current Read Cycle Timing

(1) Random Read operation allows the Master to access any memory location indicated by word address.
(2) In cases where the previous operation is Random or Current Read (which includes Sequential Read), the internal address counter is increased by one from the last accessed address (n). Thus Current Read outputs the data of the next word address (n+1).
(3) If an Acknowledge is detected and no STOP condition is generated by the Master (μ-COM), the device will continue to transmit data. (It can transmit all data (2kbit 256word))
(4) If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to standby mode.
(5) If an Acknowledge is detected with the "Low" level (not "High" level), the command will become Sequential Read, and the next data will be transmitted. Therefore, the Read command is not terminated. In order to terminate Read input Acknowledge with "High" always, then input a STOP condition.

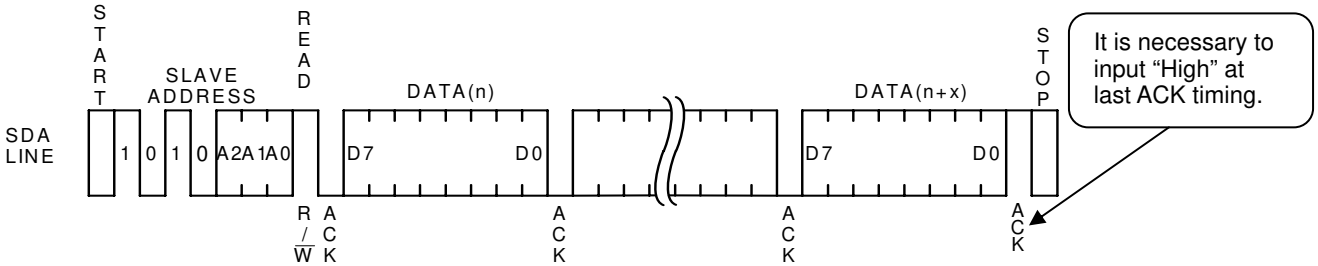


Figure 37. Sequential Read Cycle Timing（With Current Read）

3. Write Protect Cycle

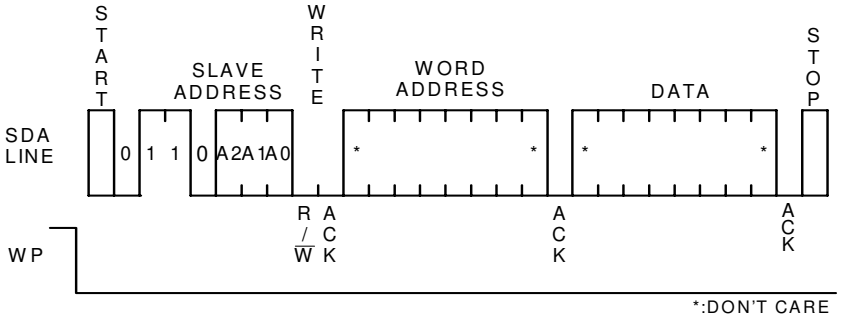


Figure 38. Permanent Set Write Protect Cycle

(1) Permanent Set Write Protect Cycle

(a) Permanent set Write Protect command set data of 00h to 7Fh in 256 words write protection block. Cancel of write protection block which is set by permanent set Write Protect command at once is impossibility. When these commands are carried out, WP pin must be OPEN or GND.

(b) Permanent Set Write Protect command needs t_{WR} from stop condition same as Byte Write and Page Write, during t_{WR}, input command is canceled.

(c) Refer to Page14 about reply of ACK in each protect state.

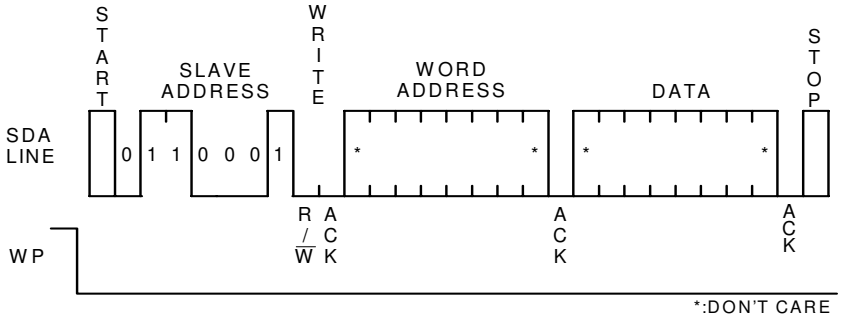


Figure 39. Set Write Protect Cycle

(2) Set Write Protect Cycle

(a) Set Write Protect command set data of 00h to 7Fh in 256 words write protection block. Clear Write Protect command can cancel write protection block which is set by set write Protect command. When these commands are carried out, WP pin must be OPEN or GND.

(b) Set write Protect command needs t_{WR} from stop condition same as Byte Write and Page Write, during t_{WR}, input command is canceled.

(c) Refer to Page14 about reply of ACK in each protect state.

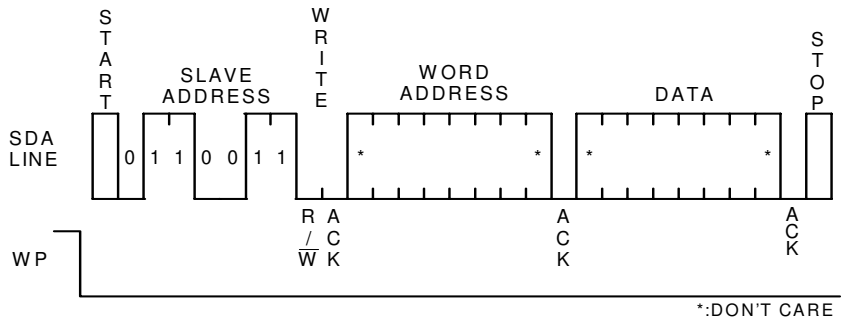


Figure 40. Clear Write Protect Cycle

(3) Clear Write Protect Cycle

(a) Clear Write Protect command can cancel write protection block which is set by set write Protect command. When these commands are carried out, WP pin must be OPEN or GND.

(b) Clear Write Protect command needs t_{WR} from stop condition same as Byte Write and Page Write, during t_{WR}, input command is canceled.

(c) Refer to Page14 about reply of ACK in each protect state.

Software Reset

Software reset is executed to avoid malfunction after power on and during command input. Software reset has several kinds and 3 kinds of them are shown in the figure below. (Refer to Figure 41.-(a), Figure 41.-(b), and Figure 41.-(c).) Within the dummy clock input area, the SDA bus is released ('H' by pull up) and ACK output and read data '0' (both 'L' level) may be output from EEPROM. Therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

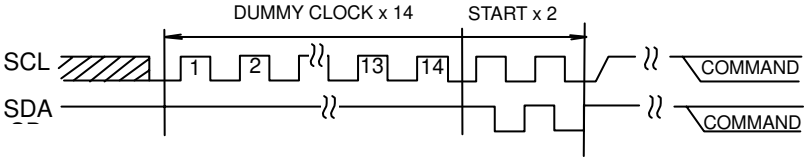


Figure 41-(a). DUMMY CLOCK x 14 + START + START

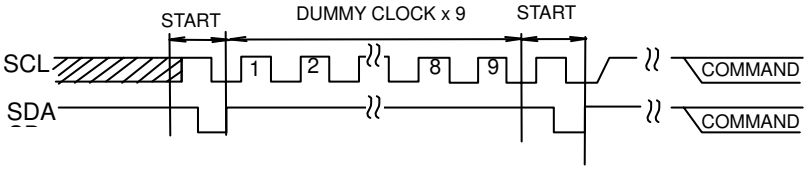


Figure 41-(b). START + DUMMY CLOCK x 9 + START

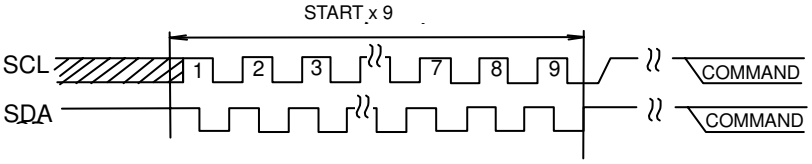


Figure 41-(c). START x 9

∗ COMMAND starts with start condition.

Acknowledge Polling

During internal write execution, all input commands are ignored, therefore ACK is not returned. During internal automatic write execution after write cycle input, next command (slave address) is sent. If the first ACK signal sends back 'L', then it means end of write operation, else 'H' is returned, which means writing is still in progress. By the use of acknowledge polling, next command can be executed without waiting for t_{WR} = 5ms.

To write continuously, $R/\overline{W}$ = 0, then to carry out current read cycle after write, slave address with $R/\overline{W}$ = 1 is sent. If ACK signal sends back 'L', and then execute word address input and data output and so forth.

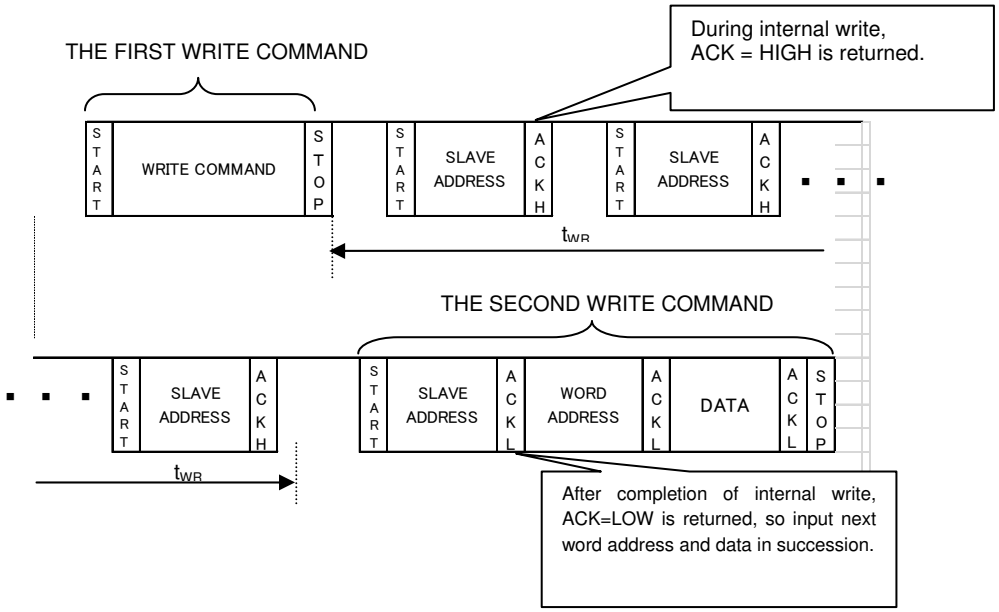


Figure 42. Case of Continuous Write by Acknowledge Polling

WP Effective Timing

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so on, observe the following WP valid timing. During write cycle execution, inside cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to take in D0 of data(in page write cycle, the first byte data) is the cancel invalid area.

WP input in this area becomes ‘Don't care’. The area from the rise of SCL to take in D0 to the stop condition input is the cancel valid area. Furthermore, after the execution of forced end by WP, the IC enters standby status..

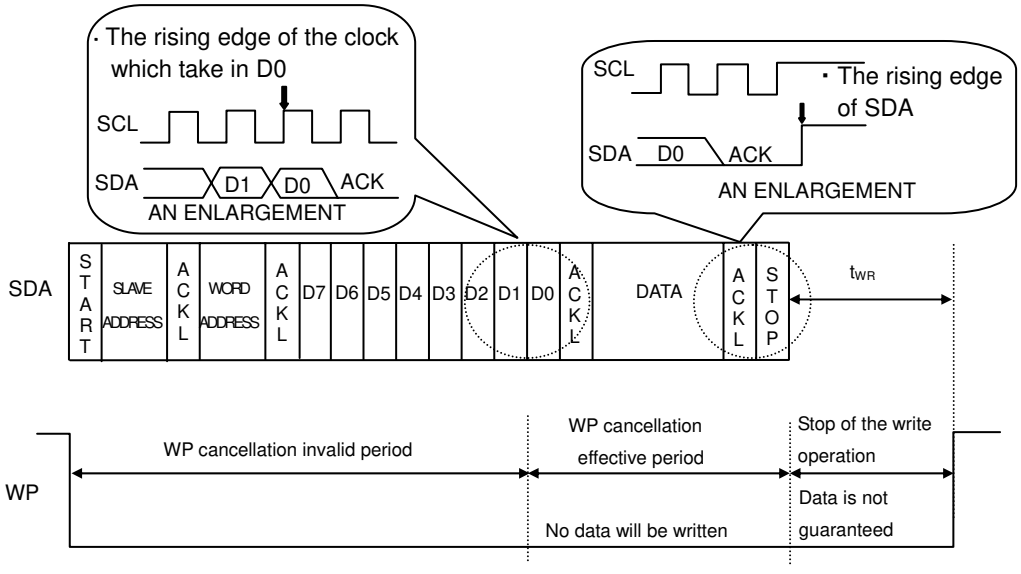


Figure 43. WP Effective Timing

Command Cancellation from the START and STOP Conditions

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Figure 44.) However, within ACK output area and during data read, SDA bus may output 'L'. In this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. When command is cancelled by start-stop condition during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined. Therefore, it is not possible to carry out current read cycle in succession. To carry out read cycle in succession, carry out random read cycle.

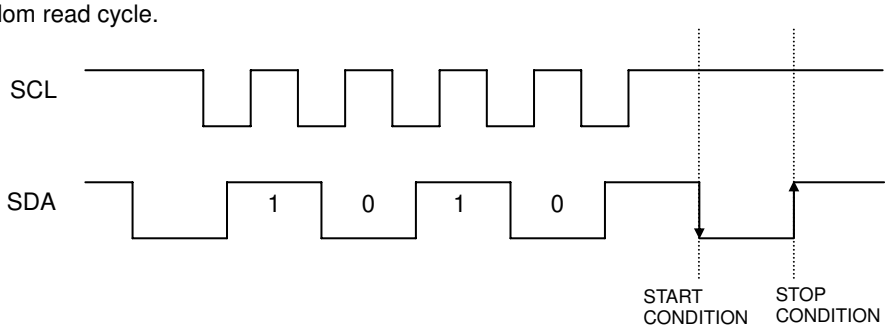


Figure 44. Command Cancellation by the START and STOP Conditions during Input of the Slave Address

I/O Peripheral Circuit

1. Pull-Up Resistance of SDA Terminal

SDA is NMOS open drain, so it requires a pull up resistor. As for this resistance value (R_{PU}), select an appropriate value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, operating frequency is limited. The smaller the R_{PU}, the larger is the supply current (Read).

2. Maximum R_{PU}

The maximum value of R_{PU} is determined by the following factors.

(1) SDA rise time to be determined by the capacitance (C_{BUS}) of bus line and R_{PU} of SDA should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.

(2) The bus. electric potential Ⓐ to be determined by the input current leak total (I_L) of device connected to bus at output of 'H' to the SDA line and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin of 0.2Vcc.

$$V_{CC}-I_L R_{PU}-0.2\,V_{CC} \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leqq \frac{0.8V_{CC}-V_{IH}}{I_L}$$

Examples: When V_{CC} =3V, I_L=10μA, V_{IH}=0.7 V_{CC}
According to (2)

$$R_{PU} \leqq \frac{0.8\times3-0.7\times3}{10\times10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

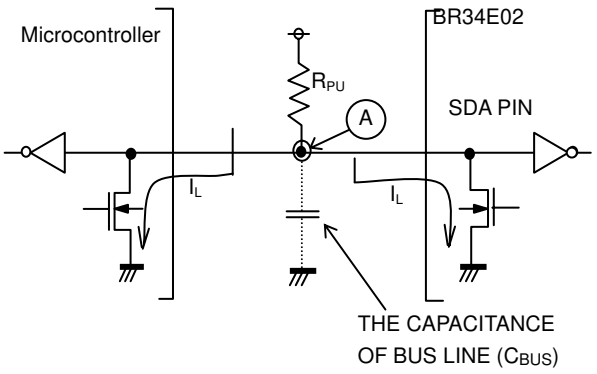


Figure 45. I/O Circuit

3. Minimum R_{PU}

The minimum value of RPU is determined by following factors.

(1) Meets the condition that VOLMAX=0.4V, IOLMAX=3mA when the output is Low.

$$\frac{V_{CC}-V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{V_{CC}-V_{OL}}{I_{OL}}$$

(2) VOLMAX=0.4V must be lower than the input Low level of the micro controller and the EEPROM including the recommended noise margin of 0.1VCC.

$$V_{OLMAX} \leqq V_{IL}-0.1\ V_{CC}$$

Examples: VCC=3V, VOL=0.4V, IOL=3mA, the VIL of the micro controller and the EEPROM is VIL=0.3VCC,

According to (1) $R_{PU} \geqq \frac{3-0.4}{3\times10^{-3}}$

$\geqq 867\ [\Omega]$

And $V_{OL}=0.4$ [V]

And $V_{IL}=0.3\times3$

$=0.9$ [V]

so that condition (2) is met

4. Pull-up Resistance of SCL Terminal

When SCL control is made at the CMOS output port, there is no need for a pull up resistor. But when there is a time where SCL becomes 'Hi-Z', add a pull up resistor. As for the pull up resistor value, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

A0, A1, A2, WP Pin Connections

1. Device Address Pin (A0, A1, A2) Connections

The status of the device address pins is compared with the device address sent by the Master. One of the devices that are connected to the identical BUS is selected. Pull up or down these pins or connect them to VCC or GND. Pins that are not used as device address (N.C.Pins) may be High, Low, or Hi-Z.

2. WP Pin Connection

The WP input allows or prohibits write operations. When WP is High, only Read is available and Write to all address is prohibited. Both Read and Write are available when WP is Low.
In the event that the device is used as a ROM, it is recommended that the WP input be pulled up or connected to VCC. When both READ and WRITE are operated, the WP input must be pulled down or connected to GND or controlled.

Microcontroller Connection

1. R_S

In I^2C BUS, it is recommended that SDA port is of open drain input/output. However, when using CMOS input / output of tri state to SDA port, insert a series resistance R_S between the pull up resistor Rpu and the SDA terminal of EEPROM. This is to control over current that may occur when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. R_S also plays the role of protecting the SDA terminal against surge. Therefore, even when SDA port is open drain input/output, R_S can be used.

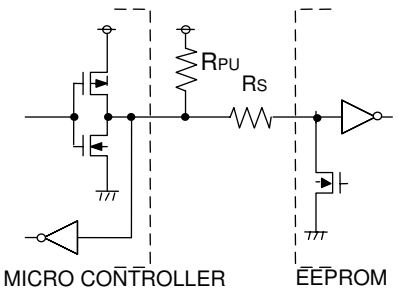


Figure 46. I/O Circuit

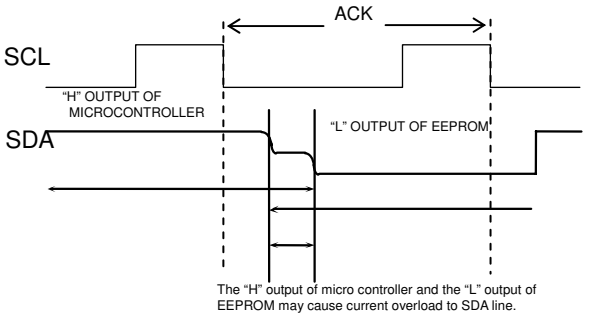


Figure 47. Input/Output Collision Timing

2. Maximum Value of R_S

The maximum value of R_S is determined by the following relations.

(1) SDA rise time to be determined by the capacitance (C_{BUS}) of bus line and R_{PU} of SDA should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.

(2) The bus' electric potential Ⓐ to be determined by R_{PU} and R_S the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin of 0.1Vcc.

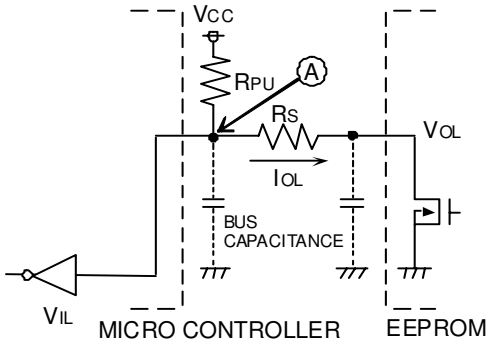


Figure 48. I/O Circuit

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

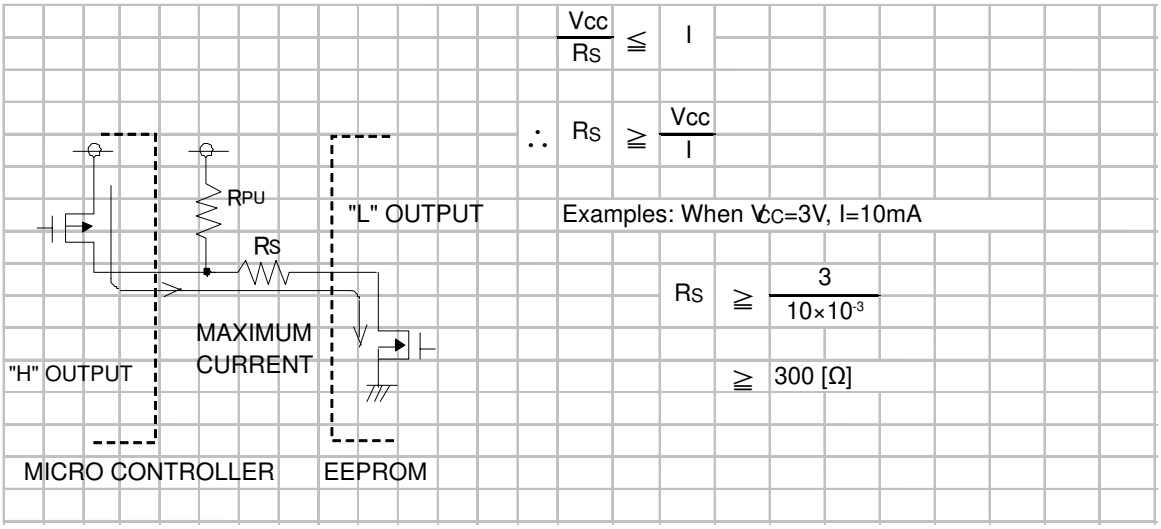
Examples: When V_{CC}=3V, V_{IL}=0.3V_{CC}, V_{OL}=0.4V, R_{PU}=20k

$$\text{According } R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67[k\Omega]$$

3. Minimum Value of R_S

The minimum value of R_S is determined by over current at bus collision. When over current flows, noises in power source line and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of the impedance of power source line in set and so forth. Set the over current to EEPROM at 10mA or lower.



$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{V_{CC}}{I}$$

Examples: When V_{CC}=3V, I=10mA

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300\ [\Omega]$$

Figure 49. I/O Circuit

I/O Equivalence Circuit

1. **Input (A0,A1,A2,SCL)**

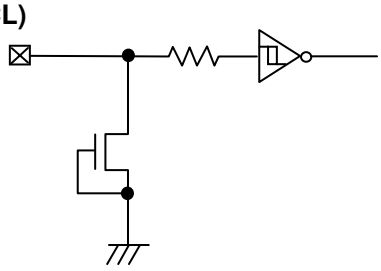


Figure 50. Input Pin Circuit Diagram

2. **Input (SDA)**

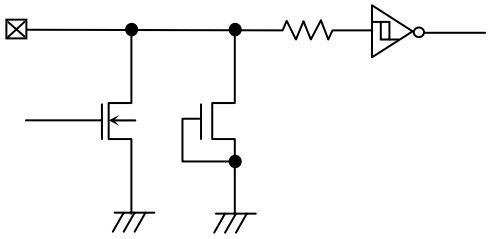


Figure 51. Input Pin Circuit Diagram

3. **Input (WP)**

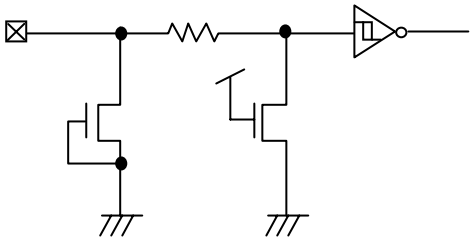


Figure 52. Input Pin Circuit Diagram

Power-Up/Down Conditions

At power ON, the IC's internal circuits may go through unstable low voltage area as the Vcc rises, making the IC's internal logic circuit not completely reset, hence, malfunction may occur. To prevent this, the IC is equipped with POR circuit and LVCC circuit. To assure the operation, observe the following conditions at power ON.

1. "SDA='H'" and "SCL='L' or 'H'".
2. Follow the recommended conditions of t_R, t_{OFF}, Vbot so that P.O.R. will be activated during power up.

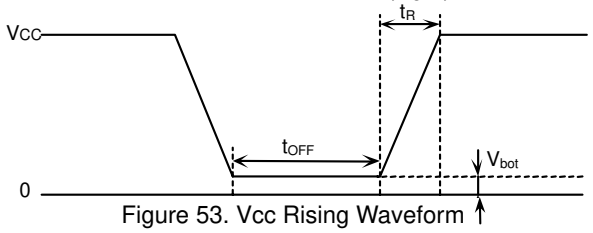


Figure 53. Vcc Rising Waveform

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

3. Set SDA and SCL so as not to become "Hi-Z".
   When the above conditions 1 and 2 cannot be observed, take following countermeasures.

   (1) In the case when the above condition 1 cannot be observed such that SDA becomes 'L' at power ON.
   →Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

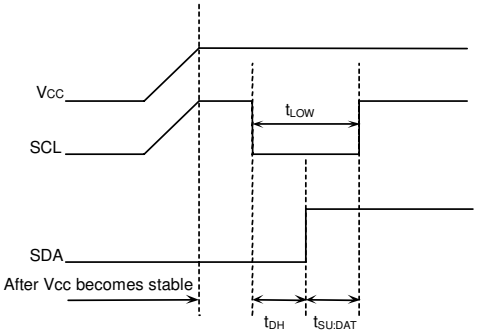


Figure 54. SCL="H" and SDA="L"

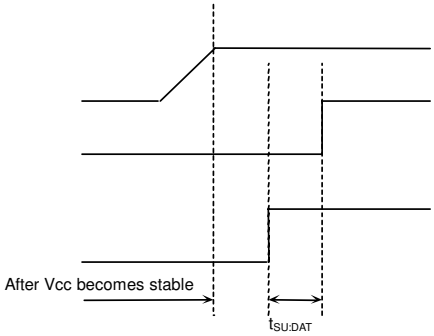


Figure 55. SCL="L" and SDA="L"

   (2) In the case when the above condition 2 cannot be observed.
   →After the power source become stable, execute software reset.(Figure 41)
   (3) In the case when the above condition 1 and 2 cannot be observed.
   →Carry out (1), and then carry out (2).

Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite operation at low power, and prevents write error. At LVCC voltage (Typ =1.2V) or below, data rewrite is prevented.

Noise Countermeasures

1. Bypass Capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, it is recommended to connect a bypass capacitor (0.1µF) between IC Vcc and GND pins. Connect the capacitor as close to IC as possible. In addition, it is also recommended to connect a bypass capacitor between board's Vcc and GND.

Operational Notes

1. Described numeric values and data are design representative values only, and the values are not guaranteed.

2. We believe that the application circuit examples in this document are recommendable. However, in actual use, confirm characteristics further sufficiently. If changing the fixed number of external parts is desired, make your decision with sufficient margin in consideration of static characteristics, transient characteristics, and fluctuations of external parts and our LSI.

3. Absolute maximum ratings
   If the absolute maximum ratings such as supply voltage, operating temperature range, and so on are exceeded, LSI may be destroyed. Do not supply voltage or subject the IC to temperatures exceeding the absolute maximum ratings. In the case of fear of exceeding the absolute maximum ratings, take physical safety countermeasures such as adding fuses, and see to it that conditions exceeding the absolute maximum ratings should not be supplied to the LSI.

4. GND electric potential
   Set the voltage of GND terminal lowest at any operating condition. Make sure that each terminal voltage is not lower than that of GND terminal.

5. Thermal design
   Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.

6. Short between Pins and Mounting Errors
   Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

7. Operating the IC in the presence of strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.