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Serial EEPROM series Standard EEPROM

MicroWire BUS EEPROM (3-Wire)

BR93G66-3A

General Description

BR93G66-3A is serial EEPROM of Serial 3-Line Interface Method.
They are 16bit organization and CS PIN is the first PIN in their PIN configuration.

Features

- 3-Line Communications of chip select, serial clock, serial data input / output (the case where input and output are shared)
- Operations available at High Speed 3MHz clock (4.5 V to 5.5 V)
- High Speed Write available (Write Time 5ms Max)
- Same package and pin configuration from 1Kbit to 16Kbit
- 1.7V to 5.5V Single Power Source Operation
- Address Auto Increment Function at read Operation
- Write Error Prevention Function
  - »Write Prohibition at Power On
  - »Write Prohibition by Command Code
  - »Write Error Prevention function at Low Voltage
- Self-timed Programming Cycle
- Program Condition Display by READY / $\overline{\text{BUSY}}$
- Compact Package
  SOP8 SOP-J8 SSOP-B8 TSSOP-B8 MSOP8
  TSSOP-B8J DIP-T8 VSON008X2030
- More than 40 years data retention
- More than 1million write cycles
- Initial delivery state all addresses FFFFh

Packages W(Typ) x D(Typ)x H(Max)

DIP-T8
9.30mm x 6.50mm x 7.10mm

TSSOP-B8
3.00mm x 6.40mm x 1.20mm

SOP8
5.00mm x 6.20mm x 1.71mm

TSSOP-B8J
3.00mm x 4.90mm x 1.10mm

SOP- J8
4.90mm x 6.00mm x 1.65mm

MSOP8
2.90mm x 4.00mm x 0.90mm

SSOP-B8
3.00mm x 6.40mm x 1.35mm

VSON008X2030
2.00mm x 3.00mm x 0.60mm

BR93G66-3A

Capacity	Bit Format	Type	Power Source Voltage	DIP-T8(1)	SOP8	SOP-J8	SSOP-B8	TSSOP-B8	TSSOP-B8J	MSOP8	VSON008 X2030
4Kbit	256×16	BR93G66-3A	1.7V to 5.5V	●	●	●	●	●	●	●	●

(1) DIP-T8 is not halogen free package

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	V_{CC}	-0.3 to +6.5	V	
Permissible Dissipation	Pd	800 (DIP-T8)	mW	Derate by 8.0mW/°C when operating above Ta=25°C
		450 (SOP8)		Derate by 4.5mW/°C when operating above Ta=25°C
		450 (SOP-J8)		Derate by 4.5mW/°C when operating above Ta=25°C
		300 (SSOP-B8)		Derate by 3.0mW/°C when operating above Ta=25°C
		330 (TSSOP-B8)		Derate by 3.3mW/°C when operating above Ta=25°C
		310 (TSSOP-B8J)		Derate by 3.1mW/°C when operating above Ta=25°C
		310 (MSOP8)		Derate by 3.1mW/°C when operating above Ta=25°C
		300 (VSON008X2030)		Derate by 3.0mW/°C when operating above Ta=25°C
Storage Temperature	Tstg	-65 to +150	℃	
Operating Temperature	Topr	-40 to +85	℃	
Input Voltage/ Output Voltage	-	-0.3 to Vcc+1.0	V	The Max value of Input Voltage/ Output Voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of Input Voltage/ Output Voltage is not below -0.8V.
Junction Temperature	Tjmax	150	℃	Junction temperature at the storage condition

Memory Cell Characteristics (V_{CC}=1.7V to 5.5V)

Parameter	Limit			Unit	Conditions
	Min	Typ	Max		
Write Cycles (1)	1,000,000	-	-	Times	Ta=25℃
Data Retention (1)	40	-	-	Years	Ta=25℃

○Initial data in all addresses are FFFFh(X16) upon delivery.
(1) Not 100% TESTED

Recommended Operating Ratings

Parameter	Symbol	Limit	Unit
Supply Voltage	V_{CC}	1.7 to 5.5	V
Input Voltage	V_{IN}	0 to V_{CC}	

DC Characteristics (Unless otherwise specified, V_{CC}=1.7V to 5.5V, Ta=-40℃ to +85℃)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Low Voltage	V_{IL}	-0.3(1)	-	$0.3V_{CC}$	V	$1.7V \leqq V_{CC} \leqq 5.5V$
Input High Voltage	V_{IH}	$0.7V_{CC}$	-	V_{CC}+1.0	V	$1.7V \leqq V_{CC} \leqq 5.5V$
Output Low Voltage 1	V_{OL1}	0	-	0.4	V	I_{OL}=2.1mA, $2.7V \leqq V_{CC} \leqq 5.5V$
Output Low Voltage 2	V_{OL2}	0	-	0.2	V	I_{OL}=100μA
Output High Voltage 1	V_{OH1}	2.4	-	V_{CC}	V	I_{OH}=-0.4mA, $2.7V \leqq V_{CC} \leqq 5.5V$
Output High Voltage 2	V_{OH2}	V_{CC}-0.2	-	V_{CC}	V	I_{OH}=-100μA
Input Leakage Current1	I_{LI1}	-1	-	+1	μA	V_{IN}=0V to V_{CC}(CS,SK,DI)
Output Leakage Current	I_{LO}	-1	-	+1	μA	V_{OUT}=0V to V_{CC}, CS=0V
Supply Current	I_{CC1}	-	-	1.0	mA	V_{CC}=1.7V, f_{SK}=1MHz, $t_{E/W}$=5ms (WRITE)
		-	-	2.0	mA	V_{CC}=5.5V ,f_{SK}=3MHz, $t_{E/W}$=5ms (WRITE)
	I_{CC2}	-	-	0.5	mA	f_{SK}=1MHz (READ)
		-	-	1.0	mA	f_{SK}=3MHz (READ)
	I_{CC3}	-	-	2.0	mA	V_{CC}=2.5V, f_{SK}=1MHz $t_{E/W}$=5ms (WRAL, ERAL)
		-	-	3.0	mA	V_{CC}=5.5V ,f_{SK}=3MHz $t_{E/W}$=5ms (WRAL, ERAL)
Standby Current	I_{SB1}	-	-	2.0	μA	CS=0V

(1) When the pulse width is 50ns or less, the Min value of V_{IL} is admissible to -0.8V.

AC Characteristics (Unless otherwise specified, V_{CC}=1.7V to 2.5V, Ta=-40℃ to +85℃)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
SK Frequency	f_{SK}	-	-	1	MHz
SK High Time	t_{SKH}	250	-	-	ns
SK Low Time	t_{SKL}	250	-	-	ns
CS Low Time	t_{CS}	250	-	-	ns
CS Setup Time	t_{CSS}	200	-	-	ns
DI Setup Time	t_{DIS}	100	-	-	ns
CS Hold Time	t_{CSH}	0	-	-	ns
DI Hold Time	t_{DIH}	100	-	-	ns
Data “1” Output Delay	t_{PD1}	-	-	400	ns
Data “0” Output Delay	t_{PD0}	-	-	400	ns
Time from CS to Output Establishment	t_{SV}	-	-	400	ns
Time from CS to High-Z	t_{DF}	-	-	200	ns
Write Cycle Time	$t_{E/W}$	-	-	5	ms

(Unless otherwise specified, V_{CC}=2.5V to 4.5V, Ta=-40℃ to +85℃)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
SK Frequency	f_{SK}	-	-	2	MHz
SK High Time	t_{SKH}	230	-	-	ns
SK Low Time	t_{SKL}	200	-	-	ns
CS Low Time	t_{CS}	200	-	-	ns
CS Setup Time	t_{CSS}	50	-	-	ns
DI Setup Time	t_{DIS}	100	-	-	ns
CS Hold Time	t_{CSH}	0	-	-	ns
DI Hold Time	t_{DIH}	100	-	-	ns
Data “1” Output Delay	t_{PD1}	-	-	200	ns
Data “0” Output Delay	t_{PD0}	-	-	200	ns
Time from CS to Output Establishment	t_{SV}	-	-	150	ns
Time from CS to High-Z	t_{DF}	-	-	100	ns
Write Cycle Time	$t_{E/W}$	-	-	5	ms

(Unless otherwise specified, V_{CC}=4.5V to 5.5V, Ta=-40℃ to +85℃)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
SK Frequency	f_{SK}	-	-	3	MHz
SK High Time	t_{SKH}	100	-	-	ns
SK Low Time	t_{SKL}	100	-	-	ns
CS Low Time	t_{CS}	200	-	-	ns
CS Setup Time	t_{CSS}	50	-	-	ns
DI Setup Time	t_{DIS}	50	-	-	ns
CS Hold Time	t_{CSH}	0	-	-	ns
DI Hold Time	t_{DIH}	50	-	-	ns
Data “1” Output Delay	t_{PD1}	-	-	200	ns
Data “0” Output Delay	t_{PD0}	-	-	200	ns
Time from CS to Output Establishment	t_{SV}	-	-	150	ns
Time from CS to High-Z	t_{DF}	-	-	100	ns
Write Cycle Time	$t_{E/W}$	-	-	5	ms

Serial Input / Output Timing

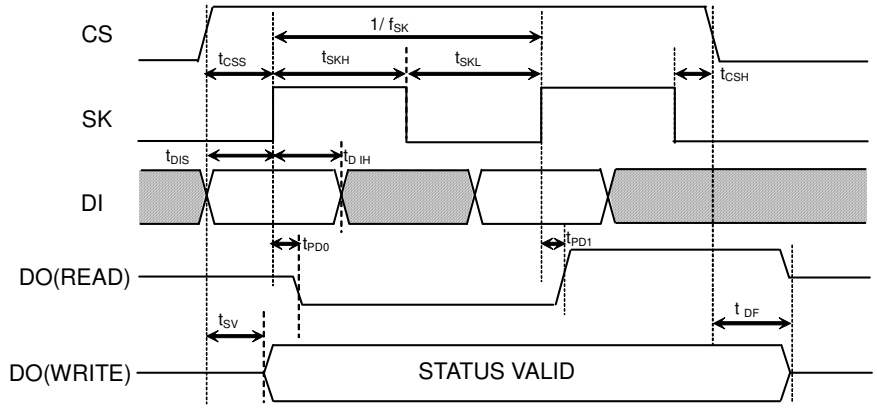


Figure 1. Serial Input / Output Timing

1. Data is taken by DI sync with the rise of SK.
2. At read operation, data is output from DO in sync with the rise of SK.
3. The STATUS signal at Write (READY / $\overline{\text{BUSY}}$) is output after t_{CS} from the fall of CS after write command input, at the area DO where CS is high, and valid until the next command start bit is input. And, while CS is low, DO becomes High-Z.
4. After completion of each mode execution, set CS low once for internal circuit reset, and execute the following operation mode.
5. $1/f_{SK}$ is the SK clock cycle, even if f_{SK} is maximum, the SK clock cycle can't be t_{SKH}(Min)+t_{SKL}(Min)
6. For "Write cycle time $t_{E/W}$", please see Figure 36,37,39,40.
7. For "CS low time t_{CS}", please see Figure 36,37,39,40.

Block Diagram

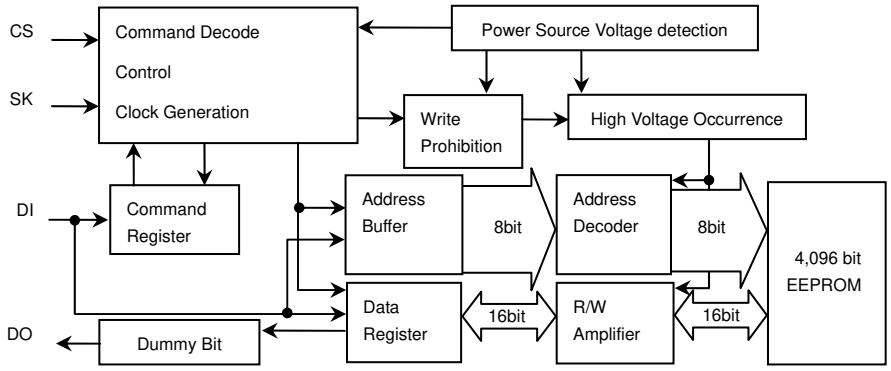


Figure 2. Block Diagram

Pin Configuration

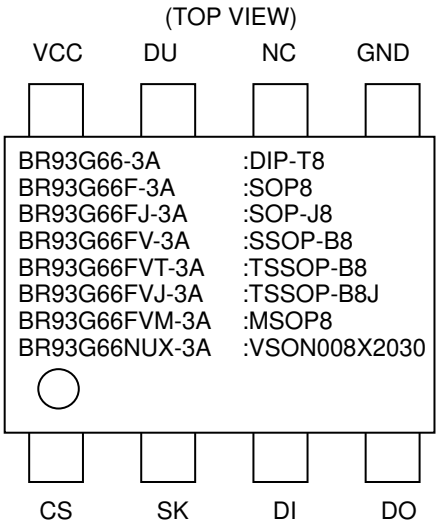


Figure 3. Pin Configuration

Pin Description

Pin Name	I / O	Descriptions
CS	Input	Chip select input
SK	Input	Serial clock input
DI	Input	Start bit, ope code, address, and serial data input
DO	Output	Serial data output, READY / $\overline{\text{BUSY}}$ STATUS display output
GND	-	All input / output reference voltage, 0V
NC	-	Non connected terminal(1)
DU	-	Don't use terminal(1)
VCC	-	Supply voltage

(1) Terminals not used may be set to any of high, low, and OPEN

Typical Performance Curves

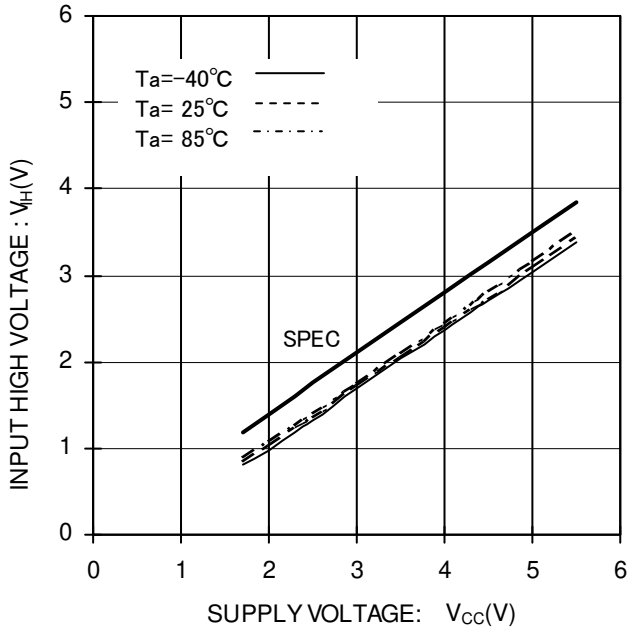


Figure 4. Input High Voltage vs Supply Voltage (CS,SK,DI)

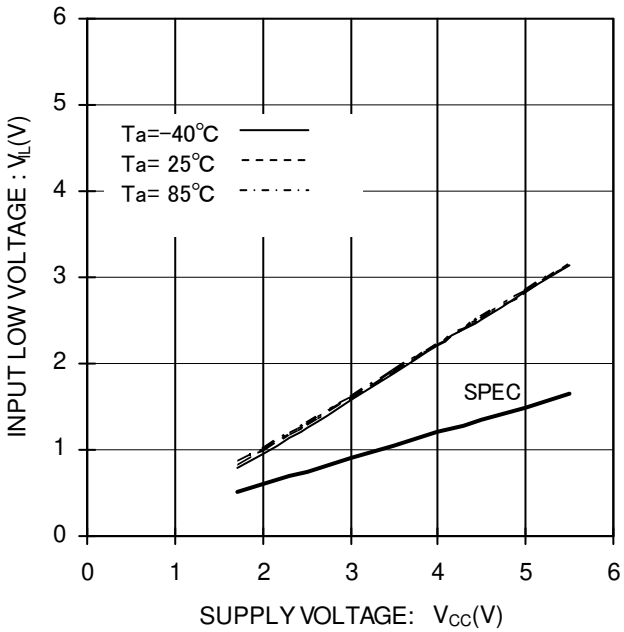


Figure 5. Input Low Voltage vs Supply Voltage (CS,SK,DI)

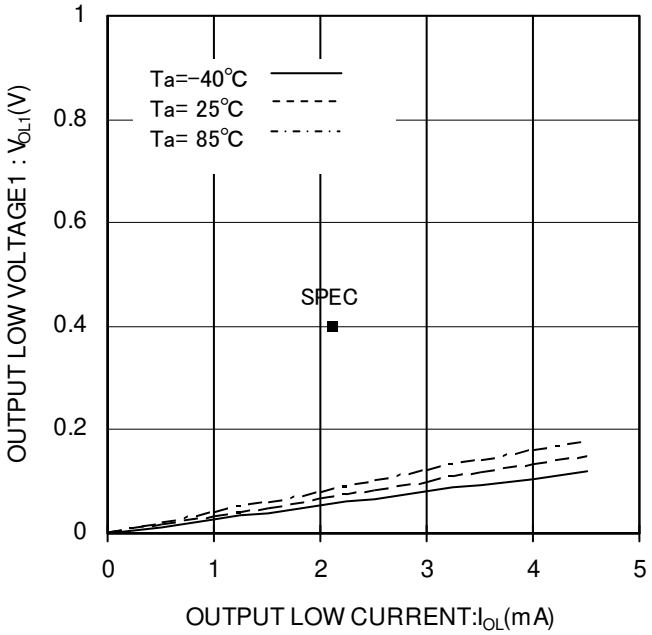


Figure 6. Output Low Voltage1 vs Output Low Current (V_{CC}=2.7V)

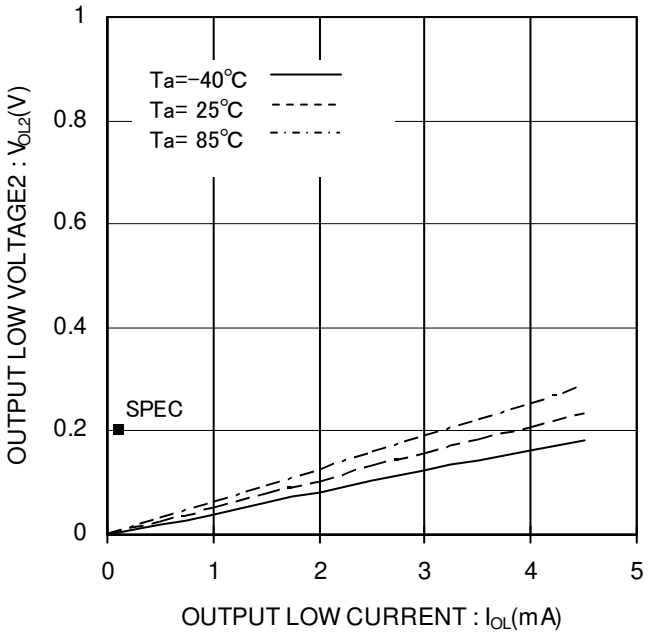


Figure 7. Output Low Voltage2 vs Output Low Current (V_{CC}=1.7V)

Typical Performance Curves - Continued

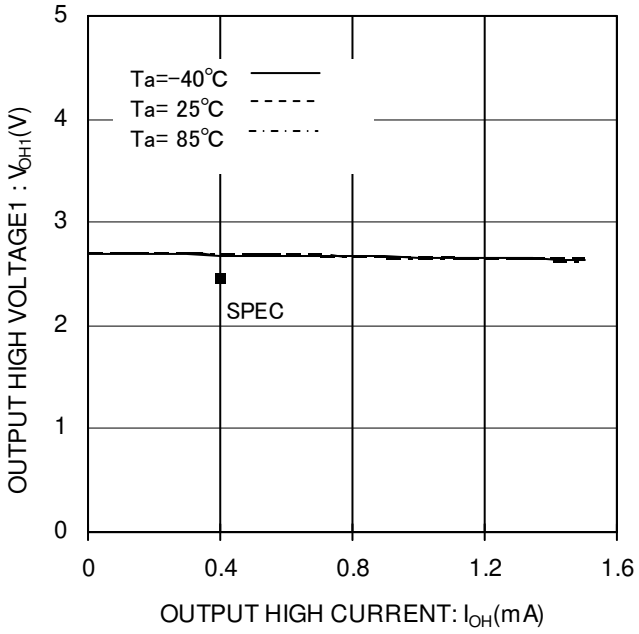


Figure 8. Output High Voltage1 vs Output High Current (V_{CC}=2.7V)

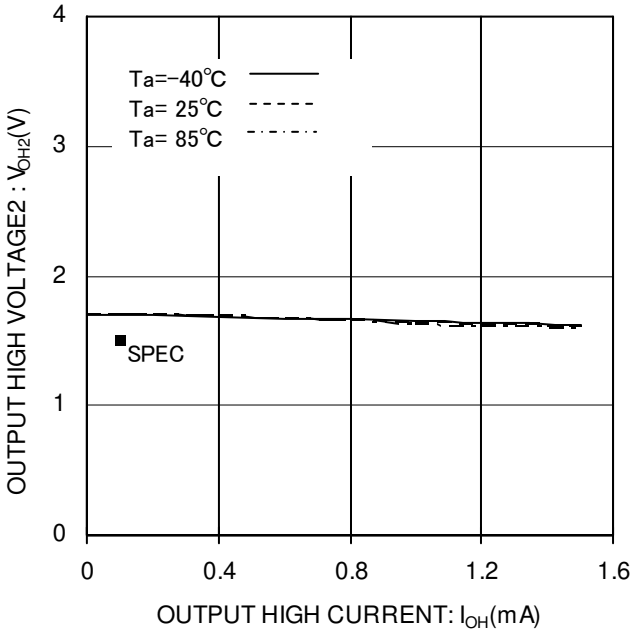


Figure 9. Output High Voltage2 vs Output High Current (V_{CC}=1.7V)

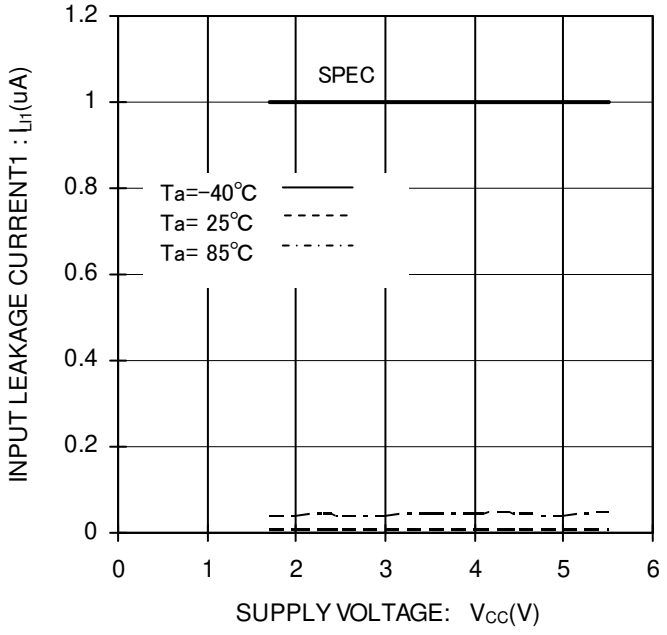


Figure 10. Input Leakage Current (CS) vs Supply Voltage

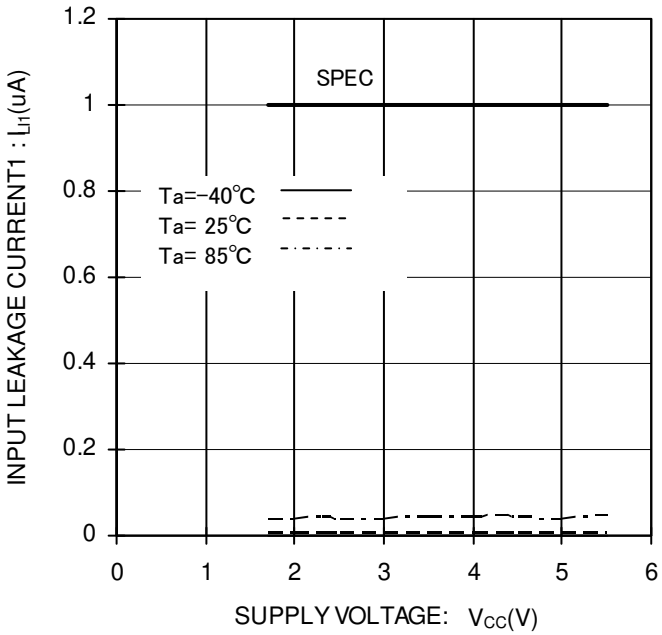


Figure 11. Input Leakage Current (SK) vs Supply Voltage

Typical Performance Curves - Continued

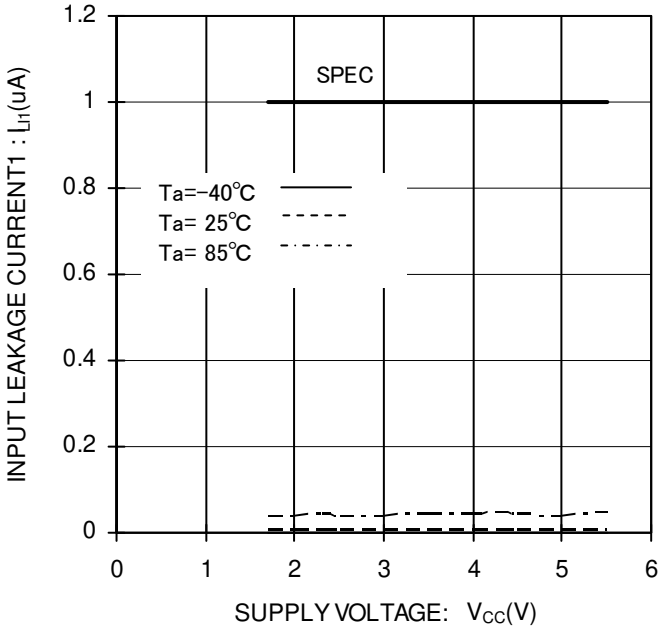


Figure 12. Input Leakage Current (DI)
vs Supply Voltage

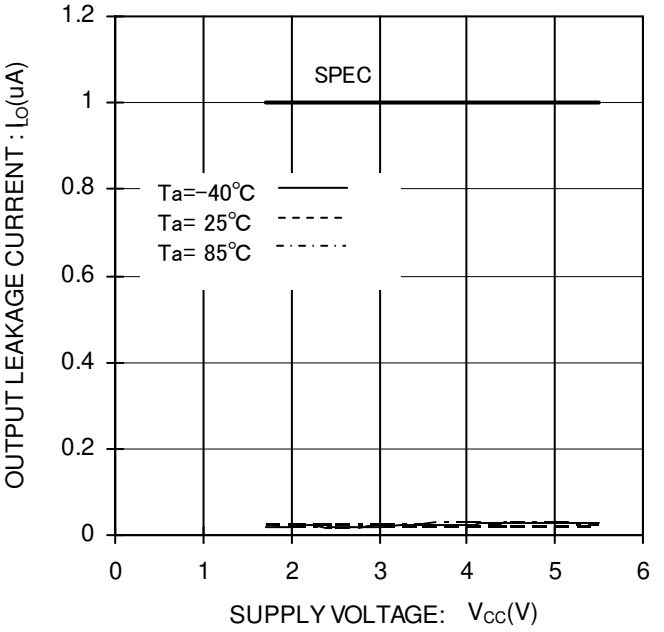


Figure 13. Output Leakage Current (DO)
vs Supply Voltage

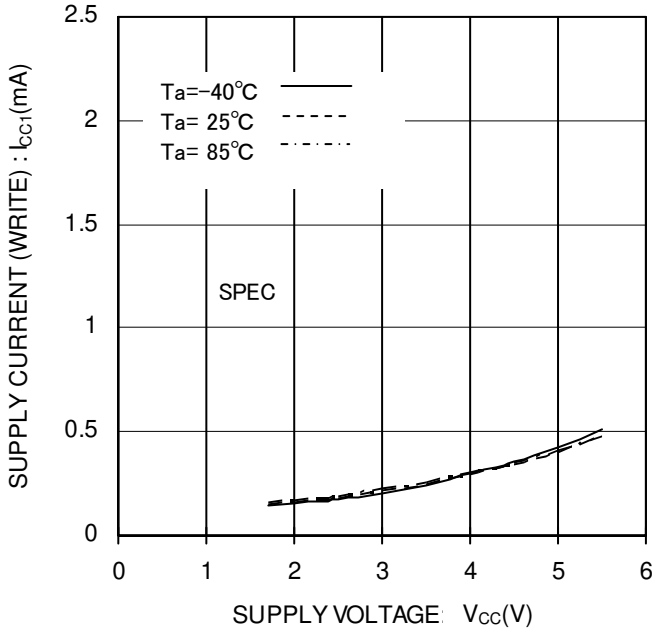


Figure 14. Supply Current (WRITE) vs Supply Voltage
(f_{SK}=1MHz)

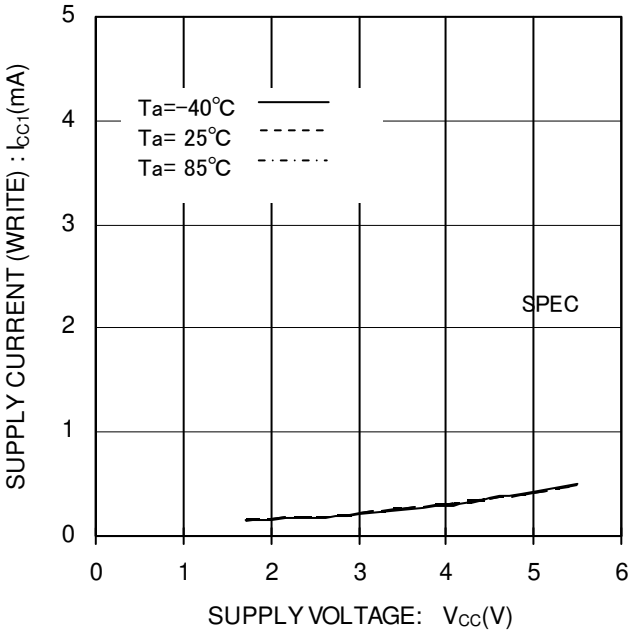


Figure 15. Supply Current (WRITE) vs Supply Voltage
(f_{SK}=3MHz)

Typical Performance Curves - Continued

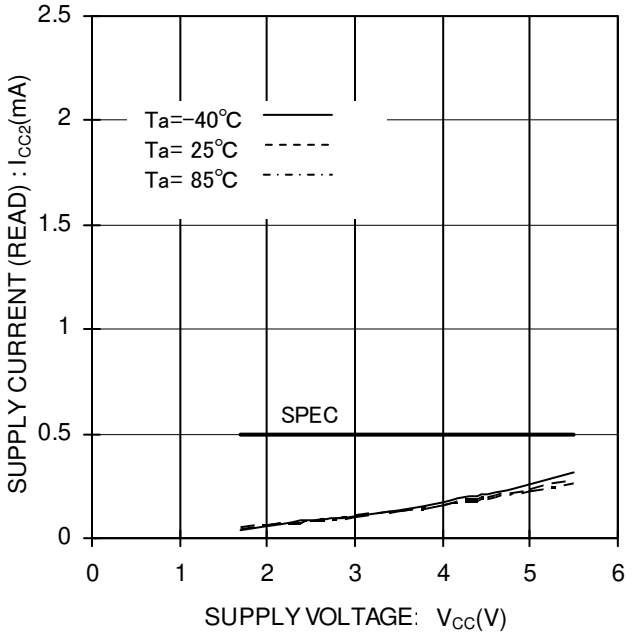


Figure 16 Supply Current (READ) vs Supply Voltage (f_{SK}=1MHz).

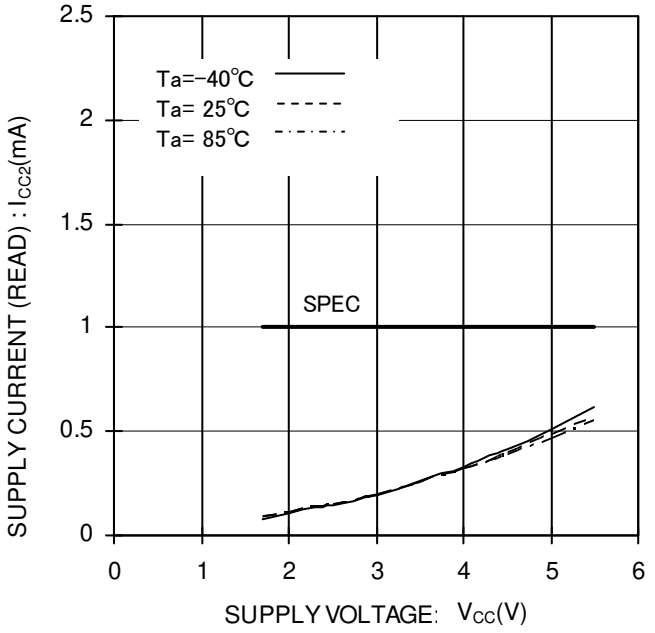


Figure 17. Supply Current (READ) vs Supply Voltage (f_{SK}=3MHz)

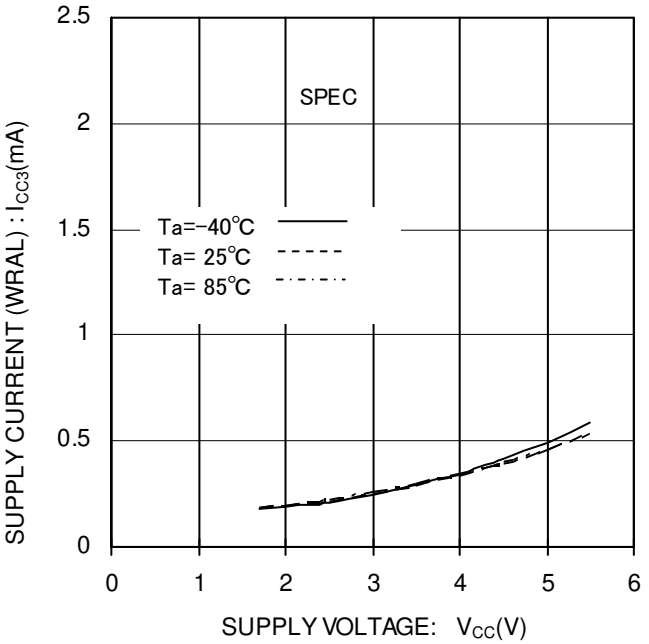


Figure 18. Supply Current (WRAL) vs Supply Voltage (f_{SK}=1MHz)

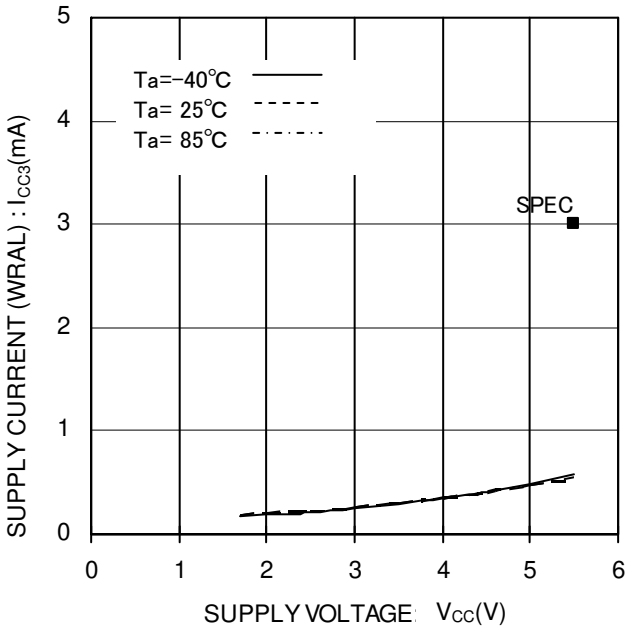


Figure 19. Supply Current (WRAL) vs Supply Voltage (f_{SK}=3MHz)

Typical Performance Curves - Continued

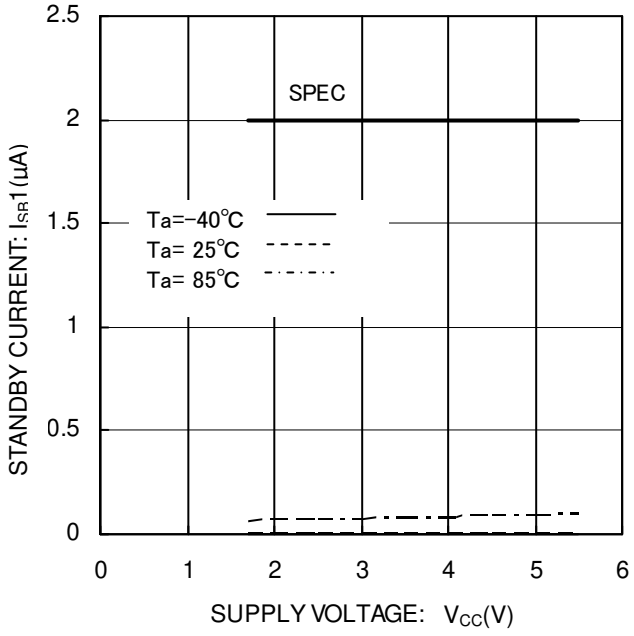


Figure 20. Standby Current vs Supply Voltage (CS=0V)

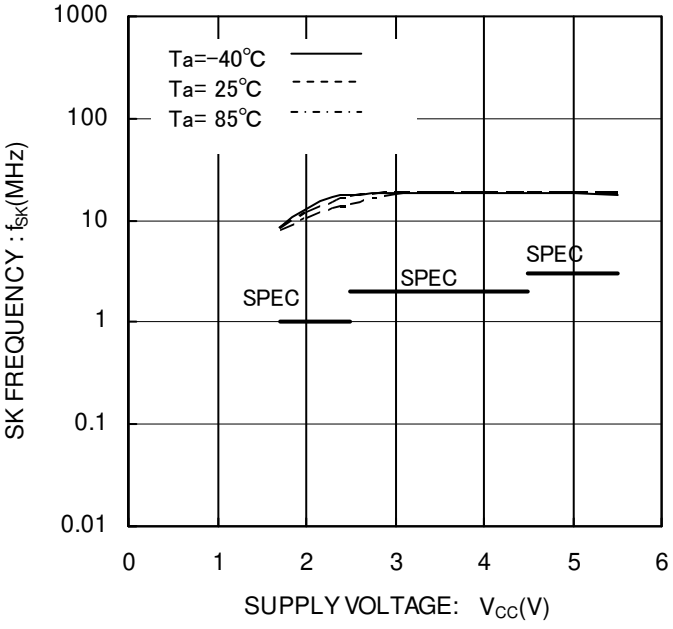


Figure 21. SK Frequency vs Supply Voltage

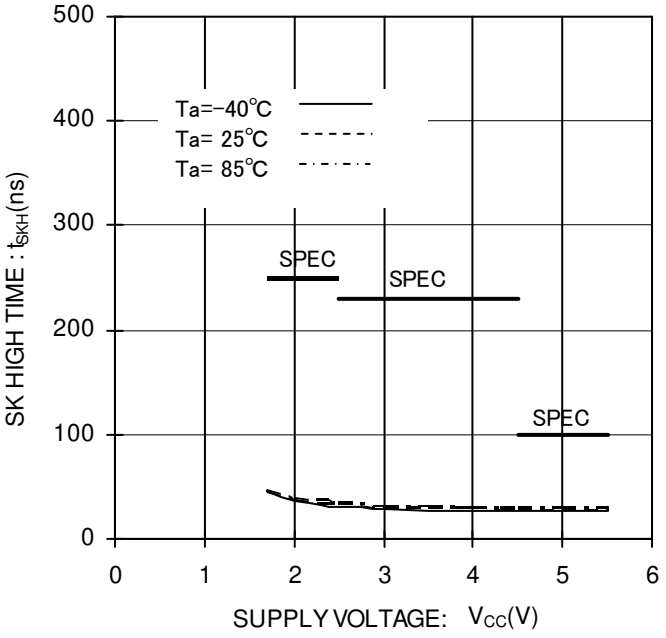


Figure 22. SK High Time vs Supply Voltage

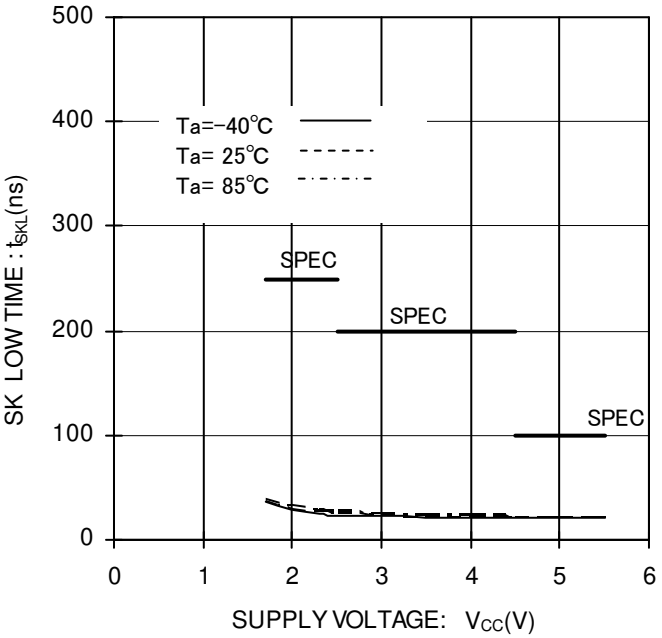


Figure 23. SK Low Time vs Supply Voltage

Typical Performance Curves - Continued

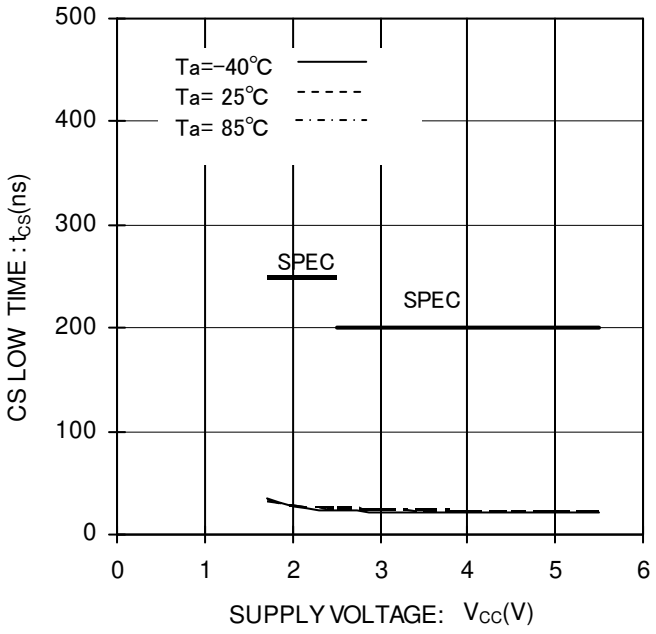


Figure 24. CS Low Time vs Supply Voltage

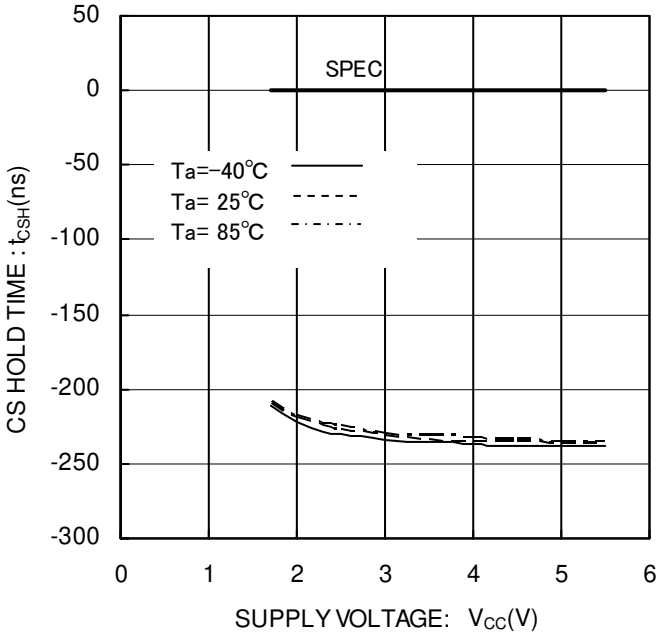


Figure 25. CS Hold Time vs Supply Voltage

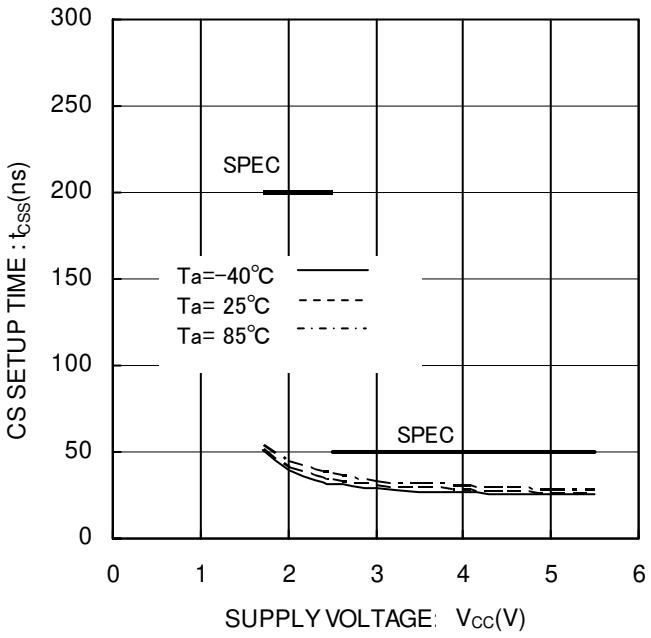


Figure 26. CS Setup Time vs Supply Voltage

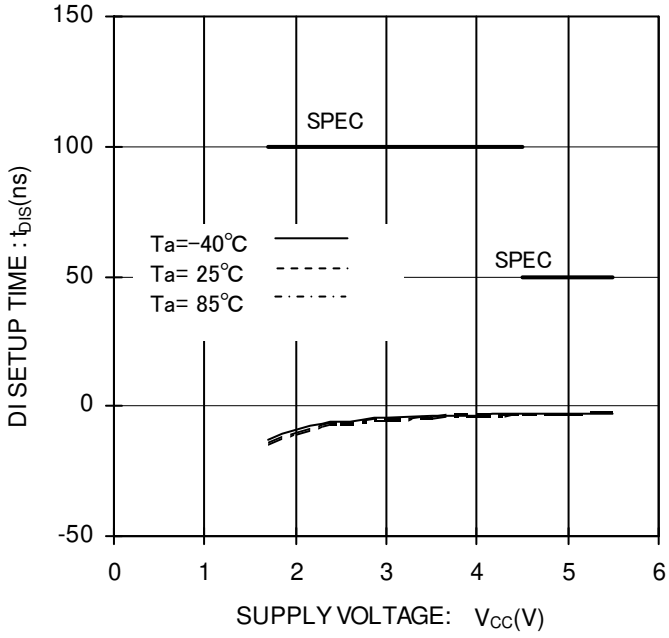


Figure 27. DI Setup Time vs Supply Voltage

Typical Performance Curves - Continued

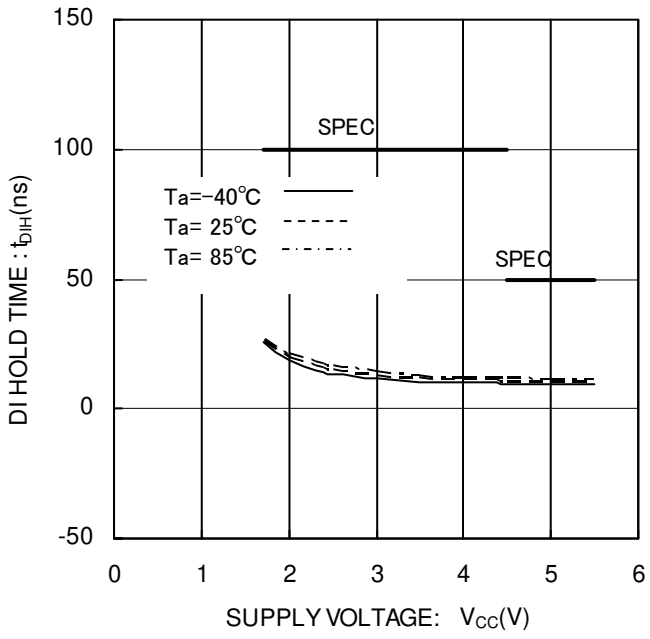


Figure 28. DI Hold Time vs Supply Voltage

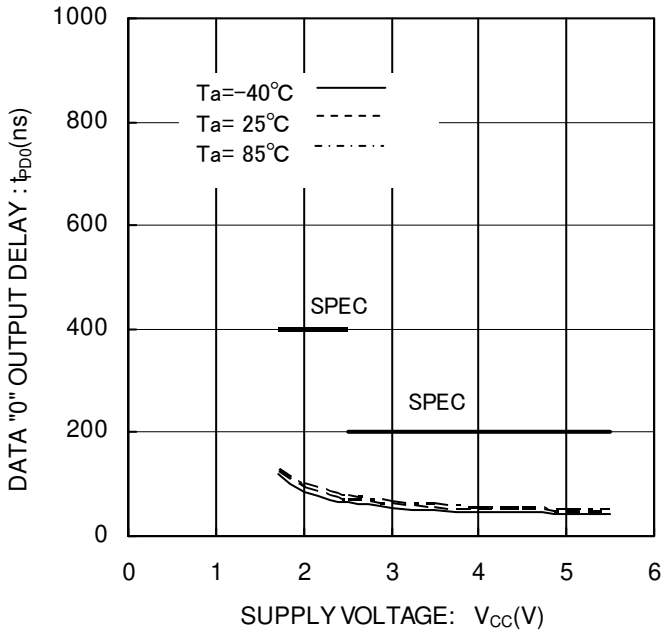


Figure 29. Data "0" Output Delay vs Supply Voltage

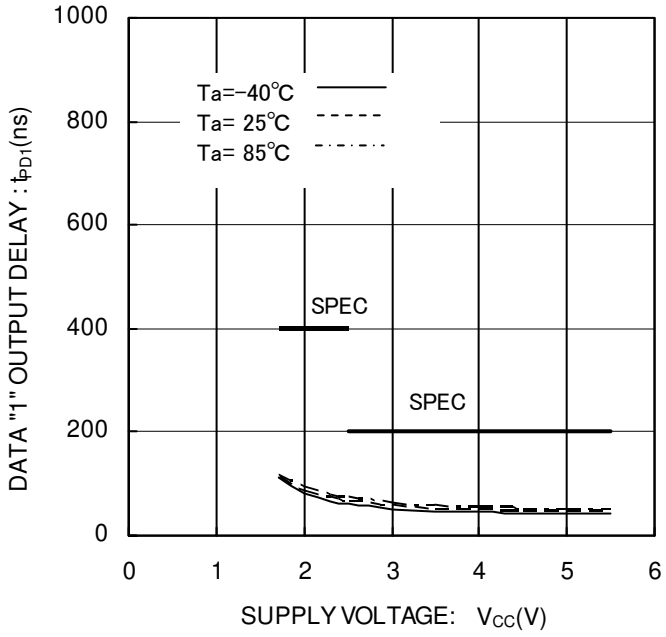


Figure 30. Data "1" Output Delay vs Supply Voltage

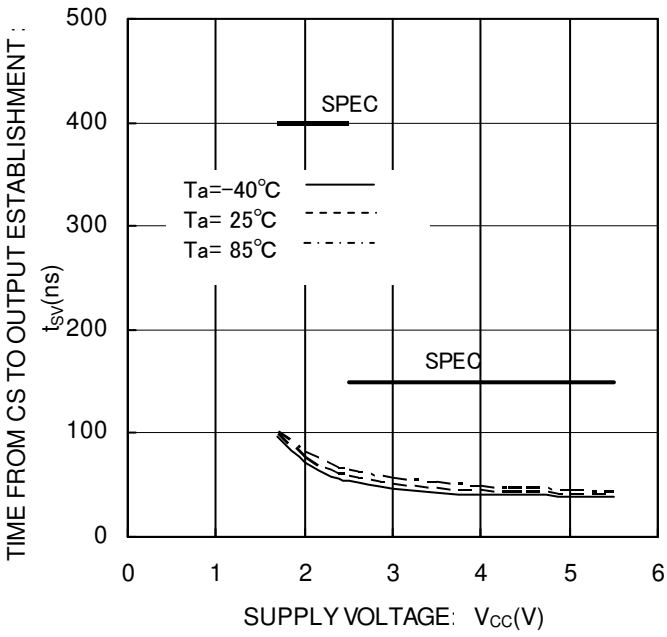


Figure 31. Time from CS to Output establishment vs Supply Voltage

Typical Performance Curves - Continued

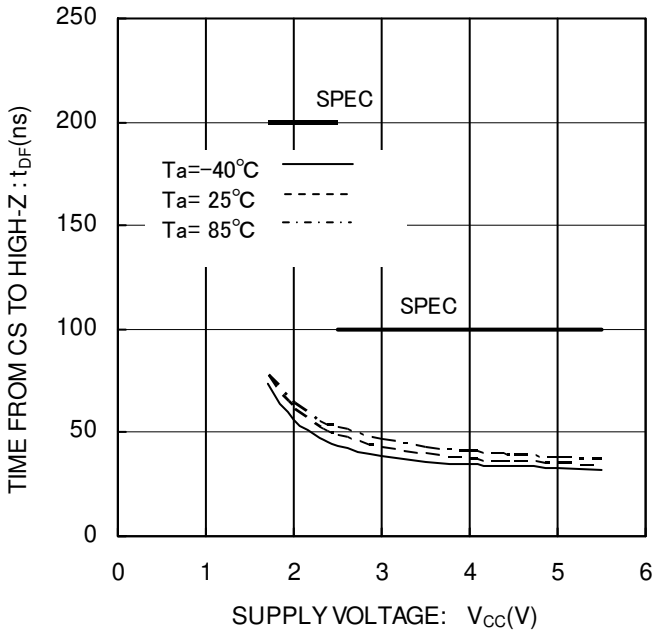


Figure 32. Time from CS to High-Z vs Supply Voltage

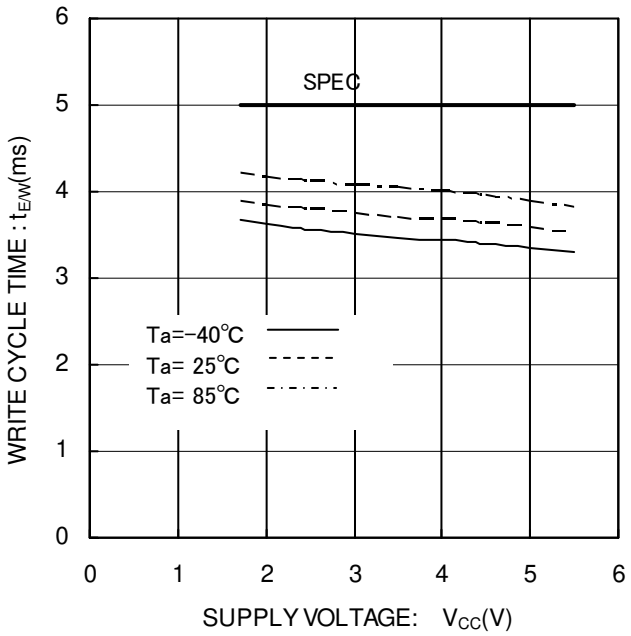
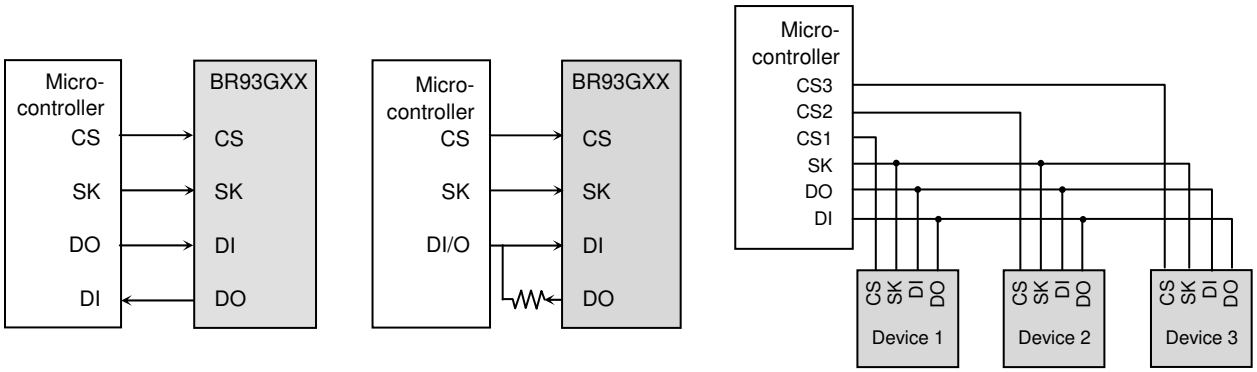


Figure 33. Write Cycle Time vs Supply Voltage

Description of Operations

Communications of the MicroWire BUS are carried out by SK (serial clock), DI (serial data input),DO (serial data output) ,and CS (chip select) for device selection.
When connecting one EEPROM to a microcontroller, connect it as shown in Figure 34(a) or Figure 34(b). And when using the input and output common I/O port of the microcontroller, connect DI and DO of EEPROM via a resistor as shown in Figure 34(b) (Refer to pages 21, 22.), wherein connection by 3 lines is possible.

In the case of connecting multiple EEPROM devices, refer to Figure 34 (c).



(a). Connection by 4 lines (b). Connection by 3 lines (c). Connection Example of Multiple Devices

Figure 34. Connection Method with Microcontroller

Communications on MicroWire BUS is started by the first “1” input after the rise of CS. This input is called the “Start Bit”. After the start bit, the Ope code, address and data are then inputted sequentially. Address and data are all inputted with MSB first.
“0” inputs from the rise of CS to the start bit input are all ignored. Therefore, when there is limitation in the bit width of PIO of the microcontroller, input “0” before the start bit input, to control the bit width.

Command Mode

Command	Start Bit	Ope Code	Address BR93G66-3 MSB of Address(Am) is A7	Data MSB of Data(Dx) is D15	Required Clocks(n)
Read (READ) (1)	1	10	A7,A6,A5,A4,A3,A2,A1,A0	D15 to D0(READ DATA)	BR93G66-3:n=27
Write Enable (WEN)	1	00	1 1 * * * * * *		BR93G66-3:n=11
Write Disable (WDS)	1	00	0 0 * * * * * *		
Write (WRITE) (2)	1	01	A7,A6,A5,A4,A3,A2,A1,A0	D15 to D0(WRITE DATA)	BR93G66-3:n=27
Write All (WRAL) (2)	1	00	0 1 * * * * * *	D15 to D0(WRITE DATA)	
Erase (ERASE)	1	11	A7,A6,A5,A4,A3,A2,A1,A0		BR93G66-3:n=11
Erase All (ERAL)	1	00	1 0 * * * * * *		

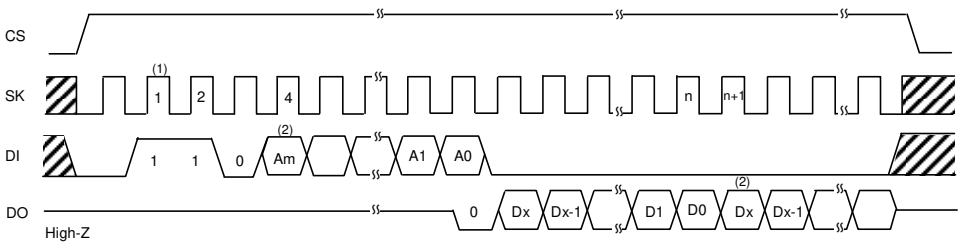
- Input the address and the data in MSB first manners.
- As for *, input either “1” or “0” .

*Start bit
Acceptance of all the commands of this IC starts at recognition of the start bit.
The start bit means the first “1” input after the rise of CS.

(1) As for read, by continuous SK clock input after setting the read command, data output of the set address starts, and address data in significant order are sequentially output continuously. (Auto Increment Function)
(2) For write or write all commands, an internal erase or erase all is included and no separate erase or erase all is needed before write or write all command.

Timing Chart

1. Read Cycle (READ)



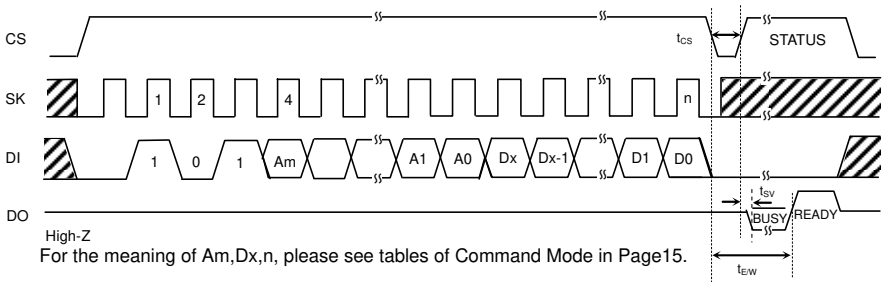
Am: MSB of address
Dx: MSB of data
n: required clocks

(1) Start bit
After the rising edge of CS, the first data "1" input will be recognized as the start bit and the following operation starts. All "0s" preceding the start bit are ignored. This applies to all command that will be discussed later.
(2) For the meaning of Am,Dx,n,please see tables of Command Mode in Page15. For example, Am=A7,Dx=D15,n=27.

Figure 35. Read Cycle

(1) When the READ command is received, data is clocked out to DO synchronously with the rising edge of SK. A "0" (dummy bit) is output first in sync with the address bit A0. Then follows the 16-bit data from the selected address MSB first.
This IC has an Address Auto Increment function that is available only for READ command. After the first 16-bit data has been output to DO and CS is kept High, a continuous SK clock input causes the address to increment automatically and the IC outputs a stream of successive data from consecutive addresses.

2. Write Cycle (WRITE)



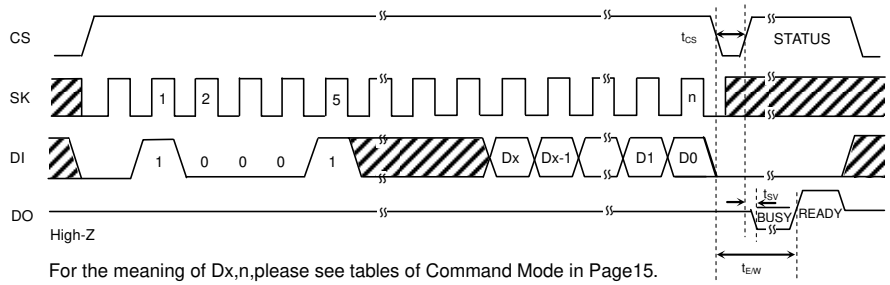
Am: MSB of address
Dx: MSB of data
n: required clocks

For the meaning of Am,Dx,n, please see tables of Command Mode in Page15.

Figure 36. Write Cycle

(1) In this command, input 16bit data are written to designated addresses (Am to A0). The actual write starts by the fall of CS of D0 taken SK clock.
When STATUS is not detected (CS=low fixed),make sure Max 5ms time is in comforming with $t_{E/W}$.
When STATUS is detected (CS=high), all commands are not accepted for areas where low ($\overline{BUSY}$) is output from DO, therefore, do not input any command.

3. Write All Cycle (WRAL)



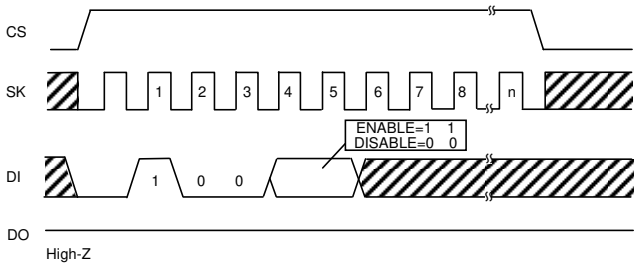
Dx: MSB of data
n: required clocks

For the meaning of Dx,n,please see tables of Command Mode in Page15.

Figure 37. Write All Cycle

(1) In this command, input 16bit data is written simultaneously to all adresses. Data is not written continuously per one word but is written in bulk, the write time is only Max 5ms in conformity with $t_{E/W}$.
In WRAL, STATUS can be detected in the same manner as in WRITE command.

4. Write Enable (WEN) / Disable (WDS) Cycle



n: required clocks

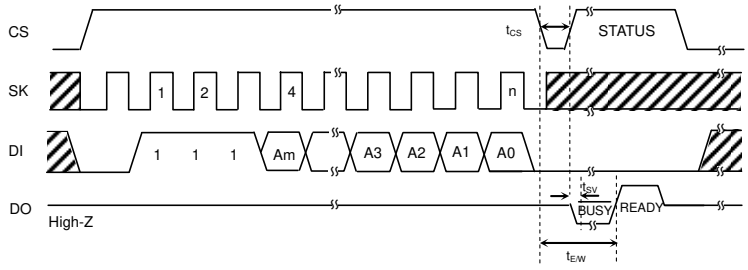
For the meaning of n,please see tables of Command Mode in Page15.

Figure 38. Write Enable (WEN) / Disable (WDS) Cycle

(1) At power on, this IC is in write disable status by the internal RESET circuit. Before executing the write command, it is necessary to execute the write enable command. And, once this command is executed, it is valid unitl the write disable command is executed or the power is turned off. However, the read command is valid irrespective of write enable / diable command. Input to SK after 6 clocks of this command is available by either “1” or “0”, but be sure to input it.

(2) When the write enable command is executed after power on, write enable status gets in. When the write disable command is executed then, the IC gets in write disable status as same as at power on, and then the write command is canceled thereafter in software manner. However, the read command is executable. In write enable status, even when the write command is input by fault, write is started. To prevent such error, it is recommended to execute the write disable command after completion of write.

5. Erase Cycle (ERASE)



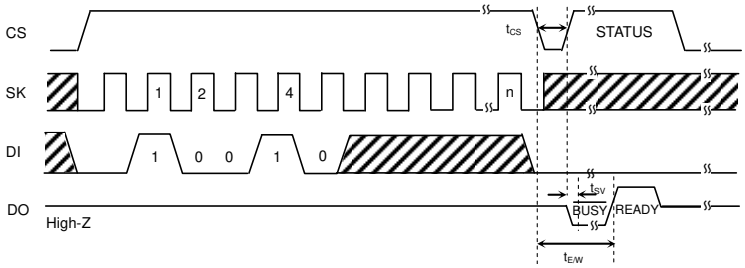
Am: MSB of address
n: required clocks

For the meaning of Am,n,please see tables of Command Mode in Page15.

Figure 39. Erase Cycle

(1) In this command, data of the designated address is made into “1”. The data of the designated address becomes “FFFFh”.
Actual ERASE starts at the fall of CS after the fall of A0 taken SK clock.
In ERASE, STATUS can be detected in the same manner as in WRITE command.

6. Erase All Cycle (ERAL)



n: required clocks

For the meaning of n,please see tables of Command Mode in Page15.

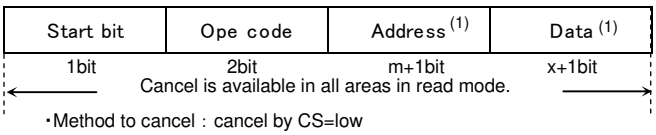
Figure 40. Erase All Cycle

(1) In this command, data of all addresses is made into “1”. Data of all addresses becomes ”FFFFh”.
Actual ERASE starts at the fall of CS after the falll of the n-th clock from the start bit input.
In ERAL, STATUS can be detected in the same manner as in WRAL command.

Application

1. Method to cancel each command

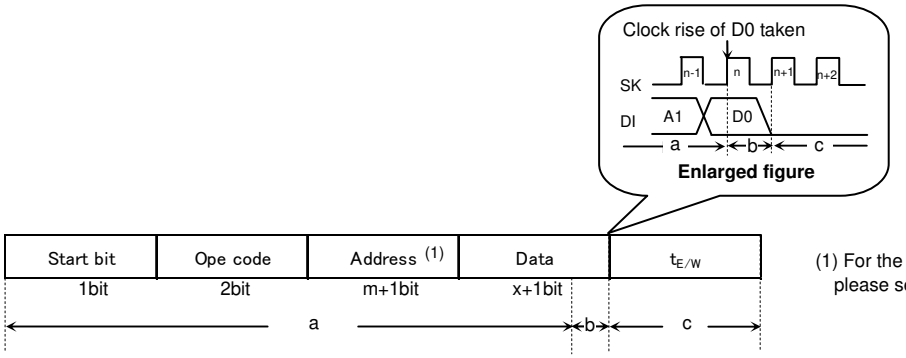
(1) READ



(1) For the meaning of m,x, please see tables of command mode in Page15

Figure 41. READ Cancel Available Timing

(2) WRITE,WRAL



(1) For the meaning of m,n,x, please see tables of Command Mode in Page15

a : From start bit to the clock rise of D0 taken
Cancel by CS=low

b : When taken after the clock rise of D0.
Cancellation will be no longer possible.

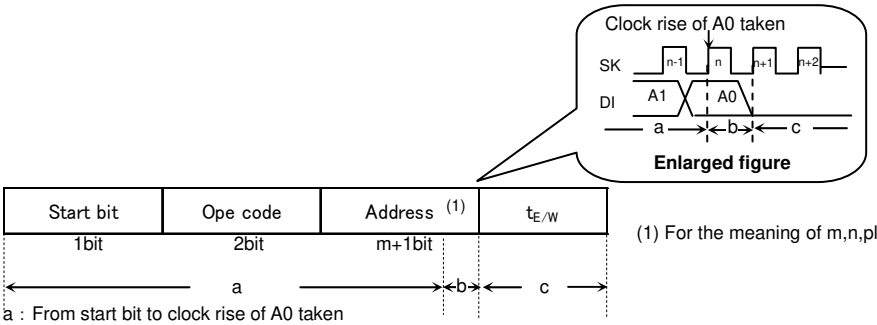
c : n+1 clock rise and after
Cancel by CS=low
However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is output continuously cancel function is not available.

Note 1) If Vcc is turned OFF in this area, designated address data is not guaranteed, therefore, it is recommended to execute WRITE once again.

Note 2) If CS is started at the same timing as that of the SK rise, write execution/cancel becomes uncertain. Therefore, it is recommended to set CS to low in SK=low area.
As for SK rise, recommended timing is t_{CSS}/t_{CSH} or higher.

Figure 42. WRITE, WRAL Cancel Available Timing

(3) ERASE, ERAL



(1) For the meaning of m,n,please see tables of Command Mode in Page15

a : From start bit to clock rise of A0 taken
Cancel by CS=low

b : Clock rise of A0 taken
Cancellation will be no longer possible.

c : n+1 clock rise and after
Cancel by CS=low
However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is output continuously cancel function is not available.

Note 1) If Vcc is turned OFF in this area, designated address data is not guaranteed, therefore, it is recommended to execute WRITE once again.

Note 2) If CS is started at the same timing as that of the SK rise, write execution/cancel becomes unstable, therefore, it is recommended to fall in SK=low area.
As for SK rise, recommended timing is t_{CSS}/t_{CSH} or higher.

Figure 43. ERASE, ERAL Cancel Available Timing

2. At Standby

When CS is low , even if SK, DI, DO are low, high or with middle electric potential, current does not exceed I_{SB1} Max.

3. I/O Peripheral Circuit

(1) Pull Down CS.

By making CS=low at power ON/OFF, wrong operation and write error are prevented.

(a) Pull Down Resistance R_{CS} of CS pin

To prevent wrong operation and write error at power ON/OFF, CS pull down resistor is necessary. Select an appropriate resistor value from microcontroller V_{OH}, I_{OH}, and V_{IL} characteristics of this IC.

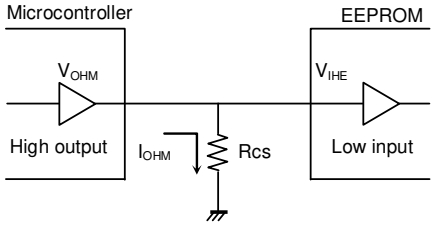


Figure 44. CS Pull Down Resistance

$$Rcs \geqq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ①$$

$$V_{OHM} \geqq V_{IHE} \quad \cdots ②$$

Example) When V_{CC} =5V, V_{IHE}=2V, V_{OHM}=2.4V, I_{OHM}=2mA, from the equation ①,

$$Rcs \geqq \frac{2.4}{2 \times 10^{-3}}$$

$$\therefore \quad Rcs \geqq 1.2\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, V_{OHM} becomes 2.4V or higher, and V_{IHE} (=2.0V), the equation ② is also satisfied.

- V_{IHE} : EEPROM VIH specifications
- V_{OHM} : Microcontroller V_{OH} specifications
- I_{OHM} : Microcontroller I_{OH} specifications

(2) DO is available in both pull up and pull down.

DO output always is High-Z except in READY / BUSY STATUS and data output in read command.
When malfunction occurs at High-Z input of the microcontroller port connected to DO, it is necessary to pull down and pull up DO. When there is no influence upon the microcontroller operations, DO may be left OPEN.
If DO is OPEN during transition of output from BUSY to READY status, and at an instance where CS=high, SK=high, DI=high, EEPROM recognizes this as a start bit, resets READY output, and sets DO=High-Z. Therefore, READY signal cannot be detected. To avoid such output, pull up DO pin for improvement.

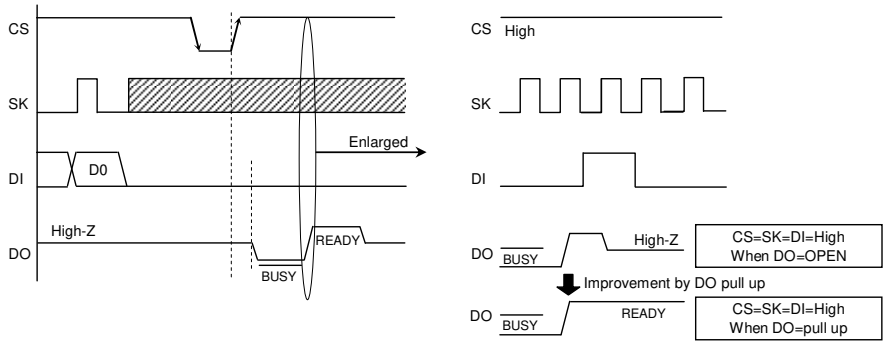


Figure 45. READY Output Timing at DO=OPEN

(a) Pull Up Resistance R_{PU} and Pull Down Resistance R_{PD} of DO pin
As for pull up and pull down resistance value, select an appropriate resistor value from microcontroller V_{IH}, V_{IL}, and V_{OH}, I_{OH}, V_{OL}, I_{OL} characteristics of this IC.

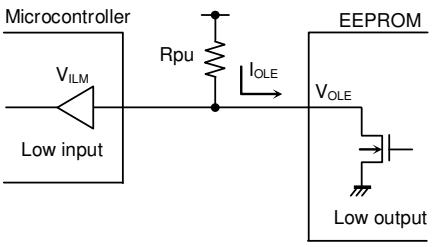


Figure 46. DO Pull Up Resistance

$$Rpu \geqq \frac{V_{CC}-V_{OLE}}{I_{OLE}} \quad \cdot\cdot\cdot ③$$

$$V_{OLE} \leqq V_{ILM} \quad \cdot\cdot\cdot ④$$

Example) When V_{CC} =5V, V_{OLE}=0.4V, I_{OLE}=2.1mA, V_{ILM}=0.8V, from the equation ③,

$$Rpu \geqq \frac{5-0.4}{2.1\times10^{-3}}$$

$$\therefore \quad Rpu \geqq 2.2\ [k\Omega]$$

With the value of Rpu to satisfy the above equation, V_{OLE} becomes 0.4V or below, and with V_{ILM}(=0.8V), the equation ④ is also satisfied.

- V_{OLE} : EEPROM V_{OL} specifications
- I_{OLE} : EEPROM I_{OL} specifications
- V_{ILM} : Microcontroller V_{IL} specifications

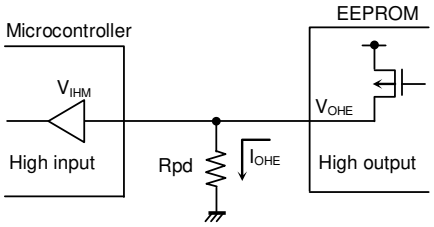


Figure 47. DO Pull Down Resistance

$$Rpd \geqq \frac{V_{OHE}}{I_{OHE}} \quad \cdot\cdot\cdot ⑤$$

$$V_{OHE} \geqq V_{IHM} \quad \cdot\cdot\cdot ⑥$$

Example) When V_{CC} =5V, $V_{OHE}=V_{CC}-0.2V$, I_{OHE}=0.1mA, $V_{IHM}=V_{CC}\times0.7V$ from the equation ⑤,

$$Rpd \geqq \frac{5-0.2}{0.1\times10^{-3}}$$

$$\therefore \quad Rpd \geqq 48\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, V_{OHE} becomes 2.4V or below, and with V_{IHM} (=3.5V), the equation ⑥ is also satisfied.

- V_{OHE} : EEPROM V_{OH} specifications
- I_{OHE} : EEPROM I_{OH} specifications
- V_{IHM} : Microcontroller V_{IH} specifications

(b) READY / $\overline{\text{BUSY}}$ STATUS Display (DO terminal)
This display outputs the internal STATUS signal. When CS is started after t_{CS} from CS fall after write command input, high or low is output.

R/$\overline{\text{B}}$ display=low ($\overline{\text{BUSY}}$) = write under execution
(DO STATUS)
After the timer circuit in the IC works and creates the period of $t_{E/W}$, this timer circuit completes automatically.
And the memory cell is written in the period of $t_{E/W}$, and during this period, other command is not accepted.

R/$\overline{\text{B}}$ display = high (READY) = command wait STATUS
(DO STATUS)
After $t_{E/W}$ (Max5ms) the following command is accepted.
Therefore, CS=high in the period of $t_{E/W}$, and If signals are input in SK, DI, malfunction may occur, therefore, DI=low in the area
CS=high. (Especially, in the case of shared input port, attention is required.)

*Do not input any command while STATUS signal is active. Command input in $\overline{\text{BUSY}}$ area is cancelled, but command input in READY area is accepted. Therefore, STATUS READY output is cancelled, and malfunction and write error may occur.

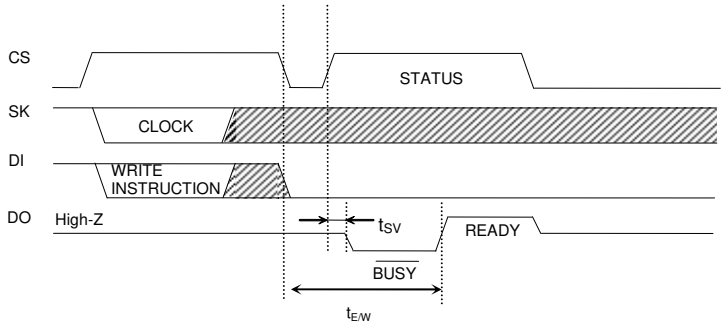


Figure 48. READY/$\overline{\text{BUSY}}$ STATUS Output Timing Chart

4. When to directly connect DI and DO

This IC has independent input terminal DI and output terminal DO, wherein signals are handled separately on timing chart. But, by inserting a resistance R between these DI and DO terminals, it is possible to carry out control by a single control line.

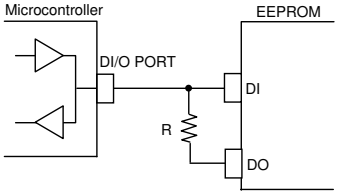


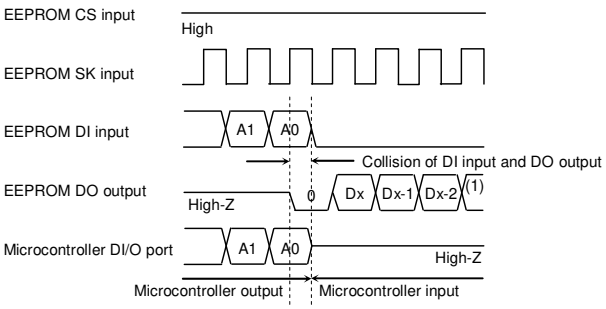
Figure 49. DI, DO Control Line Common Connection

Data collision of microcontroller DI/O output and DO output and feedback of DO output to DI input of EEPROM.
Drive from the microcontroller DI/O output to DI input of EEPROM on I/O timing, and output signal from DO output of EEPROM occur at the same time in the following points.

(1) 1 clock cycle to take in A0 address data at read command

Dummy bit "0" is output to DO terminal.

→When address data A0 = "1" input, through current route occurs.



(1) X=15,for the meaning of x ,
please see tables of command mode in Page15.

Figure 50. Collision Timing at Read Data Output at DI, DO Direct Connection

(2) Timing of CS = high after write command. DO terminal in READY / $\overline{\text{BUSY}}$ function output.

When the next start bit input is recognized, High-Z gets in.

→Especially, at command input after write, when CS input is started with microcontroller DI/O output low, READY output high is output from DO terminal, and through current route occurs.

Feedback input at timing of these (1) and (2) does not cause disorder in basic operations, if resistance R is inserted.

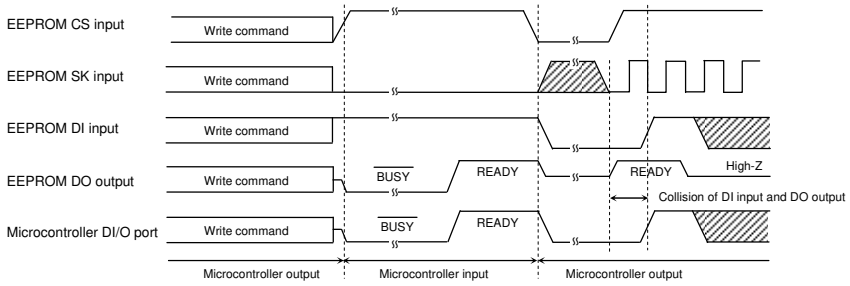


Figure 51. Collision Timing at DI, DO Direct Connection

Note) As for the case (2), attention must be paid to the following.

When STATUS READY is active, DO and DI are shared, DI=high and the microcontroller DI/O=High-Z or the microcontroller DI/O=high,if SK clock is input, DO output is input to DI and is recognized as a start bit, and malfunction may occur. As a method to avoid malfunction, at STATUS READY output, set SK=low, or start CS within 4 clocks after high of READY signal is output.

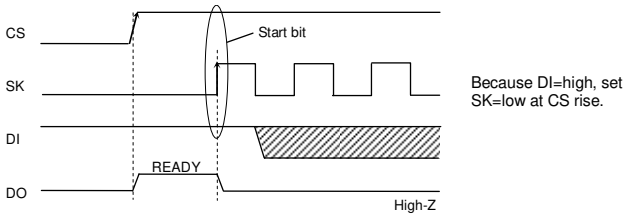


Figure.52 Start bit input timing at DI, DO direct connection

Selection of resistance value R

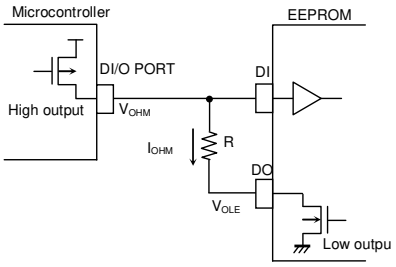
The resistance R becomes a short-circuit current limiting resistance during signal conflicts and it does not affect the basic operations of the device. When short-circuit current flows, glitches in the power source lines may be produced. Determine the maximum transient current in the power lines wherein glitches are not produced. Select the value of resistance R that will satisfy the EEPROM input level V_{IH}/V_{IL}, even under the influence of voltage fluctuations resulting from short-circuit current and so forth. Assuming the allowable short-circuit current defined as I, the following relation should be satisfied.

(3) Address Data A0 = "1" Input, Dummy Bit "0" Output Timing

(When microcontroller DI/O output is high, EEPROM DO outputs low, and high is input to DI)

(a) Make the through current to EEPROM 10mA or below.

(b) See to it that the level V_{IH} of EEPROM should satisfy the following.



Conditions

$$V_{IHE} \leqq I_{OHM} \times R + V_{OLE}$$

At this moment, if V_{OLE}=0V,

$$V_{IHE} \leqq I_{OHM} \times R$$

$$\therefore \quad R \geqq \frac{V_{IHE}}{I_{OHM}} \quad \cdot\cdot\cdot ⑦$$

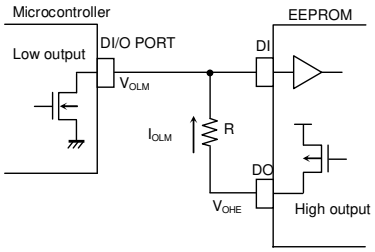
- V_{IHE} : EEPROM V_{IH} specifications
- V_{OLE} : EEPROM V_{OL} specifications
- I_{OHM} : Microcontroller I_{OH} specifications

Figure 53. Circuit at DI, DO direct connection (Microcontroller DI/O high output, EEPROM low output)

(4) DO STATUS READY Output Timing

(When the microcontroller DI/O is low, EEPROM DO output high, and low is input to DI)

(a) Set the EEPROM input level V_{IL} so as to satisfy the following.



Conditions

$$V_{ILE} \geqq V_{OHE} - I_{OLM} \times R$$

As this moment, $V_{OHE}=V_{CC}$

$$V_{ILE} \geqq V_{CC} - I_{OLM} \times R$$

$$\therefore \quad R \geqq \frac{V_{CC} - V_{ILE}}{I_{OLM}} \quad \cdot\cdot\cdot ⑧$$

- V_{ILE} : EEPROM V_{IL} specifications
- V_{OHE} : EEPROM V_{OH} specifications
- I_{OLM} : Microcontroller I_{OL} specifications

Example) When V_{CC}=5V, V_{OHM}=5V, I_{OHM}=0.4mA, V_{OLM}=5V, I_{OLM}=0.4mA,

From the equation ⑦,

$$R \geqq \frac{V_{IHE}}{I_{OHM}}$$

$$R \geqq \frac{3.5}{0.4 \times 10^{-3}}$$

$$\therefore \quad R \geqq 8.75\ [k\Omega] \quad \cdot\cdot\cdot ⑨$$

From the equation⑧,

$$R \geqq \frac{V_{CC} - V_{ILE}}{I_{OLM}}$$

$$R \geqq \frac{5 - 1.5}{2.1 \times 10^{-3}}$$

$$\therefore \quad R \geqq 1.67\ [k\Omega] \quad \cdot\cdot\cdot ⑩$$

Therefore, from the equations ⑨ and ⑩,

$$\therefore \quad R \geqq 8.75\ [k\Omega]$$

Figure 54. Circuit at DI, DO Direct Connection (Microcontroller DI/O low output, EEPROM high output)

5. I/O Equivalence Circuit

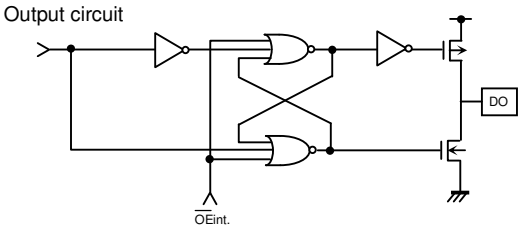


Figure 55. Output Circuit (DO)

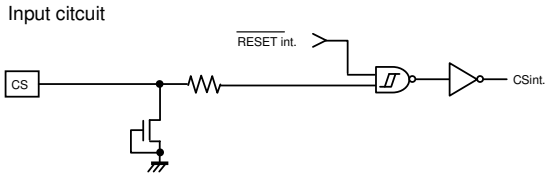


Figure 56. Input Circuit (CS)

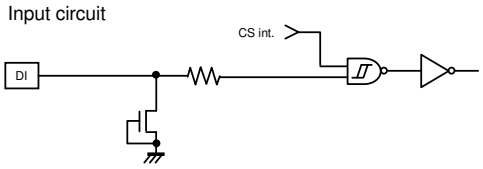


Figure 57. Input Circuit (DI)

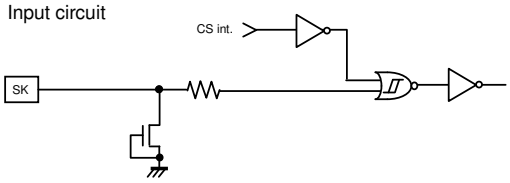


Figure 58. Input Circuit (SK)

6. Power-Up/Down Conditions

(1) At Power ON/OFF, set CS low.

When CS is high, this IC gets in input accept status (active). At power ON, set CS low to prevent malfunction and write error from noise (When CS is in low status, all inputs are cancelled.). At power decline, low power status may prevail. Therefore, at power OFF, set CS low to prevent malfunction from noise.

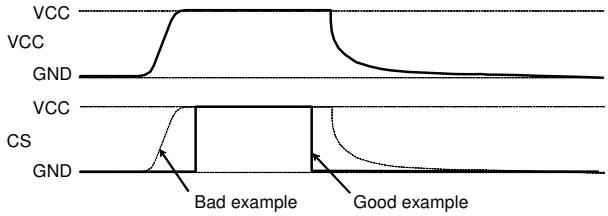


Figure 59. Timing at Power ON/OFF

（Bad example）CS pin is pulled up to V_{CC}

When IC is turned ON while CS is high, EEPROM malfunction write error may occur due to noise and the likes.

It's also possible to happen even when CS input is High-Z.

（Good example）It is low at power ON/OFF.

Set 10ms or higher to recharge at power OFF.

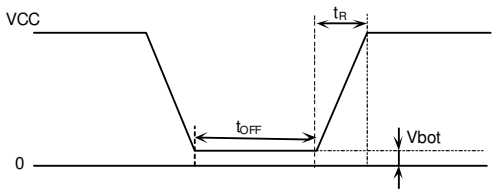
When power is turned on without observing this condition, IC internal circuit may not be reset, so please note.

(2) POR Circuit

This IC has a POR (Power On Reset) circuit as a write error countermeasure. After POR operation, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is high at power ON/OFF, it may become write enable status owing to noises and the likes. For secure operations, observe the follwing conditions.

(a) Set CS=low

(b) Turn on power so as to satisfy the recommended conditions of t_R, t_{OFF}, Vbot for POR circuit operation.



Recommended conditions of t_R, t_{OFF}, Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Figure 60. Rise Waveform Diagram

(3) LVCC Circuit

LVCC (V_{CC}-Lockout) circuit prevents data rewrite operation at low power, and prevents wrong write.

At LVCC voltage (Typ=1.2V) or below, it prevents data rewrite

7. Noise Countermeasures

(1) VCC Noise (Bypass Capacitor)

When noise or surge gets in the power source line, malfunction may occur. Therefore, in removing these, it is recommended to connect a bypass capacitor (0.1μF) between IC VCC and GND, At that moment, connect the capacitor as close to IC as possible. And, it is also recommended to connect a bypass capacitor between board's VCC and GND.

(2) SK Noise

When the rise time of SK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time of SK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

Operational Notes

1. Described numeric values and data are design representative values only, and the values are not guaranteed.

2. We believe that application circuit examples are recommendable. However, in actual use, confirm characteristics further sufficiently. If changing the fixed number of external parts is desired, make your decision with sufficient margin in consideration of static characteristics, transient characteristics, and fluctuations of external parts and our IC.

3. Absolute maximum ratings
   If the absolute maximum ratings such as supply voltage and operating temperature and so forth are exceeded, LSI may be destroyed. Do not supply voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be supplied to LSI.

4. GND electric potential
   Set the voltage of GND terminal lowest at any operating condition. Make sure that each terminal voltage is not lower than that of GND terminal at any time, even during transient condition.

5. Thermal design
   Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.

6. Short between pins and mounting errors
   Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

7. Operating the IC in the presence of strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.