Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Serial EEPROM series Standard EEPROM
MicroWire BUS EEPROM (3-Wire)

BR93G86-3A

●General Description

BR93G86-3A is serial EEPROM of serial 3-line Interface method.
They are 16bit organization and CS PIN is the first PIN in their PIN configuration.

●Features

- 3-line communications of chip select, serial clock, serial data input / output (the case where input and output are shared)
- Operations available at high speed 3MHz clock (4.5 V~5.5 V)
- High speed write available (write time 5ms max.)
- Same package and pin configuration from 1Kbit to 16Kbit
- 1.7~5.5V single power source operation
- Address auto increment function at read operation
- Write mistake prevention function
  - » Write prohibition at power on
  - » Write prohibition by command code
  - » Write mistake prevention function at low voltage
- Self-timed programming cycle
- Program condition display by READY / $\overline{\text{BUSY}}$
- Compact package
  SOP8/SOP-J8/SSOP-B8/TSSOP-B8/MSOP8/
  TSSOP-B8J/DIP-T8/VSON008X2030
- More than 40 years data retention
- More than 1 million write cycles
- Initial delivery state all addresses FFFFh

●Packages W(Typ.) x D(Typ.)x H(Max.)


DIP-T8
9.30mm x 6.50mm x 7.10mm


TSSOP-B8
3.00mm x 6.40mm x 1.20mm


SOP8
5.00mm x 6.20mm x 1.71mm


TSSOP-B8J
3.00mm x 4.90mm x 1.10mm


SOP- J8
4.90mm x 6.00mm x 1.65mm


MSOP8
2.90mm x 4.00mm x 0.90mm


SSOP-B8
3.00mm x 6.40mm x 1.35mm


VSON008X2030
2.00mm x 3.00mm x 0.60mm

●BR93G86-3A

*1 DIP-T8 is not halogen free package

Capacity	Bit Format	Type	Power Source Voltage	Package
16Kbit	1024×16	BR93G86-3A	1.7V to 5.5V	DIP-T8
		BR93G86F-3A		SOP8
		BR93G86FJ-3A		SOP-J8
		BR93G86FV-3A		SSOP-B8
		BR93G86FVT-3A		TSSOP-B8
		BR93G86FVJ-3A		TSSOP-B8J
		BR93G86FVM-3A		MSOP8
		BR93G86NUX-3A		VSON008X2030

●**Absolute Maximum Ratings**

Parameter	Symbol	Ratings	Unit	Remarks
Supply voltage	VCC	-0.3 to +6.5	V	
Permissible dissipation	Pd	0.80 (DIP-T8)	W	When using at Ta=25℃ or higher 8.0mW to be reduced per 1℃.
		0.45 (SOP8)		When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃.
		0.45 (SOP-J8)		When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃.
		0.30 (SSOP-B8)		When using at Ta=25℃ or higher 3.0mW to be reduced per 1℃.
		0.33 (TSSOP-B8)		When using at Ta=25℃ or higher 3.3mW to be reduced per 1℃.
		0.31 (TSSOP-B8J)		When using at Ta=25℃ or higher 3.1mW to be reduced per 1℃.
		0.31 (MSOP8)		When using at Ta=25℃ or higher 3.1mW to be reduced per 1℃.
		0.30 (VSON008X2030)		When using at Ta=25℃ or higher 3.0mW to be reduced per 1℃.
Storage temperature	Tstg	−65 to +150	℃	
Operating temperature	Topr	−40 to +85	℃	
Input voltage/ Output voltage	-	-0.3 to Vcc+1.0	V	The Max value of Input voltage/Output voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of Input voltage/Output voltage is not under -0.8V.
Junction temperature	Tjmax	150	℃	Junction temperature at the storage condition

●**Memory cell characteristics (VCC=1.7~5.5V)**

Parameter	Limit			Unit	Condition
	Min.	Typ.	Max.		
Write cycles *1	1,000,000	-	-	Times	Ta=25℃
Data retention *1	40	-	-	Years	Ta=25℃

○Shipment data all address FFFFh
*1 Not 100% TESTED

●**Recommended Operation Ratings**

Parameter	Symbol	Limits	Unit
Supply voltage	VCC	1.7~5.5	V
Input voltage	V_{IN}	0~VCC	

●**DC characteristics** (Unless otherwise specified, VCC=1.7~5.5V, Ta=-40~+85℃)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Input low voltage	V_{IL}	-0.3[*1]	-	0.3VCC	V	1.7V≦VCC≦5.5V
Input high voltage	V_{IH}	0.7VCC	-	VCC+1.0	V	1.7V≦VCC≦5.5V
Output low voltage 1	V_{OL1}	0	-	0.4	V	I_{OL}=2.1mA, 2.7V≦VCC≦5.5V
Output low voltage 2	V_{OL2}	0	-	0.2	V	I_{OL}=100μA
Output high voltage 1	V_{OH1}	2.4	-	VCC	V	I_{OH}=-0.4mA, 2.7V≦VCC≦5.5V
Output high voltage 2	V_{OH2}	VCC-0.2	-	VCC	V	I_{OH}=-100μA
Input leakage current1	I_{LI1}	-1	-	+1	μA	V_{IN}=0V~VCC(CS,SK,DI)
Output leakage current	I_{LO}	-1	-	+1	μA	V_{OUT}=0V~VCC, CS=0V
Supply current	I_{CC1}	-	-	1.0	mA	VCC=1.7V, f_{SK}=1MHz, $t_{E/W}$=5ms (WRITE)
		-	-	2.0	mA	VCC=5.5V ,f_{SK}=3MHz, $t_{E/W}$=5ms (WRITE)
	I_{CC2}	-	-	0.5	mA	f_{SK}=1MHz (READ)
		-	-	1.0	mA	f_{SK}=3MHz (READ)
	I_{CC3}	-	-	2.0	mA	VCC=2.5V, f_{SK}=1MHz $t_{E/W}$=5ms (WRAL, ERAL)
		-	-	3.0	mA	VCC=5.5V ,f_{SK}=3MHz $t_{E/W}$=5ms (WRAL, ERAL)
Standby current	I_{SB1}	-	-	2.0	μA	CS=0V

*1 When the pulse width is 50ns or less, the Min value of V_{IL} is admissible to -0.8V.

●**AC characteristics** (Unless otherwise specified, VCC=1.7~2.5V, Ta=-40~+85℃)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SK frequency	f_{SK}	-	-	1	MHz
SK high time	t_{SKH}	250	-	-	ns
SK low time	t_{SKL}	250	-	-	ns
CS low time	t_{CS}	250	-	-	ns
CS setup time	t_{CSS}	200	-	-	ns
DI setup time	t_{DIS}	100	-	-	ns
CS hold time	t_{CSH}	0	-	-	ns
DI hold time	t_{DIH}	100	-	-	ns
Data “1” output delay	t_{PD1}	-	-	400	ns
Data “0” output delay	t_{PD0}	-	-	400	ns
Time from CS to output establishment	t_{SV}	-	-	400	ns
Time from CS to High-Z	t_{DF}	-	-	200	ns
Write cycle time	$t_{E/W}$	-	-	5	ms

(Unless otherwise specified, VCC=2.5~4.5V, Ta=-40~+85℃)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SK frequency	f_{SK}	-	-	2	MHz
SK high time	t_{SKH}	230	-	-	ns
SK low time	t_{SKL}	200	-	-	ns
CS low time	t_{CS}	200	-	-	ns
CS setup time	t_{CSS}	50	-	-	ns
DI setup time	t_{DIS}	100	-	-	ns
CS hold time	t_{CSH}	0	-	-	ns
DI hold time	t_{DIH}	100		-	ns
Data “1” output delay	t_{PD1}	-	-	200	ns
Data “0” output delay	t_{PD0}	-	-	200	ns
Time from CS to output establishment	t_{SV}	-	-	150	ns
Time from CS to High-Z	t_{DF}	-	-	100	ns
Write cycle time	$t_{E/W}$	-	-	5	ms

(Unless otherwise specified, VCC=4.5~5.5V, Ta=-40~+85℃)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SK frequency	f_{SK}	-	-	3	MHz
SK high time	t_{SKH}	100	-	-	ns
SK low time	t_{SKL}	100	-	-	ns
CS low time	t_{CS}	200	-	-	ns
CS setup time	t_{CSS}	50	-	-	ns
DI setup time	t_{DIS}	50	-	-	ns
CS hold time	t_{CSH}	0	-	-	ns
DI hold time	t_{DIH}	50	-	-	ns
Data “1” output delay	t_{PD1}	-	-	200	ns
Data “0” output delay	t_{PD0}	-	-	200	ns
Time from CS to output establishment	t_{SV}	-	-	150	ns
Time from CS to High-Z	t_{DF}	-	-	100	ns
Write cycle time	$t_{E/W}$	-	-	5	ms

●**Serial input / output timing**

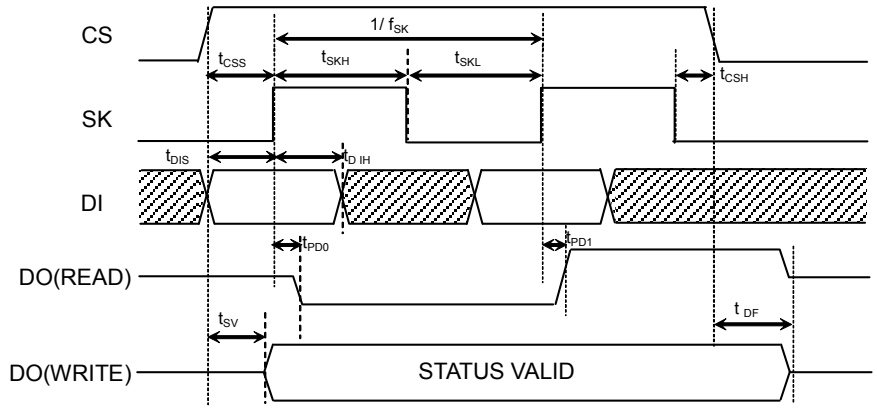


Figure 1. Sync data input / output timing

○Data is taken by DI sync with the rise of SK.
○At read operation, data is output from DO in sync with the rise of SK.
○The STATUS signal at write (READY / BUSY) is output after t_{CS} from the fall of CS after write command input, at the area DO where CS is high, and valid until the next command start bit is input. And, while CS is low, DO becomes High-Z.
○After completion of each mode execution, set CS low once for internal circuit reset, and execute the following operation mode.
○1/f_{SK} is the SK clock cycle, even if f_{SK} is maximum, the SK clock cycle can't be t_{SKH}(Min.)+t_{SKL}(Min.)
○For "Write cycle time $t_{E/W}$", please see Figure 36,37,39,40.
○For "CS low time t_{CS}", please see Figure 36,37,39,40.

●**Block diagram**

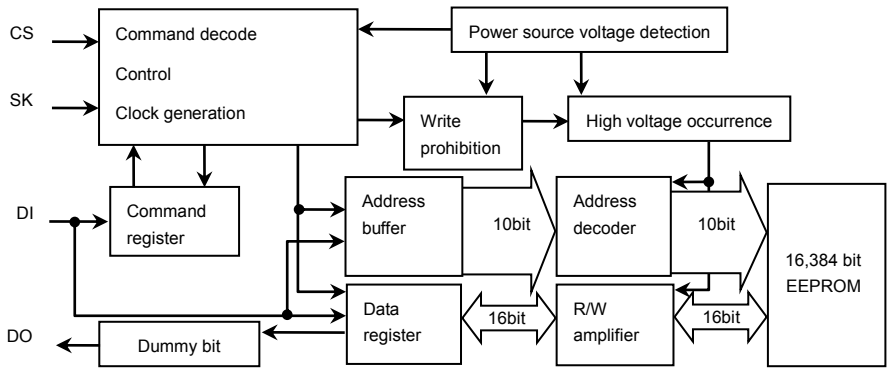


Figure 2. Block diagram

●Pin Configuration

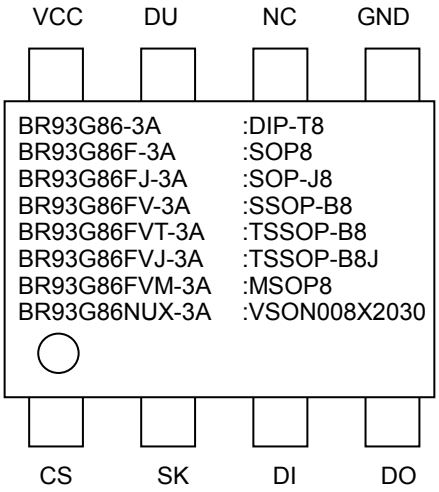


Figure 3. Pin Configuration

●Pin Descriptions

Pin name	I / O	Function
CS	Input	Chip select input
SK	Input	Serial clock input
DI	Input	Start bit, ope code, address, and serial data input
DO	Output	Serial data output, READY / $\overline{\text{BUSY}}$ STATUS display output
GND	-	All input / output reference voltage, 0V
NC	-	Non connected terminal*1
DU	-	Don't use terminal*1
VCC	-	Supply voltage

*1 Terminals not used may be set to any of high,low, and OPEN

●**Typical Performance Curves**

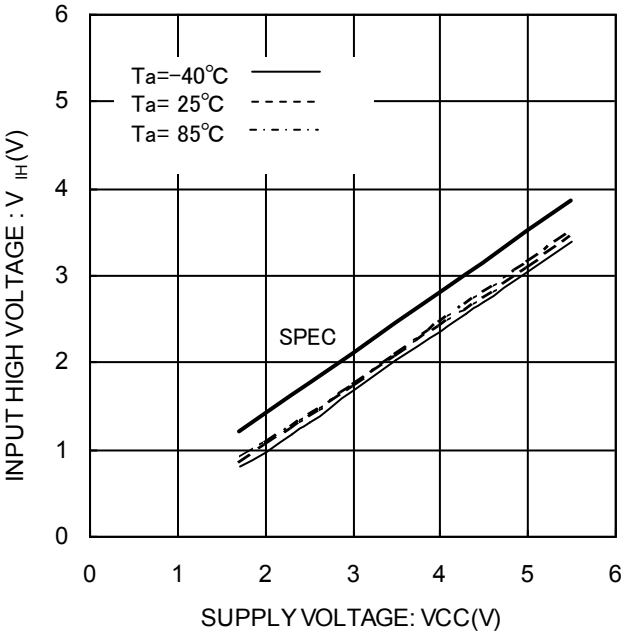


Figure 4. Input high voltage V_{IH}(CS,SK,DI)

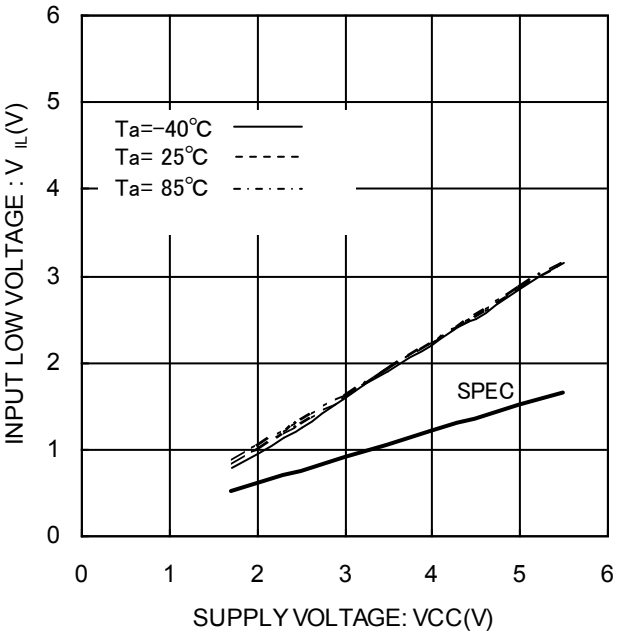


Figure 5. Input low voltage V_{IL}(CS,SK,DI)

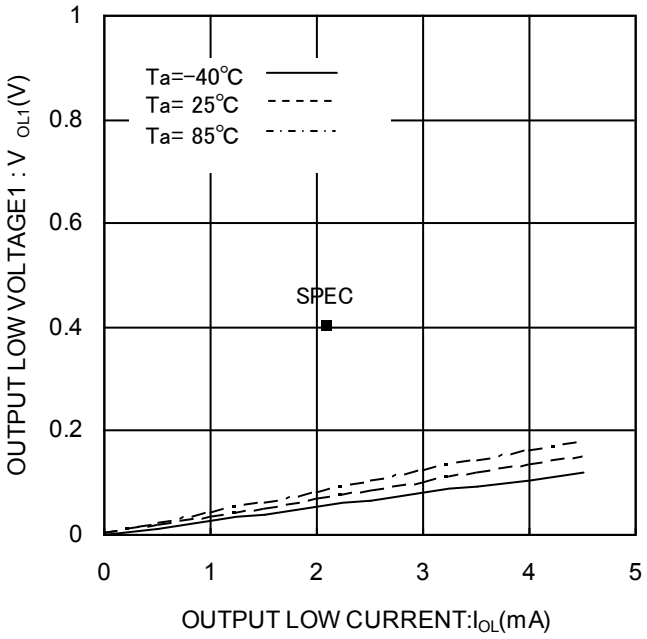


Figure 6. Output low voltage1 V_{OL1}(VCC=2.7V)

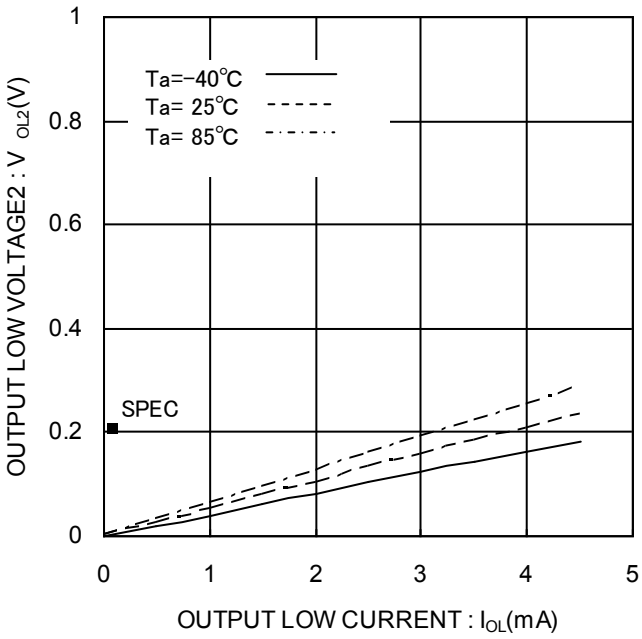


Figure 7. Output low voltage2 V_{OL2}(VCC=1.7V)

●**Typical Performance Curves - Continued**

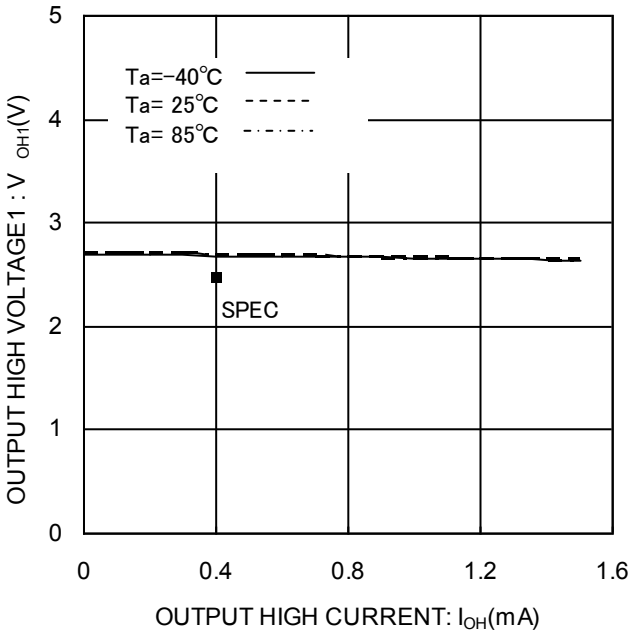


Figure 8. Output high voltage1 V_{OH1}(VCC=2.7V)

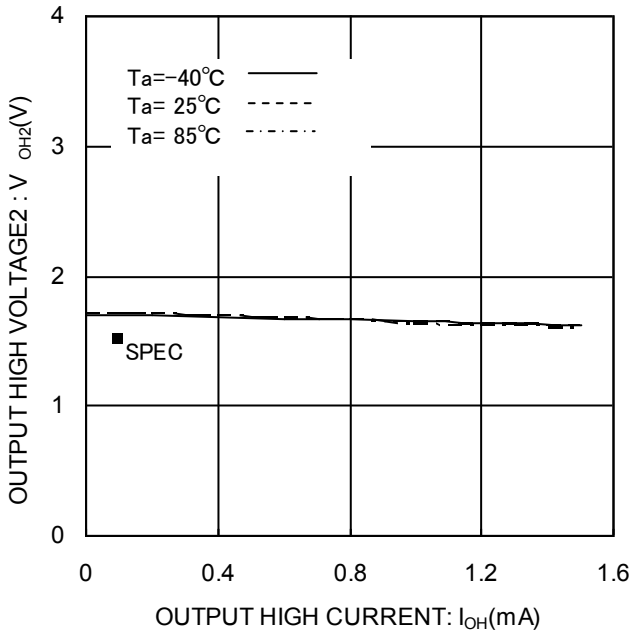


Figure 9. Output high voltage2 V_{OH2}(VCC=1.7V)

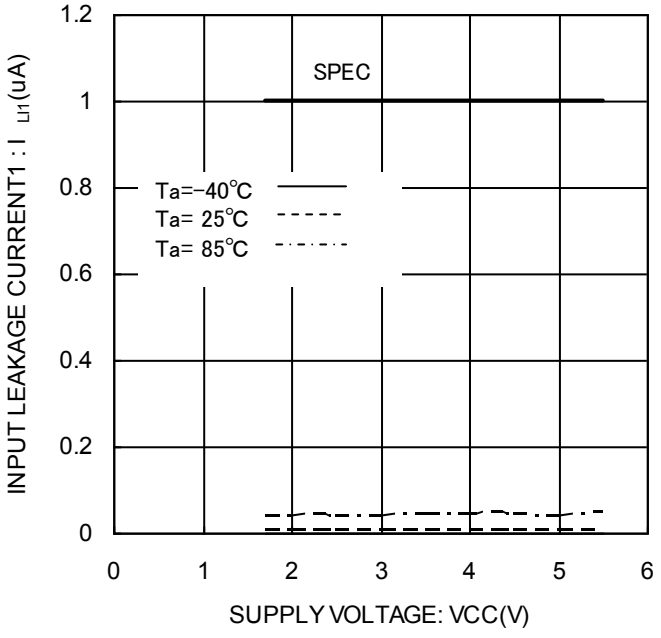


Figure 10. Input leakage current1 I_{LI1} (CS)

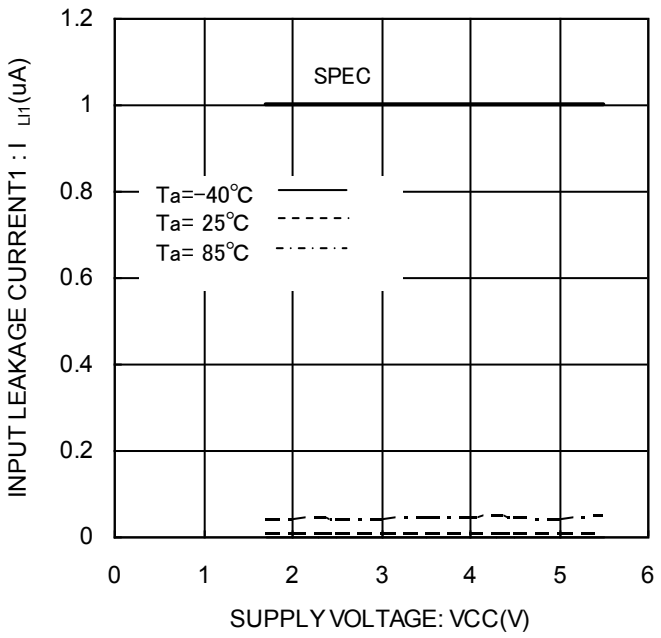


Figure 11. Input leakage current1 I_{LI1}(SK)

●**Typical Performance Curves - Continued**

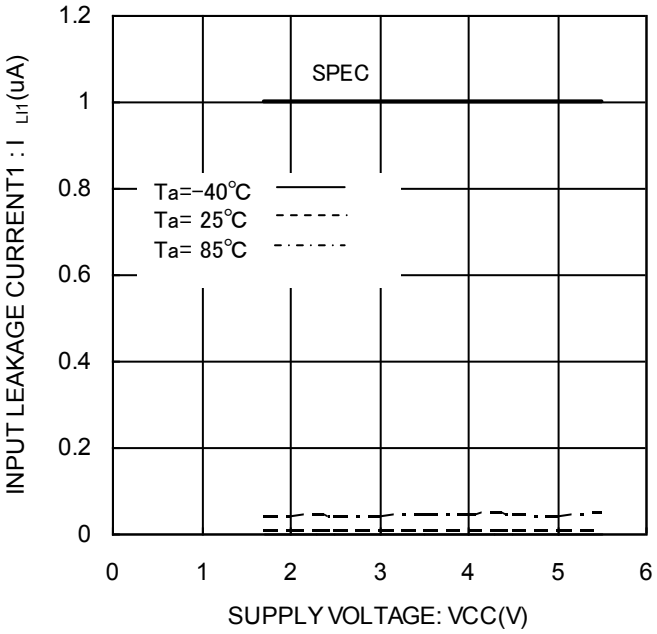


Figure 12. Input leakage current1 I_{LI1}(DI)

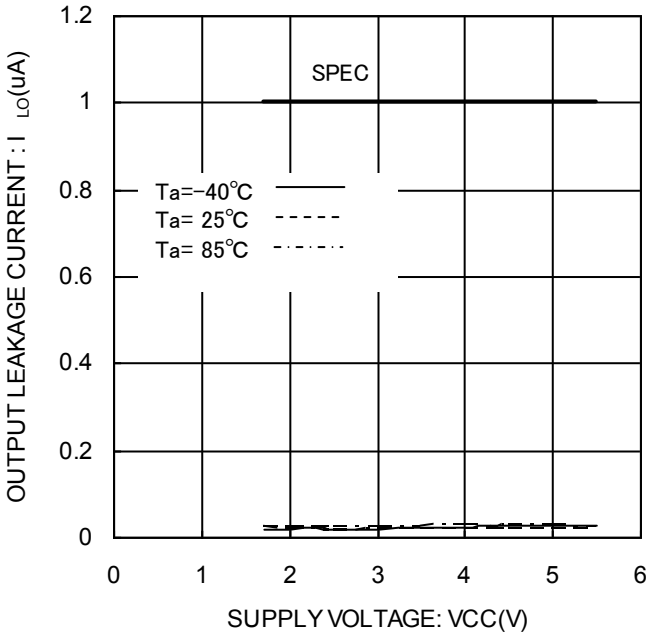


Figure 13. Output leakage current I_{LO}(DO)

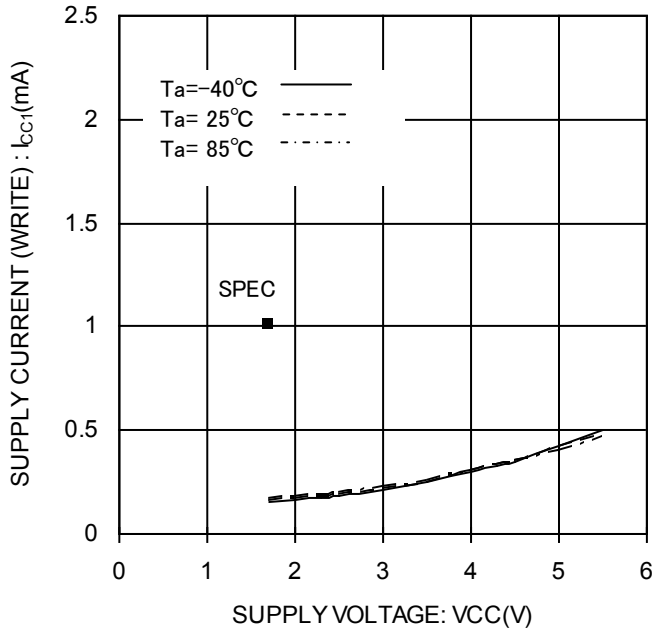


Figure 14. Supply current (WRITE)
I_{CC1}(WRITE, f_{SK}=1MHz)

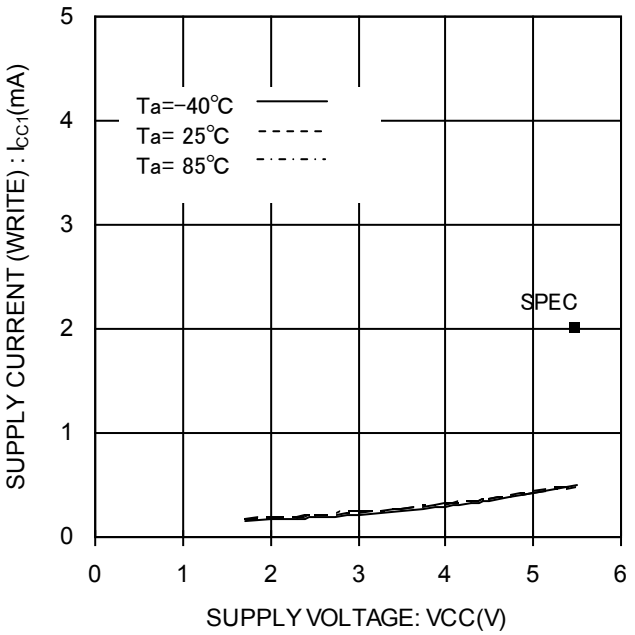


Figure 15. Supply current (WRITE)
I_{CC1}(WRITE,f_{SK}=3MHz)

●**Typical Performance Curves - Continued**

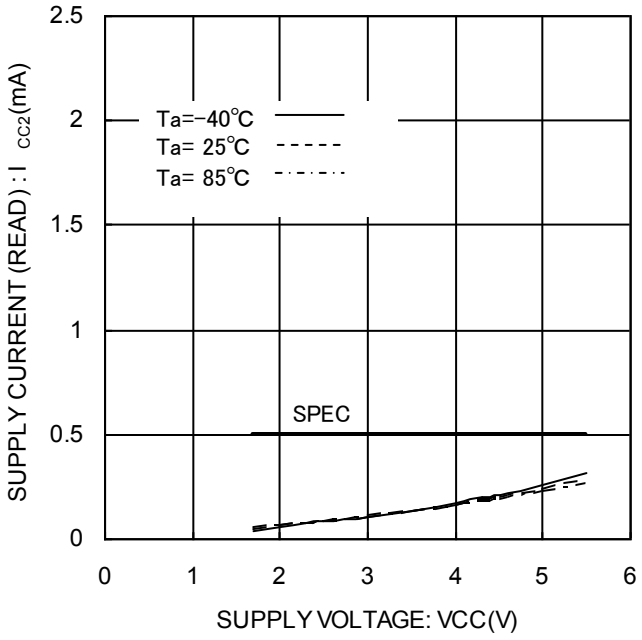


Figure 16 Supply current (READ)
I_{CC2}(READ,f_{SK}=1MHz).

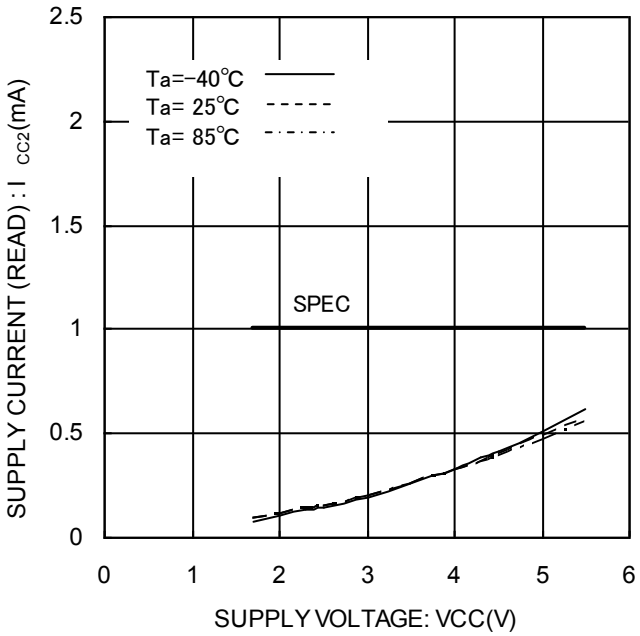


Figure 17. Supply current (READ)
I_{CC2}(READ,f_{SK}=3MHz)

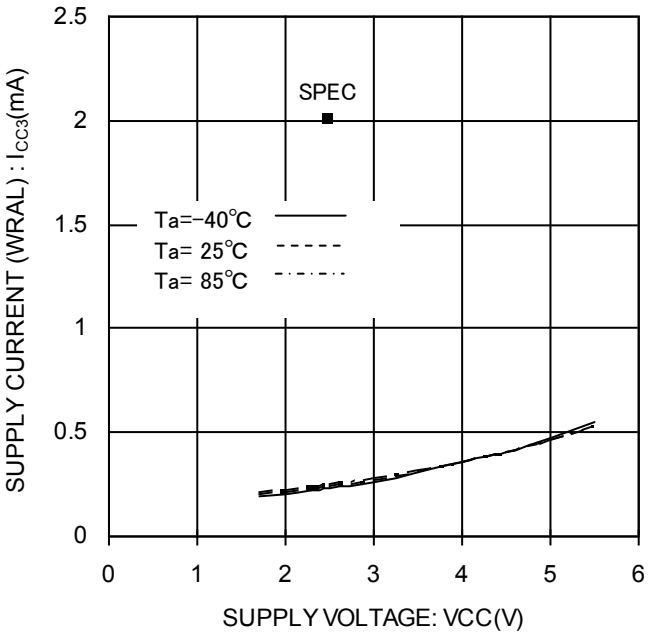


Figure 18. Supply current (WRAL)
I_{CC3}(WRAL,f_{SK}=1MHz)

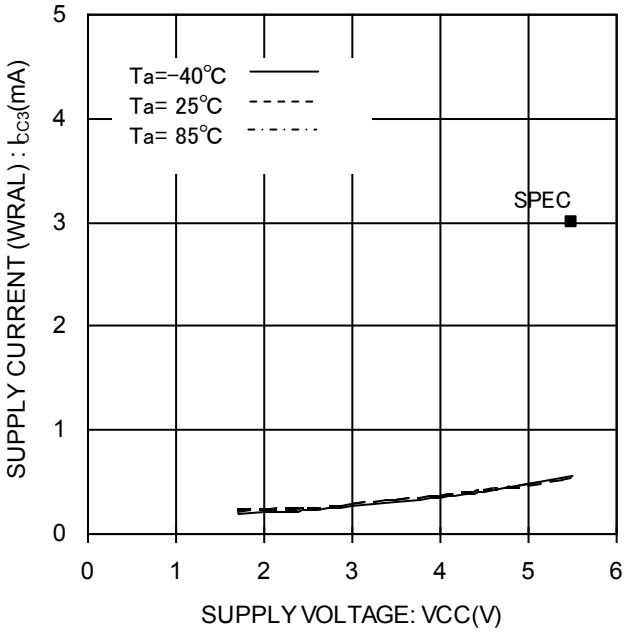


Figure 19. Supply current (WRAL)
I_{CC3}(WRAL,f_{SK}=3MHz)

●**Typical Performance Curves - Continued**

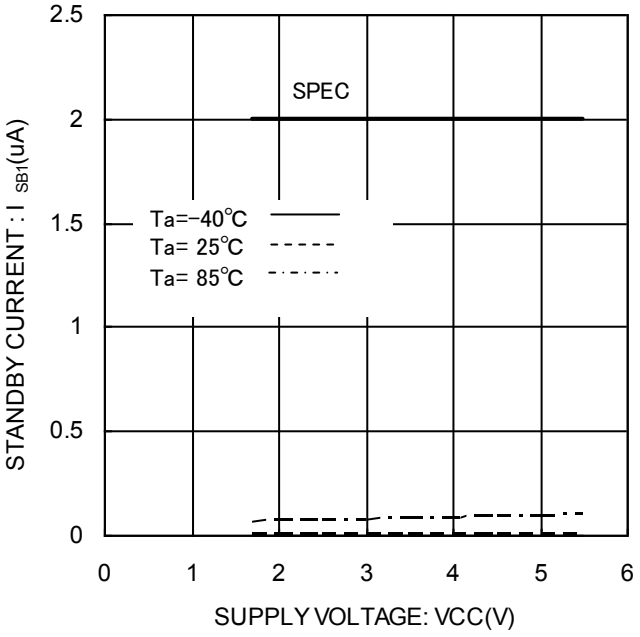


Figure 20. Standby current
I_{SB1}(CS=0V)

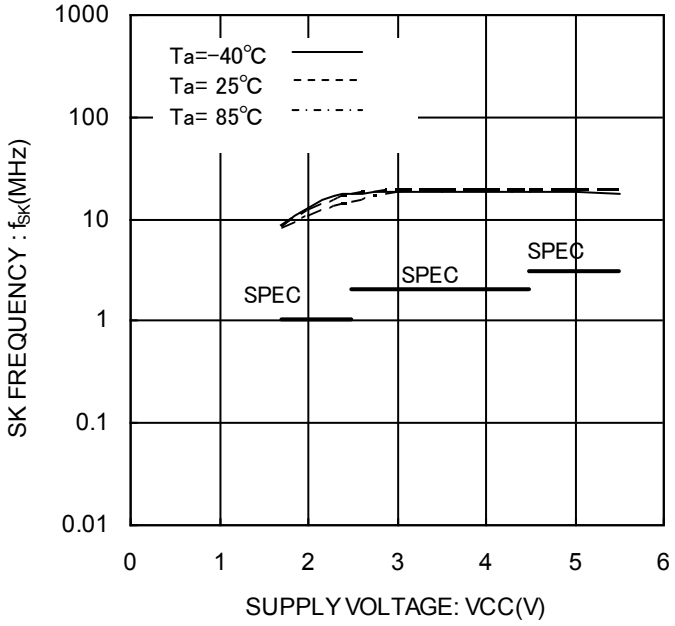


Figure 21. SK frequency f_{SK}

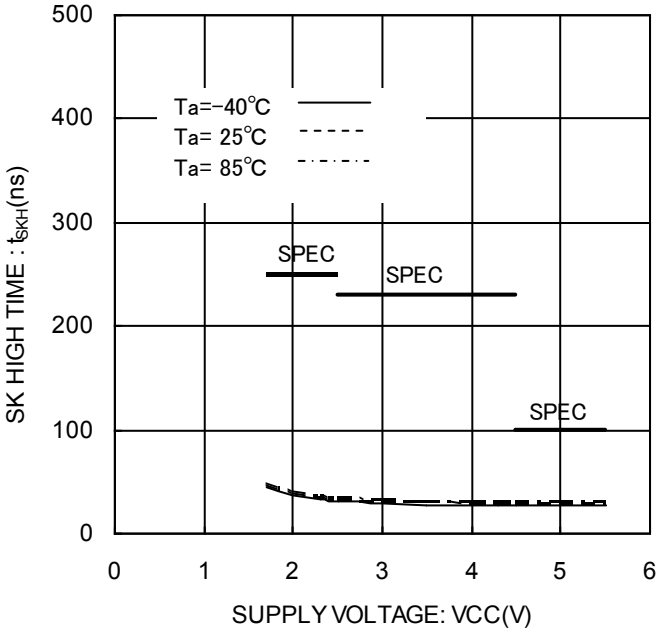


Figure 22. SK high time t_{SKH}

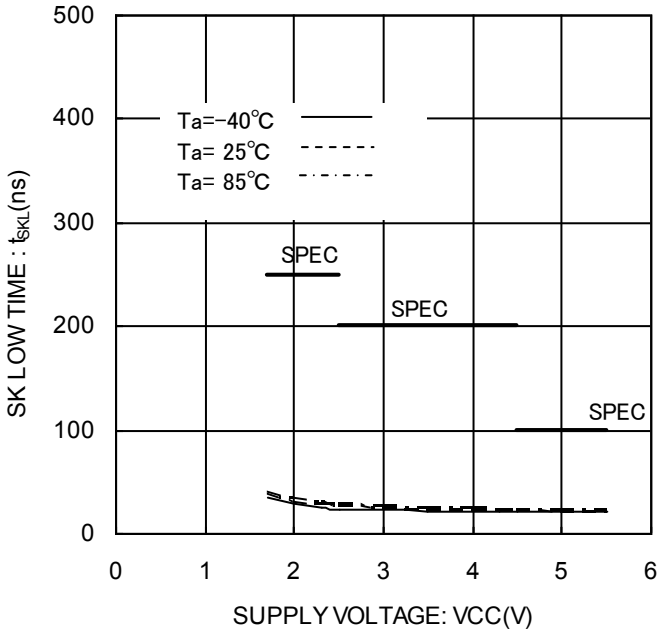


Figure 23. SK low time t_{SKL}

●**Typical Performance Curves - Continued**

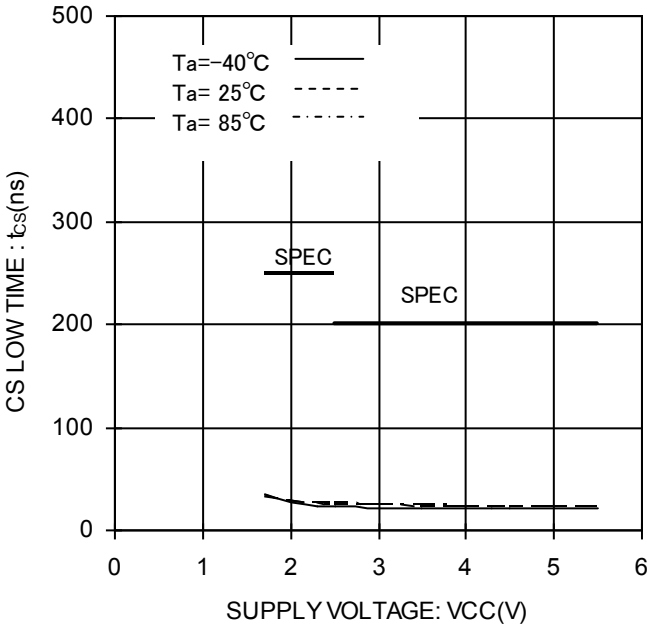


Figure 24. CS low time t_{CS}

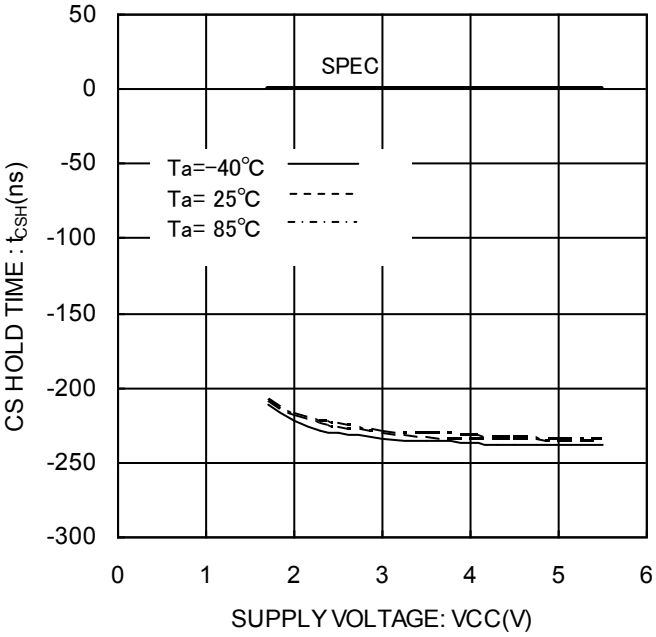


Figure 25. CS hold time t_{CSH}

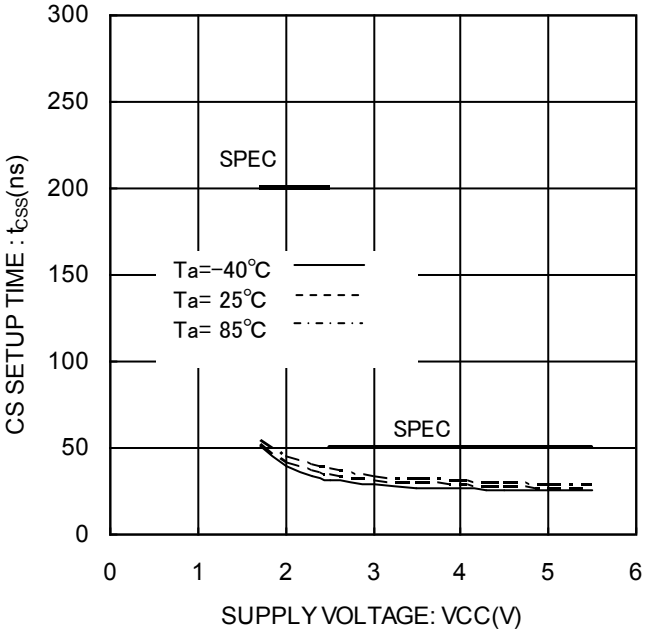


Figure 26. CS setup time t_{CSS}

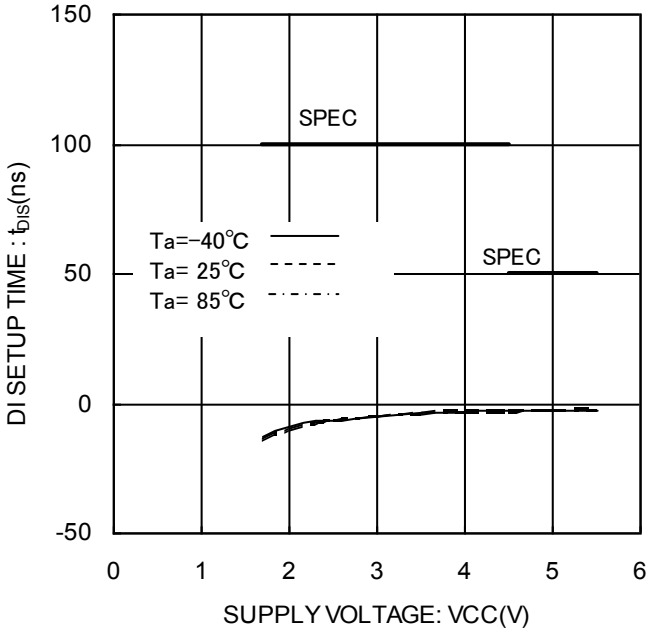


Figure 27. DI setup time t_{DIS}

●**Typical Performance Curves - Continued**

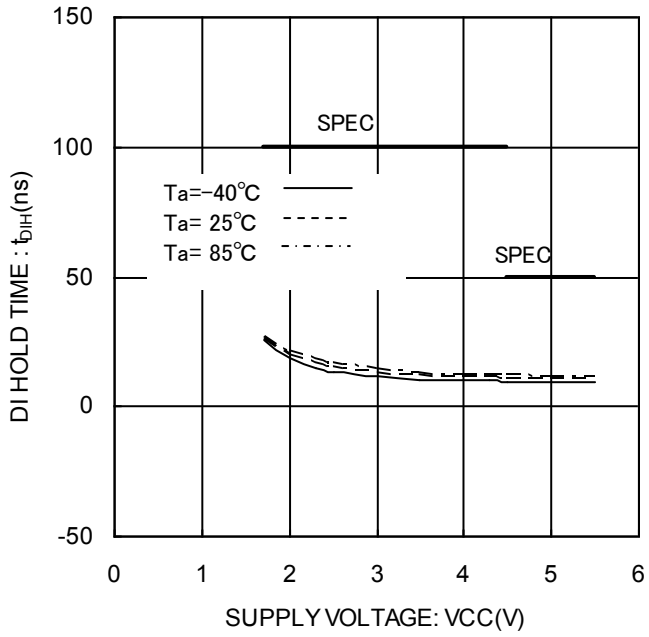


Figure 28. DI hold time t_{DIH}

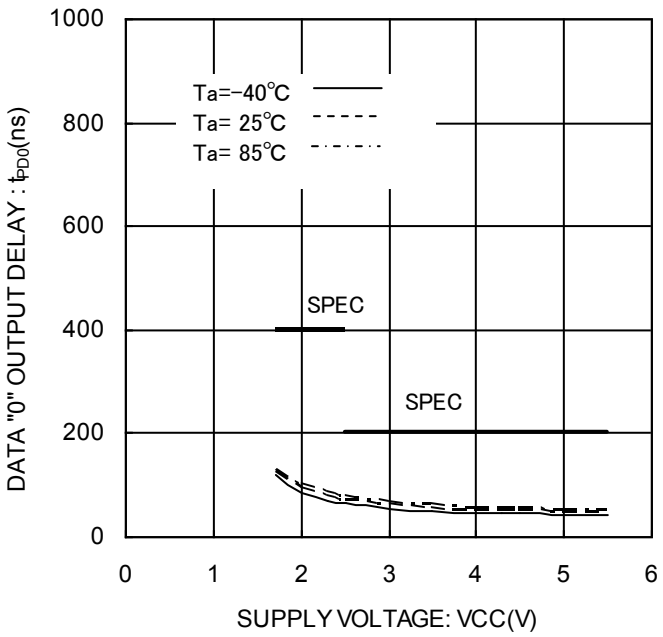


Figure 29. Data "0" output delay t_{PD0}

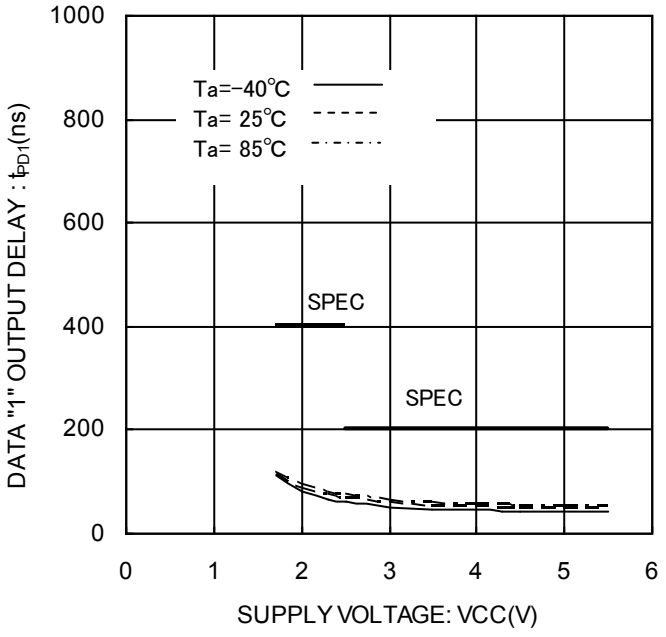


Figure 30. Data "1" output delay t_{PD1}

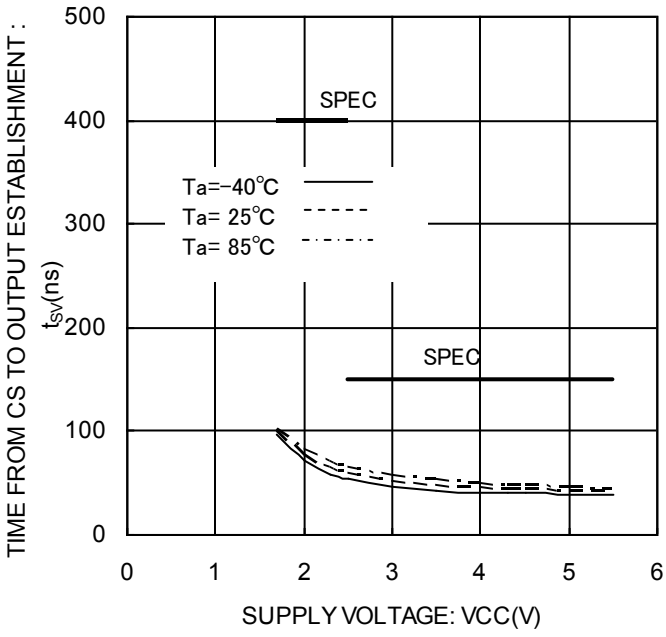


Figure 31. Time from CS to output establishment t_{SV}

●**Typical Performance Curves - Continued**

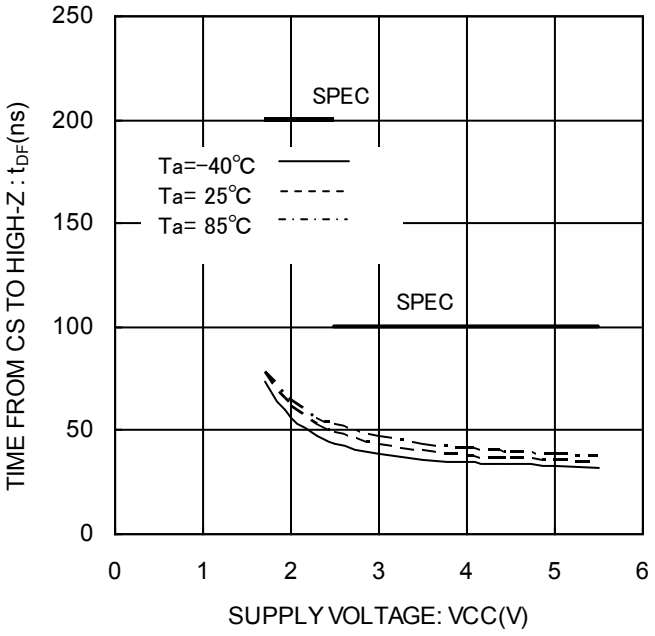


Figure 32. Time from CS to High-Z t_{DF}

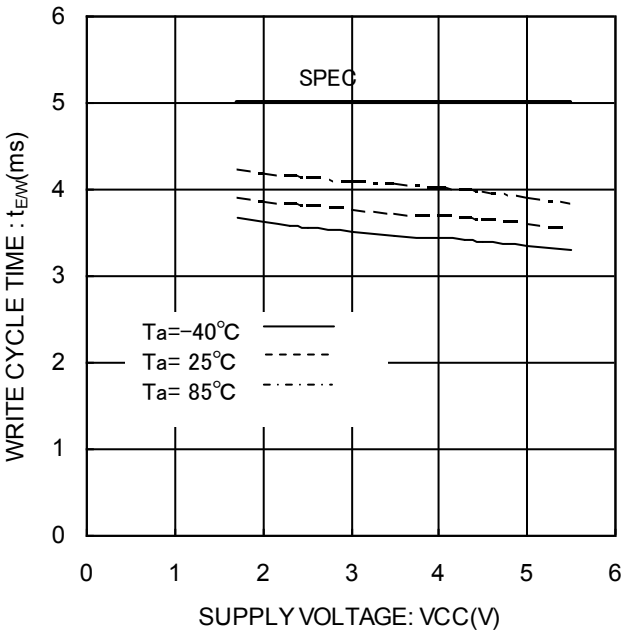
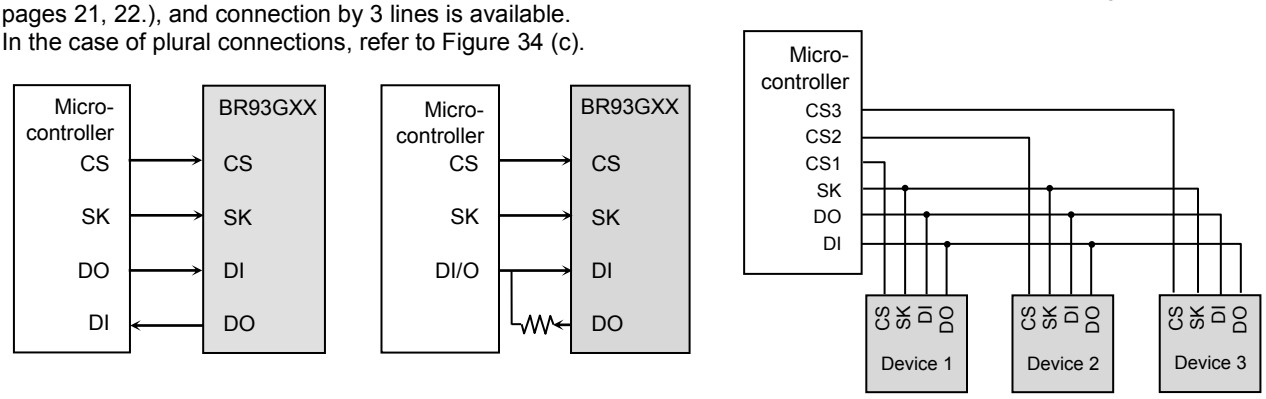


Figure 33. Write cycle time $t_{E/W}$

●Description of operations

Communications of the MicroWire BUS are carried out by SK (serial clock), DI (serial data input),DO (serial data output) ,and CS (chip select) for device selection.
When to connect one EEPROM to a microcontroller, connect it as shown in Figure 34(a) or Figure 34(b). When to use the input and output common I/O port of the microcontroller, connect DI and DO via a resistor as shown in Figure 34(b) (Refer to pages 21, 22.), and connection by 3 lines is available.
In the case of plural connections, refer to Figure 34 (c).



(a). Connection by 4 lines (b). Connection by 3 lines (c). Connection example of plural devices

Figure 34. Connection method with microcontroller

Communications of the MicroWire BUS are started by the first “1” input after the rise of CS. This input is called a start bit. After input of the start bit, input ope code, address and data. Address and data are input all in MSB first manners.
“0” input after the rise of CS to the start bit input is all ignored. Therefore, when there is limitation in the bit width of PIO of the microcontroller, input “0” before the start bit input, to control the bit width.

●Command mode

Command	Start bit	Ope code	Address BR93G86-3 MSB of Address(Am) is A9	Data MSB of Data(Dx) is D15	Required clocks(n)
Read (READ) *1	1	10	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	D15~D0(READ DATA)	BR93G86-3:n=29
Write enable (WEN)	1	00	1 1 * * * * * * * *		BR93G86-3:n=13
Write disable (WDS)	1	00	0 0 * * * * * * * *		
Write (WRITE) *2	1	01	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	D15~D0(WRITE DATA)	BR93G86-3:n=29
Write all (WRAL) *2	1	00	0 1 * * * * * * * *	D15~D0(WRITE DATA)	
Erase (ERASE)	1	11	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0		BR93G86-3:n=13
Erase all (ERAL)	1	00	1 0 * * * * * * * *		

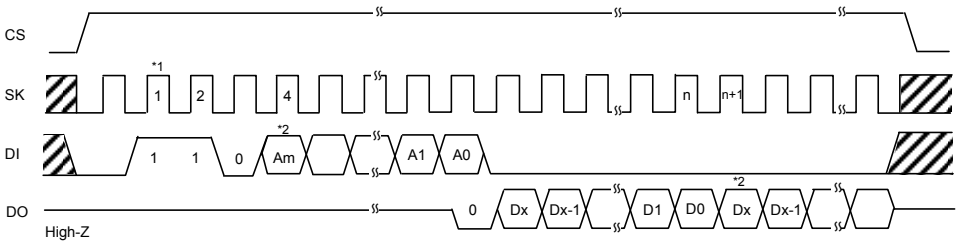
・ Input the address and the data in MSB first manners.
・ As for *, input either “1” or “0” .

*Start bit
Acceptance of all the commands of this IC starts at recognition of the start bit.
The start bit means the first “1” input after the rise of CS.

*1 As for read, by continuous SK clock input after setting the read command, data output of the set address starts, and address data in significant order are sequentially output continuously. (Auto increment function)
*2 For write or write all commands, an internal erase or erase all is included and no separate erase or erase all is needed before write or write all command.

●Timing chart

1) Read cycle (READ)



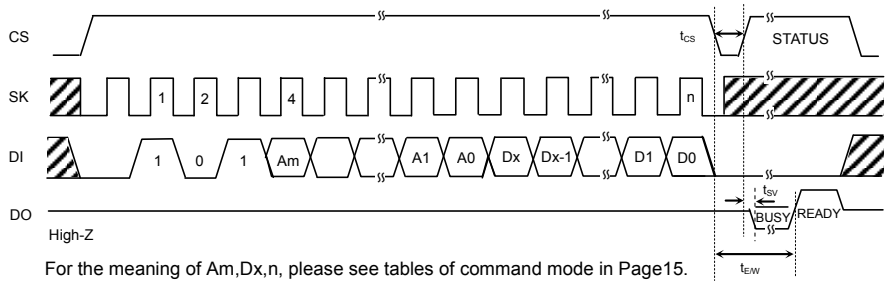
Am: MSB of address
Dx: MSB of data
n: required clocks

*1 Start bit
When data "1" is input for the first time after the rise of CS, this is recognized as a start bit. And when "1" is input after plural "0" are input, it is recognized as a start bit, and the following operation is started. This is common to all the commands to described hereafter.
*2 For the meaning of Am,Dx,n,please see tables of command mode in Page15. For example, Am=A9,Dx=D15,n=29.

Figure 35. Read cycle

○When the read command is recognized, input address data (16bit) is output to serial. And at that moment, at taking A0, in sync with the rise of SK, "0" (dummy bit) is output. And, the following data is output in sync with the rise of SK.
This IC has an address auto increment function which is valid only at read command. This is the function where after the above read execution, by continuously inputting SK clock, the above address data is read sequentially. And, during the auto increment, keep CS at high.

2) Write cycle (WRITE)



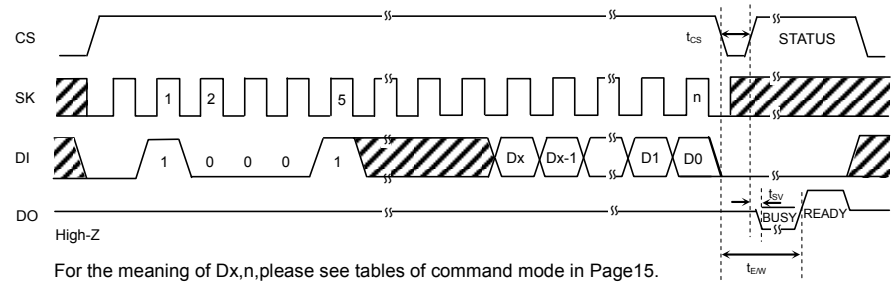
Am: MSB of address
Dx: MSB of data
n: required clocks

For the meaning of Am,Dx,n, please see tables of command mode in Page15.

Figure 36. Write cycle

○In this command, input 16bit data are written to designated addresses (Am~A0). The actual write starts by the fall of CS of D0 taken SK clock.
When STATUS is not detected (CS=low fixed),make sure Max 5ms time is in comforming with $t_{E/W}$.
When STATUS is detected (CS=high), all commands are not accepted for areas where low ($\overline{BUSY}$) is output from DO, therefore, do not input any command.

3) Write all cycyle (WRAL)



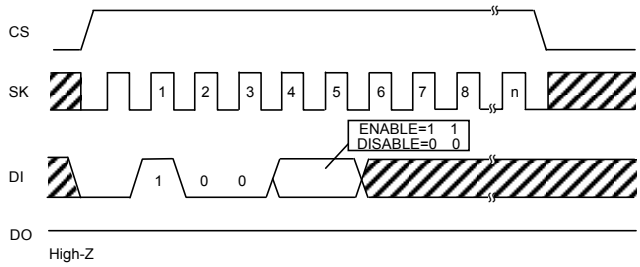
Dx: MSB of data
n: required clocks

For the meaning of Dx,n,please see tables of command mode in Page15.

Figure 37. Write all cycle

○In this command, input 16bit data is written simultaneously to all adresses. Data is not written continuously per one word but is written in bulk, the write time is only Max. 5ms in conformity with $t_{E/W}$.
In WRAL, STATUS can be detected in the same manner as in WRITE command.

4) Write enable (WEN) / disable (WDS) cycle



n: required clocks

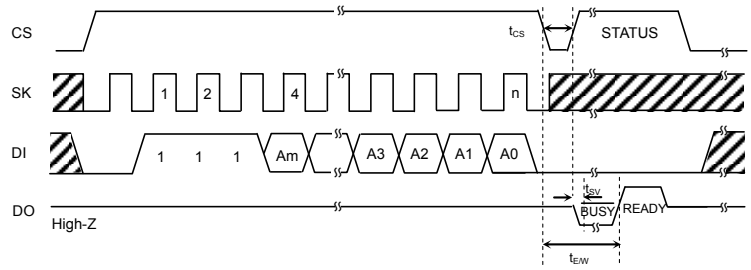
For the meaning of n,please see tables of command mode in Page15.

Figure 38. Write enable (WEN) / disable (WDS) cycle

○At power on, this IC is in write disable status by the internal RESET circuit. Before executing the write command, it is necessary to execute the write enable command. And, once this command is executed, it is valid unitl the write disable command is executed or the power is turned off. However, the read command is valid irrespective of write enable / diable command. Input to SK after 6 clocks of this command is available by either “1” or “0”, but be sure to input it.

○When the write enable command is executed after power on, write enable status gets in. When the write disable command is executed then, the IC gets in write disable status as same as at power on, and then the write command is canceled thereafter in software manner. However, the read command is executable. In write enable status, even when the write command is input by mistake, write is started. To prevent such a mistake, it is recommended to execute the write disable command after completion of write.

5) Erase cycle (ERASE)



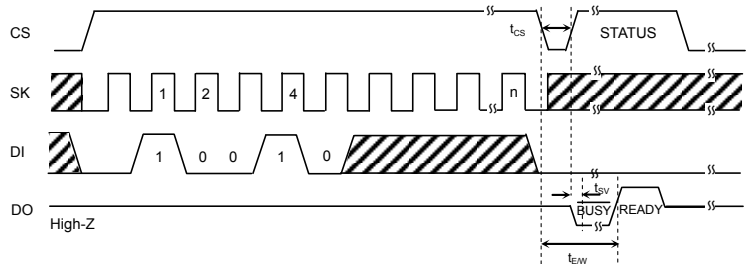
Am: MSB of address
n: required clocks

For the meaning of Am,n,please see tables of command mode in Page15.

Figure 39. Erase cycle

○In this command, data of the designated address is made into “1”. The data of the designated address becomes “FFFFh”.
Actual ERASE starts at the fall of CS after the fall of A0 taken SK clock.
In ERASE, STATUS can be detected in the same manner as in WRITE command.

6) Erase all cycle (ERAL)



n: required clocks

For the meaning of n,please see tables of command mode in Page15.

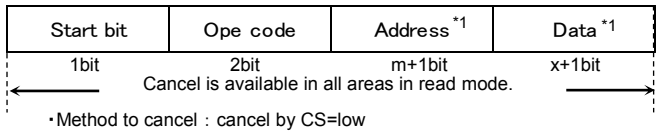
Figure 40. Erase all cycle

○In this command, data of all addresses is made into “1”. Data of all addresses becomes ”FFFFh”.
Actual ERASE starts at the fall of CS after the falll of the n-th clock from the start bit input.
In ERAL, STATUS can be detected in the same manner as in WRAL command.

●Application

1)Method to cancel each command

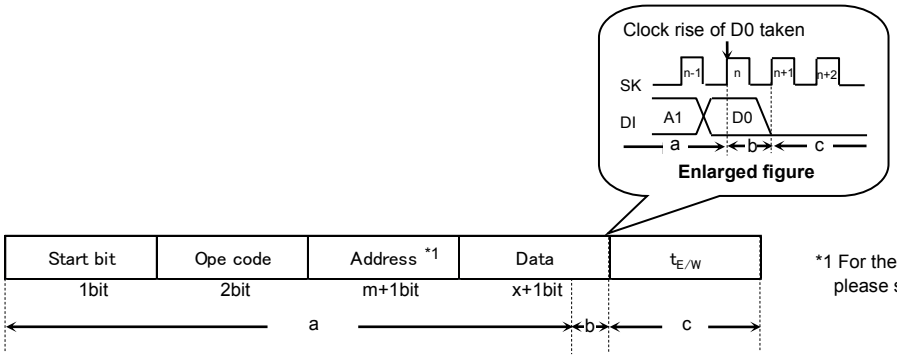
○READ



*1 For the meaning of m,x, please see tables of command mode in Page15

Figure 41. READ cancel available timing

○WRITE,WRAL



*1 For the meaning of m,n,x, please see tables of command mode in Page15

a：From start bit to the clock rise of D0 taken
Cancel by CS=low

b：The clock rise of D0 taken and after
Cancellation is not available by any means.

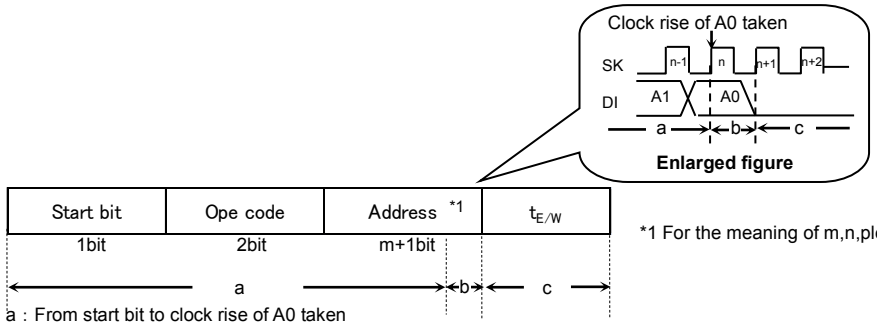
c：n+1 clock rise and after
Cancel by CS=low
However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is output continuously cancel function is not available.

Note 1) If VCC is made OFF in this area, designated address data is not guaranteed, therefore write once again is suggested.

Note 2) If CS is started at the same timing as that of the SK rise, write execution/cancel becomes unstable, therefore, it is recommended to fall in SK=low area.
As for SK rise, recommend timing of t_{CSS}/t_{CSH} or higher.

Figure 42. WRITE, WRAL cancel available timing

○ERASE, ERAL



*1 For the meaning of m,n,please see tables of command mode in Page15

a：From start bit to clock rise of A0 taken
Cancel by CS=low

b：Clock rise of A0 taken
Cancellation is not available by any means.

c：n+1 clock rise and after
Cancel by CS=low
However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is output continuously cancel function is not available.

Note 1) If VCC is made OFF in this area, designated address data is not guaranteed, therefore write once again is suggested.

Note 2) If CS is started at the same timing as that of the SK rise, write execution/cancel becomes unstable, therefore, it is recommended to fall in SK=low area.
As for SK rise, recommend timing of t_{CSS}/t_{CSH} or higher.

Figure 43. ERASE, ERAL cancel available timing

2) At standby
When CS is low , even if SK,DI,DO are low, high or with middle electric potential, current does not over I_{SB1} Max.

3) I/O peripheral circuit
3-1) Pull down CS.
By making CS=low at power ON/OFF, mistake in operation and mistake write are prevented.

○Pull down resistance Rcs of CS pin
To prevent mistake in operation and mistake write at power ON/OFF, CS pull down resistance is necessary. Select an appropriate value to this resistance value from microcontroller V_{OH}, I_{OH}, and V_{IL} characteristics of this IC.

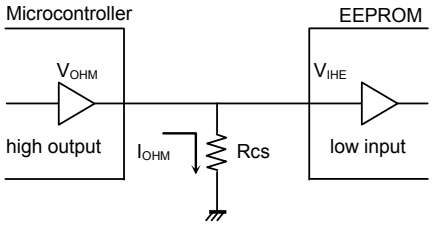


Figure 44. CS pull down resistance

$$Rcs \geqq \frac{V_{OHM}}{I_{OHM}} \quad \cdot\cdot\cdot ①$$

$$V_{OHM} \geqq V_{IHE} \quad \cdot\cdot\cdot ②$$

Example) When VCC =5V, V_{IHE}=2V, V_{OHM}=2.4V, I_{OHM}=2mA, from the equation ①,

$$Rcs \geqq \frac{2.4}{2\times10^{-3}}$$

$$\therefore \quad Rcs \geqq 1.2\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, V_{OHM} becomes 2.4V or higher, and V_{IHE} (=2.0V), the equation ② is also satisfied.

- V_{IHE} : EEPROM VIH specifications
- V_{OHM} : Microcontroller V_{OH} specifications
- I_{OHM} : Microcontroller I_{OH} specifications

3-2) DO is available in both pull up and pull down.
Do output always is High-Z except in READY / $\overline{\text{BUSY}}$ STATUS and data output in read command.
Malfunction may occur when High-Z is input to the microcontroller port connected to DO, it is necessary to pull down and pull up DO. When there is no influence upon the microcontroller operations, DO may be OPEN.
If DO is OPEN, and at timing to output STATUS READY, at timing of CS=high, SK=high, DI=high, EEPROM recognizes this as a start bit, resets READY output, and DO=High-Z, therefore, READY signal cannot be detected. To avoid such output, pull up DO pin for improvement.

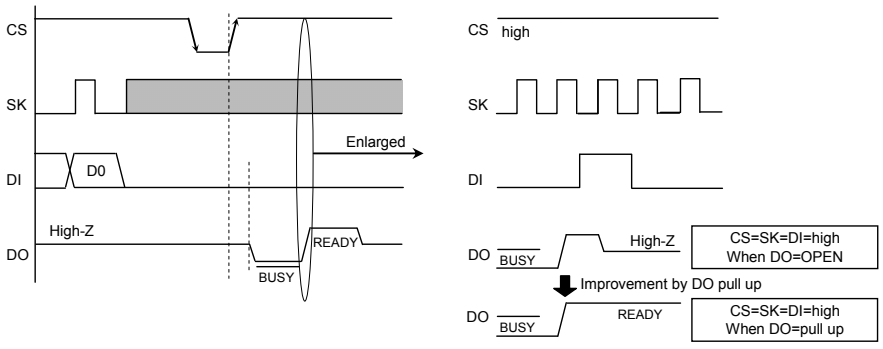


Figure 45. READY output timing at DO=OPEN

○Pull up resistance Rpu and pull down resistance Rpd of DO pin

As for pull up and pull down resistance value, select an appropriate value to this resistance value from microcontroller V_{IH}, V_{IL}, and V_{OH}, I_{OH}, V_{OL}, I_{OL} characteristics of this IC.

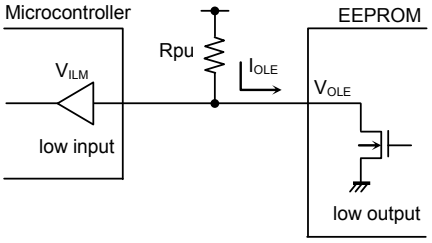


Figure 46. DO pull up resistance

$$Rpu \geqq \frac{VCC - V_{OLE}}{I_{OLE}} \quad \cdot\cdot\cdot ③$$

$$V_{OLE} \leqq V_{ILM} \quad \cdot\cdot\cdot ④$$

Example) When VCC =5V, V_{OLE}=0.4V, I_{OLE}=2.1mA, V_{ILM}=0.8V, from the equation ③,

$$Rpu \geqq \frac{5-0.4}{2.1\times10^{-3}}$$

$$\therefore \quad Rpu \geqq 2.2\ [k\Omega]$$

With the value of Rpu to satisfy the above equation, V_{OLE} becomes 0.4V or below, and with V_{ILM}(=0.8V), the equation ④ is also satisfied.

- V_{OLE} : EEPROM V_{OL} specifications
- I_{OLE} : EEPROM I_{OL} specifications
- V_{ILM} : Microcontroller V_{IL} specifications

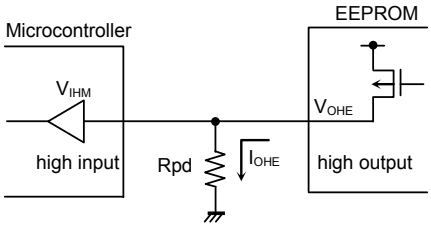


Figure 47. DO pull down resistance

$$Rpd \geqq \frac{V_{OHE}}{I_{OHE}} \quad \cdot\cdot\cdot ⑤$$

$$V_{OHE} \geqq V_{IHM} \quad \cdot\cdot\cdot ⑥$$

Example) When VCC =5V, V_{OHE}=VCC－0.2V, I_{OHE}=0.1mA, V_{IHM}=VCC×0.7V from the equation ⑤,

$$Rpd \geqq \frac{5-0.2}{0.1\times10^{-3}}$$

$$\therefore \quad Rpd \geqq 48\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, V_{OHE} becomes 2.4V or below, and with V_{IHM} (=3.5V), the equation ⑥ is also satisfied.

- V_{OHE} : EEPROM V_{OH} specifications
- I_{OHE} : EEPROM I_{OH} specifications
- V_{IHM} : Microcontroller V_{IH} specifications

○READY / $\overline{BUSY}$ STATUS display (DO terminal)

This display outputs the internal STATUS signal. When CS is started after t_{CS} from CS fall after write command input, high or low is output.

R/$\overline{B}$ display＝low ($\overline{BUSY}$) = write under execution
(DO STATUS)
After the timer circuit in the IC works and creates the period of $t_{E/W}$, this timer circuit completes automatically.
And the memory cell is written in the period of $t_{E/W}$, and during this period, other command is not accepted.

R/$\overline{B}$ display = high (READY) = command wait STATUS
(DO STATUS)
After $t_{E/W}$ (max.5ms) the following command is accepted.
Therefore, CS=high in the period of $t_{E/W}$, and If signals are input in SK, DI, malfunction may occur, therefore, DI=low in the area
CS=high. (Especially, in the case of shared input port, attention is required.)

*Do not input any command while STATUS signal is output. Command input in $\overline{BUSY}$ area is cancelled, but command input in READY area is accepted. Therefore, STATUS READY output is cancelled, and malfunction and mistake write may occur.

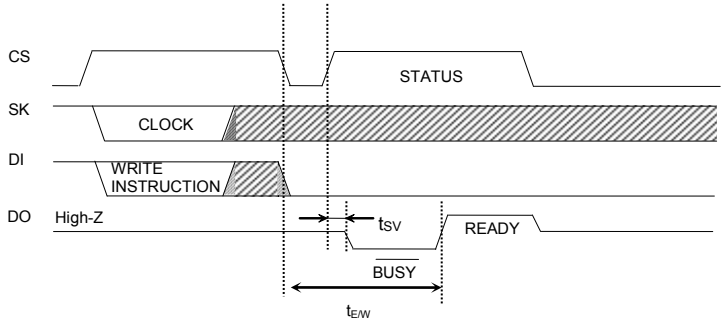


Figure 48. READY/$\overline{BUSY}$ STATUS output timing chart

4) When to directly connect DI and DO

This IC has independent input terminal DI and output terminal DO, and separate signals are handled on timing chart, meanwhile, by inserting a resistance R between these DI and DO terminals, it is possible to carry out control by 1 control line.

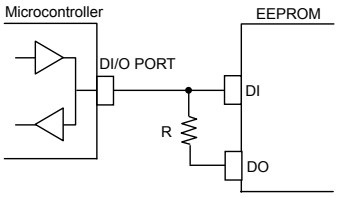


Figure 49. DI, DO control line common connection

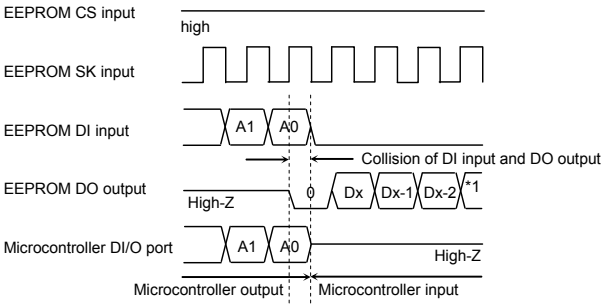
○Data collision of microcontroller DI/O output and DO output and feedback of DO output to DI input of EEPROM.

Drive from the microcontroller DI/O output to DI input of EEPROM on I/O timing, and output signal from DO output of EEPROM occur at the same time in the following points.

4-1) 1 clock cycle to take in A0 address data at read command

Dummy bit “0” is output to DO terminal.

→When address data A0 = “1” input, through current route occurs.



*1 X=15,for the meaning of x ,
please see tables of command mode in Page15.

Figure 50. Collision timing at read data output at DI, DO direct connection

4-2) Timing of CS = high after write command. DO terminal in READY / $\overline{\text{BUSY}}$ function output.

When the next start bit input is recognized, High-Z gets in.

→Especially, at command input after write, when CS input is started with microcontroller DI/O output low, READY output high is output from DO terminal, and through current route occurs.

Feedback input at timing of these (4-1) and (4-2) does not cause disorder in basic operations, if resistance R is inserted.

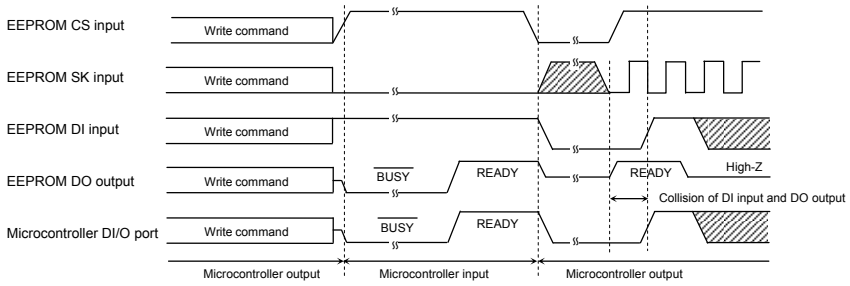


Figure 51. Collision timing at DI, DO direct connection

Note) As for the case (4-2), attention must be paid to the following.

When STATUS READY is output, DO and DI are shared, DI=high and the microcontroller DI/O=High-Z or the microcontroller DI/O=high,if SK clock is input, DO output is input to DI and is recognized as a start bit, and malfunction may occur. As a method to avoid malfunction, at STATUS READY output, set SK=low, or start CS within 4 clocks after high of READY signal is output.

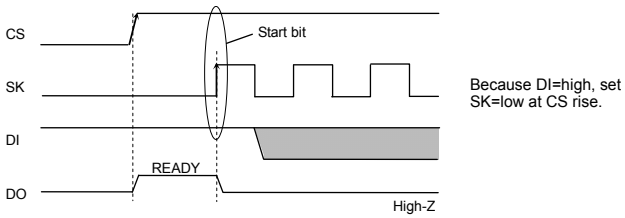


Figure.52 Start bit input timing at DI, DO direct connection

○Selection of resistance value R

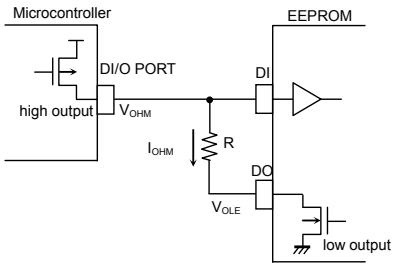
The resistance R becomes through current limit resistance at data collision. When through current flows, noises of power source line and instantaneous stop of power source may occur. When allowable through current is defined as I, the following relation should be satisfied. Determine allowable current amount in consideration of impedance and so forth of power source line in set. And insert resistance R, and set the value R to satisfy EEPROM input level V_{IH}/V_{IL} even under influence of voltage decline owing to leak current and so forth. Insertion of R will not cause any influence upon basic operations.

4-3) Address data A0 = "1" input, dummy bit "0" output timing

(When microcontroller DI/O output is high, EEPROM DO outputs low, and high is input to DI)

・Make the through current to EEPROM 10mA or below.

・See to it that the level V_{IH} of EEPROM should satisfy the following.



Conditions

$$V_{IHE} \leqq I_{OHM} \times R + V_{OLE}$$

At this moment, if V_{OLE}=0V,

$$V_{IHE} \leqq I_{OHM} \times R$$

$$\therefore \quad R \geqq \frac{V_{IHE}}{I_{OHM}} \quad \cdots ⑦$$

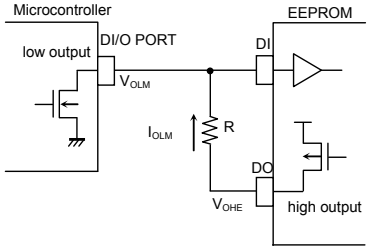
・V_{IHE} : EEPROM V_{IH} specifications
・V_{OLE} : EEPROM V_{OL} specifications
・I_{OHM} : Microcontroller I_{OH} specifications

Figure 53. Circuit at DI, DO direct connection (Microcontroller DI/O high output, EEPROM low output)

4-4) DO STATUS READY output timing

(When the microcontroller DI/O is low, EEPROM DO output high, and low is input to DI)

・Set the EEPROM input level V_{IL} so as to satisfy the following.



Conditions

$$V_{ILE} \geqq V_{OHE} - I_{OLM} \times R$$

As this moment, V_{OHE}=VCC

$$V_{ILE} \geqq VCC - I_{OLM} \times R$$

$$\therefore \quad R \geqq \frac{VCC - V_{ILE}}{I_{OLM}} \quad \cdots ⑧$$

・V_{ILE} : EEPROM V_{IL} specifications
・V_{OHE} : EEPROM V_{OH} specifications
・I_{OLM} : Microcontroller I_{OL} specifications

Example) When VCC=5V, V_{OHM}=5V, I_{OHM}=0.4mA, V_{OLM}=5V, I_{OLM}=0.4mA,

From the equation ⑦,

$$R \geqq \frac{V_{IHE}}{I_{OHM}}$$

$$R \geqq \frac{3.5}{0.4 \times 10^{-3}}$$

$$\therefore \quad R \geqq 8.75\ [k\Omega] \quad \cdots ⑨$$

From the equation⑧,

$$R \geqq \frac{VCC - V_{ILE}}{I_{OLM}}$$

$$R \geqq \frac{5 - 1.5}{2.1 \times 10^{-3}}$$

$$\therefore \quad R \geqq 1.67\ [k\Omega] \quad \cdots ⑩$$

Therefore, from the equations ⑨ and ⑩,

$$\therefore \quad R \geqq 8.75\ [k\Omega]$$

Figure 54. Circuit at DI, DO direct connection (Microcontroller DI/O low output, EEPROM high output)

5) I/O equivalence circuit

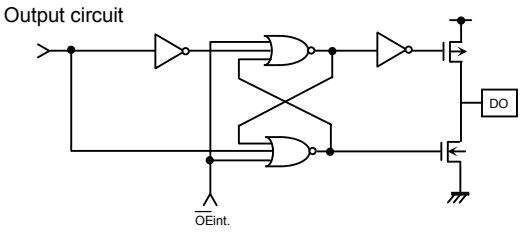


Figure 55. Output circuit (DO)

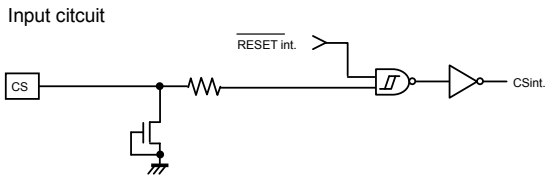


Figure 56. Input circuit (CS)

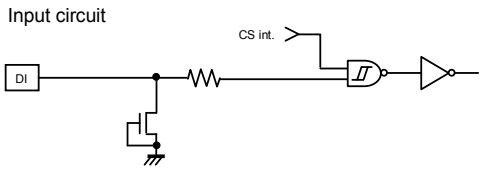


Figure 57. Input circuit (DI)

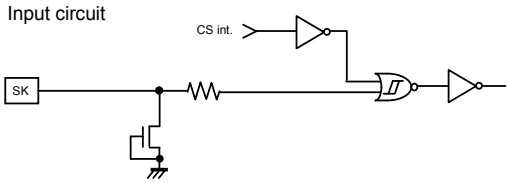


Figure 58. Input circuit (SK)

6)Power-Up/Down conditions

○At power ON/OFF, set CS low.

When CS is high, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CS low. (When CS is in low status all inputs are cancelled.) And at power decline, owing to power line capacity and so forth, low power status may continue long. At this case too, owing to the same reason, malfunction, mistake write may occur, therefore, at power OFF too, set CS low.

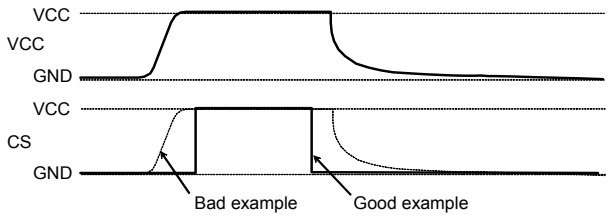


Figure 59. Timing at power ON/OFF

（Bad example）CS pin is pulled up to VCC

In this case, CS becomes high (active status), and EEPROM may have malfunction, mistake write owing to noise and the likes.

Even when CS input is High-Z, the status becomes like this case, which please note.

（Good example）It is low at power ON/OFF.

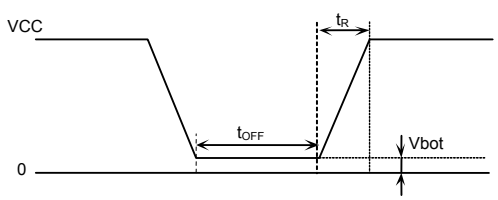
Set 10ms or higher to recharge at power OFF.

When power is turned on without observing this condition, IC internal circuit may not be reset, which please note.

○POR citcuit

This IC has a POR (Power On Reset) circuit as a mistake write countermeasure. After POR operation, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is high at power ON/OFF, it may become write enable status owing to noises and the likes. For secure operations, observe the follwing conditions.

1. Set CS=low
2. Turn on power so as to satisfy the recommended conditions of t_R, t_{OFF}, Vbot for POR circuit operation.



Recommended conditions of t_R, t_{OFF}, Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Figure 60. Rise waveform diagram

○LVCC circuit

LVCC (VCC-Lockout) circuit prevents data rewrite operation at low power, and prevents wrong write.

At LVCC voltage (Typ.=1.2V) or below, it prevent data rewrite

7)Noise countermeasures

○VCC noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC VCC and GND, At that moment, attach it as close to IC as possible.And, it is also recommended to attach a bypass capacitor between board VCC and GND.

○SK noise

When the rise time of SK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time of SK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

●Operational Notes

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute Maximum Ratings
If the absolute maximum ratings such as supply voltage and operating temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any operating condition. Make sure that each terminal voltage is not lower than that of GND terminal in consideration of transition status.

(5) Heat design
In consideration of allowable loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal short circuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of pin short between LSI terminals and terminals, terminals and power source, terminals and GND owing to unconnect use, LSI may be destructed.

(7) Using this LSI in a strong electromagnetic field may cause malfunction, therefore, evaluate the design sufficiently.