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Serial EEPROM Series Industrial EEPROM

125℃ Operation Microwire BUS EEPROM (3-wire)

BR93H46RF-2LB

General Description

This is the product guarantees long time support in Industrial market.

BR93H46RF-2LB is a serial EEPROM of serial 3-line interface method

Features

- Long Time Support a Product for Industrial Applications.
- Conforming to Microwire BUS
- Withstands Electrostatic Voltage up to 6kV (HBM method typ)
- Wide Temperature Range -40℃ to +125℃
- Same package line-up and same pin configuration
- 2.5V to 5.5V Single Supply Voltage Operation
- Address Auto Increment Function at READ Operation
- Prevention of write mistake
  - Write prohibition at power on
  - Write prohibition by command code
  - Write mistake prevention circuit at low voltage
- Self-timed programming cycle
- Program Condition Display by READY / $\overline{\text{BUSY}}$
- Low Supply Current
  - Write Operation (5V) : 0.8mA (Typ)
  - Read Operation (5V) : 0.5mA (Typ)
  - Standby Operation (5V) : 0.1μA (Typ)
- Compact package
- High-Reliability using ROHM Original Double-Cell structure
- More than 100 years data retention
- More than 1 million write cycles
- Data set to FFFFh on all addresses at shipment

Package

W(Typ.) x D(Typ.) x H(Max.)

SOP8
5.00mm x 6.20mm x 1.71mm

Application

Industrial Equipment

BR93H46RF-2LB

Capacity	Bit Format	Product Name	Supply Voltage	Package
1Kbit	64×16	BR93H46RF-2LB	2.5V to 5.5V	SOP8

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to +6.5	V	
Permissible Dissipation	Pd	0.56	W	When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃.
Storage Temperature Range	Tstg	-65 to +150	℃	
Operating Temperature Range	Topr	-40 to +125	℃	
Input Voltage/Output Voltage	-	-0.3 to V_{CC}+0.3	V	

Memory Cell Characteristics (V_{CC}=2.5V to 5.5V)

Parameter	Limits			Unit	Conditions
	Min	Typ	Max		
Write Cycles (1)	1,000,000	-	-	Cycles	Ta≦85℃
	500,000	-	-	Cycles	Ta≦105℃
	300,000	-	-	Cycles	Ta≦125℃
Data Retention (1)	100	-	-	Years	Ta≦25℃
	60	-	-	Years	Ta≦105℃
	50	-	-	Years	Ta≦125℃

(1) Not 100% TESTED

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	2.5 to 5.5	V
Input Voltage	V_{IN}	0 to V_{CC}	

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DC Characteristics(Unless otherwise specified, Ta=-40℃ to +125℃, V_{CC}=2.5V to 5.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Low Voltage	V_{IL}	-0.3	-	0.3xV_{CC}	V	
Input High Voltage	V_{IH}	0.7xV_{CC}	-	V_{CC}+0.3	V	
Output Low Voltage 1	V_{OL1}	0	-	0.4	V	I_{OL}=2.1mA, 4.0V≦V_{CC}≦5.5V
Output Low Voltage 2	V_{OL2}	0	-	0.2	V	I_{OL}=100μA
Output High Voltage 1	V_{OH1}	2.4	-	V_{CC}	V	I_{OH}=-0.4mA, 4.0V≦V_{CC}≦5.5V
Output High Voltage 2	V_{OH2}	V_{CC}-0.2	-	V_{CC}	V	I_{OH}=-100μA
Input Leak Current	I_{LI}	-10	-	10	μA	V_{IN}=0V to V_{CC}
Output Leak Current	I_{LO}	-10	-	10	μA	V_{OUT}=0V to V_{CC}, CS=0V
Supply Current	I_{CC1}	-	-	3.0	mA	f_{SK}=2MHz, $t_{E/W}$=4ms (WRITE)
	I_{CC2}	-	-	1.5	mA	f_{SK}=2MHz (READ)
	I_{CC3}	-	-	3.0	mA	f_{SK}=2MHz, $t_{E/W}$=4ms (WRAL)
Standby Current	I_{SB}	-	-	10	μA	CS=0V, DO=OPEN

AC Characteristics(Unless otherwise specified, Ta=-40℃ to +125℃, V_{CC}=2.5V to 5.5V)

Parameter	Symbol	Min	Typ	Max	Unit
SK Frequency	f_{SK}	-	-	2	MHz
SK “H” Time	t_{SKH}	200	-	-	ns
SK “L” Time	t_{SKL}	200	-	-	ns
CS “L” Time	t_{CS}	200	-	-	ns
CS Setup TIme	t_{CSS}	50	-	-	ns
DI Setup Time	t_{DIS}	50	-	-	ns
CS Hold Time	t_{CSH}	0	-	-	ns
DI Hold Time	t_{DIH}	50	-	-	ns
Data “1” Output Delay Time	t_{PD1}	-	-	200	ns
Data “0” Output Delay Time	t_{PD0}	-	-	200	ns
Time from CS to Output establishment	t_{SV}	-	-	150	ns
Time from CS to High-Z	t_{DF}	-	-	150	ns
Write Cycle Time	$t_{E/W}$	-	-	4	ms

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Serial Input / Output Timing

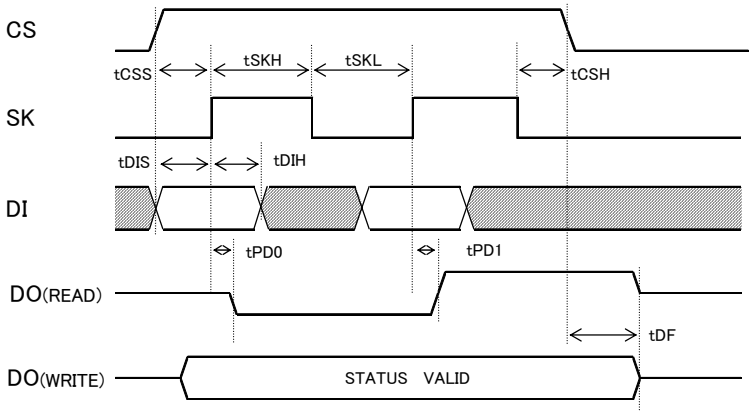

Figure 1. Serial Input / Output Timing Diagram

- ○Data is taken from DI, in sync with the rise of SK.
- ○At READ command, data is outputted from DO in sync with the rise of SK.
- ○After WRITE command input, the status signal of WRITE (READY / BUSY) can be monitored from DO by setting CS to “H” after tCS, from the fall of CS, and will display a valid status until the next command start bit is inputted. But, if CS is set to “L”, DO sets to High-Z state.
- ○To execute a series of commands, CS is set to “L” once after completion of each command for internal circuit reset.

Block Diagram

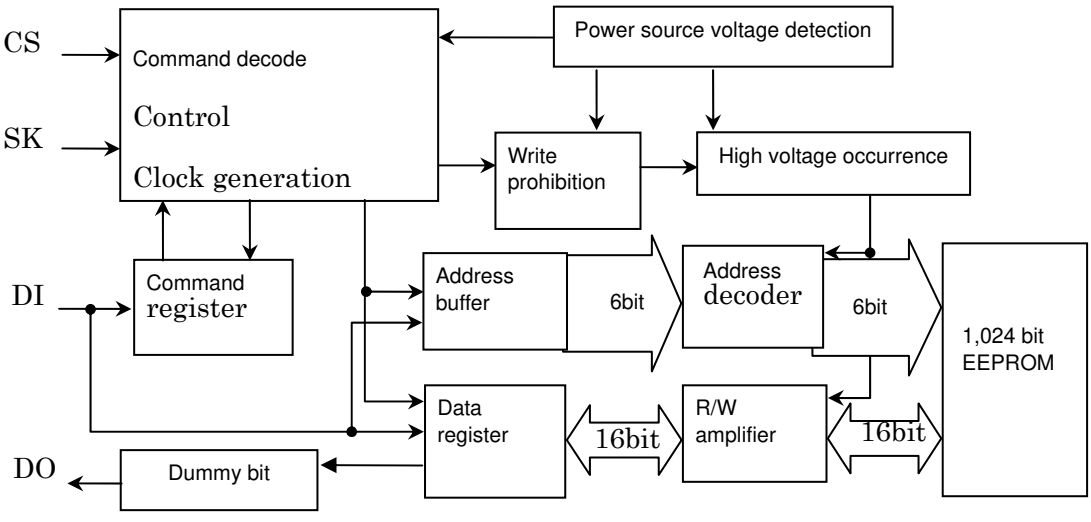

Figure 3. Block Diagram

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Pin Configuration

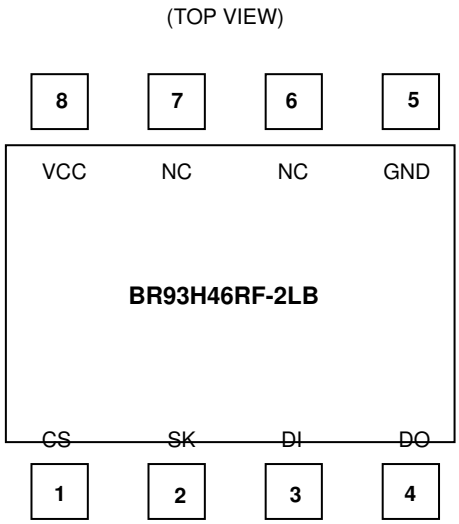

Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	I / O	Function
1	CS	Input	Chip select input
2	SK	Input	Serial clock input
3	DI	Input	Start bit, ope code, address, and serial data input
4	DO	Output	Serial data output, READY / $\overline{\text{BUSY}}$ status output
5	GND	-	Ground, 0V
6,7	NC	-	Non connected terminal, VCC, GND or OPEN
8	VCC	-	Power supply, 2.5V to 5.5V

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Typical Performance Curves

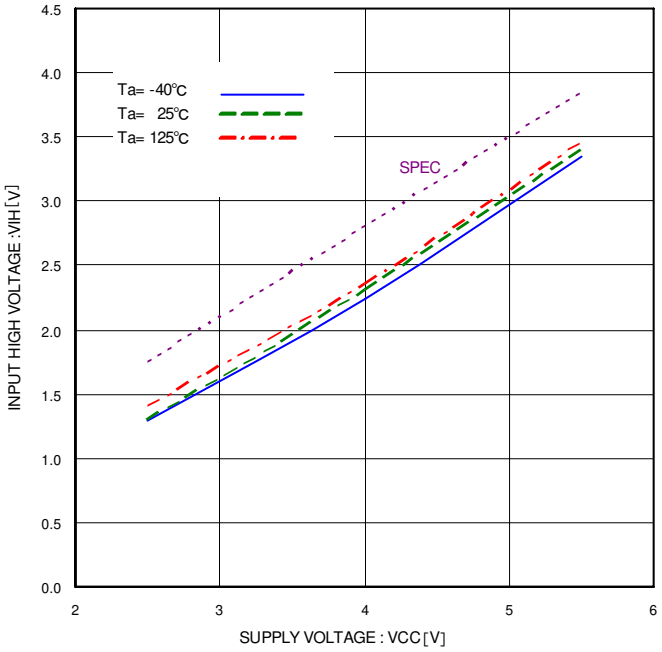

Figure 4. Input High Voltage (CS, SK, DI) vs. Supply Voltage

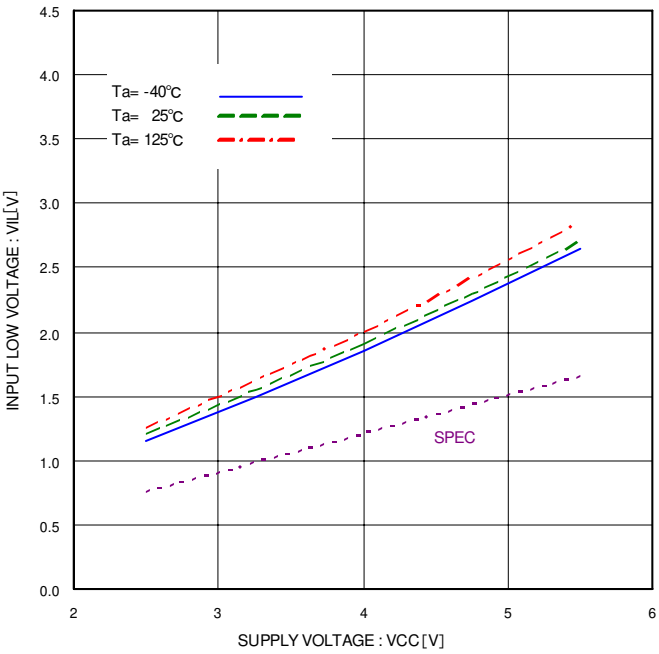

Figure 5. Input Low Voltage (CS, SK, DI) vs. Supply Voltage

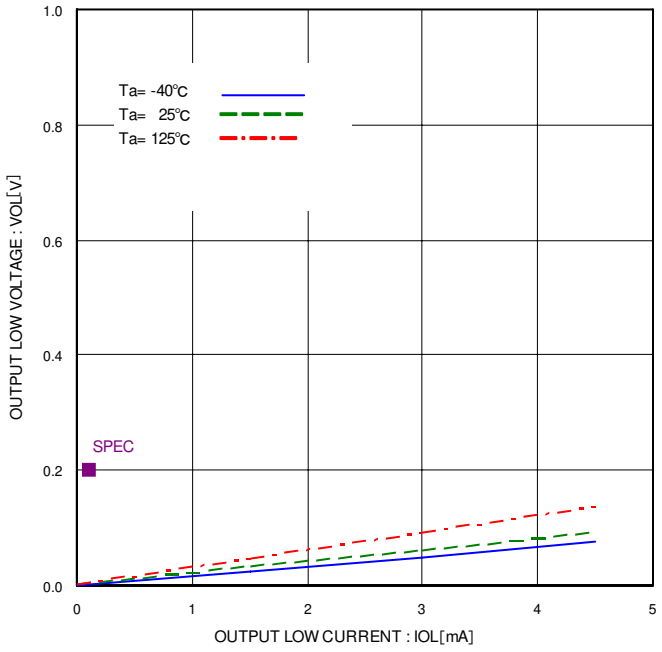

Figure 6. Output Low Voltage vs. Output Low Current (V_{CC}=2.5V)

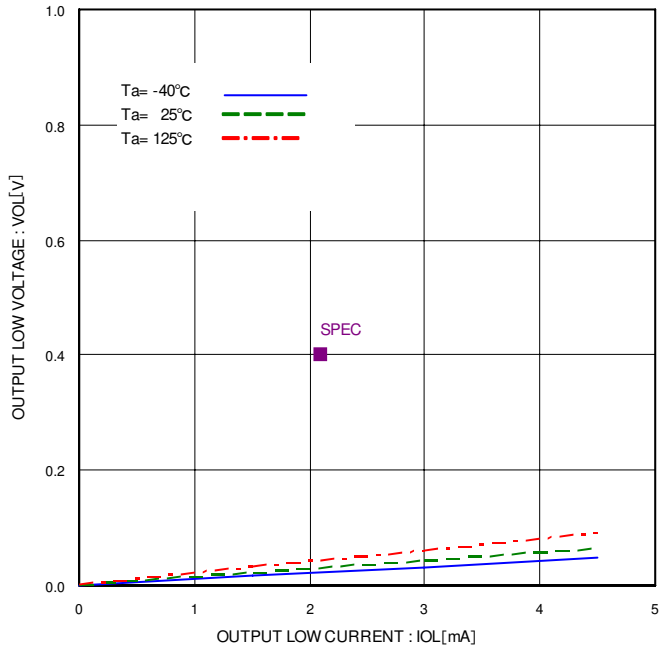

Figure 7. Output Low Voltage vs. Output Low Current (V_{CC}=4.0V)

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Typical Performance Curves - Continued

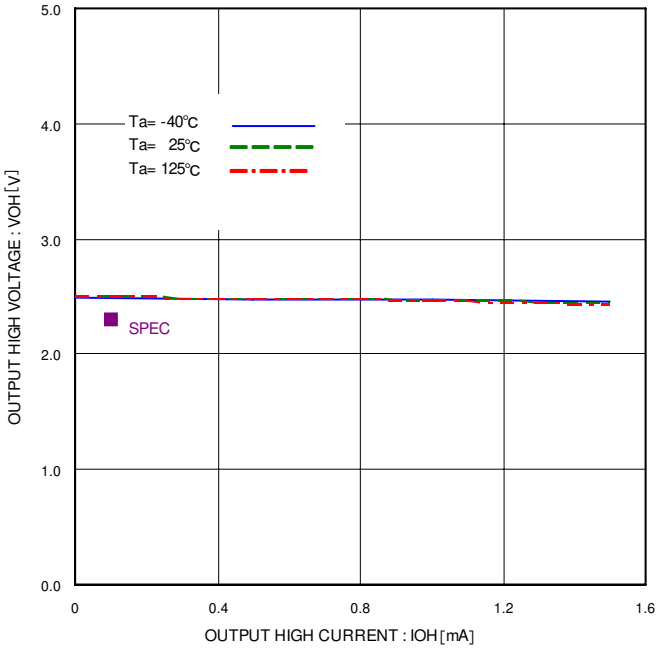

Figure 8. Output High Voltage vs. Output High Current (V_{CC}=2.5V)

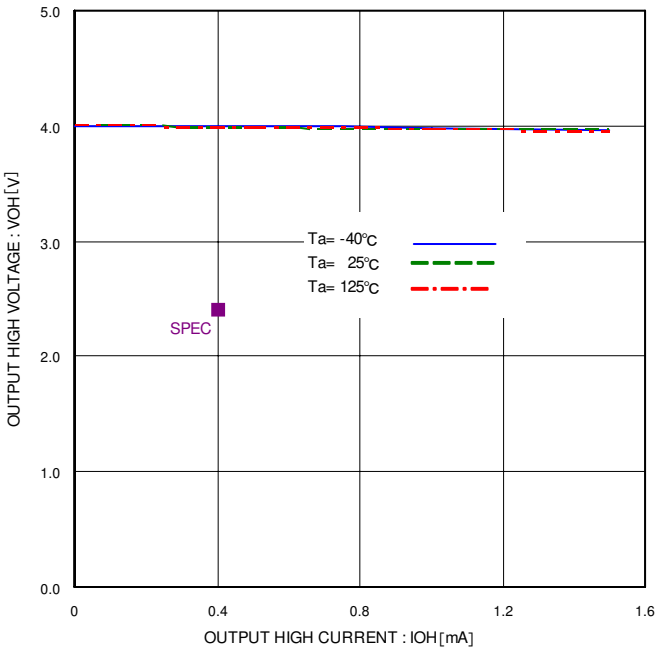

Figure 9. Output High Voltage vs. Output High Current (V_{CC}=4.0V)

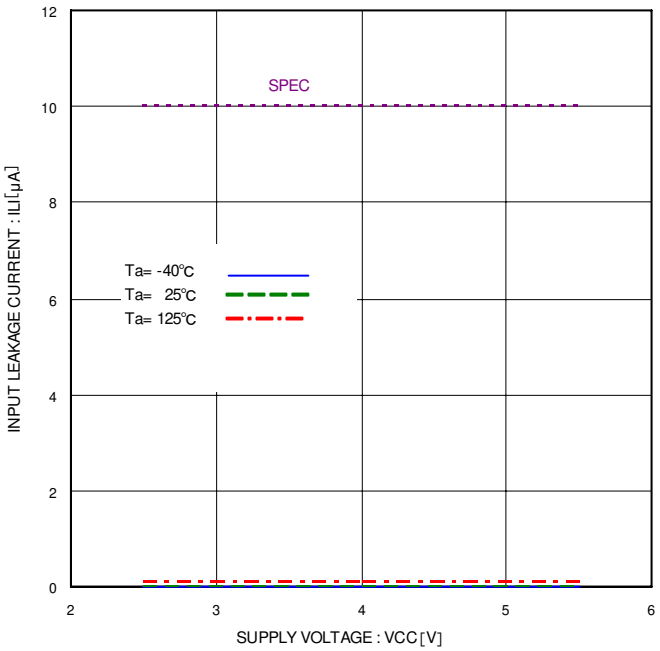

Figure 10. Input Leak Current (CS, SK, DI) vs. Supply Voltage

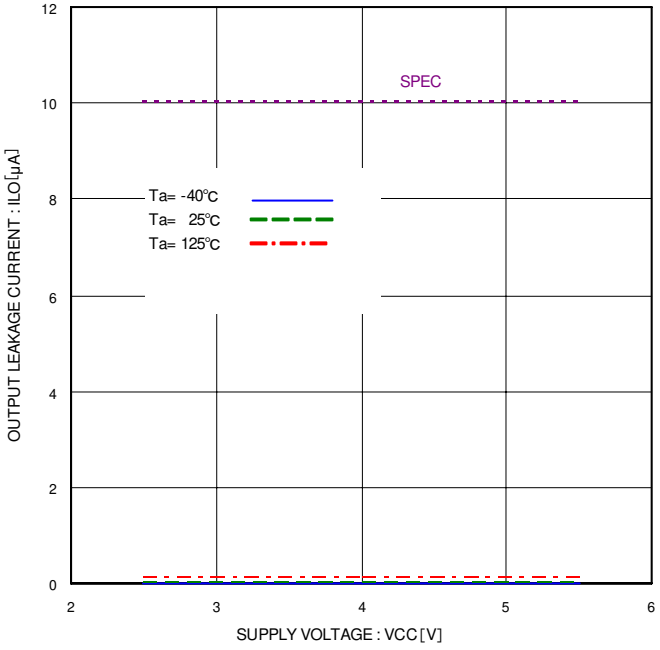

Figure 11. Output Leak Current (DO) vs. Supply Voltage

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Typical Performance Curves - Continued

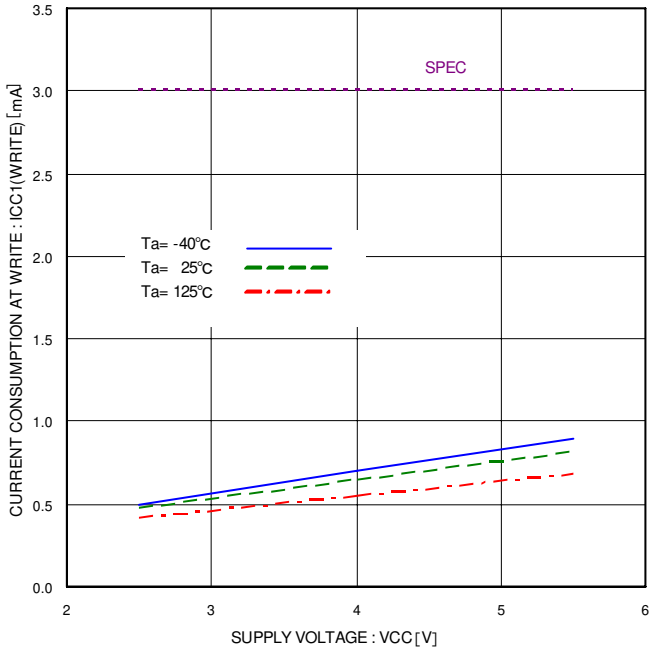

Figure 12. Supply Current at WRITE Operation vs. Supply Voltage (WRITE, f_{SK}=2.0MHz)

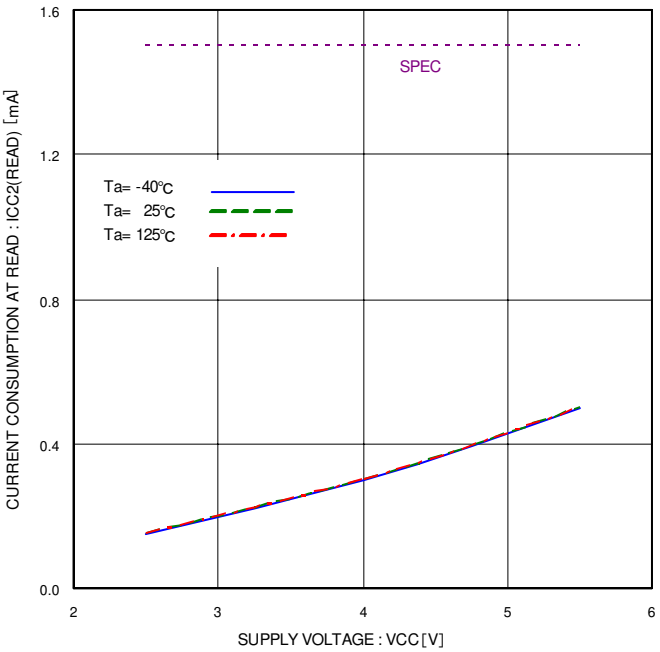

Figure 13. Supply Current at READ Operation vs. Supply Voltage (READ, f_{SK}=2.0MHz)

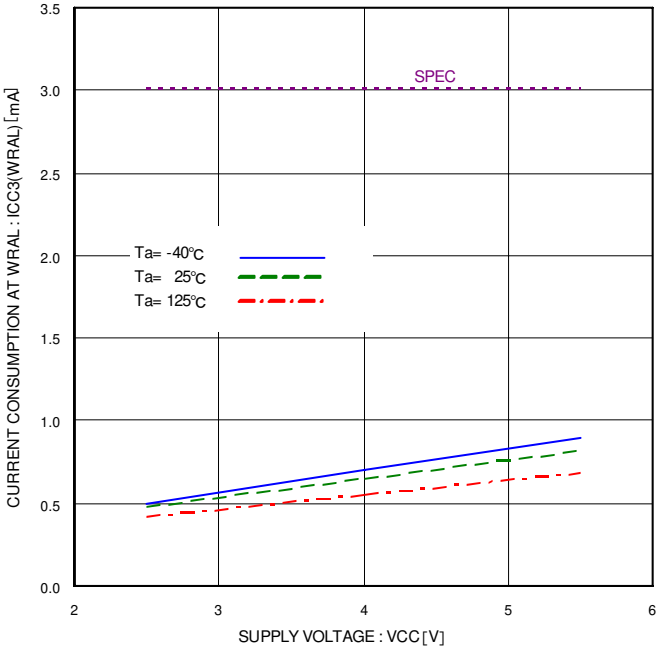

Figure 14. Supply Current at WRAL Operation vs. Supply Voltage (WRAL, f_{SK}=2.0MHz)

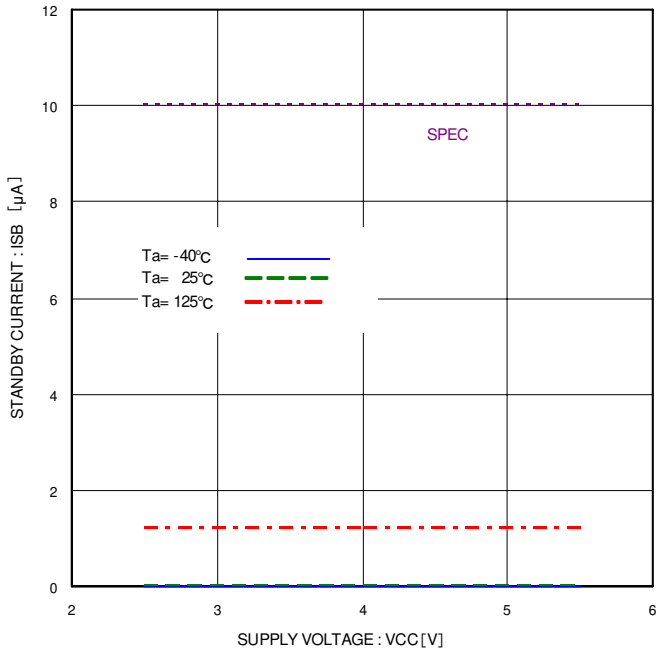

Figure 15. Standby Current vs. Supply Voltage

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Typical Performance Curves - Continued

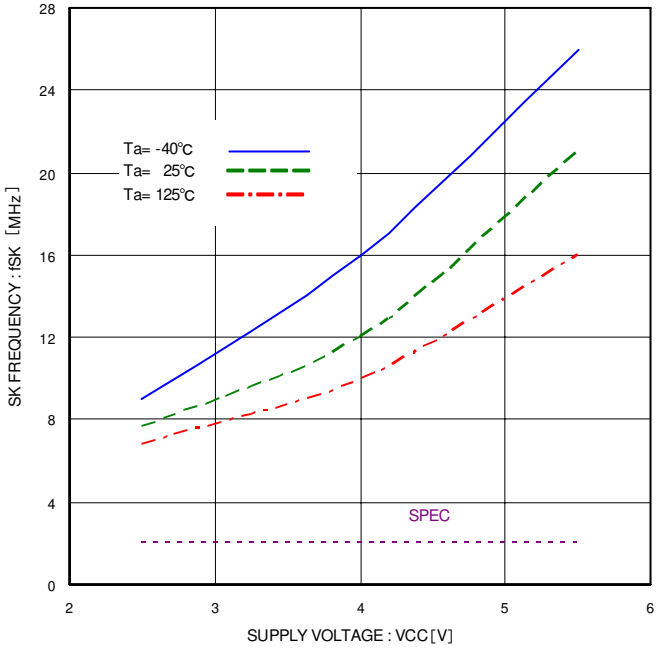

Figure 16. SK Frequency vs. Supply Voltage

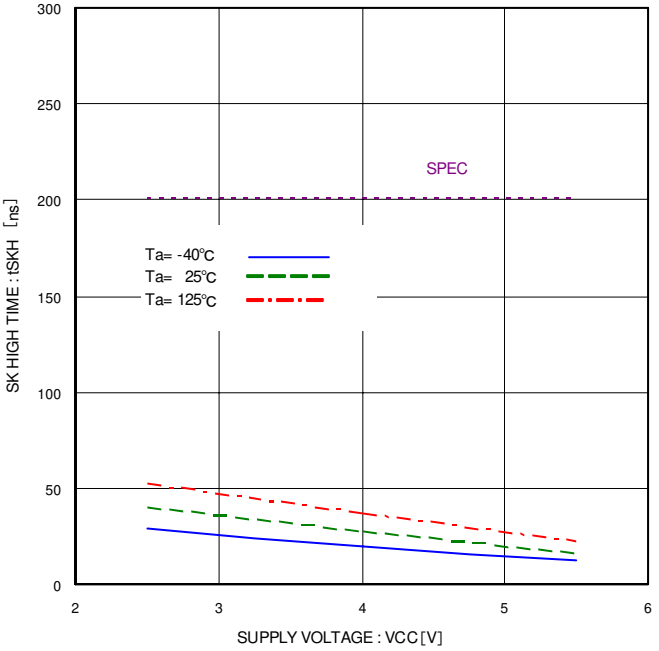

Figure 17. SK High Time vs. Supply Voltage

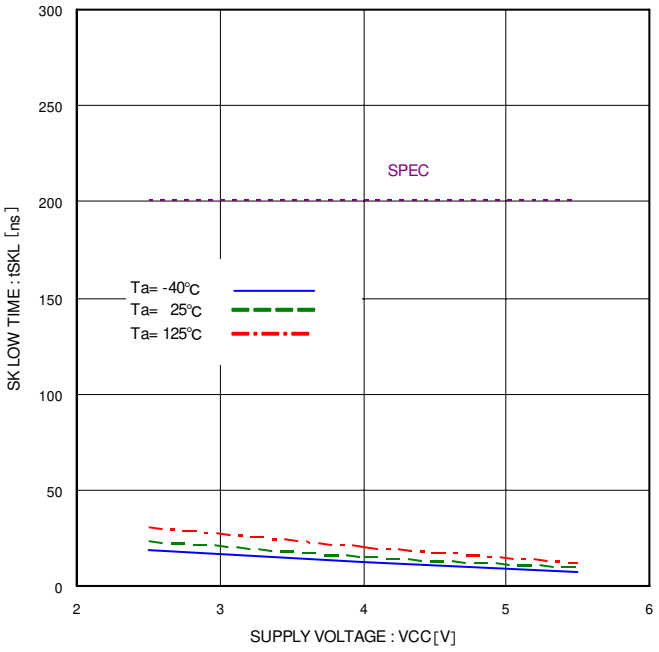

Figure 18. SK Low Time vs. Supply Voltage

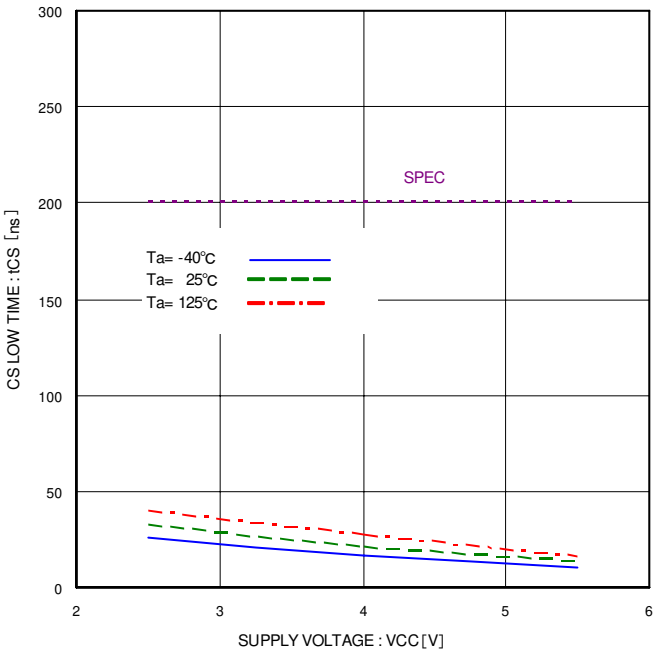

Figure 19. CS Low Time vs. Supply Voltage

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Typical Performance Curves - Continued

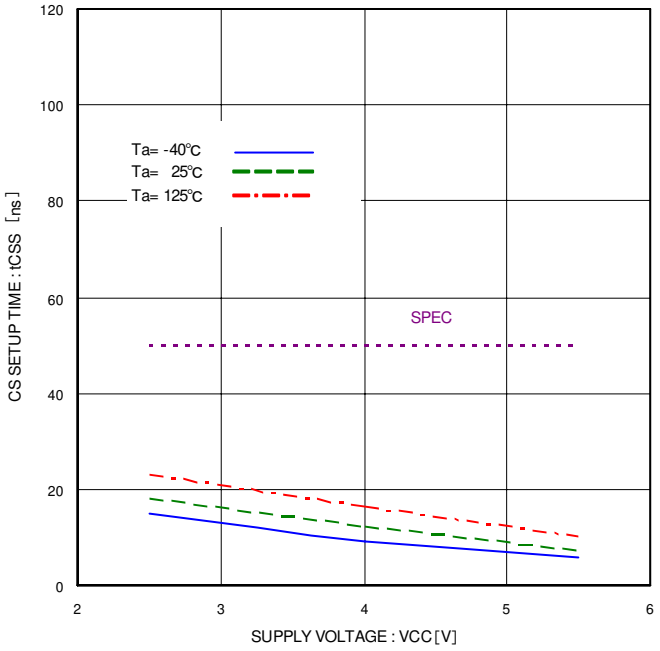

Figure 20. CS Setup Time vs. Supply Voltage

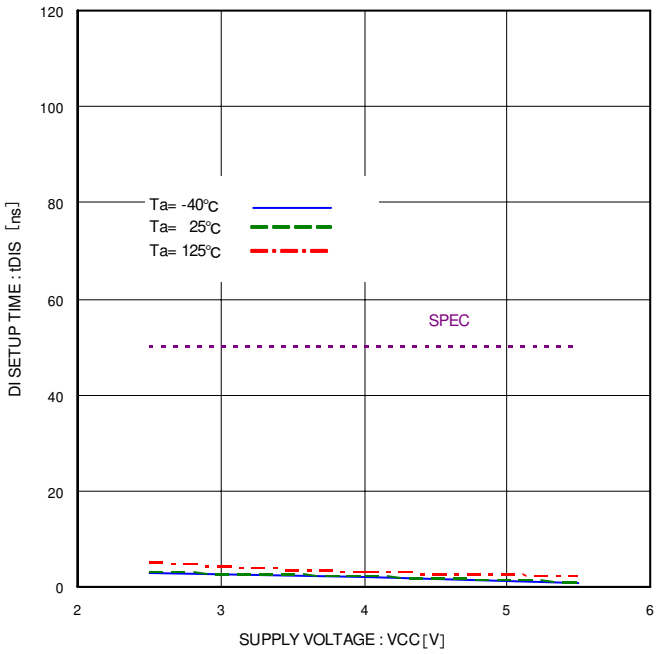

Figure 21. DI Setup Time vs. Supply Voltage

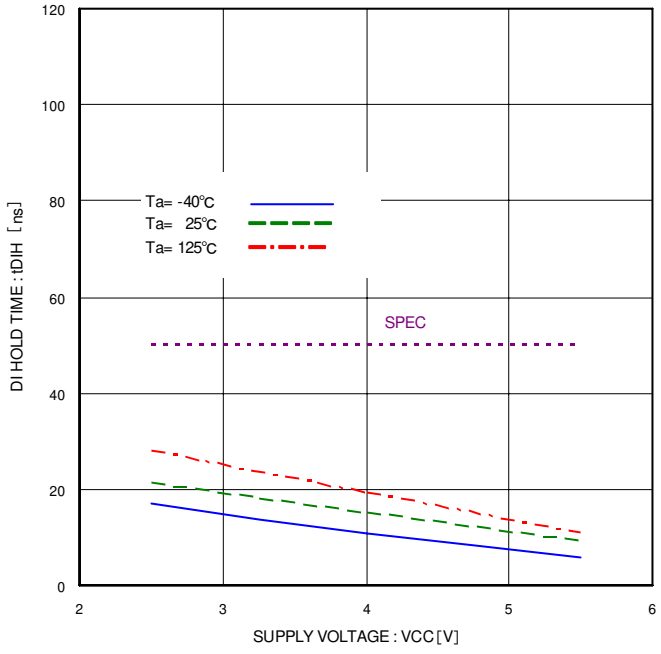

Figure 22. DI Hold Time vs. Supply Voltage

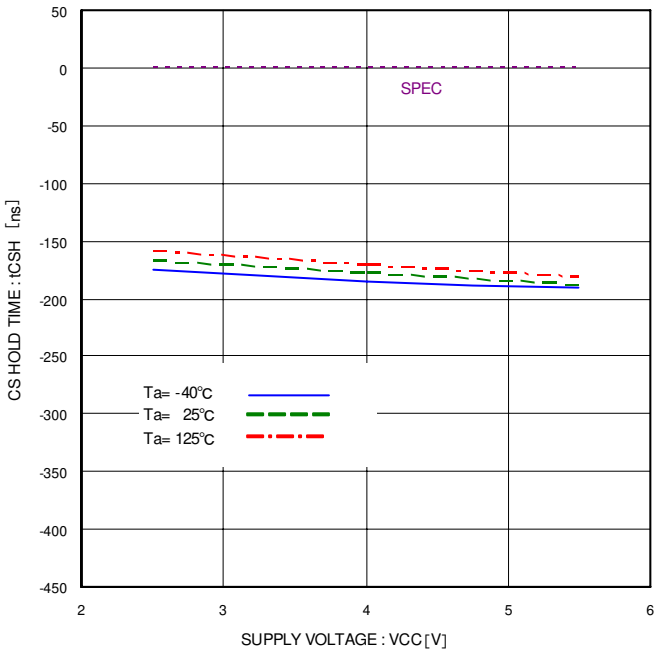

Figure 23. CS Hold Time vs. Supply Voltage

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Typical Performance Curves - Continued

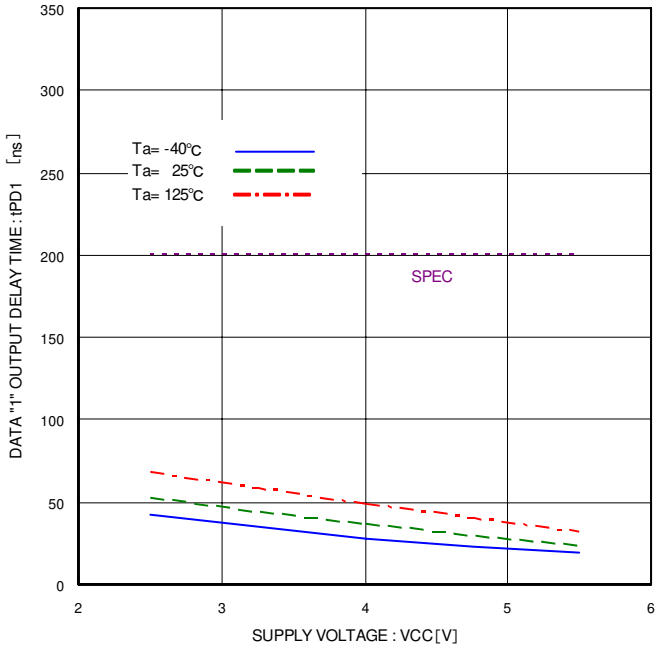

Figure 24. Data "1" Output Delay Time vs. Supply Voltage

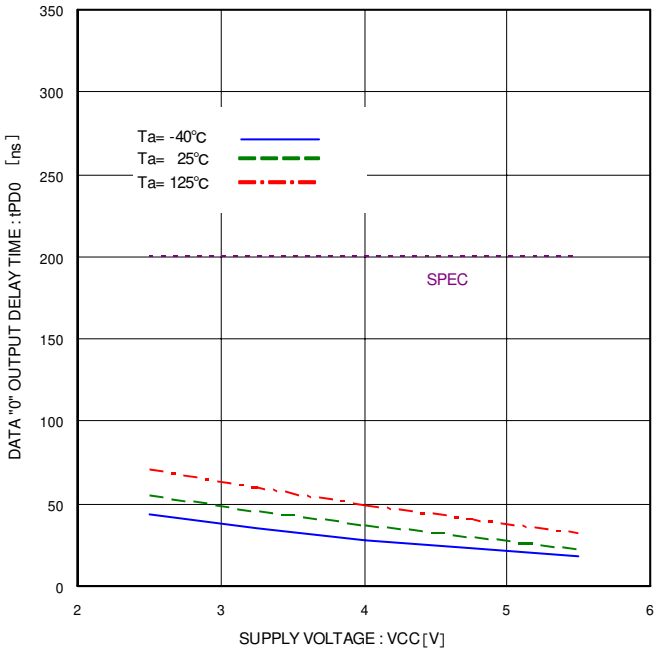

Figure 25. Data "0" Output Delay Time vs. Supply Voltage

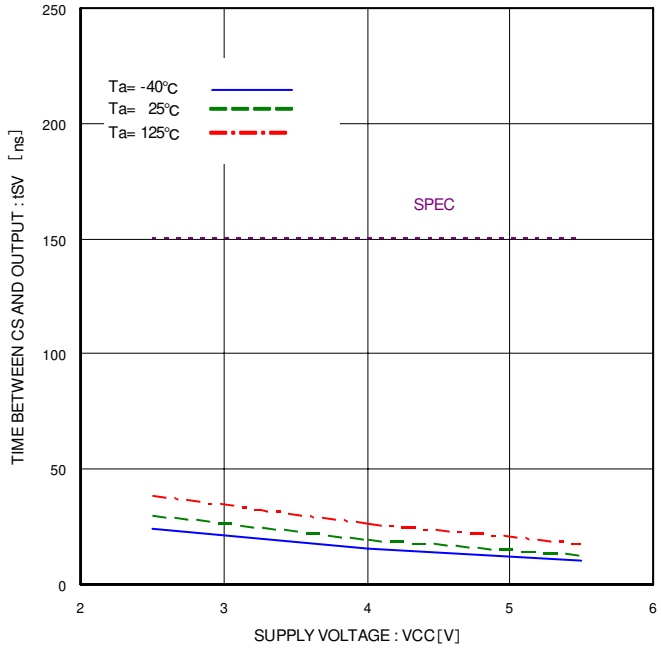

Figure 26. Time from CS Output establishment vs. Supply Voltage

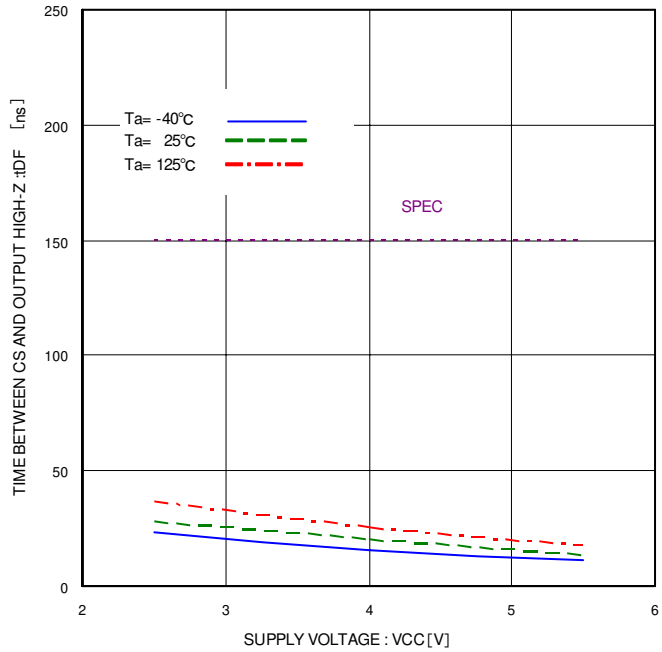

Figure 27. Time from CS to High-Z vs. Supply Voltage

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Typical Performance Curves - Continued

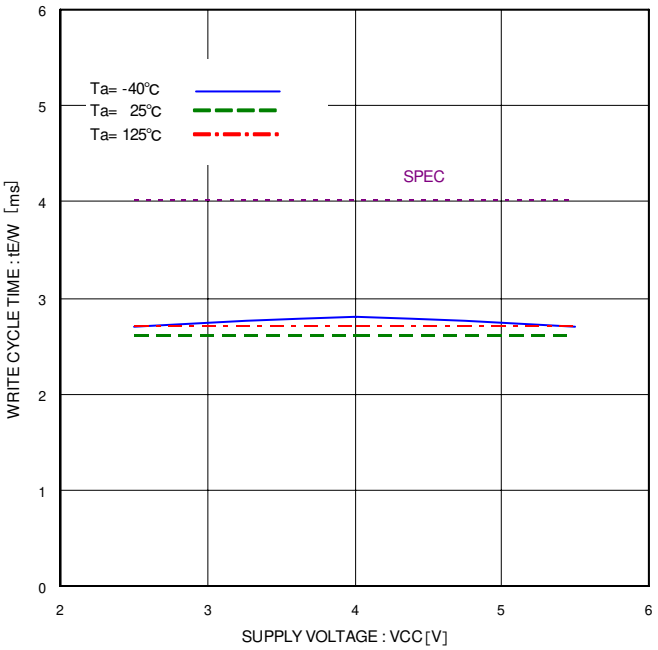

Figure 28. Write Cycle Time vs. Supply Voltage

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Description of Operation

Communications of the Microwire Bus are carried out by SK (serial clock), DI (serial data input), DO (serial data output), and CS (chip select) for device selection.

In connecting one EEPROM to a microcontroller, connect it as shown in Figure.29-(a) or Figure.29-(b). And, when using the input and output common I/O port of the microcontroller, connect DI and DO via a resistor as shown in Figure.29-(b) (Refer to pages 19-20), wherein connection by 3 lines is possible.

In case of using multiple EEPROM devices, refer to Figure. 29-(c).

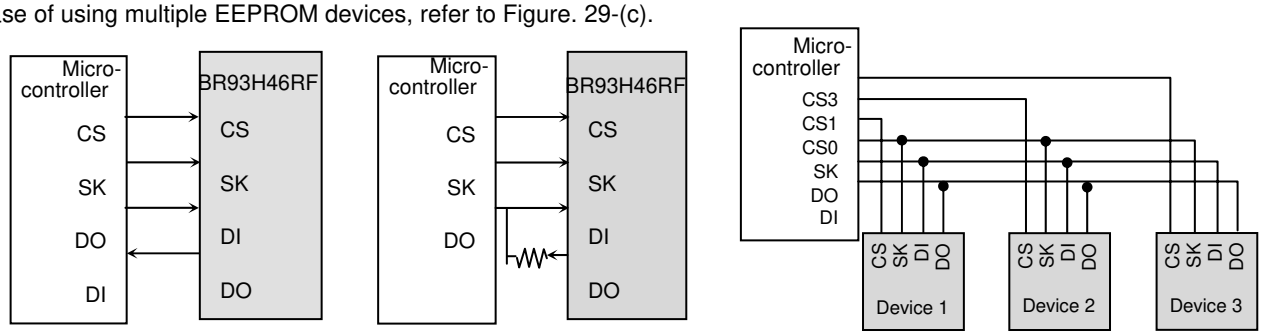

Figure 29-(a). Connection by 4 lines Figure 29-(b). Connection by 3 lines Figure 29-(c). Connection example of multiple devices

Figure 29. Connection Methods with Microcontroller

Communications of the Microwire Bus are started by the first “1” input after the rise of CS. This input is called the “Start Bit”. After input of the start bit, the “Ope Code”, Address, and Data are then inputted consecutively. Address and Data are all inputted with MSB first.
All “0” signal inputs after the rise of CS up to the start bit is ignored. Therefore, if there is a limitation in the bit width of PIC of the microcontroller, it is possible to input “0” before the start bit to control the bit width.

Command Mode

Command	Start bit	Ope code	Address	Data
			BR93H46RF-2LB	
Read (READ) *1	1	10	A5,A4,A3,A2,A1,A0	D15 to D0(READ DATA)
Write enable (WEN)	1	00	1 1 * * * *	—
Write (WRITE) *2	1	01	A5,A4,A3,A2,A1,A0	D15 to D0(WRITE DATA)
Write all (WRAL) *2	1	00	0 1 * * * *	D15 to D0(WRITE DATA)
Write disable (WDS)	1	00	0 0 * * * *	—

- Input the address and the data in MSB-first order.
- As for *, input either V_{IH} or V_{IL}.

*Start bit
Acceptance of all the commands of this IC starts at recognition of the start bit.
The “Start Bit” means the first “1” input after the rise of CS.

*1 For READ, after setting the command, the data output of the selected address starts. Then, in a sequential order of addresses, the data of the next address will be outputted , and will continuously output data of succeeding addresses with the use of a continuous SK clock input. (Auto-Increment Function)

*2 When the WRITE and the WRITE-All commands are executed, the previous data written in the selected memory cell are automatically deleted first, then the input data is written next.

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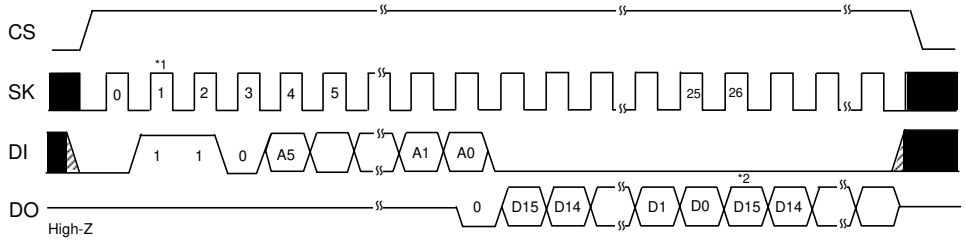
Timing Chart

1) Read Cycle (READ)



*1 Start bit
When data "1" is input for the first time after the rise of CS, this will be recognized as the start bit. And, even if multiple "0" are input after the rise of CS, the first "1" input will still be recognized as the start bit, and the following operation starts. This is common to all the commands that will be discussed hereafter.

*2 The succeeding address' data output
(Auto-Increment Function)

Figure 30. Read Cycle

○When the READ command is recognized, the data (16bit) of the selected address is output to serial. And at that moment, "0" (dummy bit) is output first, in sync with address bit A0 and with the rise of SK. Afterwhich, the main data is output in sync with the rise of SK.
This IC has Address Auto Increment Function available only for READ command, wherein after executing READ command on the first selected address, the data of the next address is read. And this will continue in a sequential order of addresses with the use of a continuous SK clock input, and by keeping CS at "H" during auto-increment.

2) Write Cycle (WRITE)

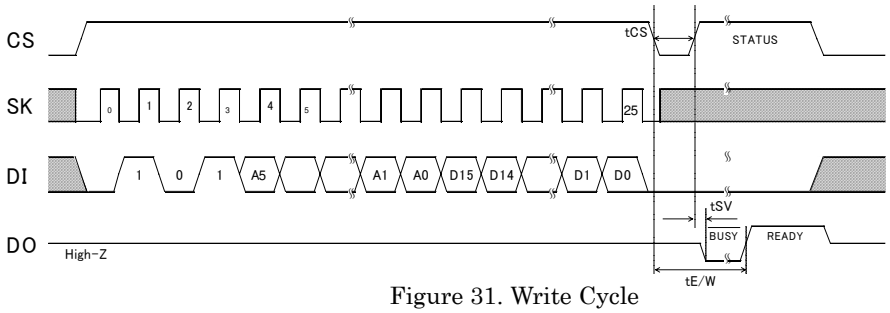


Figure 31. Write Cycle

○In this command, input 16-bit data (D15 to D0) are written to a designated address (A5 to A0). The actual write starts from the fall of CS, after D0 is sampled with SK clock (25th clock from the start bit input), to the rise of the 26th clock.
When STATUS is not detected (CS="L" fixed), WRITE time is 4ms (Max.) in conformity with tE/W. And when STATUS is detected (CS="H"), all commands are not accepted for areas where "L" ($\overline{\text{BUSY}}$) is output from D0. Therefore, do not input any command.
Write is not made or canceled if CS starts to fall after the rise of the 26th clock.
Note: Take tSKH or more from the rise of the 25th clock to the fall of CS.

3) Write all cycle (WRAL)

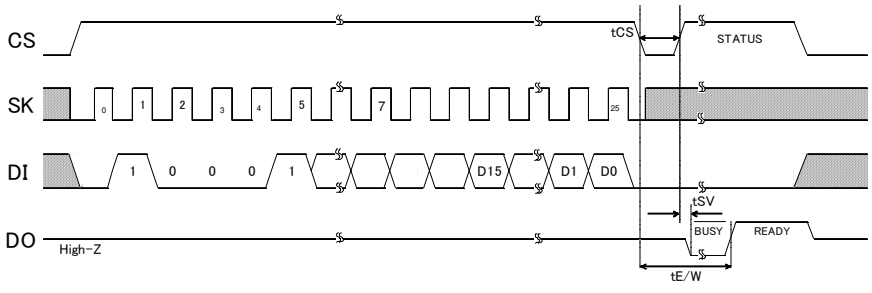


Figure 32. Write All Cycle

○In this command, input 16-bit data is written simultaneously to all addresses. Data is written in bulk at a write time of only 4ms (Max.) in conformity with tE/W.
The actual write starts from the fall of CS, after D0 is sampled with SK clock (25th clock from the start bit input), to the rise of the 26th clock. If CS was ended after the rise of the 26th clock, command is canceled, and write is not completed.
Note:Take tSKH or more from the rise of the 25th clock to the fall of CS.

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4) Write Enable (WEN) / Disable (WDS) Cycle

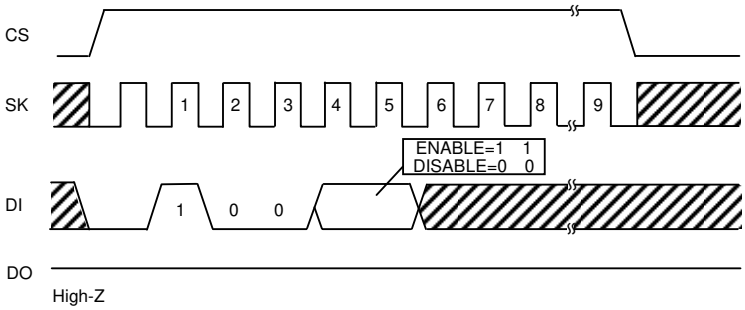


Figure 33. Write Enable (WEN) / Disable (WDS) Cycle

○At power on, this IC is in Write Disable status by the internal RESET circuit. Before executing the WRITE command, it is necessary to execute the Write Enable command first. And, once this command is executed, writing is valid unitl the Write Disable command is executed or the power is turned off. However, the READ command is valid regardless of whether Write Enable / Disable command is executed. Input to SK after 6 clocks of this command is available by either "H" or "L", but be sure to input it.

○When the Write Enable command is executed after power on, Write Enable status gets in. When the Write Disable command is executed then, the IC gets in Write Disable status as same as at power on, and then the WRITE command is canceled thereafter in software manner. However, the READ command is still executable. In Write Enable status, even when the WRITE command is input by mistake, writing will still continue. To prevent such a mistake, it is recommended to execute the Write Disable command after the completion of each WRITE execution.

Application

1) Method to cancel each command

○READ

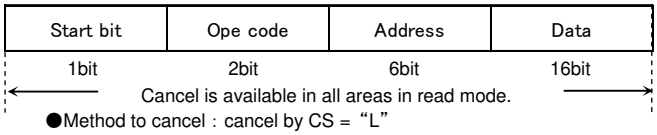
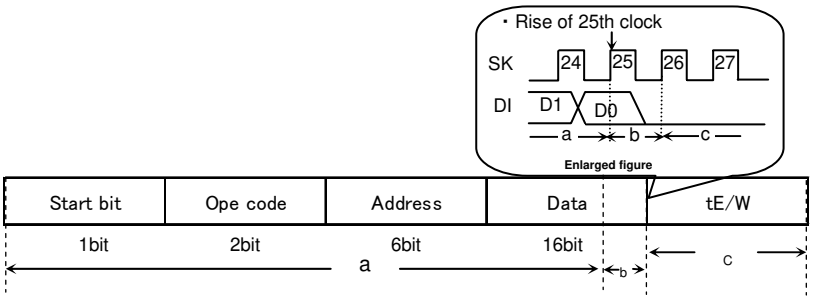


Figure 34. READ Cancel Available Timing

○WRITE, WRAL



a : From start bit to 25th clock rise
Cancel by CS="L"

b : 25th clock rise and after
Cancellation is not available by any means. If Vcc is turned OFF in this area, designated address data is not guaranteed, therefore write once again.

c : 26th clock rise and after
Cancel by CS="L"
However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is input continuously, cancellation is not available.

Note 1) If V_{CC} is turned OFF in this area, designated address data is not guaranteed. Therefore, it is recommended to execute WRITE once again.

Note 2) If CS is started at the same timing as that of the SK rise, WRITE execution/cancel becomes unstable. Therefore, it is recommended to set CS to "L" in SK="L" area. As for SK rise, recommended timing is of t_{CSS}/t_{CSH} or higher.

Figure 35. WRITE, WRAL Cancel Available Timing

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2) I/O Equivalent Circuit

○Output Circuit

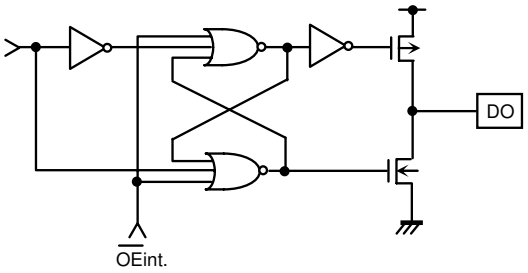

Figure 36. Output Circuit (DO)

○Input Circuit

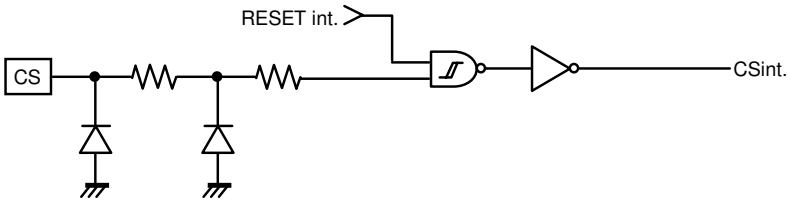

Figure 37. Input Circuit (CS)

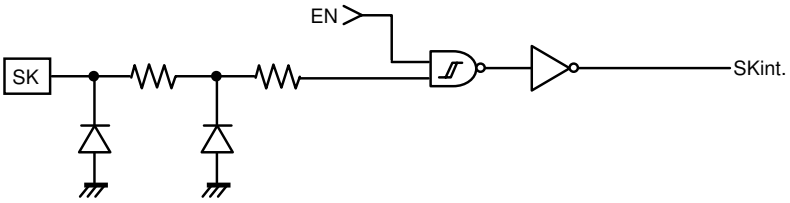

Figure 38. Input Circuit (SK)

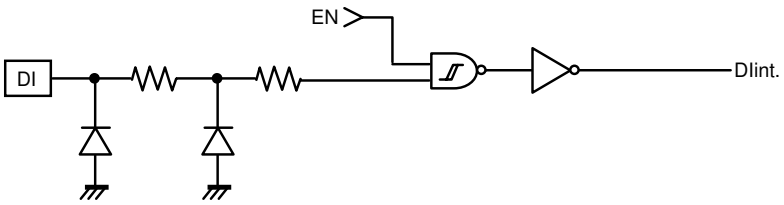

Figure 39. Input Circuit (DI)

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3) I/O Peripheral Circuit

3-1) Pull Down CS

By making CS="L" at power ON/OFF, mistake in operation and mistake write are prevented.

○Pull Down Resistance R_{pd} of CS pin

To prevent mistake in operation and mistake write at power ON/OFF, a CS pull-down resistor is necessary. Select an appropriate resistance value from microcontroller's V_{OH}, I_{OH} and this IC's VIH characteristics.

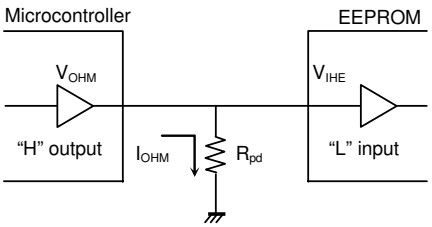

Figure 40. CS Pull-down Resistance

$$R_{pd} \geqq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ①$$

$$V_{OHM} \geqq V_{IHE} \quad \cdots ②$$

Example) When V_{CC} =5V, V_{IHE}=3.5V, V_{OHM}=4.0V, I_{OHM}=2mA, from the equation ①,

$$R_{pd} \geqq \frac{4.0}{2 \times 10\text{-}3}$$

$$\therefore \quad R_{pd} \geqq 2.0\ [k\Omega]$$

With the value of Rpd satisfying the equation above, V_{OHM} becomes 4.0V or higher, and with V_{IHE} (=3.5V), equation ② is also satisfied.

- V_{IHE} : EEPROM VIH specifications
- V_{OHM} : Microcontroller V_{OH} specifications
- I_{OHM} : Microcontroller I_{OH} specifications

3-2) DO is available for both pull up and pull down.

DO output is "High-Z" except during READY / $\overline{BUSY}$ output timing in WRITE command and, after data output at READ command. When malfunction occurs at "High-Z" input of the microcontroller port connected to DO, it is necessary to pull down and pull up DO. When there is no influence upon the microcontroller actions, DO may be left OPEN. If DO is OPEN during a transition of output from BUSY to $\overline{READY}$ status, and at an instance where CS="H", SK="H", DI="H", EEPROM recognizes this as a start bit, resets READY output, and sets DO="High-Z". Therefore, READY signal cannot be detected. To avoid such output, pull up DO pin for improvement.

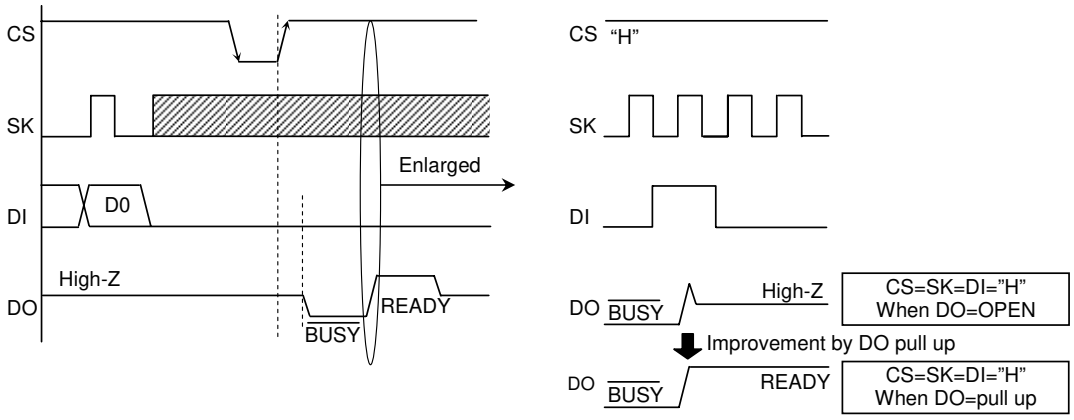

Figure 41. READY Output Timing at DO=OPEN

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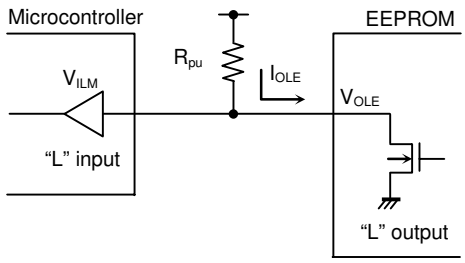
○Pull up Resistance Rpu and Pull-down Resistance Rpd of DO pin

As for pull up and pull down resistance value, select an appropriate value to this resistance value from microcontroller V_{IH}, V_{IL}, and V_{OH}, I_{OH}, V_{OL}, I_{OL} characteristics of this IC.



・V_{OLE}
・I_{OLE}
・V_{ILM}

Figure 42. DO Pull Up Resistance

$$R_{pu} \geqq \frac{V_{CC}-V_{OLE}}{I_{OLE}} \quad \cdot\cdot\cdot ③$$

$$V_{OLE} \leqq V_{ILM} \quad \cdot\cdot\cdot ④$$

Example) When V_{CC} =5V, V_{OLE}=0.4V, I_{OLE}=2.1mA, V_{ILM}=0.8V, from the equation ③,

$$R_{pu} \geqq \frac{5-0.4}{2.1\times 10\text{-}3}$$

$$\therefore \quad R_{pu} \geqq 2.2\ [k\Omega]$$

With the value of R_{pu} to satisfy the above equation, V_{OLE} becomes 0.4V or below, and with V_{ILM}(=0.8V), the equation ④ is also satisfied.

・V_{OLE} : EEPROM V_{OL} specifications
・I_{OLE} : EEPROM I_{OL} specifications
・V_{ILM} : Microcontroller V_{IL} specifications

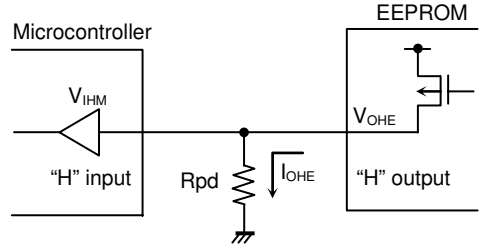


Figure 43. DO Pull Down Resistance

$$R_{pd} \geqq \frac{V_{OHE}}{I_{OHE}} \quad \cdot\cdot\cdot ⑤$$

$$V_{OHE} \geqq VI_{HM} \quad \cdot\cdot\cdot ⑥$$

Example) When V_{CC} =5V, V_{OHE}=4.8V, I_{OHE}=0.1mA, V_{IHM}=3.5V from the equation ⑤

$$R_{pd} \geqq \frac{5-0.2}{0.1\times 10\text{-}3}$$

$$\therefore \quad R_{pd} \geqq 48\ [k\Omega]$$

With the value of R_{pd} to satisfy the above equation, V_{OHE} becomes 4.8V or below, and with V_{IHM} (=3.5V), the equation ⑥ is also satisfied.

・V_{OHE} : EEPROM VOH specifications
・I_{OHE} : EEPROM IOH specifications
・V_{IHM} : Microcontroller VIH specifications

○READY / $\overline{BUSY}$ Status Display (DO terminal)

This display outputs the internal status signal. When CS is started after t_{CS} (Min.200ns) from CS fall after write command input, "H" or "L" output.

R/$\overline{B}$ display="L" ($\overline{BUSY}$) = write under execution

(DO status) After the timer circuit in the IC works and creates the period of $t_{E/W}$, this time circuit completes automatically. And write to the memory cell is made in the period of $t_{E/W}$, and during this period, other command is not accepted.

R/$\overline{B}$ display = "H" (READY) = command wait status

(DO status) Even after $t_{E/W}$ (max.4ms) from write of the memory cell, the following command is accepted. Therefore, CS="H" in the period of $t_{E/W}$, and when input is in SK, DI, malfunction may occur. Therefore, set DI="L" in the area CS="H". (Especially, in the case of shared input port, attention is required.)

*Do not input any command while status signal is output. Command input in $\overline{BUSY}$ area is canceled, but command input in READY area is accepted. Therefore, status READY output is canceled, and malfunction and mistake write may be made.

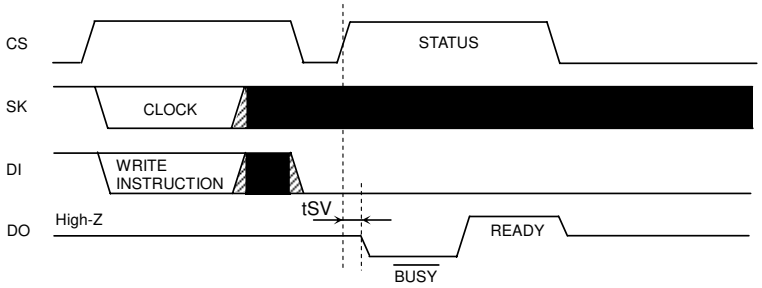


Figure 44. R/B Status Output Timing Chart

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4) When to directly connect DI and DO

This IC has independent input terminal DI and output terminal DO, wherein signals are handled separately on timing chart. But, by inserting a resistance R between these DI and DO terminals, it is possible to carry out control by only 1 control line.

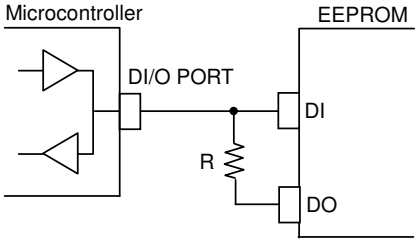

Figure 45. DI, DO Control Line Common Connection

○Data collision of microcontroller DI/O output and DO output and feedback of DO output to DI input.

Drive from the microcontroller DI/O output to DI input on I/O timing, and signal output from DO output occur at the same time in the following points.

4-1) 1 Clock cycle to take in A0 address data at read command

Dummy bit “0” is output to DO terminal.

→When address data A0 = “1” input, through current route occurs.

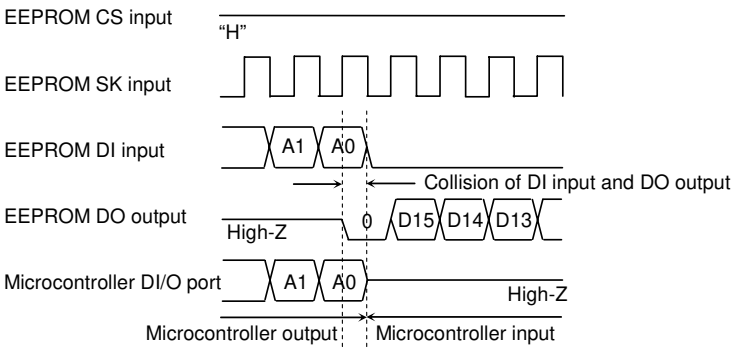

Figure 46. Collision timing at read data output at DI, DO direct connection

4-2) Timing of CS = “H” after write command. DO terminal in READY / $\overline{\text{BUSY}}$ function output.

When the next start bit input is recognized, “HIGH-Z” gets in.

→Especially, at command input after write, when CS input is started with microcontroller DI/O output “L”, READY output “H” is output from DO terminal, and through current route occurs.

Feedback input at timing of these 4-1) and 4-2) does not cause disorder in basic operations, if resistance R is inserted.

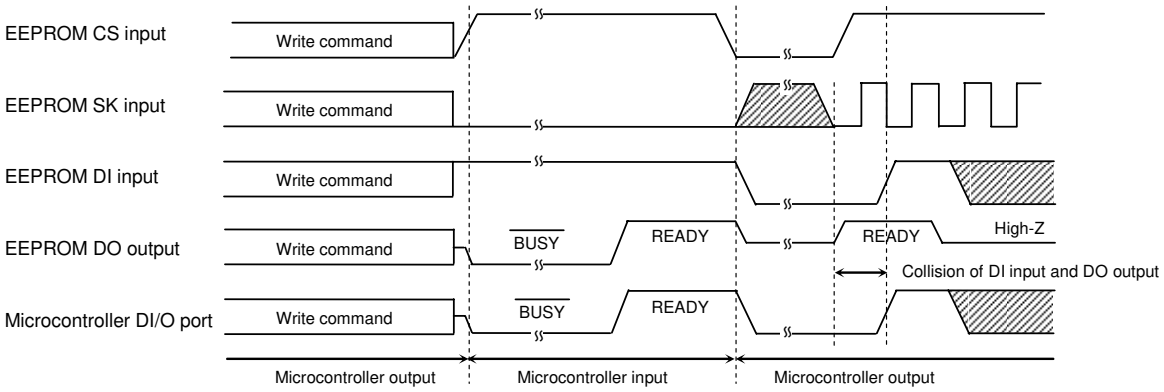

Figure 47. Collision timing at DI, DO Direct Connection

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○Selection of Resistance value R

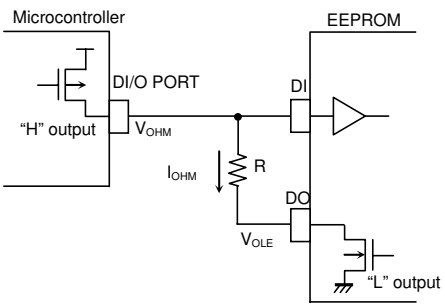
The resistance R becomes through current limit resistance at data collision. When through current flows, noises of power source line and instantaneous stop of power source may occur. When allowable through current is defined as I, the following relation should be satisfied. Determine allowable current amount in consideration of impedance and so forth of power source line in set. And insert resistance R, and set the value R to satisfy EEPROM input level V_{IH}/V_{IL}, even under influence of voltage decline owing to leak current and so forth. Insertion of R will not cause any influence upon basic operations.

4-3) Address data A0 = "1" input, dummy bit "0" output timing

(When microcontroller DI/O output is "H", EEPROM DO outputs "L", and "H" is input to DI)

・Make the through current to EEPROM 10mA or below.

・See to it that the input level V_{IH} of EEPROM should satisfy the following.



Conditions

$V_{OHM} \leqq V_{IHE}$

$V_{OHM} \leqq I_{OHM} \times R + V_{OLE}$

At this moment, if V_{OLE}=0V,

$V_{OHM} \leqq I_{OHM} \times R$

$$\therefore \quad R \geqq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ⑦$$

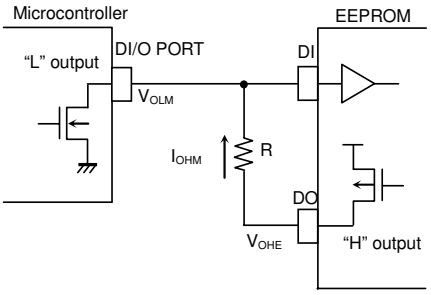
・V_{IHE} : EEPROM V_{IH} specifications
・V_{OLE} : EEPROM V_{OL} specifications
・V_{OHM} : Microcontroller V_{OH} specifications
・I_{OHM} : Microcontroller I_{OH} specifications

Figure 48. Circuit at DI, DO Direct Connection (Microcontroller DI/O "H" Output, EEPROM "L" output)

4-4) DO status READY output timing

(When the microcontroller DI/O is "L", EEPROM DO outputs "H", and "L" is input to DI)

・Set the EEPROM input level V_{IL} so as to satisfy the following.



Conditions

$V_{OLM} \geqq V_{ILE}$

$V_{OLM} \geqq V_{OHE} - I_{OLM} \times R$

As this moment, if V_{OHE}=Vcc,

$V_{OLM} \geqq V_{CC} - I_{OLM} \times R$

$$\therefore \quad R \geqq \frac{V_{CC} - V_{OLM}}{I_{OLM}} \quad \cdots ⑧$$

・V_{ILE} : EEPROM V_{IL} specifications
・V_{OHE} : EEPROM V_{OH} specifications
・V_{OLM} : Microcontroller VOL specifications
・I_{OLM}

Example) When V_{CC}=5V, V_{OHM}=5V, I_{OHM}=0.4mA, V_{OLM}=0.4V, I_{OLM}=2.1mA,

From the equation ⑦,

$$R \geqq \frac{V_{OHM}}{I_{OHM}}$$

$$R \geqq \frac{5}{0.4 \times 10\text{-}3}$$

$$\therefore \quad R \geqq 12.5\ [k\Omega] \quad \cdots ⑨$$

From the equation ⑧,

$$R \geqq \frac{V_{CC} - V_{OLM}}{I_{OLM}}$$

$$R \geqq \frac{5 - 0.4}{2.1 \times 10\text{-}3}$$

$$\therefore \quad R \geqq 2.2\ [k\Omega] \quad \cdots ⑩$$

Therefore, from the equations ⑨ and ⑩,

$$\therefore \quad R \geqq 12.5\ [k\Omega]$$

Figure 49. Circuit at DI, DO Direct Connection (Microcontroller DI/O "L" output, EEPROM "H" output)

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5) Power-Up/Down Conditions

・At power ON/OFF, set CS “L”.

When CS is “H”, this IC gets in input accept status (active). At power ON, set CS “L” to prevent malfunction from noise. (When CS is in “L” status, all inputs are canceled.) At power decline low power status may prevail. Therefore, at power OFF, set CS “L” to prevent malfunction from noise.

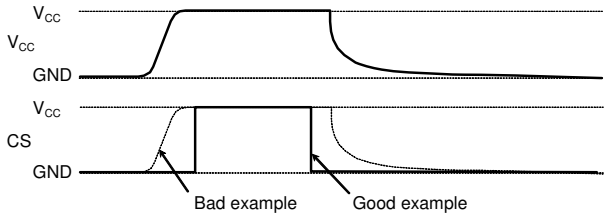


Figure 50. Timing at Power ON/OFF

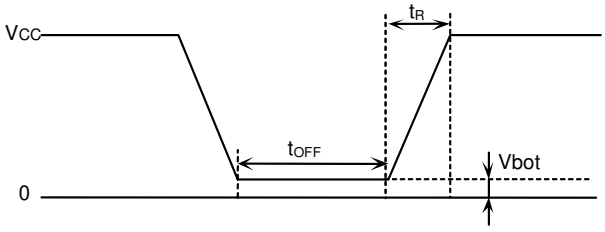
(Bad example) CS pin is pulled up to Vcc.
In this case, CS becomes “H” (active status), EEPROM may malfunction or have write error due to noises. This is true even when CS input is High-Z.

(Good example) It is “L” at power ON/OFF.
Set 10ms or higher to recharge at power OFF.
When power is turned on without observing this condition, IC internal circuit may not be reset.

○POR circuit

This IC has a POR (Power On Reset) circuit as a mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is “H” at power ON/OFF, it may become write enable status owing to noises and the likes. For secure actions, observe the following conditions.

1. Set CS=”L”
2. Turn on power so as to satisfy the recommended conditions of t_R, t_{OFF}, Vbot for POR circuit action.



Recommended conditions of tR, tOFF,

t_R	t_{OFF}	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Figure 51. Rise Waveform Diagram

○LV_{CC} Circuit

LV_{CC} (V_{CC}-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.
At LV_{CC} voltage (Typ=1.9V) or below, it prevents data rewrite.

6) Noise Countermeasures

○V_{CC} Noise (Bypass Capacitor)

When noise or surge gets in the power source line, malfunction may occur. Therefore, in removing these, it is recommended to attach a bypass capacitor (0.1 μF) between IC V_{CC} and GND as close to IC as possible. It is also recommended to attach a bypass capacitor between board V_{CC} and GND.

○SK Noise

When the rise time (tR) of SK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement.
To avoid this, a Schmitt trigger circuit is built in SK input. The hysteresis width of this circuit is set about 0.2V. If noise exists at SK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time (t_R) of S_K to 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

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Operational Notes

1. Described numeric values and data are design representative values, and the values are not guaranteed.

2. Application circuit
   Although we can recommend the application circuits contained herein with a relatively high degree of confidence, we ask that you verify all characteristics and specifications of the circuit as well as its performance under actual conditions. Please note that we cannot be held responsible for problems that may arise due to patent infringements or noncompliance with any and all applicable laws and regulations.

3. Absolute maximum ratings
   Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

4. Ground Voltage
   The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

5. Thermal consideration
   Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions. Consider Pc that does not exceed Pd in actual operating conditions (Pc≥Pd).

   Package Power dissipation : $Pd\ (W)=(Tjmax-Ta)/\theta ja$

   Power dissipation : $Pc\ (W)=(V_{CC}-Vo)\times Io+V_{CC}\times Ib$

   (Tjmax : Maximum junction temperature=150℃, Ta : Peripheral temperature[℃] ,
   θja : Thermal resistance of package-ambience[℃/W], Pd : Package Power dissipation [W],
   Pc : Power dissipation [W], V_{CC} : Input Voltage, Vo : Output Voltage, Io : Load, Ib : Bias Current)

6. Short between pins and mounting errors
   Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

7. Operation under strong electromagnetic field
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

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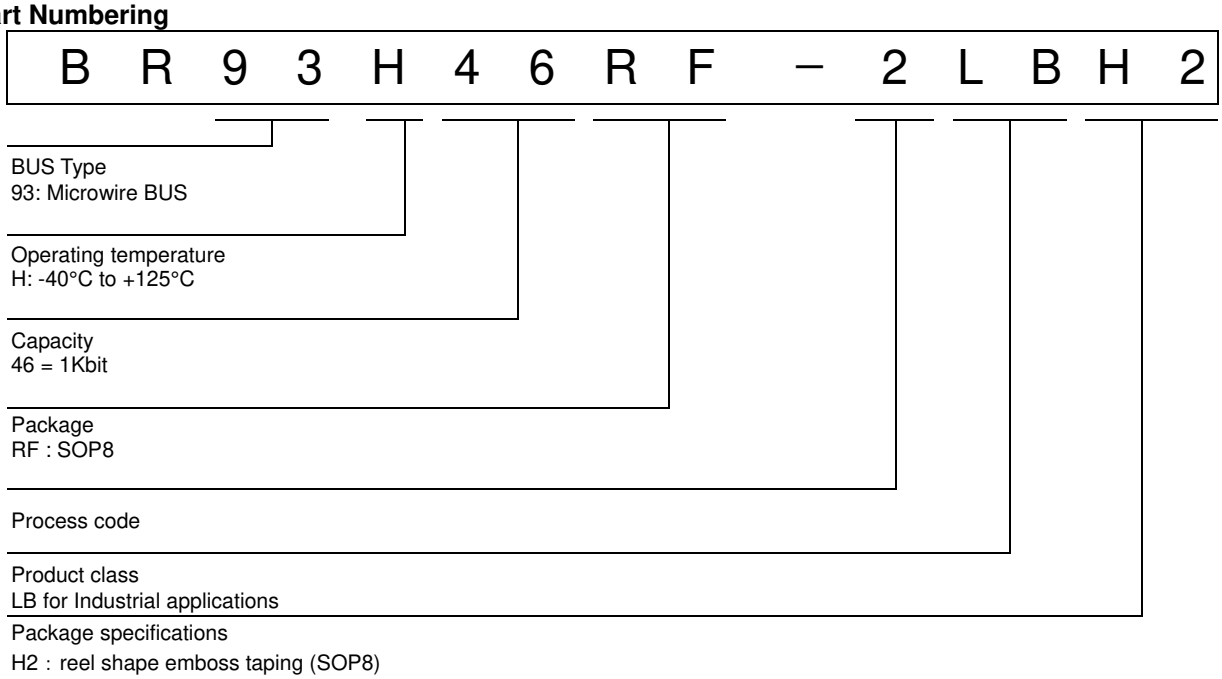
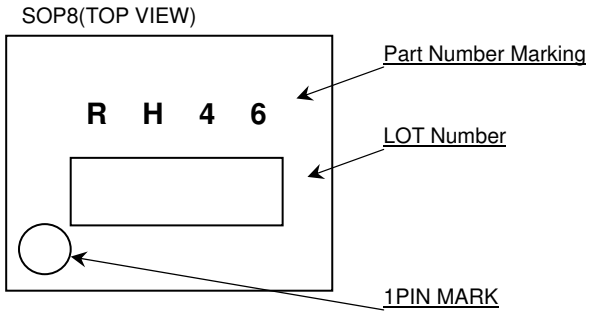
Part Numbering



Capacity	Package		Orderable Part Number
	Type	Quantity	
1K	SOP8	Reel of 250	BR93H46RF-2LBH2

Marking Diagram



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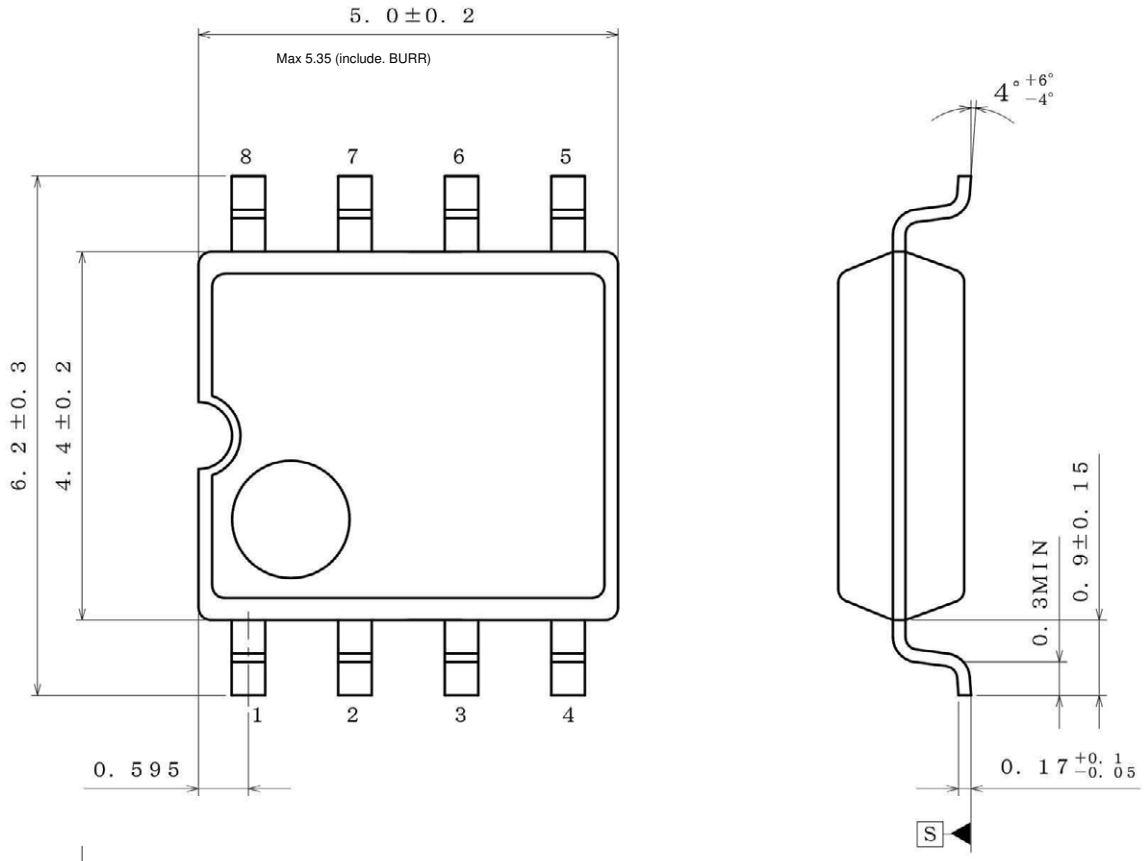
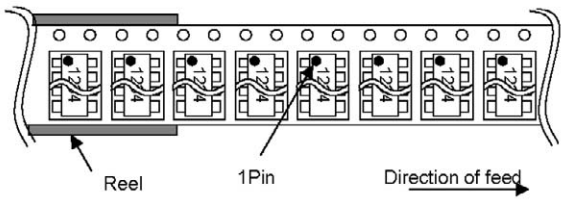
Physical Dimension Tape and Reel Information

Package Name	SOP8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	250pcs
Direction of feed	H2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
15.Nov.2013	001	New Release
27.Feb.2014	002	Delete sentence “and log life cycle” in General Description and Futures.

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