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OptiMOS™2 Power-Transistor
Features

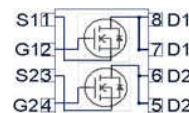
- Dual N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Low on-resistance $R_{DS(on)}$
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target application
- Ideal for high-frequency switching and synchronous rectification
- 100% avalanche tested
- Halogen-free according to IE61249-2-21


Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	75	m Ω
I_D	13	A

PG-TDSON-8


Type	Package	Marking
BSC750N10ND G	PG-TDSON-8	750N10ND


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			≤10 secs	steady state	
Continuous drain current	I_D	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	13		A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	8.5		
		$V_{GS}=10\text{ V}, T_A=25\text{ °C}^{3)}$	5.0	3.2	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	52		
Avalanche energy, single pulse	E_{AS}	$I_D=13\text{ A}, R_{GS}=25\text{ }\Omega$	17		mJ
Reverse diode dv/dt	dv/dt	$I_D=13\text{ A}, V_{DS}=80\text{ V},$ $di/dt=100\text{ A}/\mu\text{s},$ $T_{j,max}=150\text{ °C}$	6		kV/ μs
Gate source voltage	V_{GS}		±20		V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	26		W
		$T_A=25\text{ °C}^{3)}$	3.6	1.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

¹⁾ J-STD20 and JESD22

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}	bottom	-	-	4.9	K/W
		top			20	
Thermal resistance, junction - ambient, 6 cm ² cooling area ³⁾	R_{thJA}	t≤10 s	-	-	35	
		steady state	-	-	85	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=12\text{ }\mu\text{A}$	2	3	4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=13\text{ A}$	-	62	75	m Ω
Gate resistance	R_G		-	0.8	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=13\text{ A}$	6.5	13	-	S

²⁾ See figure 3

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V},$ $f=1\text{ MHz}$	-	540	720	pF
Output capacitance	C_{oss}		-	76	100	
Reverse transfer capacitance	C_{rss}		-	8	12	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V},$ $I_D=13\text{ A}, R_G=2.4\ \Omega$	-	9	13	ns
Rise time	t_r		-	4	6	
Turn-off delay time	$t_{d(off)}$		-	13	18	
Fall time	t_f		-	3	4	

Gate Charge Characteristics⁴⁾

Gate to source charge	Q_{gs}	$V_{DD}=50\text{ V}, I_D=13\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	3	4	nC
Gate to drain charge	Q_{gd}		-	2	3	
Switching charge	Q_{sw}		-	4	6	
Gate charge total	Q_g		-	8	11	
Gate plateau voltage	$V_{plateau}$		-	6	-	V
Output charge	Q_{oss}	$V_{DD}=50\text{ V}, V_{GS}=0\text{ V}$	-	8	10	

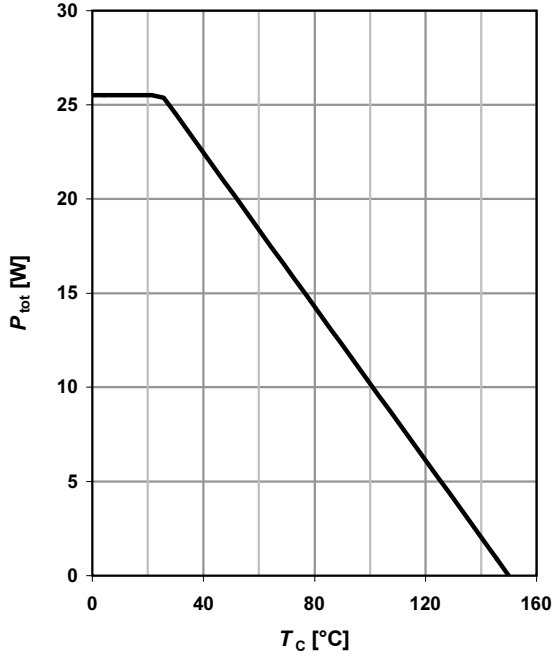
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	13	A
Diode pulse current	$I_{S,pulse}$		-	-	52	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=13\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	1	1.2	V
Reverse recovery time	t_{rr}	$V_R=50\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	67		ns
Reverse recovery charge	Q_{rr}		-	114	-	nC

⁴⁾ See figure 16 for gate charge parameter definition

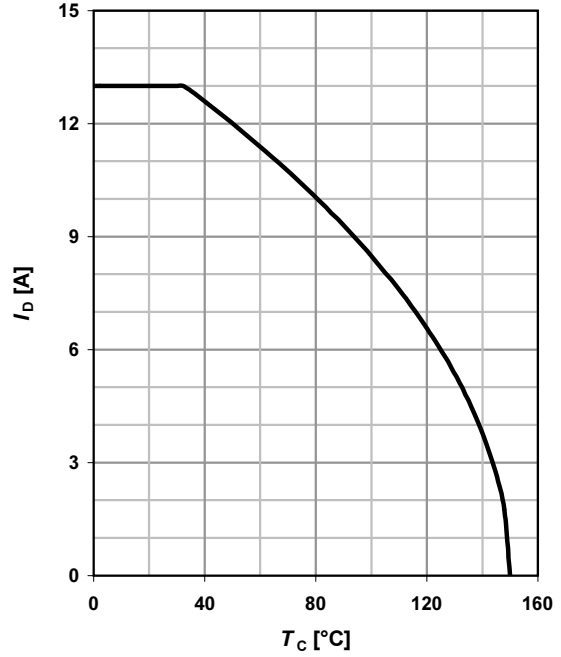
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

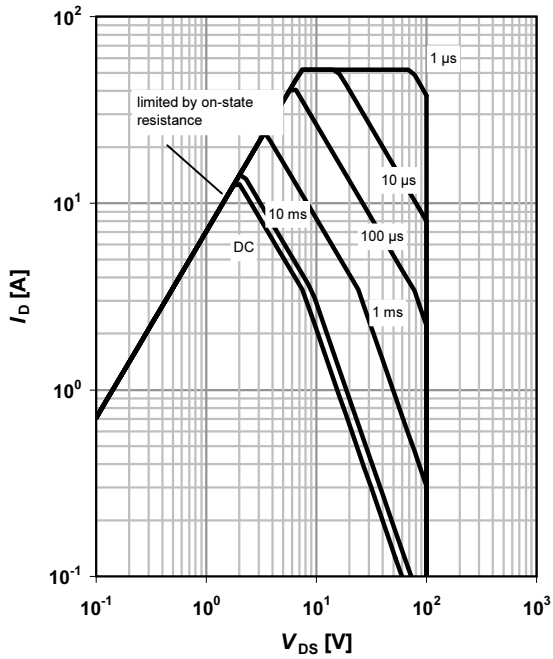
$I_D=f(T_C); V_{GS} \geq 10 V$



3 Safe operating area

$I_D=f(V_{DS}); T_C=25^\circ C; D=0$

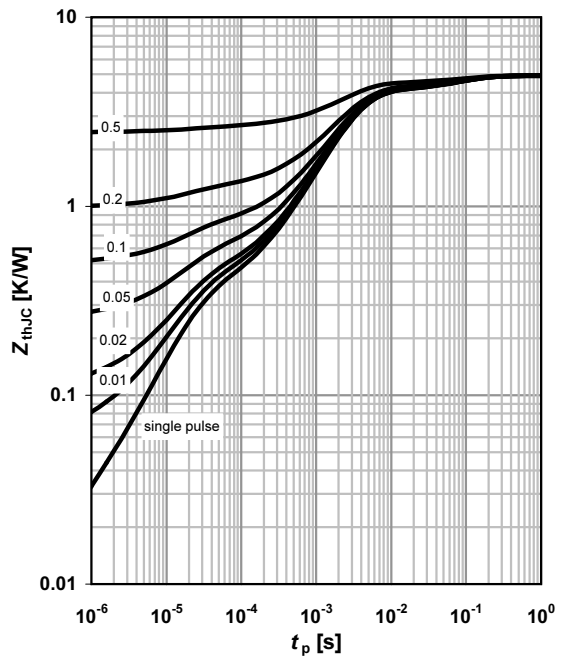
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

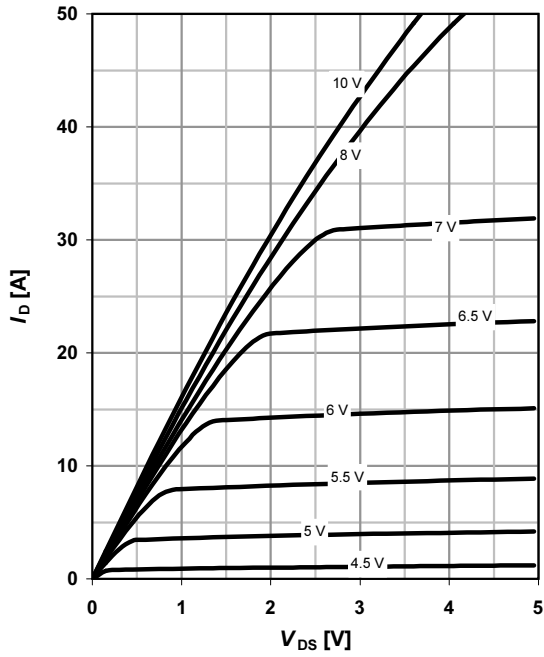
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

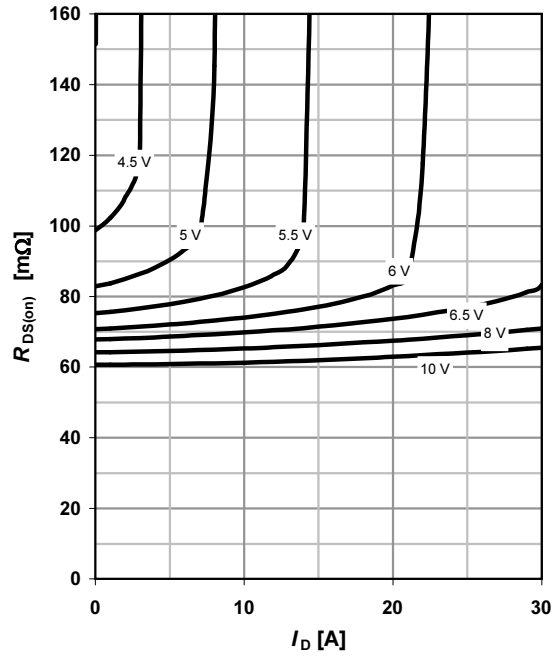
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

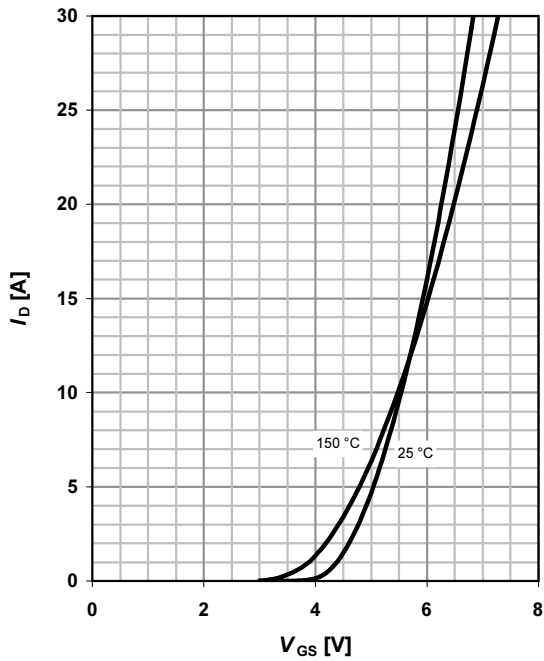
parameter: V_{GS}



7 Typ. transfer characteristics

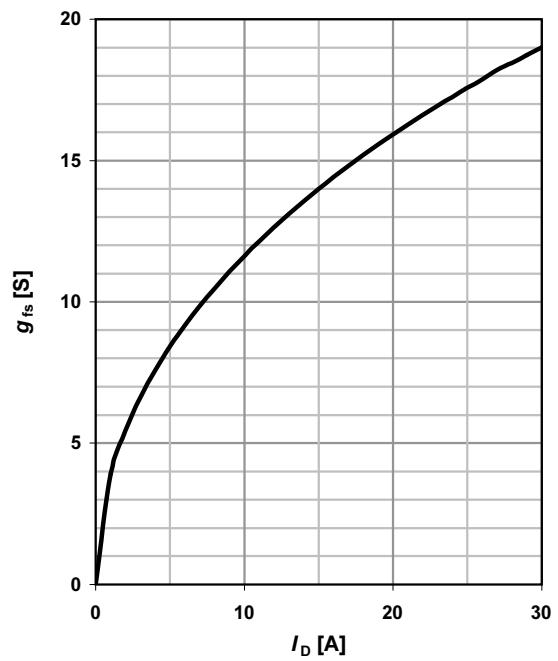
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



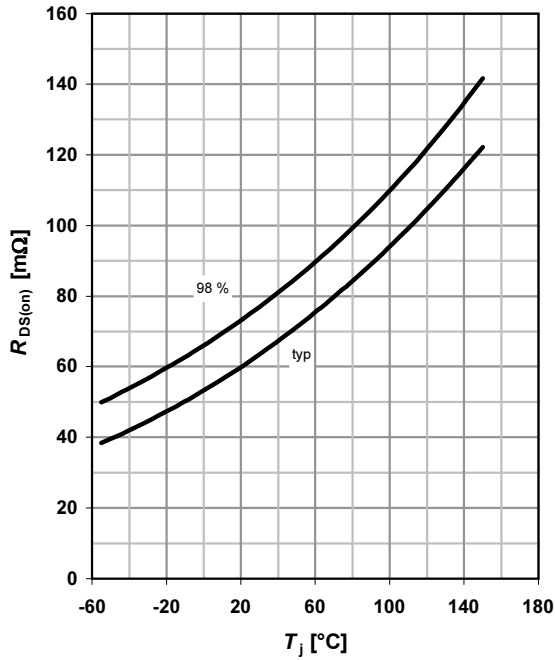
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



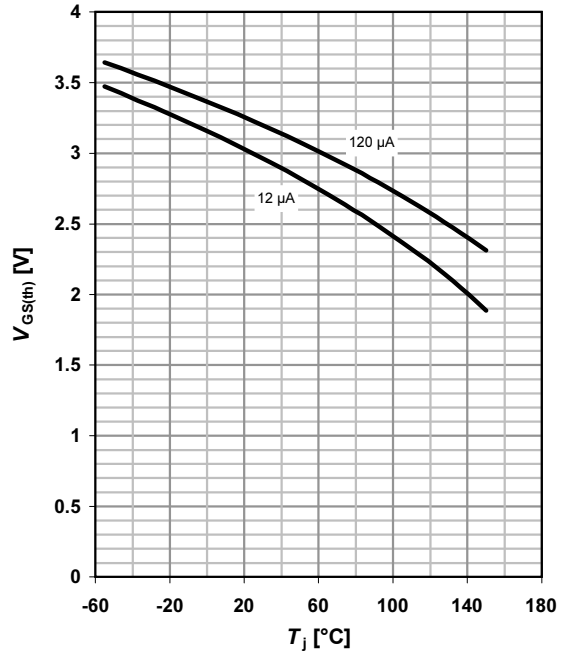
9 Drain-source on-state resistance

$R_{DS(on)} = f(T_j); I_D = 13 \text{ A}; V_{GS} = 10 \text{ V}$



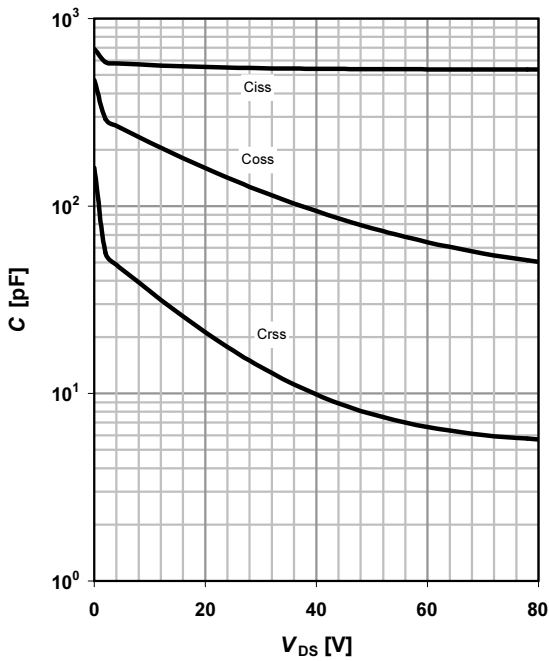
10 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$



11 Typ. capacitances

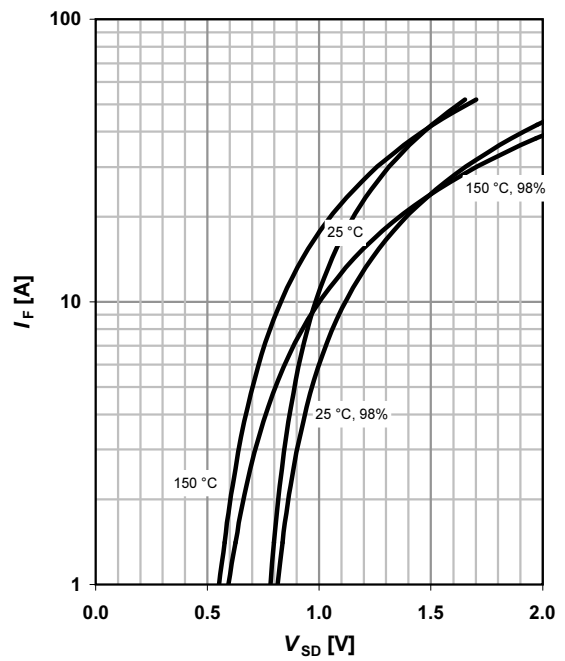
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



12 Forward characteristics of reverse diode

$I_F = f(V_{SD})$

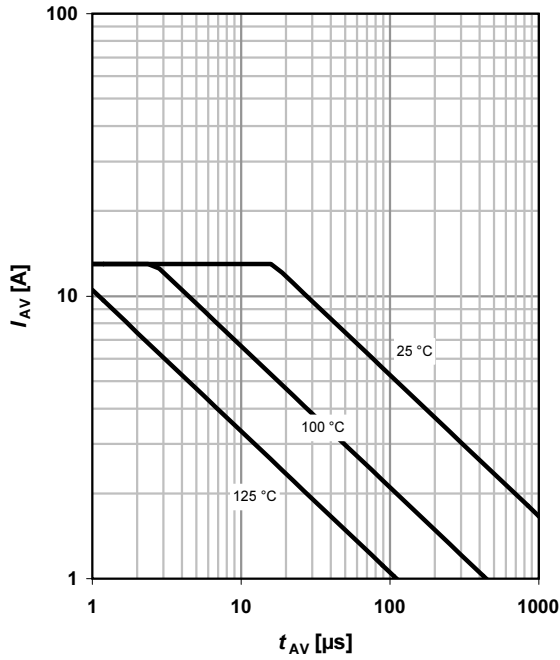
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

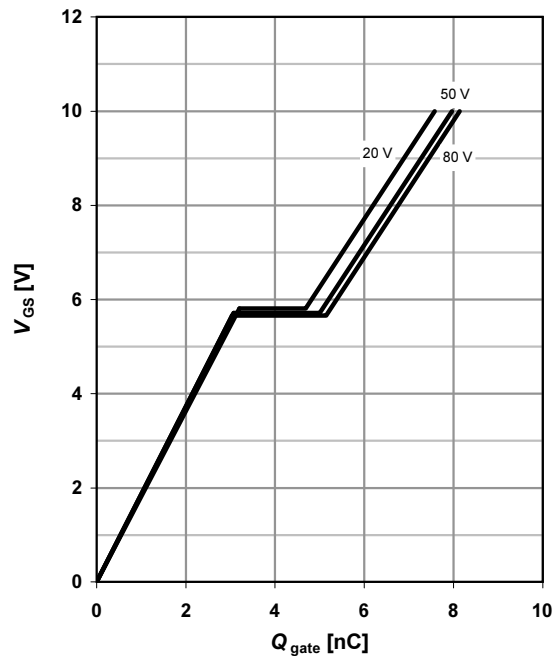
parameter: $T_{j(start)}$



14 Typ. gate charge

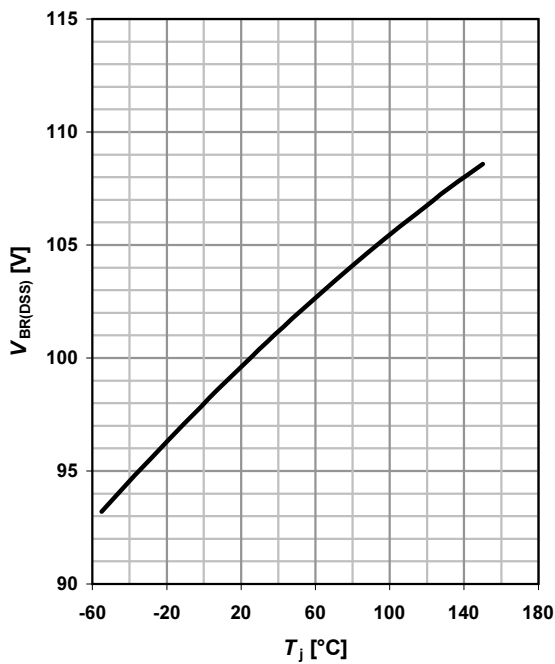
$V_{GS}=f(Q_{gate}); I_D=13 \text{ A pulsed}$

parameter: V_{DD}

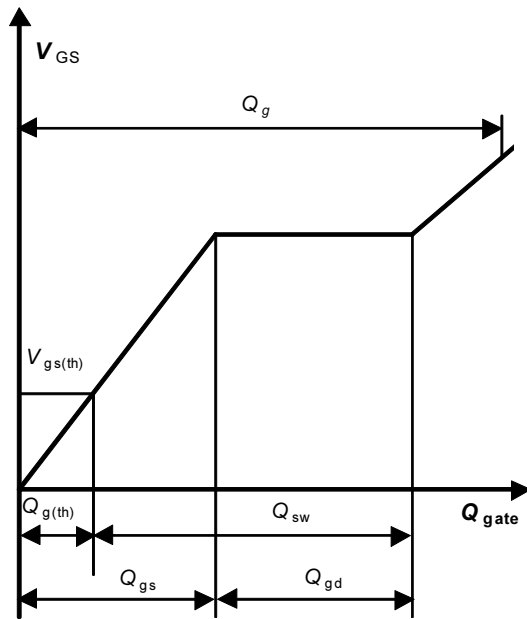


15 Drain-source breakdown voltage

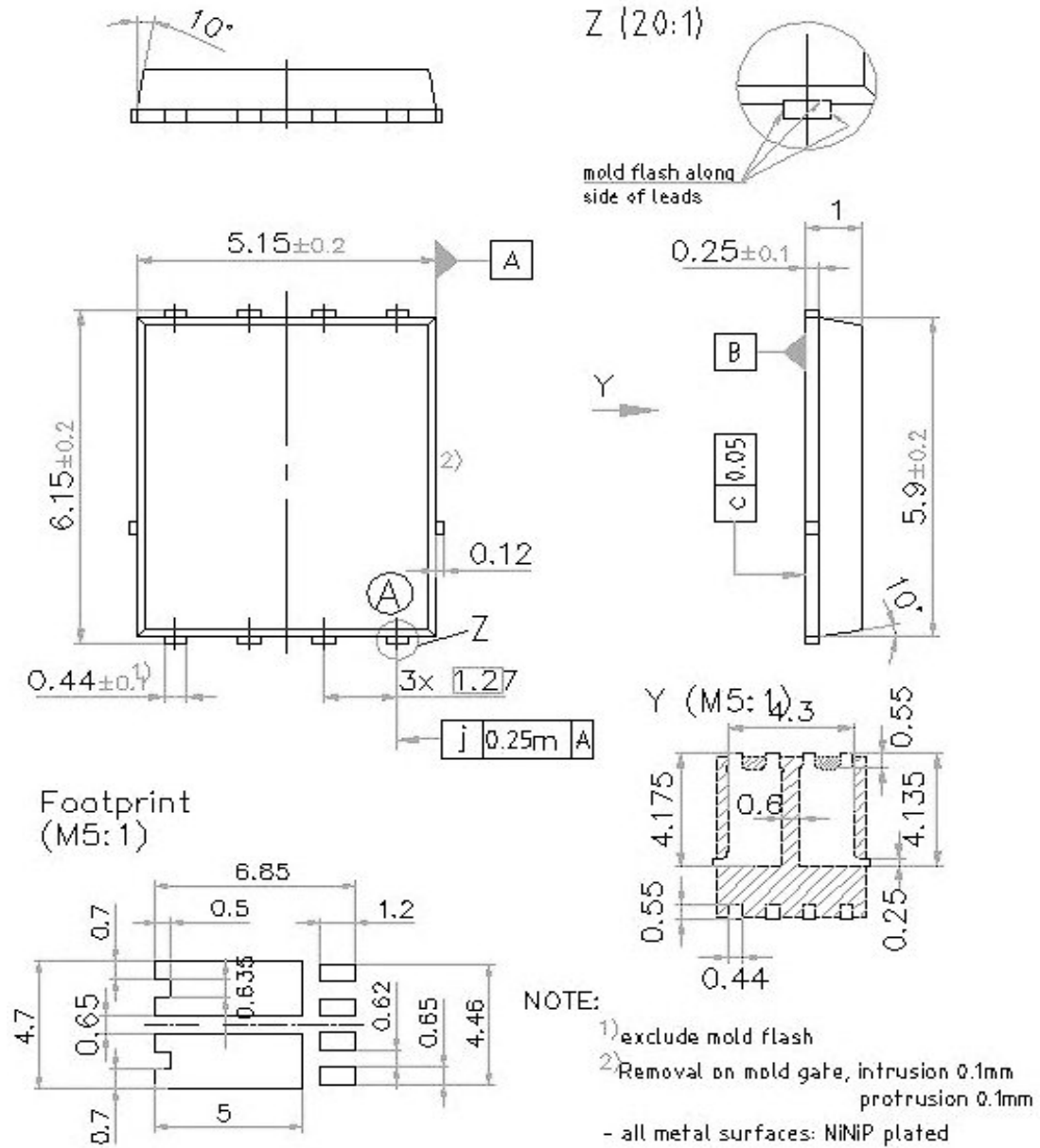
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



16 Gate charge waveforms



Package Outline and Footprint PG-TDSON-8 dual



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