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BSC9132 QDS Board Reference Manual

Devices Supported
BSC9132

BSC9132QDSRM
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Chapter 1
Overview

The BSC9132 QorIQ Development System (QDS) is a high-performance computing evaluation, development, and test platform supporting the **BSC9132** QorIQ Power Architecture® processor.

The BSC9132 QDS Board Reference Manual is optimized to support the high-bandwidth memory port, as well as the highly-configurable SerDes ports. The BSC9132 QDS Board Reference Manual is designed for a standard ATX form-factor, allowing it to be shipped in an off-the-shelf ATX chassis, if needed. The system is lead-free and RoHS-compliant.

1.1 Related documentation

For information on products and resources used with the BSC9132 QDS, use the references listed in Table 1-1.

Some of these documents may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1-1. Related Documentation

Document	Description
BSC9132 QorIQ Qonverge Multicore Baseband Processor Data Sheet (document BSC9132EC)	Provides information about Pin assignments, Electrical, characteristics, Hardware design, considerations, Package information, and Ordering information.
BSC9132 QorIQ Integrated Multicore Communication Processor Family Reference Manual (BSC9132RM)	Provides a detailed description about T2080 QorIQ multicore processor, and features, such as memory map, serial interfaces, power supply, chip features, and clock information.
The SystemID Format for Power Architecture™ Development Systems (AN3638)	Freescale Semiconductor Power Architecture™ technology-based evaluation and development platforms may optionally implement a “System ID” non-volatile memory device. This device stores important configuration data about the board.

2 Acronyms and abbreviation

The table below lists and explains the acronyms and abbreviations used in this document.

Table 2-2. Acronyms and abbreviations

Usage	Description
ADDR	Address
ATX	Advanced Technology Extended (power supply)
Komodo	Test Board for high Speed Path
AUX	Auxiliary
BRDCFG	Board Configuration
BVDD	IFC Bus Direct Current Voltage
CFG	Configuration
CLK	Clock
CLKIN	Clock Input (interchangeable with SYSCLK)
COP	Common On-Chip Processor
CVDD	Clock Driver Supply Voltage / Bus Control Voltage
DDR	Double Data Rate
DIP	Dual-In-Line Package (switches)
DRAM	Dynamic Random Access Memory
QDS	Qualification Development System
EC	Chip HW Specification
ECC	Error Detection and Correction
EEPROM	Electrically Erasable Programmable ROM
eSDHC	Enhanced Secure Digital High Capacity Card
ETH	Ethernet
evt	event
FS	Frequency Select
FCM	NAND Flash Control Machine
FLASH	Flash Memory Chip
FPGA	Field Programmable Gate Array
GETH	Giga Ethernet (GbE)
GPIO	General Purpose In/Out
GVDD	DDR Supply voltage
Host	BSC9132
HRESET	Hard Reset

Table 2-2. Acronyms and abbreviations

Usage	Description
I^2C	Inter-Integrated Circuit Multi-Master Serial Computer Bus
ID	Identification
IDE	Integrated Development Environment
IO	Input/Output
IPL	Initial Program Load
ISO	Isolated
JTAG	Joint Test Access Group (IEEE® Std. 1149.1™)
LBMAP	Local Bus Map
LED/LD	Light-emitting Diode
LSB	Least Significant Bit
LVDD	BSC9132 QDS GETH (Low) Voltage
MSB	Most Significant Bit
MUX	Multiplexer
NAND	Flash Memory
QIXIS	FPGA Block Logic Design
NOR	Flash Memory
DCM	Off-line Configuration Manager (FPGA-embedded)
OVDD	Output Voltage
PCIe/PEX	PCIe = PCI Express = PEX
PG	Power Good
PHY	Physical Layer
WP	Write Protect
PLL	Phased Lock Loop
POVDD	Parameter Operating Voltage
ppm	Parts per Million
PROC ISO	Processor Isolated
PROMJet	Memory Emulator by EmuTec Inc.
PROMJet Flash	Flash by EmuTec Inc.
PS	Power Supply
PWR	Power

Table 2-2. Acronyms and abbreviations

Usage	Description
QorIQ	Brand of power architecture based on a Freescale communications micro controller.
RC	Root Complex
RCW	Reset Configuration Word
REF	Reference
REF CLK	Reference Clock (Clock Synthesizer Input Value)
REG	Register
REG CFG	Configuration Register
REQ	Request
ROM	Read Only Memory
RST	Reset
RTC	Real-time Clock
SD	Secure Digital Card
SDHC	Secure Digital High Capacity
SDREFCLK	SerDes Reference Clock
SEL	Select
SerDes (SRDS)	Serializer/Deserializer; such as PEX, SGMII,CPRI
SGMII	Serial Gigabit Media Independent Interface
SMA	Subminiature Version B Connector
SPD	Speed
SRAM	Static Random Access Memory
STAT	Status
SVDD	Supply Voltage
SVR	System Version
SW	Switch
SYSCLK	System Clock
TAP	Telocator Alphanumeric Protocol; such as USB TAP or ETH TAP
TESTSEL	Test Select
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Table 2-2. Acronyms and abbreviations

Usage	Description
USBCLK	USB Clock
WP	Write Protect
CPRO	Public Radio Interface
SGMII	Serial GEthernet
XVDD	Phased Lock Loop Voltage

2.1 Features

The BSC9132 processor includes the following functions and features:

- Two e500-mc Power Architecture cores, each with a backside 512-KB L2 Cache with ECC
  - Three levels of instructions: user, supervisor, and hypervisor
  - Independent boot and reset
  - Secure boot capability
- Two StarCore SC3850 DSP subsystems, each with a 512-KB private L2 caches
- 32-KB of shared M3 memory
- The Multi Accelerator Platform Engine for Pico BaseStation Baseband Processing (MAPLE-B2P)
  - A multi-standard baseband algorithm accelerator for Channel Decoding/Encoding Fourier
  - Transforms UMTS chip rate processing, LTE UP/DL Channel processing, and CRC algorithms
  - 800 MHz to 1 GHz clock frequency
- Two DDR3/3L memory interfaces with 32-bit data width (40 bits including ECC), up to 1333 MHz data rate
  - data rate 32 KB 8-way level 1 data/instruction cache (L1 Dcache/ICache)
  - 512 KB 8-way level 2 unified instruction/data cache (L2 cache/M2 memory)
  - Memory management unit (MMU)
  - Enhanced programmable interrupt controller (EPIC)
  - Debug and profiling unit (DPU)
  - Two 32-bit timers
- Dedicated security engine featuring trusted
- Two DMA controllers
  - OCNDMA with four bidirectional channels
  - Sys DMA with sixteen bidirectional channels
  - IEEE 1588™ v2 support
- Interfaces
  - Two triple-speed Gigabit Ethernet controllers featuring network acceleration including - IEEE 1588™ v2 hardware support for two SGMII ports and virtualization (VeTSEC)

  - PCI Express controller, which complies with the PCI Express™ Base Specification Revision 2.0
  - Two Common Public Radio Interface (CPRI) controller lanes
  - Antenna Interface Controller (AIC), supporting four industry standard JESD207/four custom
    - ADI RF interfaces (three dual port and one single port) and a 2-lane CPRI interface
    - ADI lanes support both full duplex FDD support and half duplex TDD support
  - Universal Subscriber Identity Module (USIM) interface that facilitates communication to SIM
  - Multicore Programmable Interrupt Controller
  - Two I^2C controllers
  - Four DUART
  - Integrated Flash memory controller (IFC), supporting NAND, NOR, ASIC and GPMC.
  - Two PCI Express 2.0 controllers/ports
  - Two enhanced Serial Peripheral Interfaces (eSPI)
  - High-speed USB controller (USB 2.0)
    - Host and device support
    - ULPI interface to PHY
  - Sixteen 32-bit timers
- The two e500 cores subsystems within Power Architecture consist of the following:
  - Programmable interrupt controller (PIC) compliant with OpenPIC standard
  - 32-KB L1 instruction cache
  - Shared 512-KB L2 cache/L2 memory/L2 stash32-KB L1 data cache
  - Timers
- Each SC3850 core subsystem consists of the following:
  - 32 KB 8-way level 1 instruction cache (L1 ICache)
  - 32 KB 8-way level 1 data cache (L1 DCache)
  - 512 KB 8-way level 2 unified instruction/data cache (M2 memory)
  - Memory Management Unit (MMU)
  - Enhanced programmable interrupt controller (EPIC)
  - Debug and profiling unit (DPU)
  - Two 32-bit timers
- **QIXIS** System Logic FPGA
  - Manages system power and reset sequencing
  - Manages system, for DSP and DDR clock speed selections
  - Manages dynamic reconfiguration
  - Internal processor (GMSA) supports background data collection on voltage, power, and temperature
  - Registers allow full control of all device features
  - Support for classic test features, including:

  - POSt
  - IRS
  - Synchronous signal assertion (resets, IRQs)
- System fault monitoring and status display through LED's system fault monitoring
- Runs from ATX “hot” power rails allowing FPGA operation while system is off.

- SERDES Connections
  - Supports one 2xPCIe express channel
    - On-board 16xPCIe slot
  - Supports two CPRI channels configurations
    - On-board two SFP + optical link transceivers
  - Supports two SGMII interface links
    - On-board tow SGMII Vitesse VSC8221PHY devices
- Clocks
  - System clock (SYSCLK), DSP clock (DSPCLK) and DDR clock (DDRCLK)
    - Switch selectable to one of 4 common settings in the interval 66MHz-133MHz
    - Software selectable in 1MHz increments from 1-200MHz
  - SERDES clocks
    - Supports 100, 125 MHz for SD1 and 100, 125, 122.88 MHz clocking for SD2 port.
  - 125MHz Ethernet clock
  - 2.048Mhz TDM Clock
  - 16 MHz RTC Clock
- Power Supplies
  - Dedicated regulators for BVDD and XVDD, XPAD voltage rails
  - Dedicated regulators for G1VDD(VTT1/VREF1) and G2VDD(VTT2/VREF2) (1.5V/1.35V and 0.75V/0.675V)
  - Other regulators for CVDD, XVDD, OVDD, LVDD, general 1.5V, 1.8V and 2.5V power for peripherals

2.2 Block diagram

This section provides a high-level overview of the **BSC9132**. Figure 2-1 shows the major functional units within the device and Figure 2-2 shows the overall architecture of the BSC9132 QDS platform.

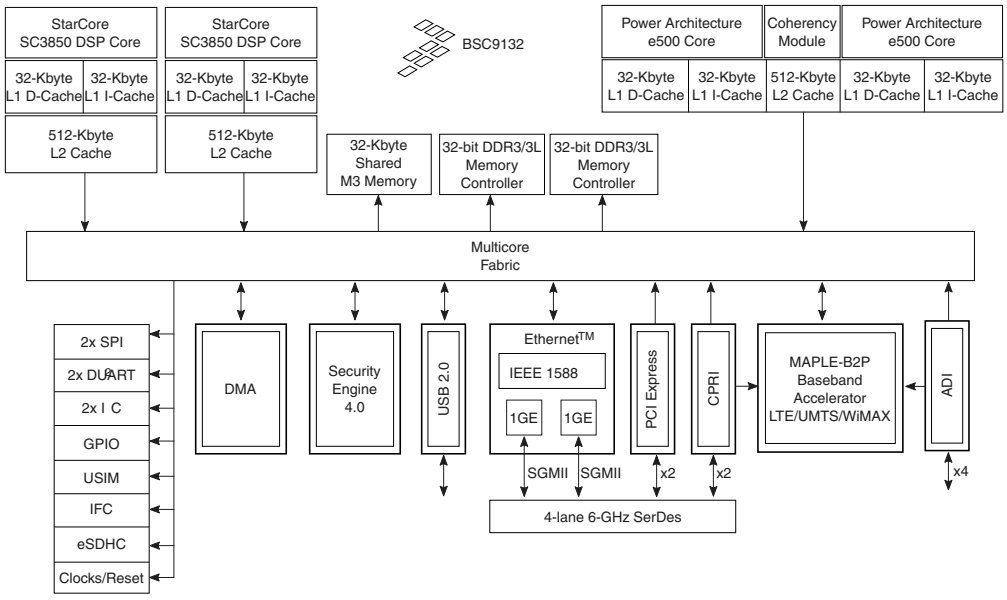

Figure 2-1. BSC9132 QorIQ block diagram

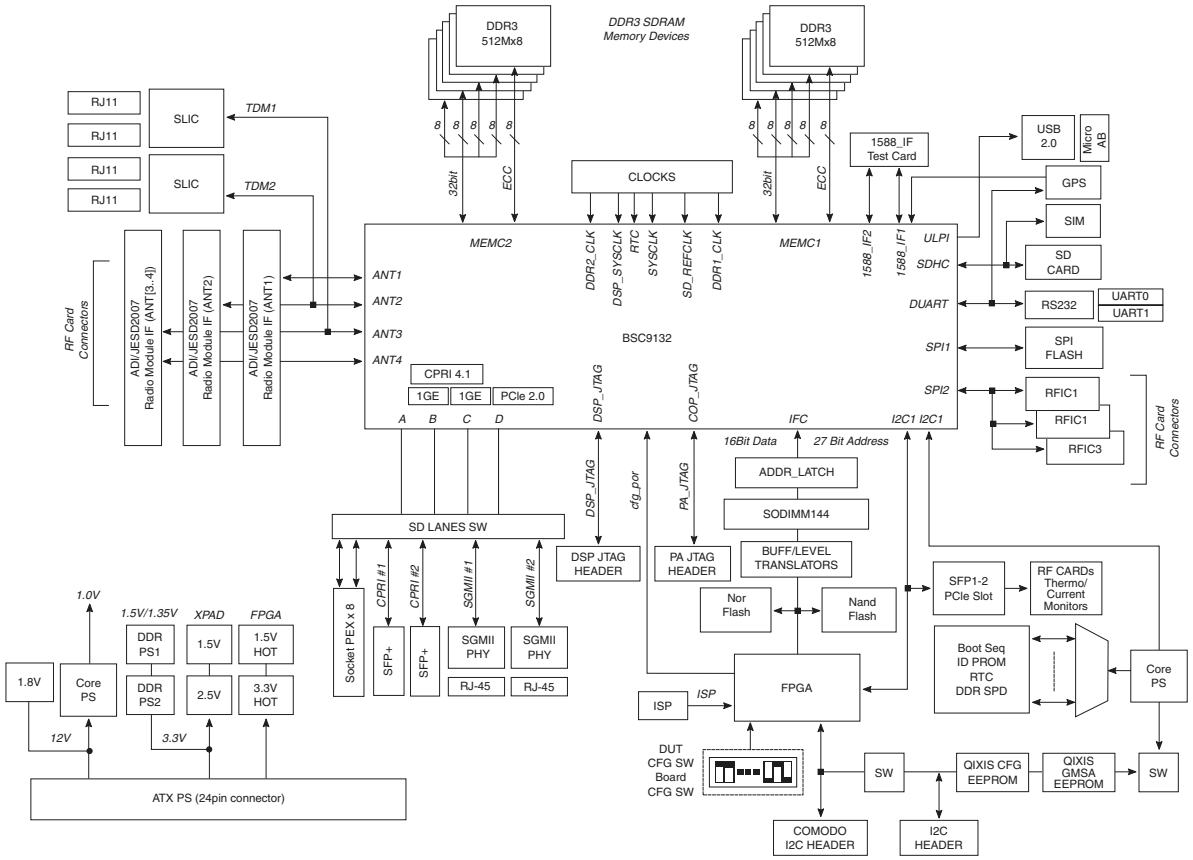

Figure 2-2. BSC9132 QDS block diagram

NOTE

To examine the details of the BSC9132 QDS board top view, you need to zoom-in the image.