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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Mosfet

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™ Power-Transistor, -30V

BSL303SPE

Data Sheet

Rev. 2.0
Final

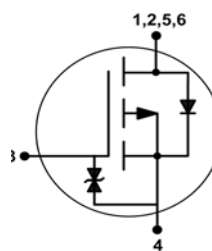
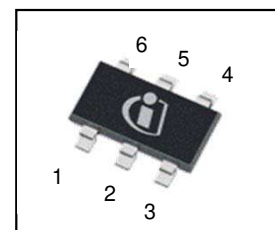
Industrial & Multimarket

OptiMOS™-P 3 Small-Signal-Transistor
Features

- P-channel
- Enhancement mode
- Logic level (4.5V rated)
- ESD protected
- Avalanche rated
- Qualified according to AEC Q101
- 100% Lead-free; RoHS compliant, halogen free


Product Summary

V_{DS}	-30	V
$R_{DS(on),max}$	$V_{GS}=-10\text{ V}$	33
	$V_{GS}=-4.5\text{ V}$	52
I_D	-6.3	A


PG-TSOP-6


Type	Package	Tape and Reel Information	Marking	Hal. Free	Packing
BSL303SPE	PG-TSOP-6	H6327: 3000 pcs/ reel	sPV	Yes	Non dry

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_A=25\text{ °C}$	-6.3	A
		$T_A=70\text{ °C}$	-5.0	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	-25.2	
Avalanche energy, single pulse	E_{AS}	$I_D=-6.3\text{ A}$, $R_{GS}=25\ \Omega$	30.0	mJ
Reverse diode dv/dt	dv/dt	$I_D=-6.3\text{ A}$, $V_{DS}=-15\text{ V}$, $di/dt=100\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ °C}$	6	kV/ μs
Gate source voltage	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_A=25\text{ °C}$	2.0	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	$^{\circ}\text{C}$
ESD Class		JESD22-A114 -HBM	2 (2KV to 4kV)	V
Soldering Temperature			260 $^{\circ}\text{C}$	$^{\circ}\text{C}$
IEC climatic category; DIN IEC 68-1			55/150/56	$^{\circ}\text{C}$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - minimal footprint	R_{thJS}		-	-	50	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	230	
		6 cm ² cooling area ¹⁾	-	-	62.5	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=0V, I_D=-30\mu A$	-2	-1.5	-1	
Drain-source leakage current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V, T_j=25\text{ °C}$	-	-	-0.1	μA
		$V_{DS}=-30V, V_{GS}=0V, T_j=150\text{ °C}$	-	-	-20	
Gate-source leakage current	I_{GSS}	$V_{GS}=-20V, V_{DS}=0V$	-	-	-7	μA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=-5A$	-	35	52	m Ω
		$V_{GS}=-10V, I_D=-6.3A$	-	25	33	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=-5A$		12.9	-	S

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (single layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air. (t < 5 sec.)

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=-15\text{ V},$ $f=1\text{ MHz}$	-	1053	1401	pF
Output capacitance	C_{oss}		-	482	641	
Reverse transfer capacitance	C_{rss}		-	33	50	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-15\text{ V}, V_{GS}=-$ $10\text{ V}, I_D=-6.3\text{ A},$ $R_{G,ext}=6\ \Omega$	-	8.0	12	ns
Rise time	t_r		-	7.7	12	
Turn-off delay time	$t_{d(off)}$		-	23.7	36	
Fall time	t_f		-	8.3	12	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=-15\text{ V}, I_D=-6.3\text{ A},$ $V_{GS}=0\text{ to }-10\text{ V}$	-	3.3	4.4	nC
Gate to drain charge	Q_{gd}		-	1.6	2.4	
Gate charge total	Q_g		-	14.0	20.9	
Gate plateau voltage	$V_{plateau}$		-	3.1	-	V

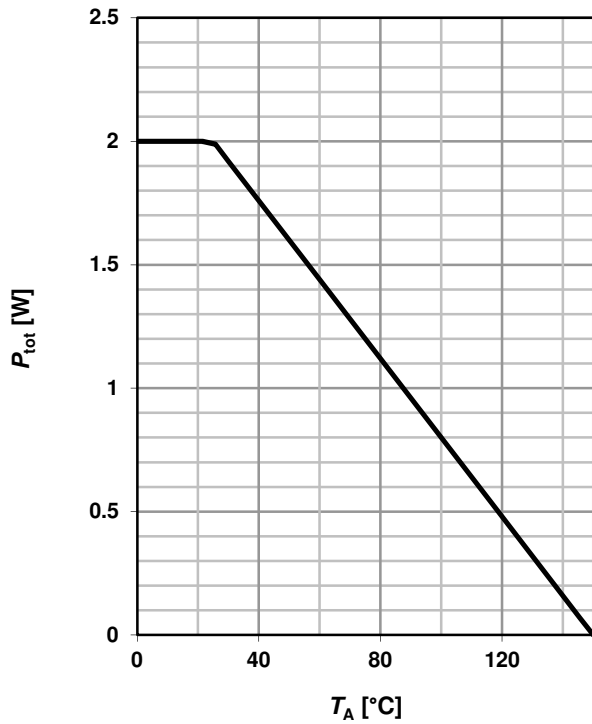
Reverse Diode

Diode continuous forward current	I_S	$T_A=25\text{ }^\circ\text{C}$	-	-	-6.3	A
Diode pulse current	$I_{S,pulse}$		-	-	-25.2	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=-6.3\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	-0.9	-1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=-15\text{ V}, I_F=-6.3\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	33	49	ns
Reverse recovery charge ²⁾	Q_{rr}		-	28	43	nC

²⁾ Defined by design. Not subjected to production test

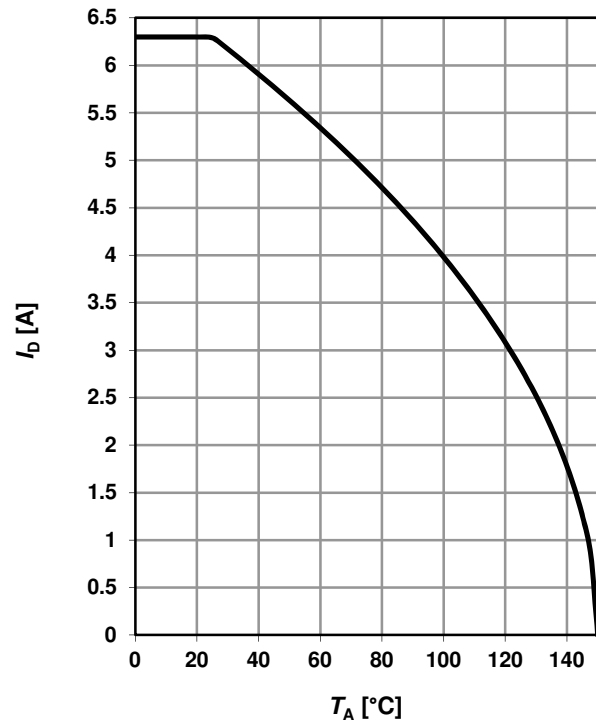
1 Power dissipation

$$P_{tot}=f(T_A)$$



2 Drain current

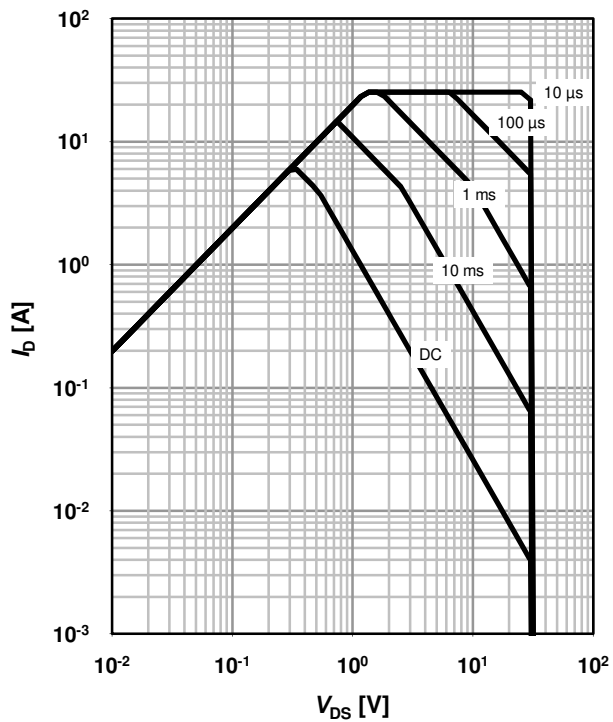
$$I_D=f(T_A); V_{GS} \leq -10 \text{ V}$$



3 Safe operating area

$$I_D=f(V_{DS}); T_A=25 \text{ °C}; D=0$$

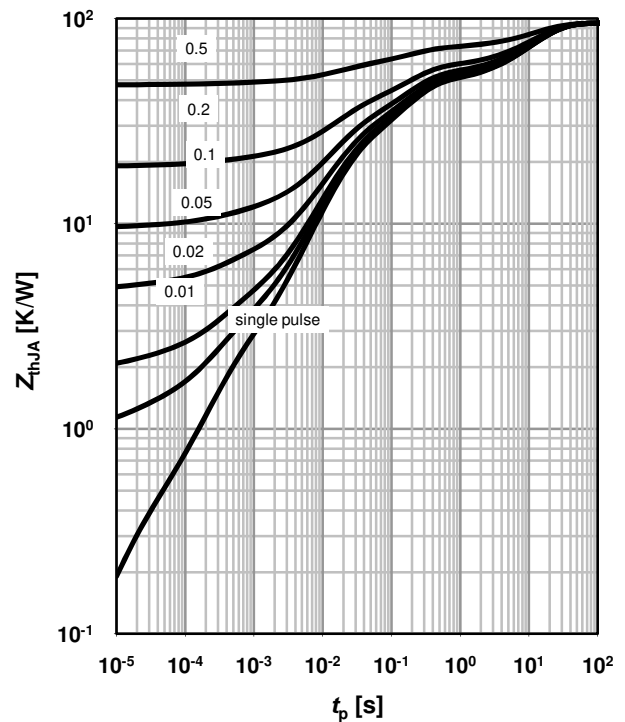
parameter: t_p



4 Max. transient thermal impedance

$$Z_{thJA}=f(t_p)$$

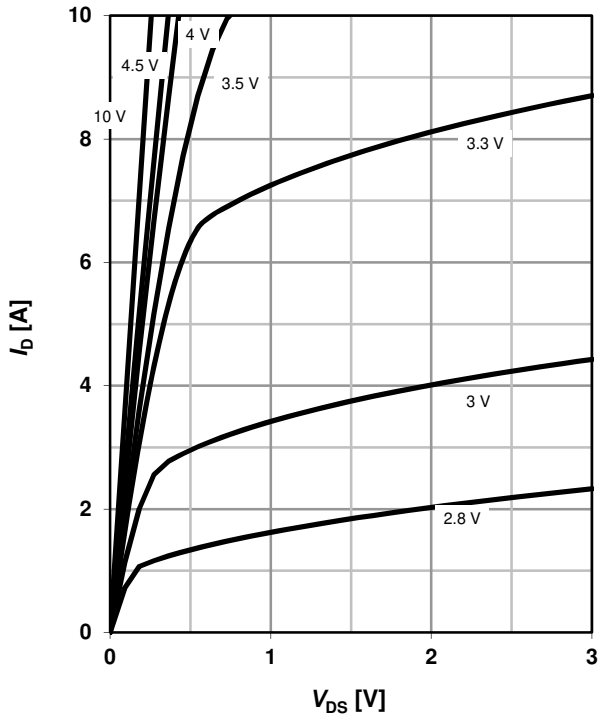
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

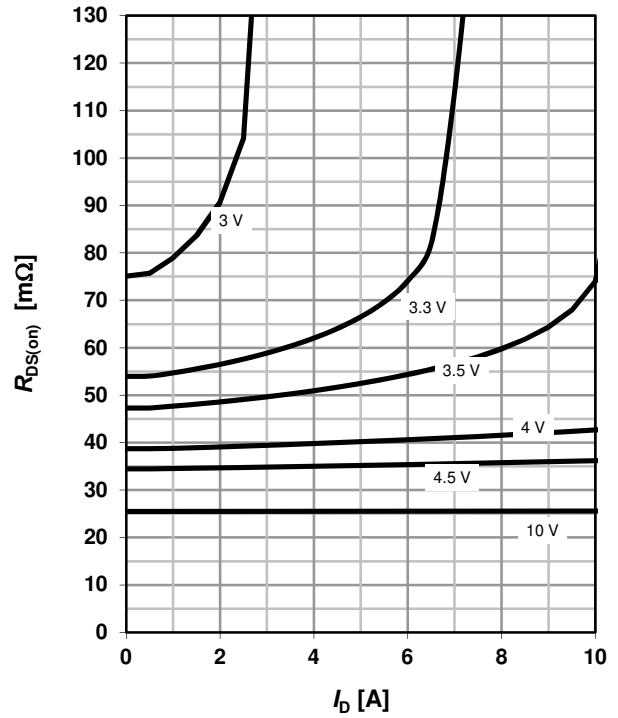
parameter: V_{GS}



6 Typ. drain-source on resistance

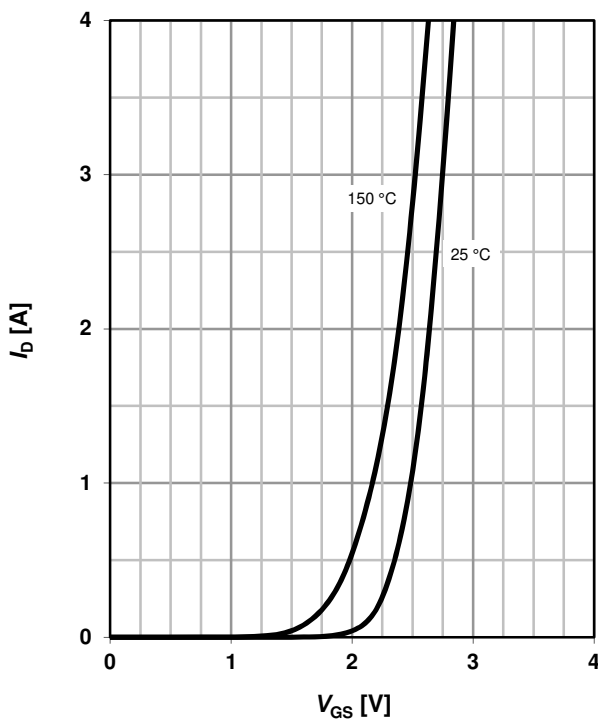
$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

parameter: V_{GS}



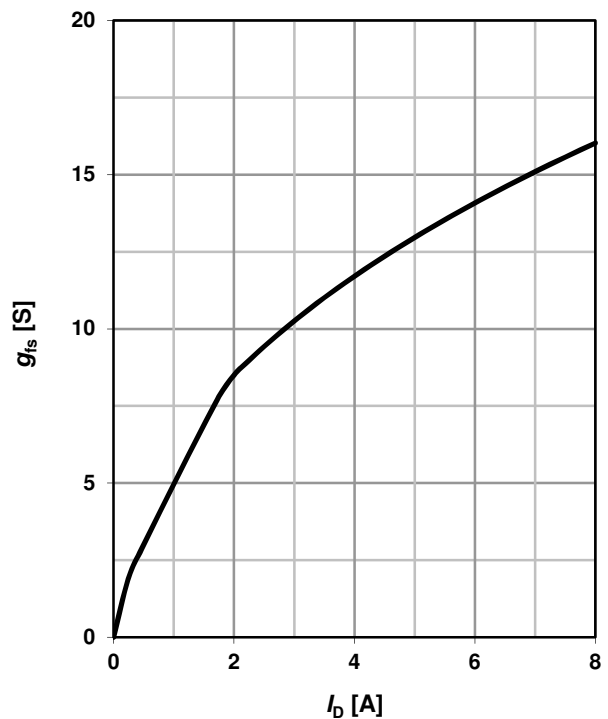
7 Typ. transfer characteristics

$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max}$



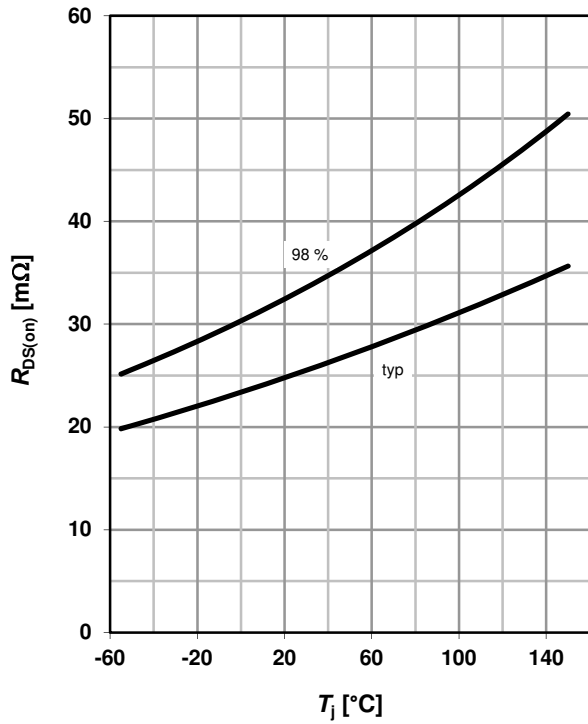
8 Typ. forward transconductance

$g_{fs}=f(I_D); T_j=25\text{ }^\circ\text{C}$



9 Drain-source on-state resistance

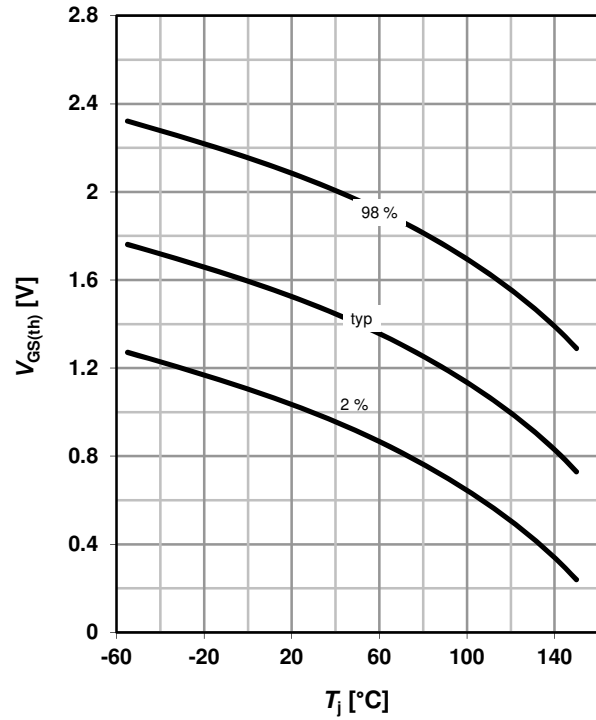
$R_{DS(on)}=f(T_j)$; $I_D=-6.3\text{ A}$; $V_{GS}=-10\text{ V}$



10 Typ. gate threshold voltage

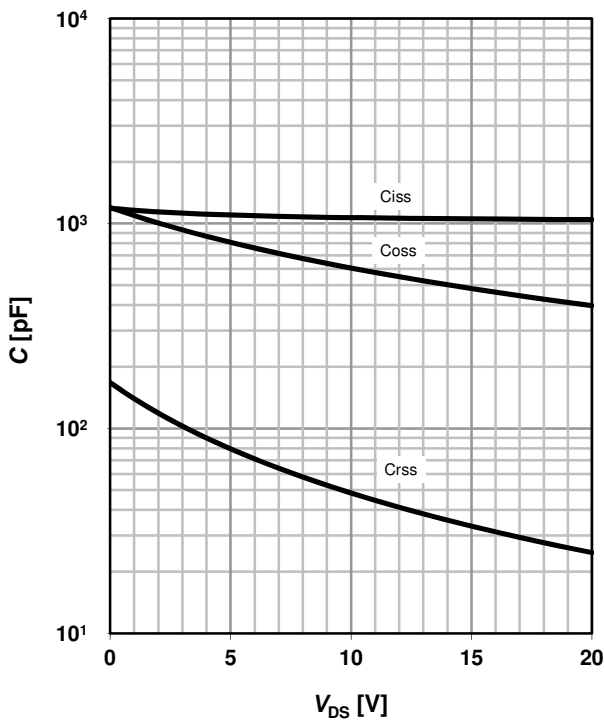
$V_{GS(th)}=f(T_j)$; $V_{DS}=V_{GS}$; $I_D=-30\text{ }\mu\text{A}$

parameter: I_D



11 Typ. capacitances

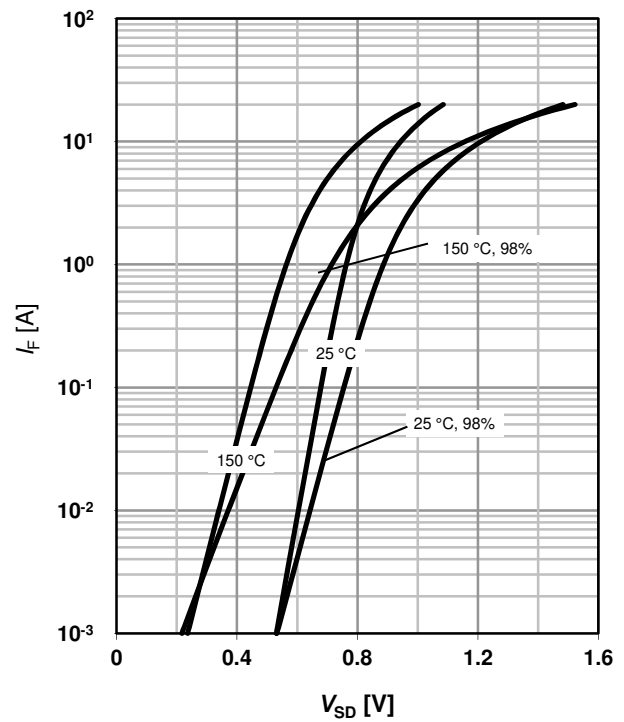
$C=f(V_{DS})$; $V_{GS}=0\text{ V}$; $f=1\text{ MHz}$; $T_j=25^\circ\text{C}$



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

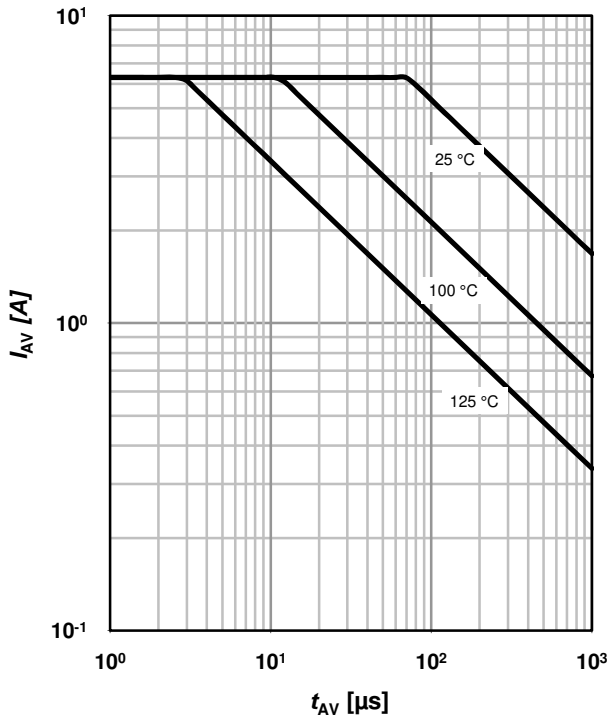
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

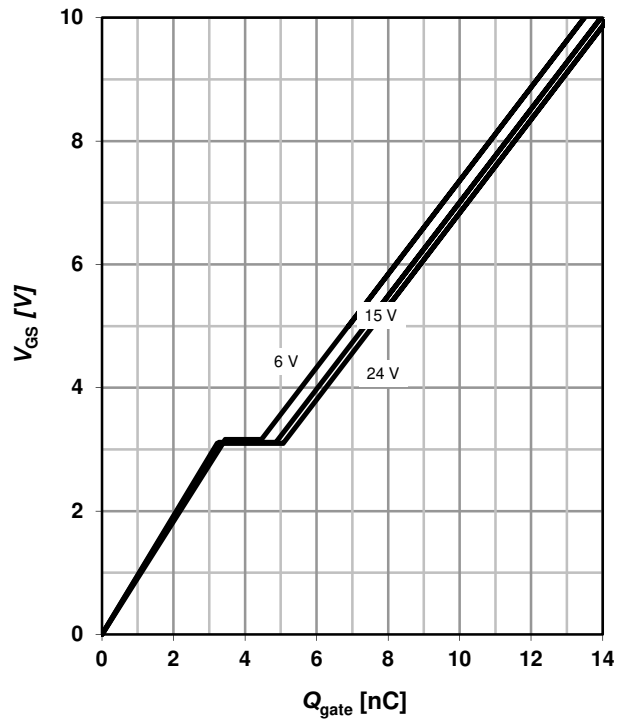
parameter: $T_{j(start)}$



14 Typ. gate charge

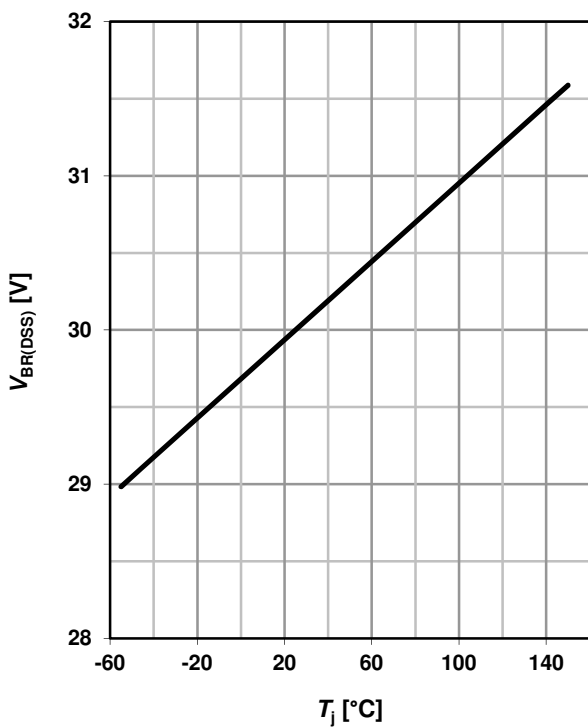
$V_{GS}=f(Q_{gate}); I_D=-6.3 \text{ A pulsed}$

parameter: V_{DD}

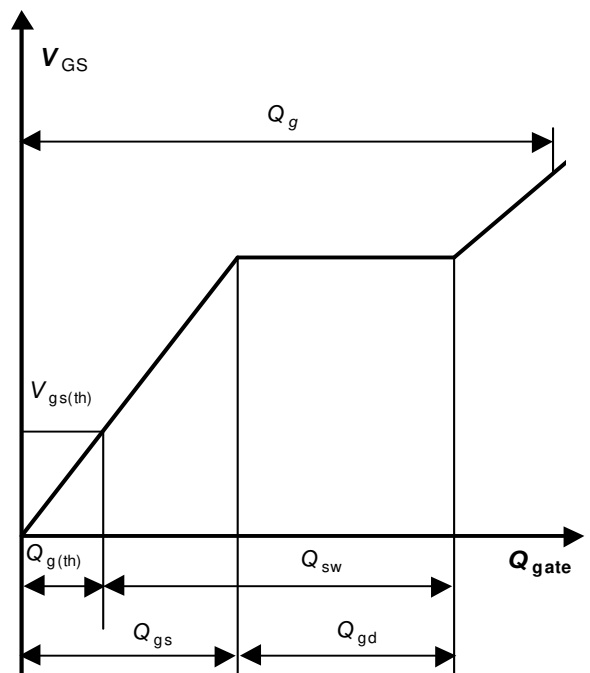


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=-250 \mu\text{A}$

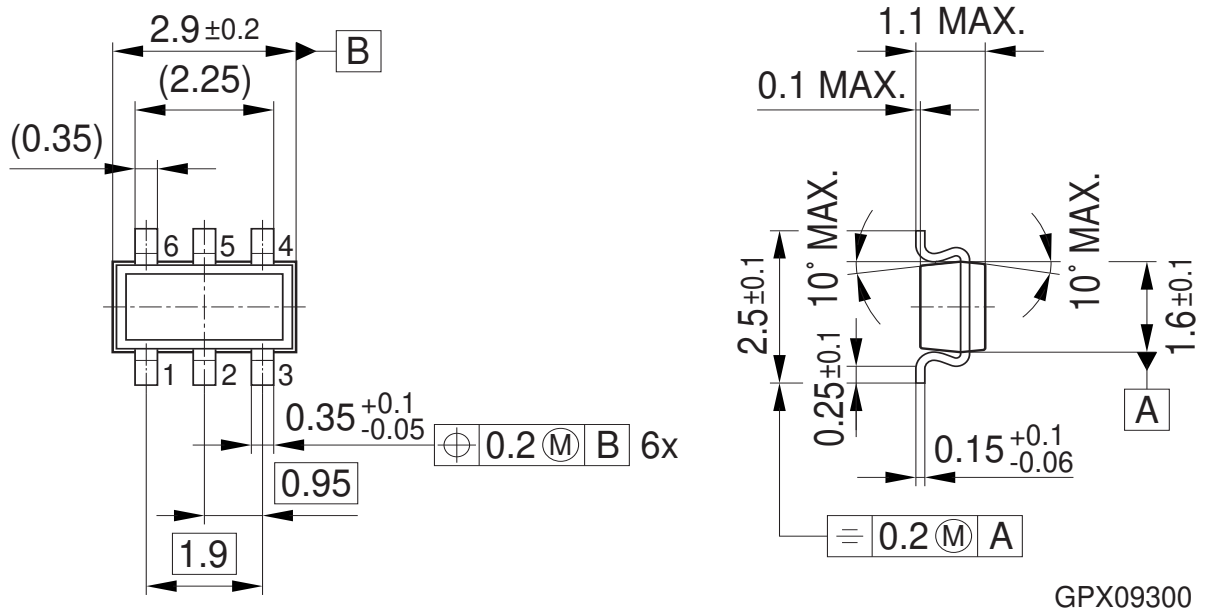


16 Gate charge waveforms

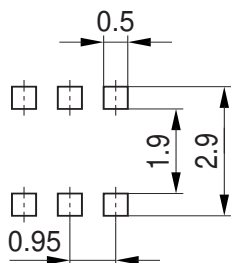


Package Outline:

TSOP-6

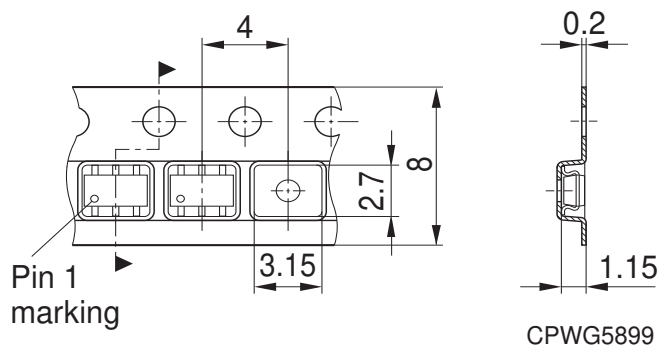


Footprint:



Remark: Wave soldering possible dep. on customers process conditions
HLG09283

Packaging:



Dimensions in mm

Note: For symmetric types there is no defined Pin 1 orientation in the reel.

Revision History

BSL303SPE

Revision: 2014-12-10, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-10	Release of final version

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