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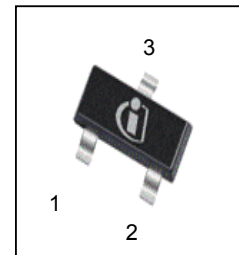
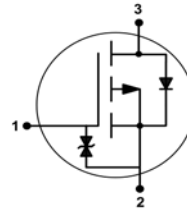
OptiMOS™ P3 Small-Signal-Transistor
Features

- P-channel
- Enhancement mode
- Logic level (4.5V rated)
- ESD protected
- Qualified according to AEC Q101
- 100% lead-free; RoHS compliant
- Halogen-free according to IEC61249-2-21


Product Summary

V_{DS}		-30	V
$R_{DS(on),max}$	$V_{GS}=-10\text{ V}$	80	m Ω
	$V_{GS}=-4.5\text{ V}$	130	
I_D		-2.0	A

PG-SOT-23



Type	Package	Tape and Reel Information	Marking	Lead Free	Packing
BSS308PE	PG-SOT23	H6327: 3000 pcs/ reel	YFs	Yes	Non dry

Maximum ratings, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_A=25\text{ }^\circ\text{C}$	-2.0	A
		$T_A=70\text{ }^\circ\text{C}$	-1.6	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ }^\circ\text{C}$	-8.0	
Avalanche energy, single pulse	E_{AS}	$I_D=-2\text{ A}$, $R_{GS}=25\text{ }\Omega$	-10.7	mJ
Reverse diode dv/dt	dv/dt	$I_D=-2\text{ A}$, $V_{DS}=-16\text{ V}$, $di/dt=-200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ }^\circ\text{C}$	6	kV/ μs
Gate source voltage	V_{GS}		± 20	V
Power dissipation ¹⁾	P_{tot}	$T_A=25\text{ }^\circ\text{C}$	0.5	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	$^\circ\text{C}$
ESD Class		JESD22-A114 -HBM	2 (2kV to 4kV)	
Soldering Temperature			260 $^\circ\text{C}$	$^\circ\text{C}$
IEC climatic category; DIN IEC 68-1			55/150/56	$^\circ\text{C}$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - ambient	R_{thJA}	minimal footprint ¹⁾	-	-	250	K/W
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Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-11\mu A$	-2.0	-1.5	-1.0	
Drain-source leakage current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V, T_j=25\text{ °C}$	-	-	-1	μA
		$V_{DS}=-30V, V_{GS}=0V, T_j=150\text{ °C}$	-	-	-100	
Gate-source leakage current	I_{GSS}	$V_{GS}=-20V, V_{DS}=0V$	-	-	-5	μA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-1.7A$	-	88	130	$m\Omega$
		$V_{GS}=-10V, I_D=-2A$	-	62	80	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=-1.6A$		4.6	-	S

¹⁾ Performed on 40mm² FR4 PCB. The traces are 1mm wide, 70 μ m thick and 20mm long; they are present on both sides of the PCB.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=-15\text{ V},$ $f=1\text{ MHz}$	-	376	500	pF
Output capacitance	C_{oss}		-	196	261	
Reverse transfer capacitance	C_{rss}		-	12	18	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-15\text{ V},$ $V_{GS}=-10\text{ V},$ $I_D=-2\text{ A}, R_G=6\ \Omega$	-	5.6	-	ns
Rise time	t_r		-	7.7	-	
Turn-off delay time	$t_{d(off)}$		-	15.3	-	
Fall time	t_f		-	2.8	-	

Gate Charge Characteristics

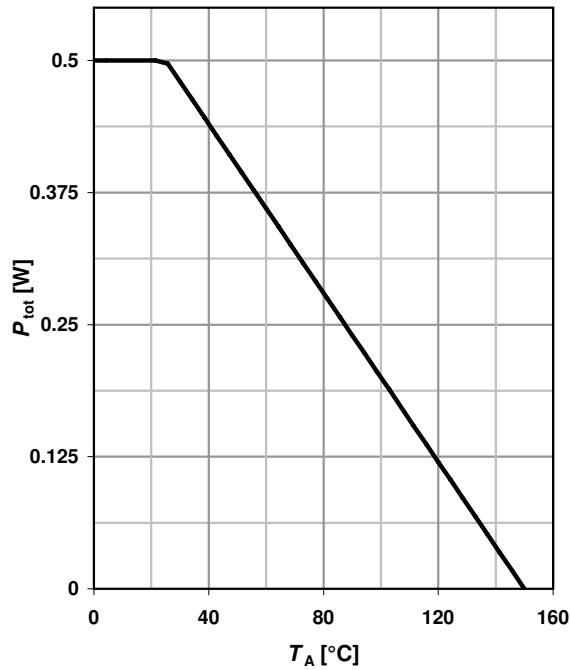
Gate to source charge	Q_{gs}	$V_{DD}=-15\text{ V}, I_D=-2\text{ A},$ $V_{GS}=0\text{ to }-10\text{ V}$	-	-1.2	-	nC
Gate to drain charge	Q_{gd}		-	-0.6	-	
Gate charge total	Q_g		-	-5.0	-	
Gate plateau voltage	$V_{plateau}$		-	-3.1	-	V

Reverse Diode

Diode continuous forward current	I_S	$T_A=25\text{ }^\circ\text{C}$	-	-	-0.4	A
Diode pulse current	$I_{S,pulse}$		-	-	-8.4	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=-2\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	-0.8	-1.1	V
Reverse recovery time	t_{rr}	$V_R=10\text{ V}, I_F=-2\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	14	-	ns
Reverse recovery charge	Q_{rr}		-	-5.9	-	nC

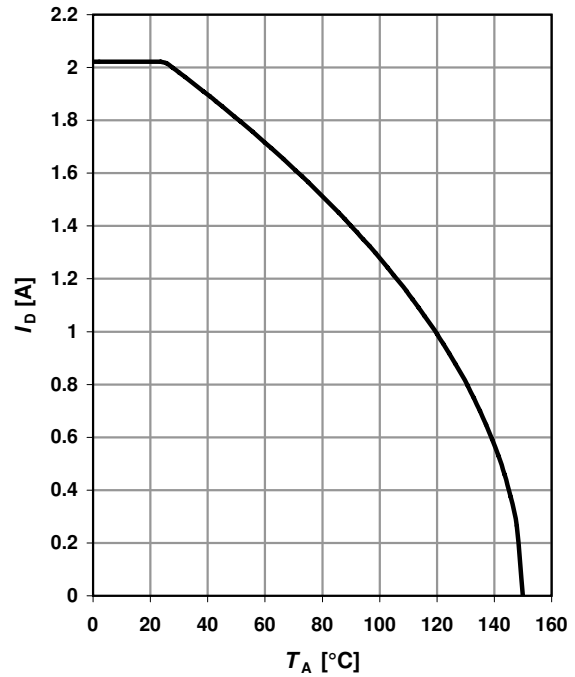
1 Power dissipation

$$P_{\text{tot}} = f(T_A)$$



2 Drain current

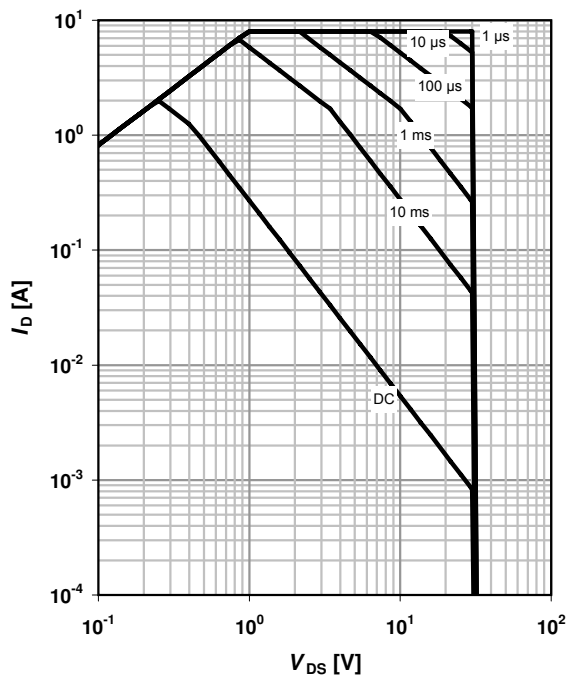
$$I_D = f(T_A); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_A = 25 \text{ °C}; D = 0$$

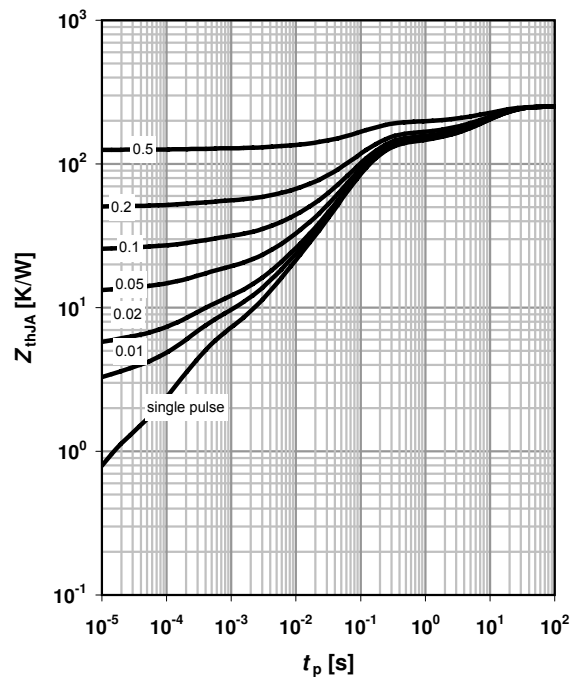
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJA}} = f(t_p)$$

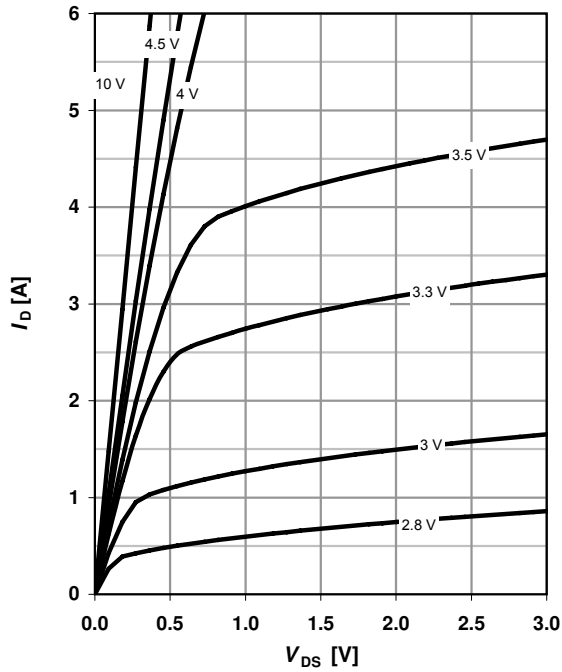
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

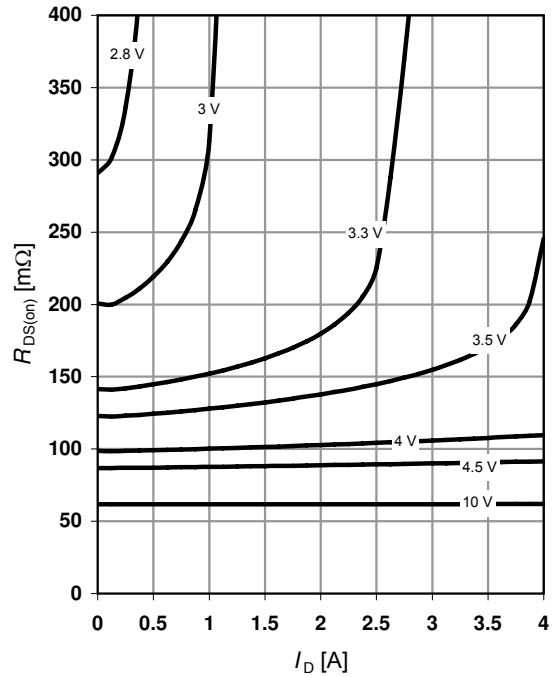
parameter: V_{GS}



6 Typ. drain-source on resistance

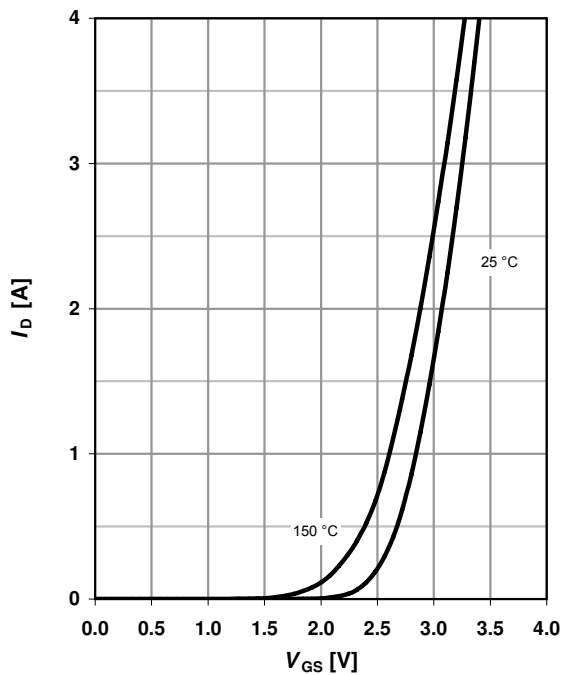
$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

parameter: V_{GS}



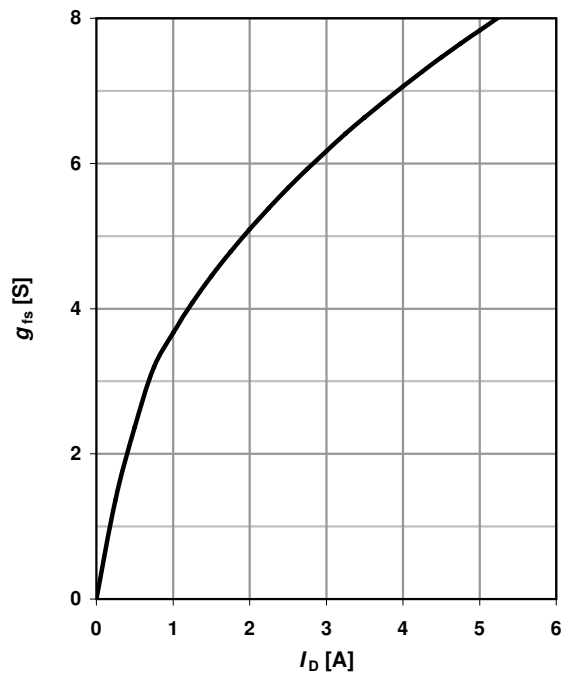
7 Typ. transfer characteristics

$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$



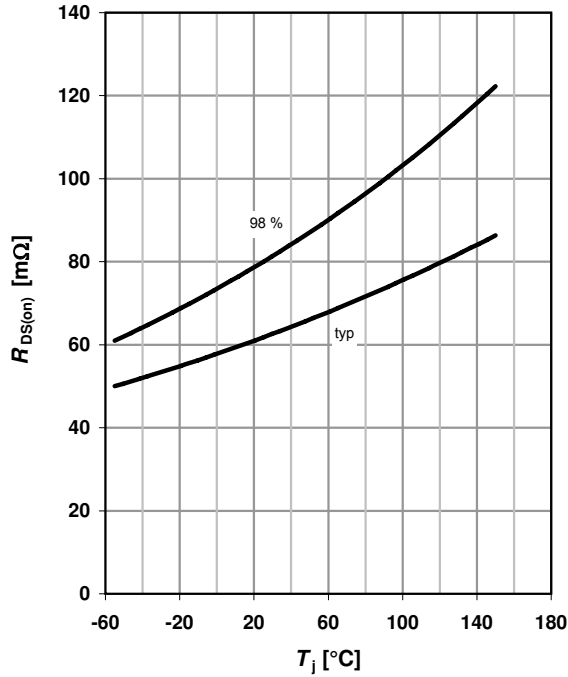
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



9 Drain-source on-state resistance

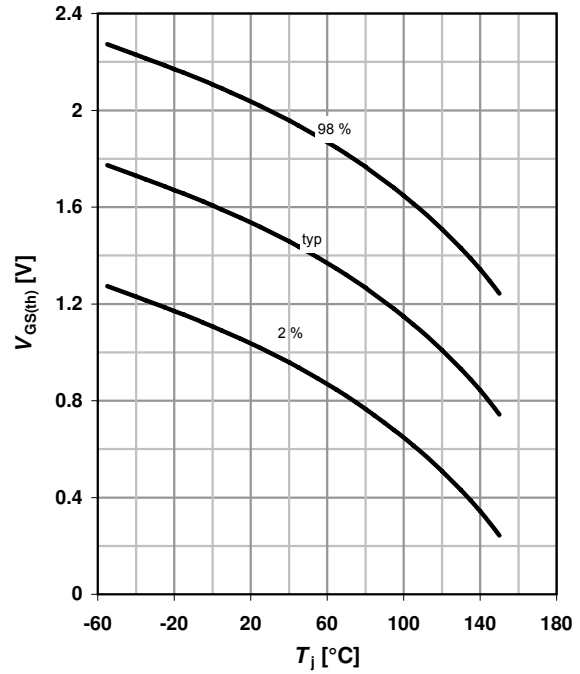
$R_{DS(on)} = f(T_j); I_D = -2 \text{ A}; V_{GS} = -10 \text{ V}$



10 Typ. gate threshold voltage

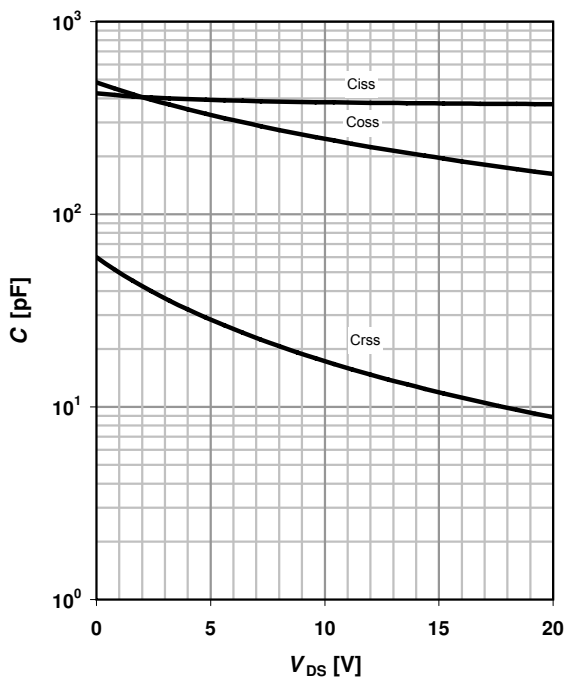
$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 11 \mu\text{A}$

parameter: I_D



11 Typ. capacitances

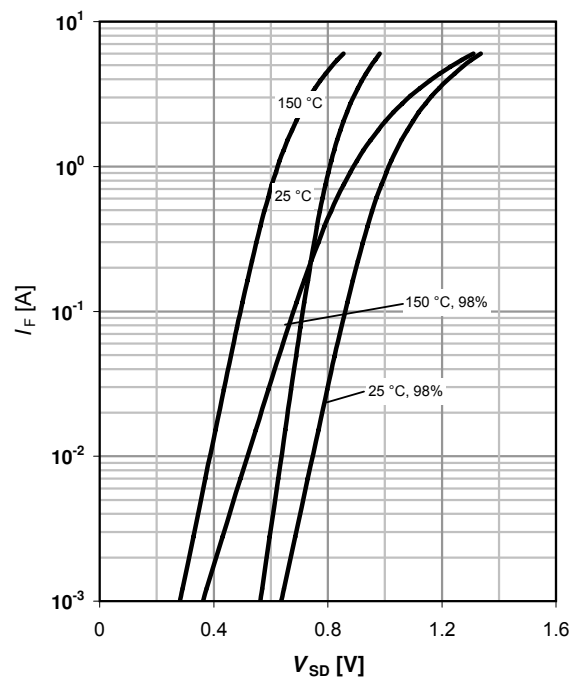
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25^\circ\text{C}$



12 Forward characteristics of reverse diode

$I_F = f(V_{SD})$

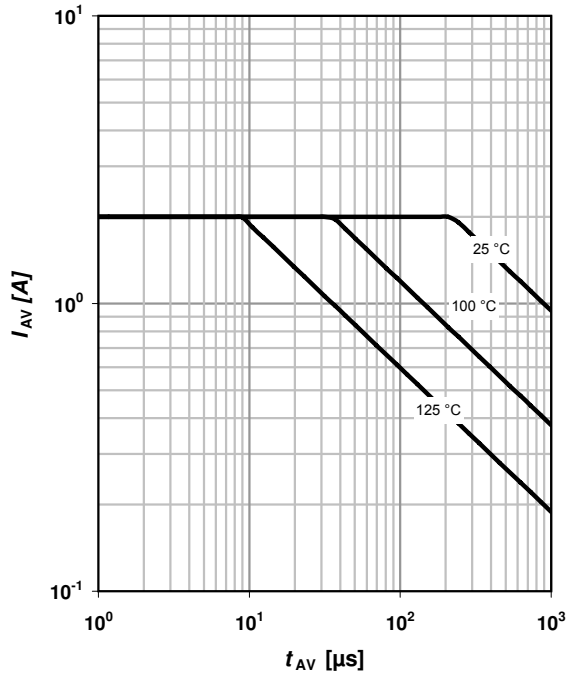
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

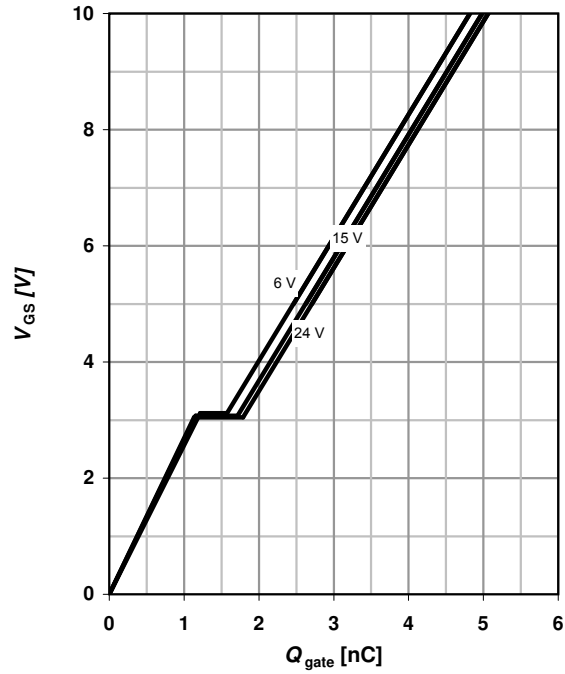
parameter: $T_{j(start)}$



14 Typ. gate charge

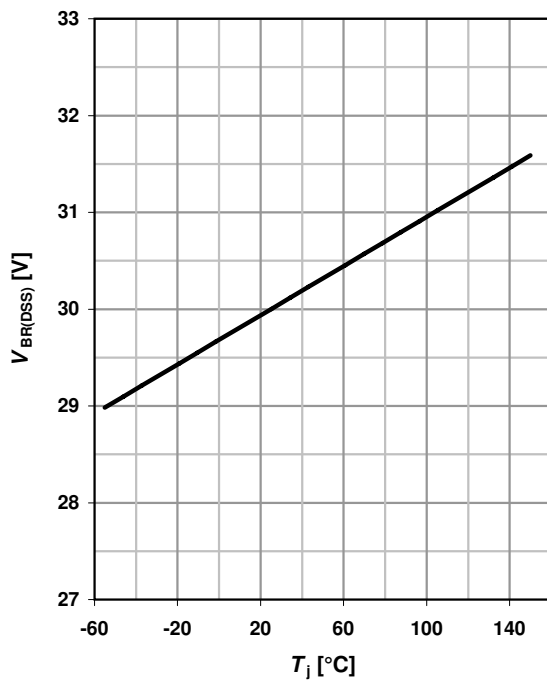
$V_{GS}=f(Q_{gate}); I_D=-2 \text{ A pulsed}$

parameter: V_{DD}

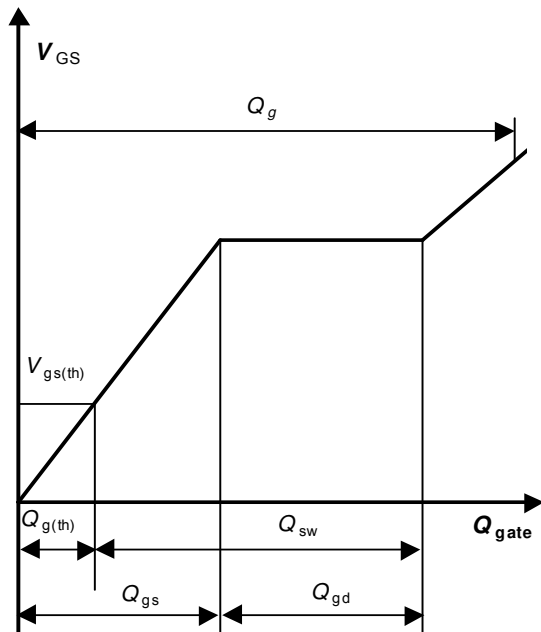


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=250 \mu\text{A}$

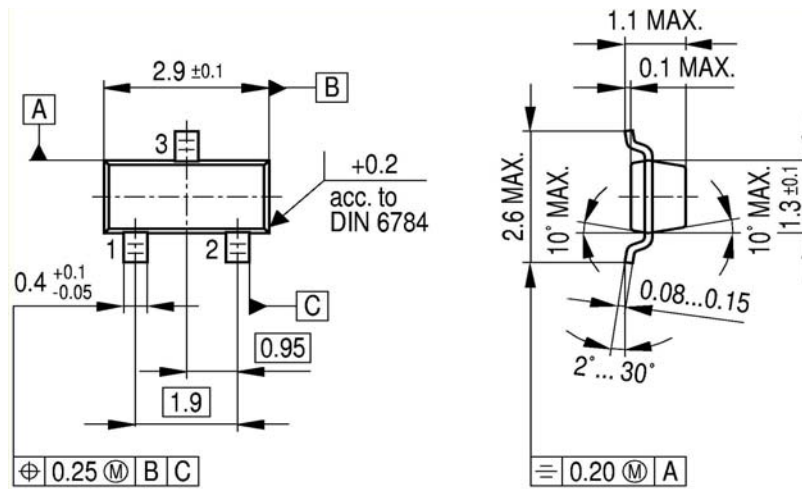


16 Gate charge waveforms

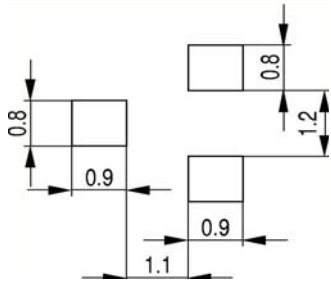


SOT-23

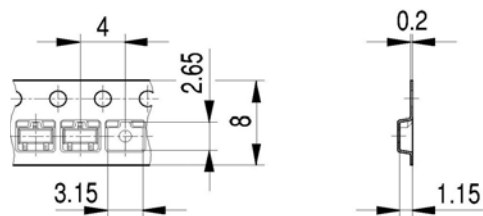
Package Outline:



Footprint:



Packaging:



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