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BT111: *Bluetooth*® Smart Ready HCI Module

DATA SHEET

Monday, 05 August 2013

Version 1.25

VERSION HISTORY

Version	Comment
1.0	First public release
1.1	Minor changes
1.2	FCC and CE update
1.21	Low energy master and slave mode supported
1.22	IC statement modified
1.23	Contact details updated
1.24	Formatting, reel dimensions
1.25	Recommended PCB land pattern added

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BT111: *Bluetooth* Smart Ready HCI Module

DESCRIPTION

BT111 is a low cost and ultra-small *Bluetooth* Smart Ready HCI module that is designed for applications where both *Bluetooth* classic and *Bluetooth* low energy connectivity is needed. BT111 integrates a *Bluetooth* 4.0 dual mode radio, HCI software stack, USB interface and an antenna. BT111 is compatible with Windows and Linux operating systems and Microsoft and BlueZ *Bluetooth* stacks and offers OEMs fast and risk free way to integrate *Bluetooth* 4.0 connectivity into their applications.

APPLICATIONS

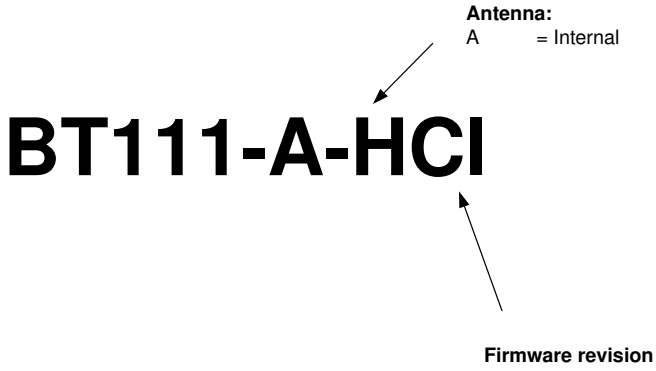
- Health and fitness gateways
- Point of sale
- M2M connectivity
- Automotive aftermarket
- Personal navigation devices
- Consumer electronics
- Industrial and home automation gateways

KEY FEATURES

- *Bluetooth* v.4.0, dual mode compliant
  - Support *Bluetooth* classic
  - Supports *Bluetooth* low energy master and slave mode
- Radio capabilities
  - Transmit power: +8dBm
  - Receiver sensitivity: -89dBm
  - Line-of-sight range: 100+ meters
  - Integrated antenna
- Interfaces
  - HCI over USB host interface
  - 802.11 co-existence interface
  - Software programmable GPIO
  - PCM or I2S audio interfaces
- Supply voltage: 1.7V to 3.6V or 3.1V to 3.6V
- Temperature range: -30C to +85C
- Ultra compact size: 13.05mm x 9.30mm
- *Bluetooth*, CE, FCC, IC and Japan

PHYSICAL OUTLOOK

1 BT111 Product numbering



Available products and product codes

Product code	Description
BT111-A-HCI	BT111 *Bluetooth* 4.0 HCI module with integrated antenna

2 Block Diagram

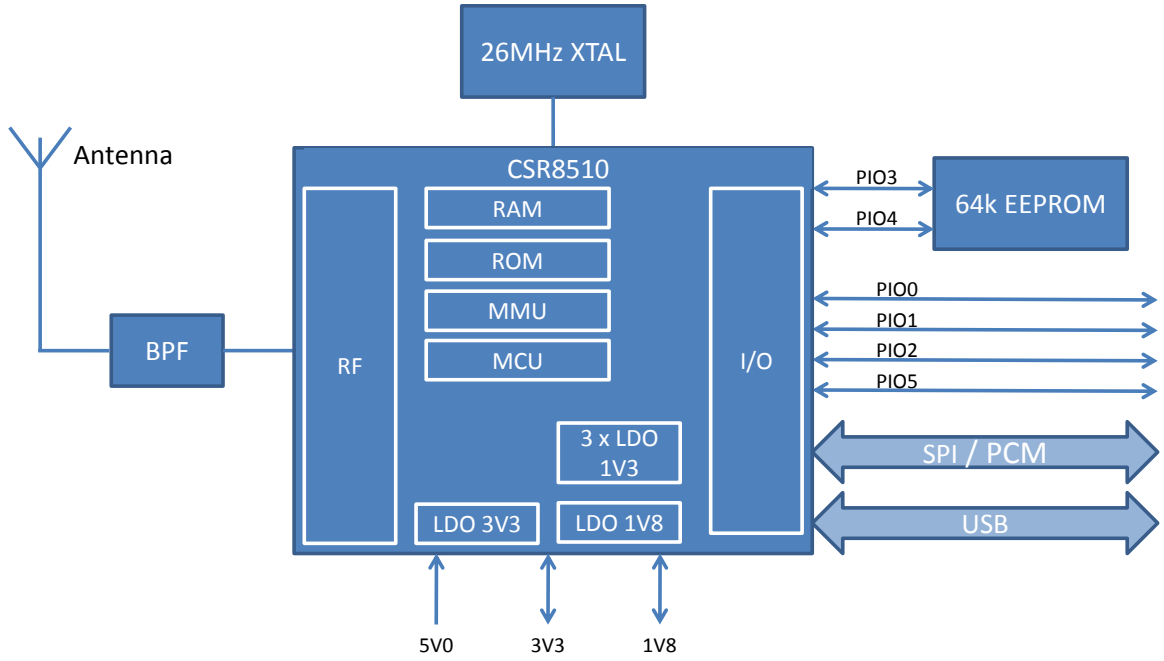


Figure 1: Block diagram of BT111

CSR8510

BT111 is based on CSR8510 dual mode chip. The chip includes all the functions required for a complete *Bluetooth* radio with on chip LDO regulators. The chip provides SPI, PCM and USB interfaces. Up to 4 general purpose I/Os are available for general usage, such as Wi-Fi coexistence or general indicators.

Antenna

Antenna is a ceramic monopole chip antenna. See the antenna characteristics in chapter 7.

Band Pass Filter

The band pass filter filters the out of band emissions from the transmitter to meet the specific regulations for type approvals of various countries.

64k EEPROM

The embedded 64k EEPROM can be used to store customizable parameters, such as maximum TX power, PCM configuration, USB product ID, USB vendor ID and USB product description.

26MHz Crystal

The embedded 26MHz crystal is used for generating the internal digital clocks.

3 Pinout and Terminal Descriptions

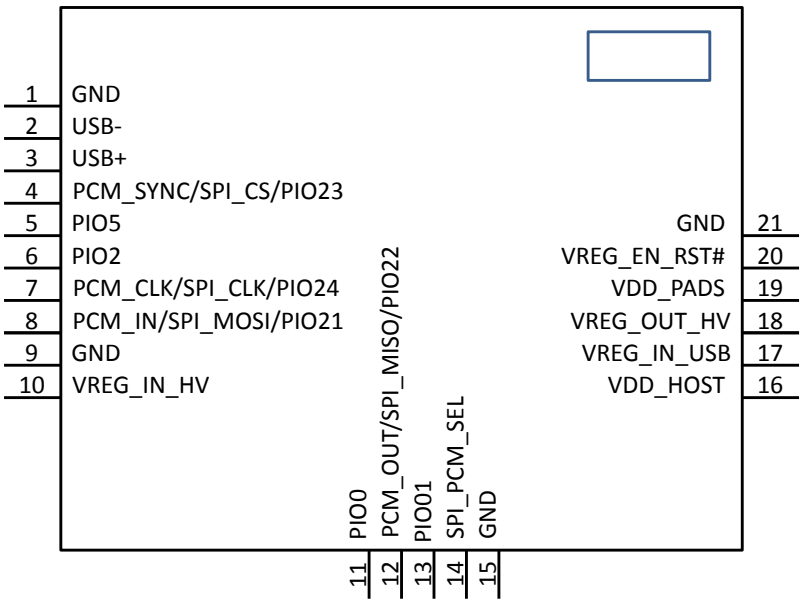


Figure 2: BT111

Power Supply	Pin No.	Pad Type	Description
VREG_EN_RST#	20	Input with strong internal pull-down	Take high to enable internal regulators. Also acts as active low reset. Maximum voltage is VDD_PADS **Note:** *USB regulator is always enabled and not controlled by this pin*
VREG_IN_HV	10	Analogue regulator input / output	Input to internal high-voltage regulator to 1.8V regulator, 3.3V output from USB regulator.
VREG_OUT_HV	18	Analogue regulator output	Output from internal high-voltage to 1.8V regulator. Input to second stage internal regulators.
VREG_IN_USB	17	Analogue regulator input	Input to USB regulator. Connect to external USB bus supply, e.g. USB_VBUS
VDD_HOST	16	VDD	USB system positive supply
VDD_PADS	19	VDD	Positive supply for digital I/O pads

Table 1: Supply Terminal Descriptions

PIO Port	Pin No.	Pad Type	Supply Domain	Description
PIO0	11	Bidirectional, tristate, with weak internal pull-down	VDD_PADS	Programmable input/output line
PIO1	13			
PIO2	6			
PIO5	5			

Table 2: I/O Terminal Descriptions

PCM Interface	Pin No.	Pad Type	Supply Domain	Description
PCM_OUT/ SPI_MISO/ PIO22	12	Output, tristate, with weak internal pull-down	VDD_PADS	PCM syncronous data output SPI data output Programmable input/output line
PCM_IN/ SPI_MOSI/ PIO21	8	Input, tristate, with weak internal pull-down		PCM syncronous data input SPI data input Programmable input/output line
PCM_SYNC/ SPI_CS#/ PIO23	4	Bidirectional, tristate, with weak internal pulldown		PCM syncronous dara sync SPI chip select, active low Programmable input/output line
PCM_CLK/ SPI_CLK/ PIO24	7			PCM syncronous data clock SPI clock Programmable input/output line
SPI_PCM#_SEL	14	Input with weak internal pull-down		High switches SPI/PCM lines to SPI, low switches SPI/PCM lines to PCM/PIO use

Table 3: PCM Interface

USB Interface	Pin No.	Pad Type	Supply Domain	Description
USB+	3	Bidirectional	VDD_HOST	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB-	2			USB data minus

Table 4: USB Interface

4 External Dimensions and Land Pattern

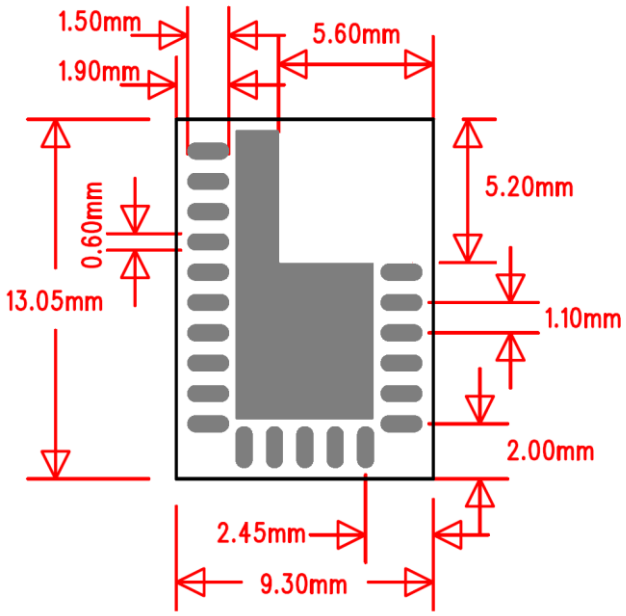


Figure 3: Footprint (top view)

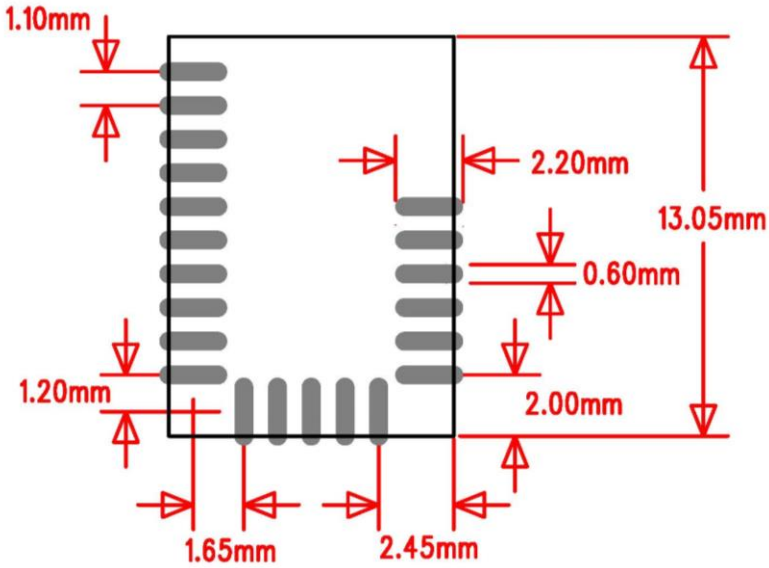


Figure 4: Recommended PCB land pattern

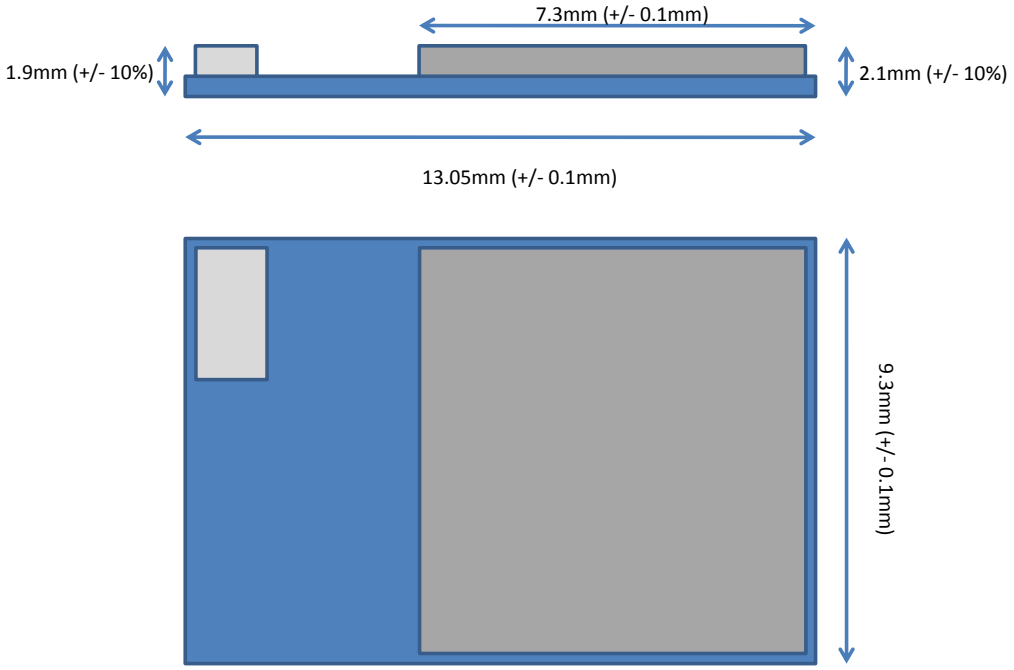


Figure 5: External dimensions

5 Layout Guidelines

Use good layout practices to avoid excessive noise coupling to supply voltage traces or sensitive analog signal traces. If using overlapping ground planes use stitching vias separated by max 3 mm to avoid emission from the edges of the PCB. Connect all the GND pins directly to a solid GND plane and make sure that there is a low impedance path for the return current following the signal and supply traces all the way from start to the end.

A good practice is to dedicate one of the inner layers to a solid GND plane and one of the inner layers to supply voltage planes and traces and route all the signals on top and bottom layers of the PCB. This arrangement will make sure that any return current follows the forward current as close as possible and any loops are minimized.

Figure 6: Typical 4-layer PCB construction

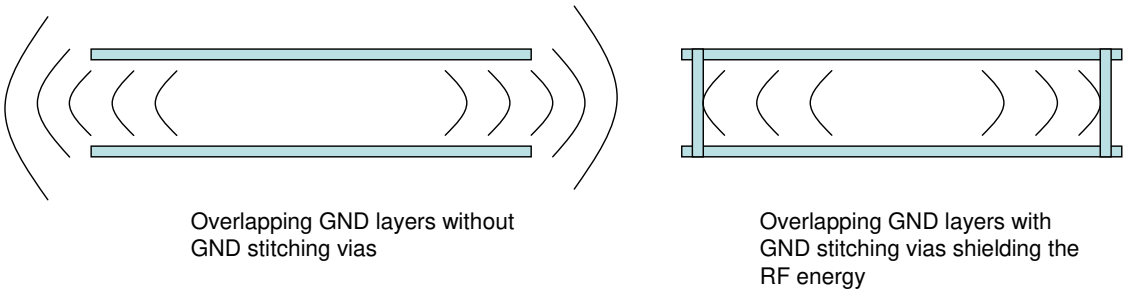


Figure 7: Use of stitching vias to avoid emissions from the edges of the PCB

5.1 BT111-A Layout Guide

For optimal performance of the antenna place the module at the corner of the PCB of the mother board as shown in the Figure 8. Optionally the module can be placed on the long edge of the mother board. In this case the metal clearance area must be extended minimum 10mm from the edge of the module, as shown in Figure 8. The layout of the mother board has an impact on the antenna characteristic and radiation pattern, see the antenna characteristics chapter. Do not place any metal (traces, components, battery etc.) within the clearance area of the antenna. Connect all the GND pins directly to a solid GND plane. Place the GND vias as close to the GND pins as possible. Use good layout practices to avoid any excessive noise coupling to signal lines or supply voltage lines. Avoid placing plastic or any other dielectric material closer than 5 mm from the antenna. Any dielectric closer than 5 mm from the antenna will detune the antenna to lower frequencies.

The antenna is optimized for mother board thickness of 1.0 mm. If the mother board is thicker than this, the resonant frequency will be tuned downwards. If the mother board thickness is thinner than 1.0 mm, the resonant frequency will be tuned upwards. S11 is a measure of how big portion of the transmitted power is reflected back from the antenna. An adequate performance can be expected if S11 is less than – 7 dB. If

using PCB thickness more than 1.6 mm, or if there is dielectric material around the antenna which is likely to detune the resonant frequency, the antenna can be tuned in the mother board layout by removing FR4 below the antenna.

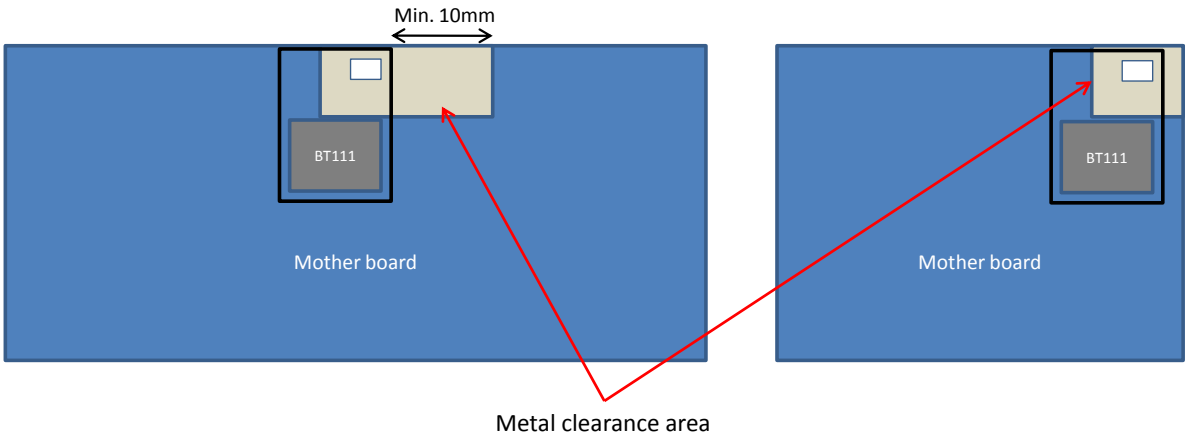


Figure 8: Recommended layouts for BT111-A

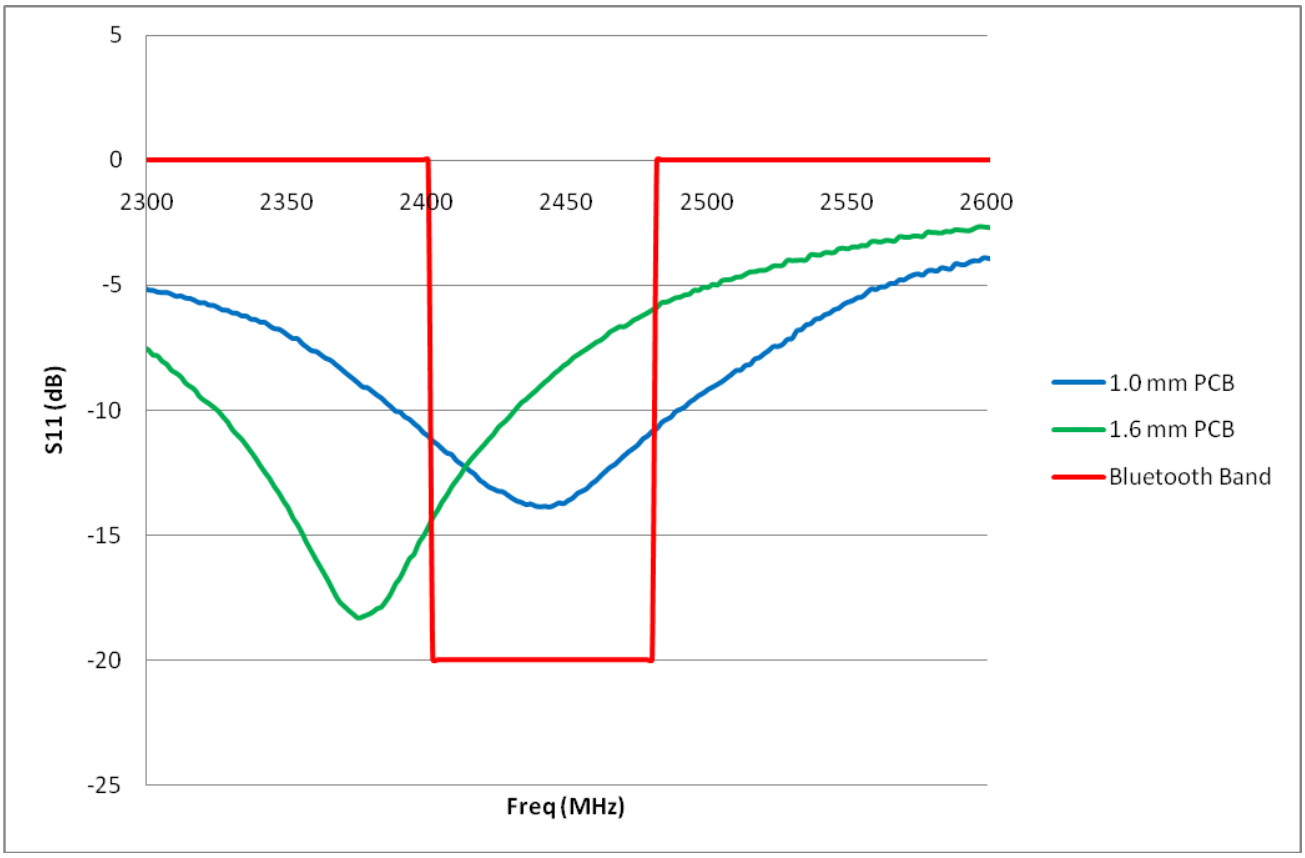


Figure 9: Impedance matching of the antenna of BT111 with two different mother board PCB thickness

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Rating	Min	Max	Unit
Storage temperature	-40	+85	ºC
VREG_IN_USB	-0.2	5.85	V
VREG_IN_HV	-0.2	4.9	V
VDD_HOST	-0.2	3.7	V
VDD_PADS	-0.2	3.7	V
Other terminal voltages	VSS - 0.4V	VDD + 0.4 V	V

Table 5: Absolute maximum ratings

Rating	Min	Max	Unit
Operating temperature	-30	+85	ºC
VREG_IN_USB	4.25	5.75	V
VREG_IN_HV	2.3	4.8	V
VDD_HOST	3.1	3.6	V
VDD_PADS (*	1.7(*	3.6(*	V

**) NOTE: The internal EEPROM is powered from VDD_PADS. To write the EEPROM, minimum supply voltage is 2.7V and maximum is 3.3V. For reading the EEPROM the minimum supply voltage is 1.7V and the maximum is 3.6V.*

Table 6: Recommended operating conditions

6.2 Input/Output Terminal Characteristics

6.2.1 USB Linear Regulator

Rating	Min	Typ	Max	Unit
Input voltage	4.25	5.0	5.75	V
Output voltage	3.2	3.3	3.4	V
Output current	-	-	150	mA

Table 7: USB linear regulator

6.2.2 High-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	2.3	3.3	4.8	V
Output voltage	1.75	1.85	1.95	V
Temperature coefficient	-200	-	200	ppm/°C
Output noise (frequency range 100Hz to 100kHz)	-	-	0.4	mV rms
Settling time (settling ti within 10% of final value)	-	-	5	µs
Output current	-	-	100	mA
Quiescent current (excluding load, I_{load} <1mA)	30	40	60	µA
Low-power Mode				
Quiescent current (excluding load, I_{load} <100µA)	14	18	23	µA

Table 8: High-voltage Linear Regulator

6.2.3 Digital

Normal Operation	Min	Typ	Max	Unit
Input Voltage				
V_{IL} input logic level low	-0.4	-	0.4	V
V_{IH} input logic level high	0.7 x VDD	-	VDD + 0.4	V
Output Voltage				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} output logic level high, I_{OL} = 4.0mA	0.75 x VDD	-	-	V
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	µA
Striong pull-down	10	40	150	µA
Weak pull-up	-5	-1.0	-0.33	µA
Weak pull-down	0.33	1.0	5.0	µA
C_I input capacitance	1.0	-	5.0	pF

Table 9: Digital I/O characteristics

6.3 Current Consumption

Normal Operation	Peak (8 dBm)	AVG	Unit
Idle		5	mA
USB Suspend		200	µA
Inguiry	73	51	mA
File Transfer	73	58	mA
LE Connected (Master)	74	(*	mA
LE Scan (Master)	48	(*	mA

*) LE AVG current consumption depends on the chosen TX interval and scanning window

Table 10: Current consumption of BT111 with 8 dBm TX power

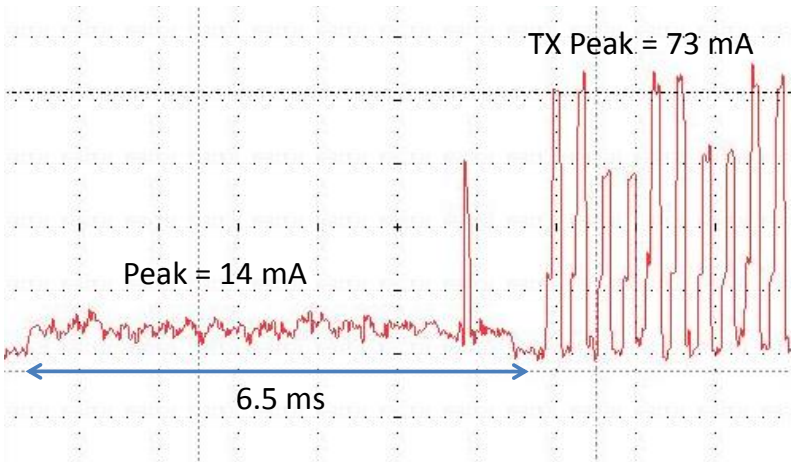


Figure 10: Current consumption profile while creating a SPP connection

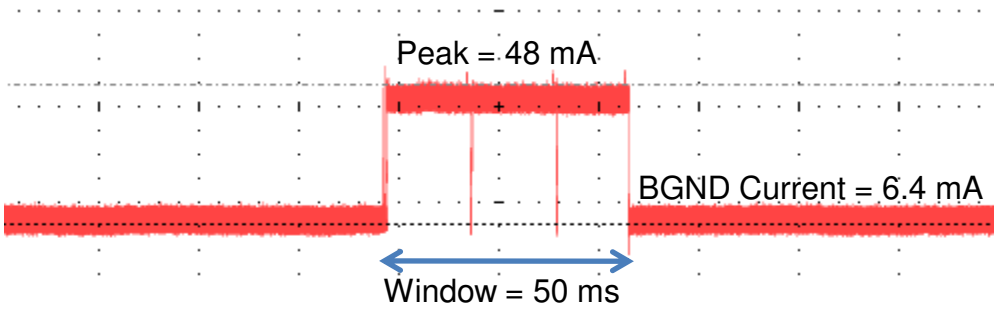


Figure 11: LE scanning with 50 ms window

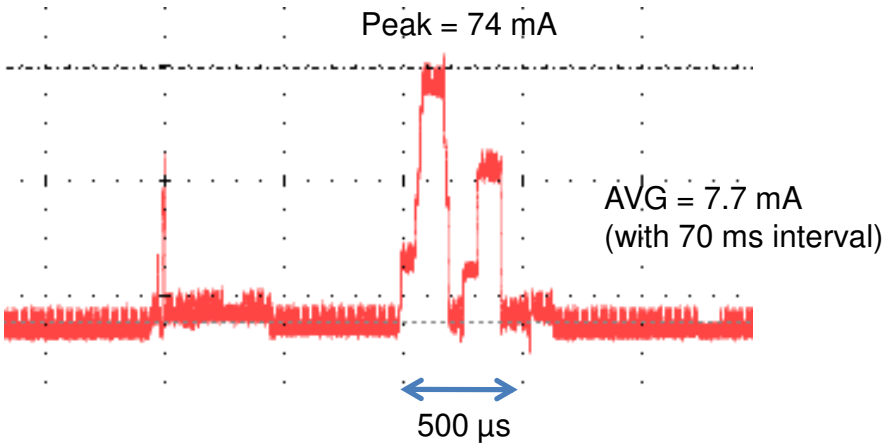


Figure 12: LE connected with 70 ms interval

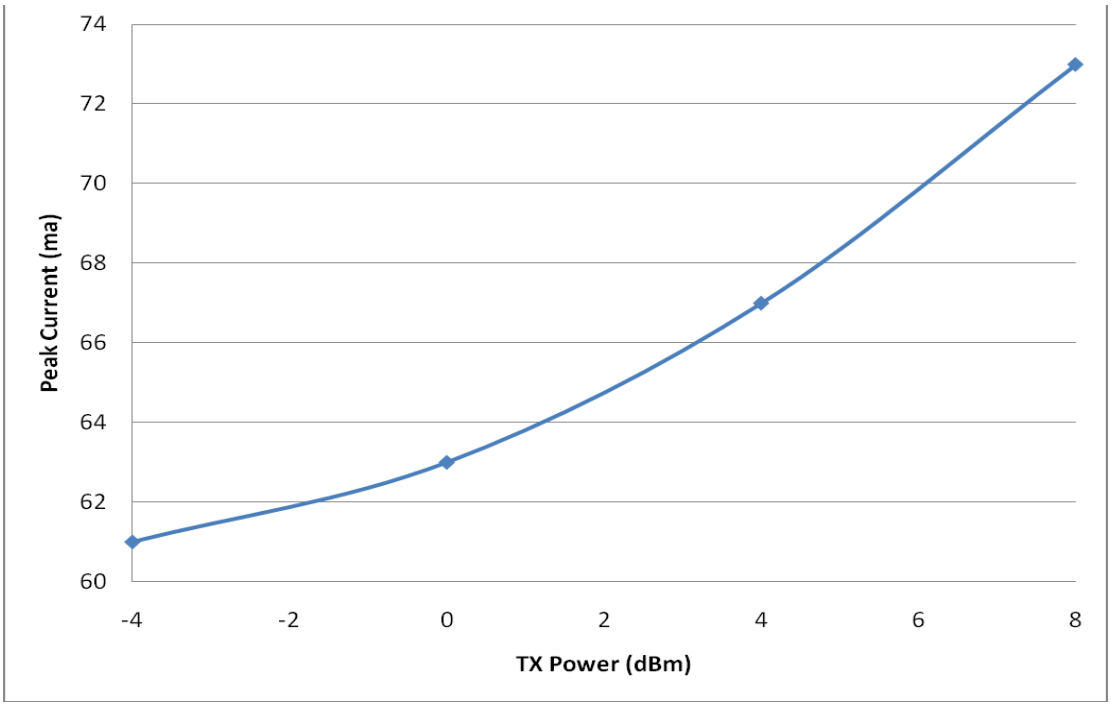


Figure 13: BDR Peak current vs TX power

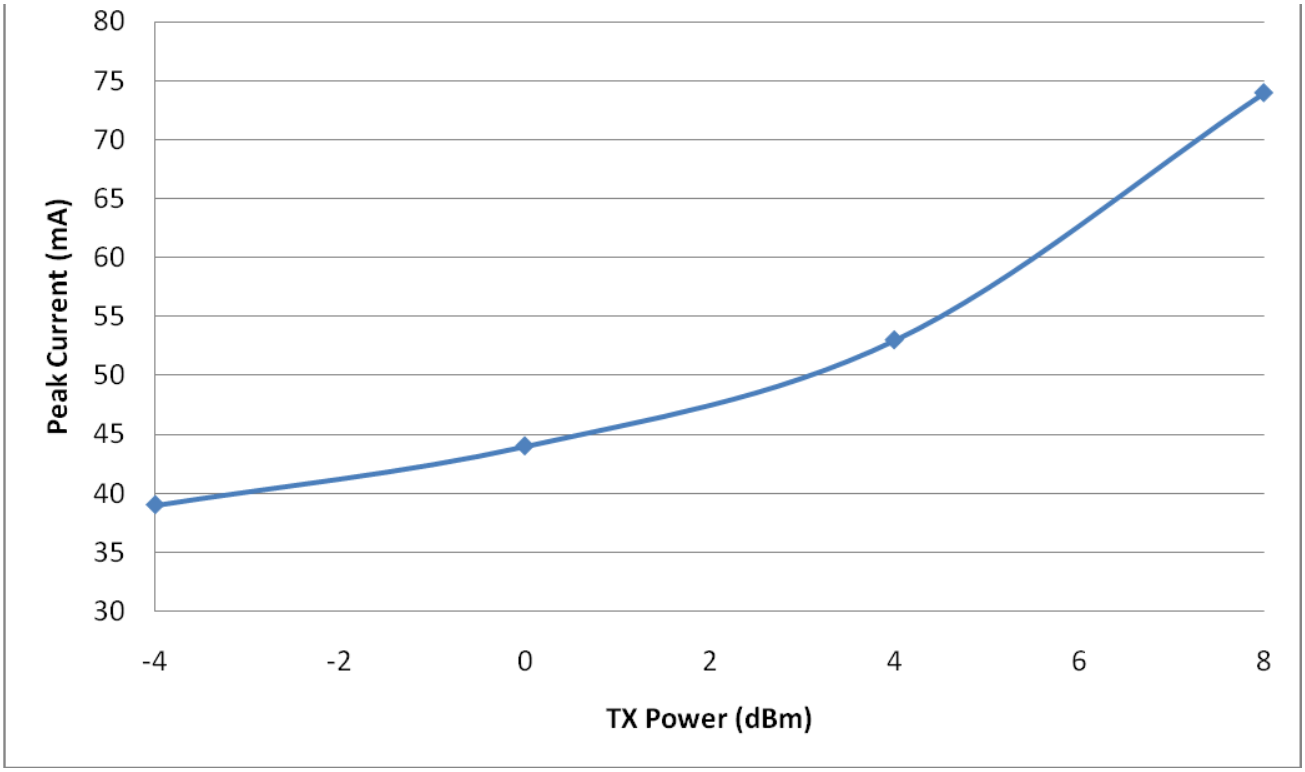


Figure 14: LE peak current vs. TX power

7 RF Characteristics

7.1 Transmitter Characteristics

RF Characetristics, VDD = 3.3V @ room temperature unless otherwise specified		Min	Typ	Max	Bluetooth Specification	Unit
maximum RF Transmit Power			8	10	20	dBm
RF power variation over temperature range			1.5		-	dB
RF power variation over supply voltage range				0.2	-	dB
RF power variation over BT band (*			2		-	dB
RF power control range		-21		8	-	dBm
20dB band width for modulated carrier					1000	kHz
ACP (1	$F = F_0 \pm 2MHz$				-20	
	$F = F_0 \pm 3MHz$				-40	
	$F = F_0 > 3MHz$				-40	
Drift rate			10		+/-25	kHz
ΔF_{1avg}			165		140<175	kHz
$\Delta F1_{max}$			168		140<175	kHz
$\Delta F_{2avg} / \Delta F_{1avg}$			0.9		>=0.8	

*) Channel 0 @2402Mhz has generally 1.0 dB lower TX power than all the other channels. All the channels between 2403 MHz and 2480 MHz are within 0.5 dB.

Table 11: Transmitter Characteristics, BDR

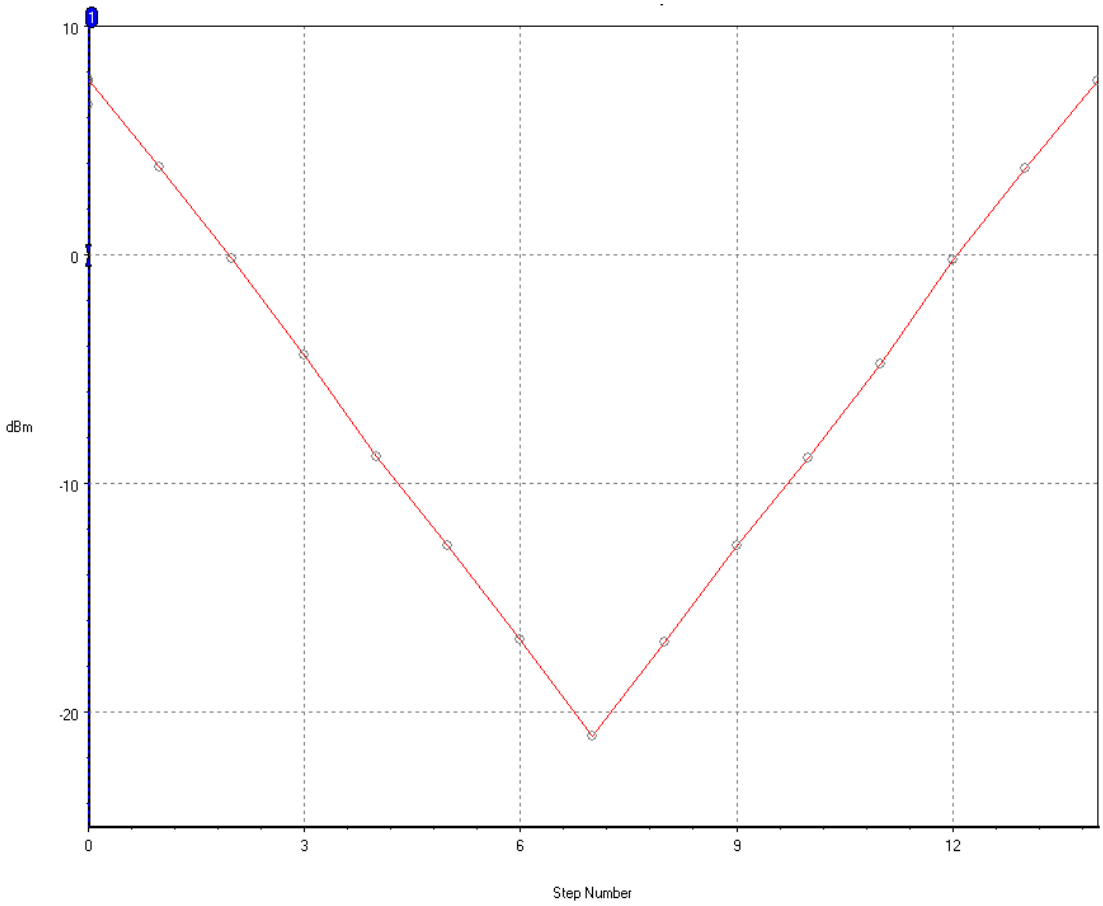


Figure 15: Power control steps of BT111

7.2 Receiver Characteristics

RF characteristis, VDD = 3.3V, room temperature	Packet type	Min	Typ	Max	Bluetooth Spefication	Unit
Sensitivity for 0.1% BER	DH1		-89		-70	dBm
	DH3		-89			dBm
	DH5		-89			dBm
	2-DH5		-92			dBm
	3-DH5		-85			dBm
Sensitivity variation over BT band (*	All		2			dB
Sensitivity variation over temperature range	All		TBD			dB

*) Channel 0 @2402Mhz is generally 1.5dB less sensitive than all the other channels. All the channels between 2403 MHz and 2480 MHz are within 0.5 dB.

Table 12: BDR and EDR receiver sensitivity

7.3 Radiated Spurious Emissions

Standard	Band / Frequency	Min (AVG / PEAK)	Typ (AVG / PEAK)	Max (AVG / PEAK)	Limit by the Standard (AVG / PEAK)	Unit
FCC part 15 transmitter spurious emissions	2nd harmonic		51 / 58		54 / 74	dBuV/m
	3rd harmonic		< 50		54 / 74	dBuV/m
	Band edge 2483.5MHz		48 / -		54 / 74	dBuV/m
	Band edge 2400MHz		-50		-20	dBc
	Band edge 2483.5MHz		-35		-20	dBc
ETSI EN 300 328 transmitter spurious emissions	Band edge 2400MHz		-42		-30	dBm
	2nd harmonic		-36		-30	dBm
	3rd harmonic		<-40		-30	dBm
ETSI EN 300 328 receiver spurious emissions	(2400 - 2479) MHz		<-70		-47	dBm
	(1600 - 1653) MHz		<-70		-47	dBm

Table 13: Radiated Spurious Emissions

7.4 Antenna Characteristics

The antenna is a standard monopole chip antenna. The radiation pattern is strongly dependent on the layout of the mother board. Usually the gain is highest to the directions where there is most GND and weakest to the opposite direction. Typically the total radiated efficiency is around 25% - 35%. The maximum gain is 0.5 dBi.

8 Clock Generation

BT111 is using an internal 26 MHz crystal oscillator. All internal digital clocks are generated using a phase locked loop, which is locked to the 26 MHz crystal oscillator. 26 MHz clock is calibrated in production and the calibrated settings are stored to the internal EEPROM of BT111. The 32.768 kHz sleep clock is generated internally to the module. BT111 does not need any external clock sources.

9 *Bluetooth* Stack Microcontroller

BT111 uses a 16-bit RISC MCU for low power consumption and efficient use of memory.

The MCU, interrupt controller and event timer run the *Bluetooth* software stack and control the *Bluetooth* radio and host interfaces.

10 Programmable I/O Ports

See the Device Terminal Functions section for the list of supplies to the PIOs.

PIO lines are configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset and have additional individual bus keeper configuration. The default configuration for all the IO pins is input with weak pull-up.

11 Wi-Fi Coexistence Interface

Dedicated hardware is provided to implement a variety of Wi-Fi coexistence schemes. There is support for:

- Channel skipping AFH
- Priority signaling
- Channel signaling
- Host passing of channel instructions

The BT111 supports the Wi-Fi coexistence schemes:

- Unity-3
- Unity-3e
- Unity+

Contact support (support@bluegiga.com) for more information

12 Memory Management

12.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimize the overheads on the processor during data/voice transfers.

12.2 System RAM

56KB of integrated RAM supports the RISC MCU and is shared between the ring buffers for holding voice/data for each active connection and the general-purpose memory required by the *Bluetooth* stack.

12.3 Internal ROM Memory (5Mb)

5Mb of internal ROM memory is available on BT111. This memory is provided for system firmware, storing BT111 settings and program code.

12.4 Internal EEPROM

64kb internal EEPROM is available on BT111 to store device specific configuration information (PS Keys) such as *Bluetooth* address, USB descriptors, PCM configuration and maximum TX power. The internal EEPROM is powered from VDD_PADS. The minimum supply voltage writing the EEPROM is 2.7V and the minimum supply voltage for reading the EEPROM is 1.7V.