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IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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WeEn Semiconductors



1. General description

Passivated sensitive gate Silicon Controlled Rectifier (SCR) in a SOT428 (DPAK) surface mountable plastic package intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Direct interfacing with low power drivers and microcontrollers
- High bidirectional blocking voltage capability
- High junction operating temperature capability
- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Very sensitive gate for logic level controls

3. Applications

- General purpose switching and phase control
- Ignition circuits, CDI for 2- and 3-wheelers
- Motor control - e.g. small kitchen appliances
- Protection circuits for Switched-Mode Power Supplies (SMPS)
- Protection circuits in lighting ballasts

4. Quick reference data

Table 1. Quick reference data

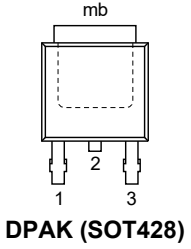

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
V_{RRM}	repetitive peak reverse voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	75	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	-	82	A
T_j	junction temperature	[1]	-	-	150	°C
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 135\text{ °C}$; Fig. 1	-	-	5	A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 135\text{ °C}$; Fig. 2 ; Fig. 3	-	-	8	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 8	20	-	50	μA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 150\text{ °C}$; $R_{GK} = 100\ \Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 13	35	70	-	$\text{V}/\mu\text{s}$

[1] Operation above junction temperatures of 110 °C may require the use of a gate to cathode resistor of 1 k Ω or less.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p style="text-align: center;">DPAK (SOT428)</p>	
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT258S-800LT	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

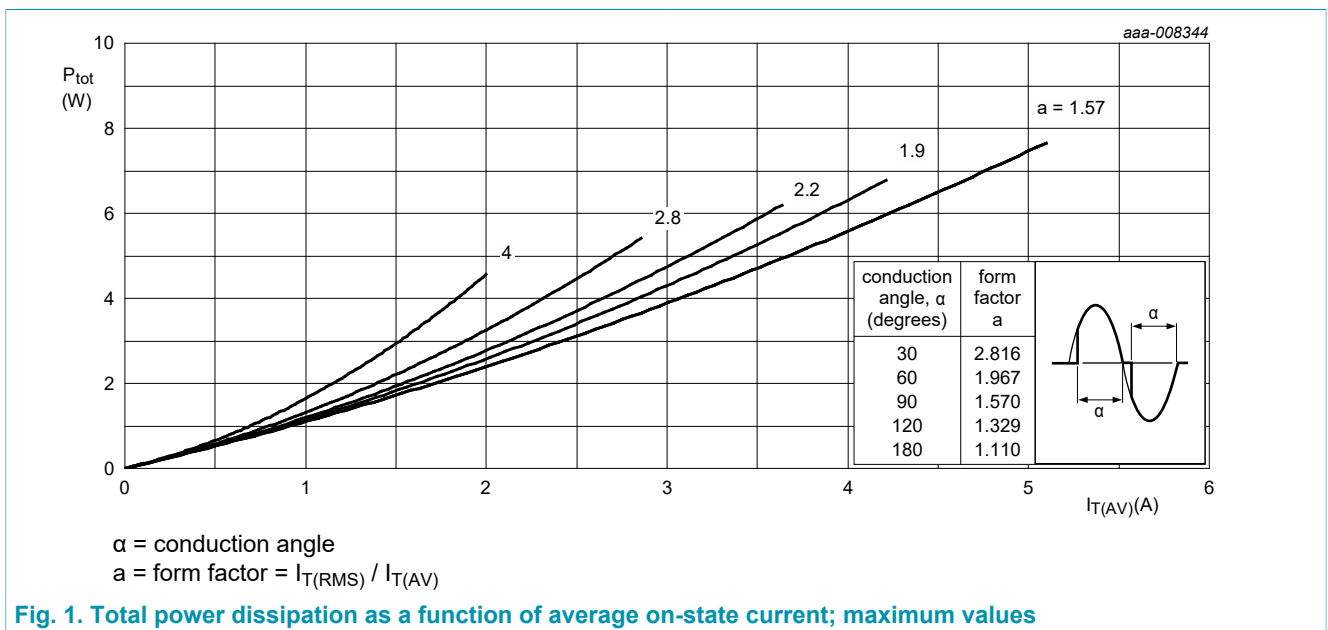
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
V_{RRM}	repetitive peak reverse voltage		-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 135\text{ °C}$; Fig. 1	-	5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 135\text{ °C}$; Fig. 2 ; Fig. 3	-	8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	75	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	82	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	28	A ² s
di_T/dt	rate of rise of on-state current	$I_T = 10\text{ A}$; $I_G = 50\text{ mA}$; $di_G/dt = 50\text{ mA}/\mu\text{s}$	-	50	A/ μs
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		[1]	150	°C

[1] Operation above junction temperatures of 110 °C may require the use of a gate to cathode resistor of 1 kΩ or less.



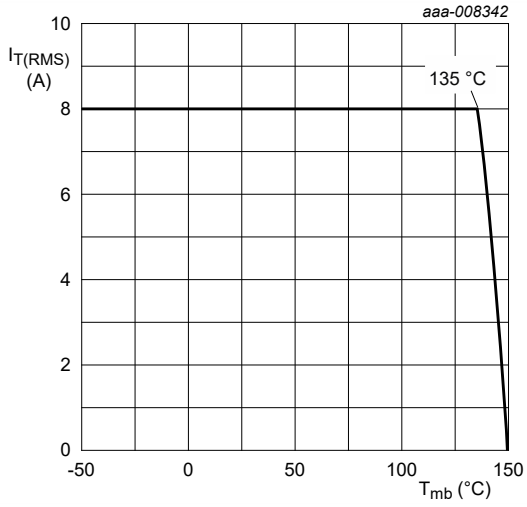
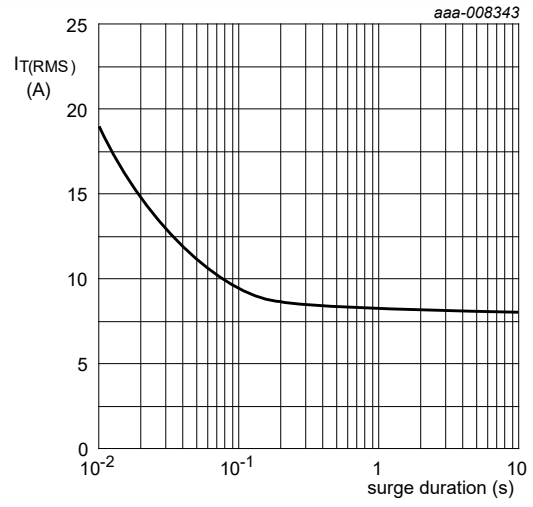
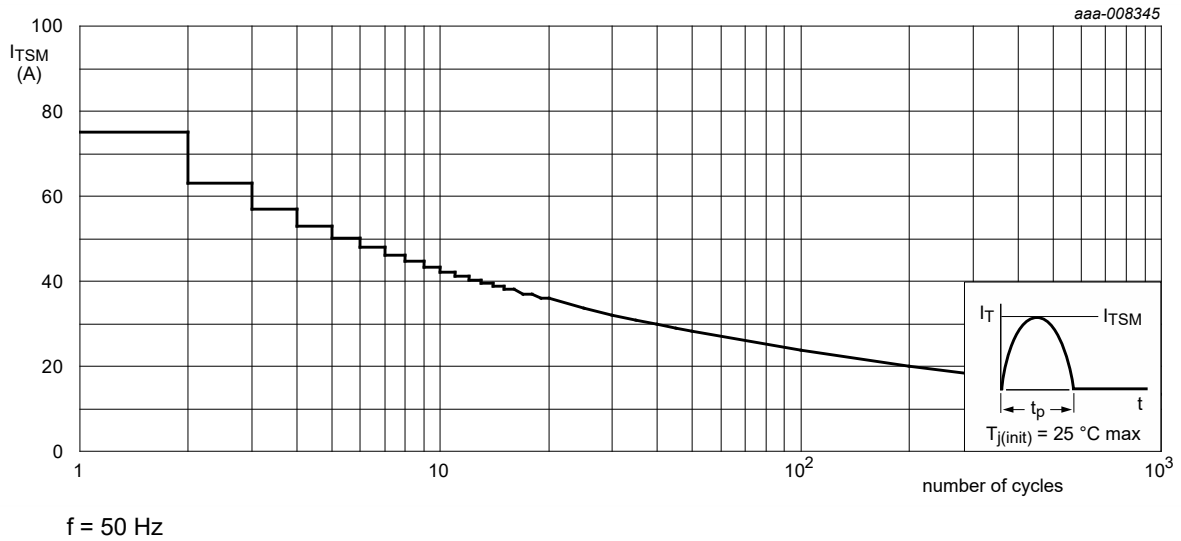


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



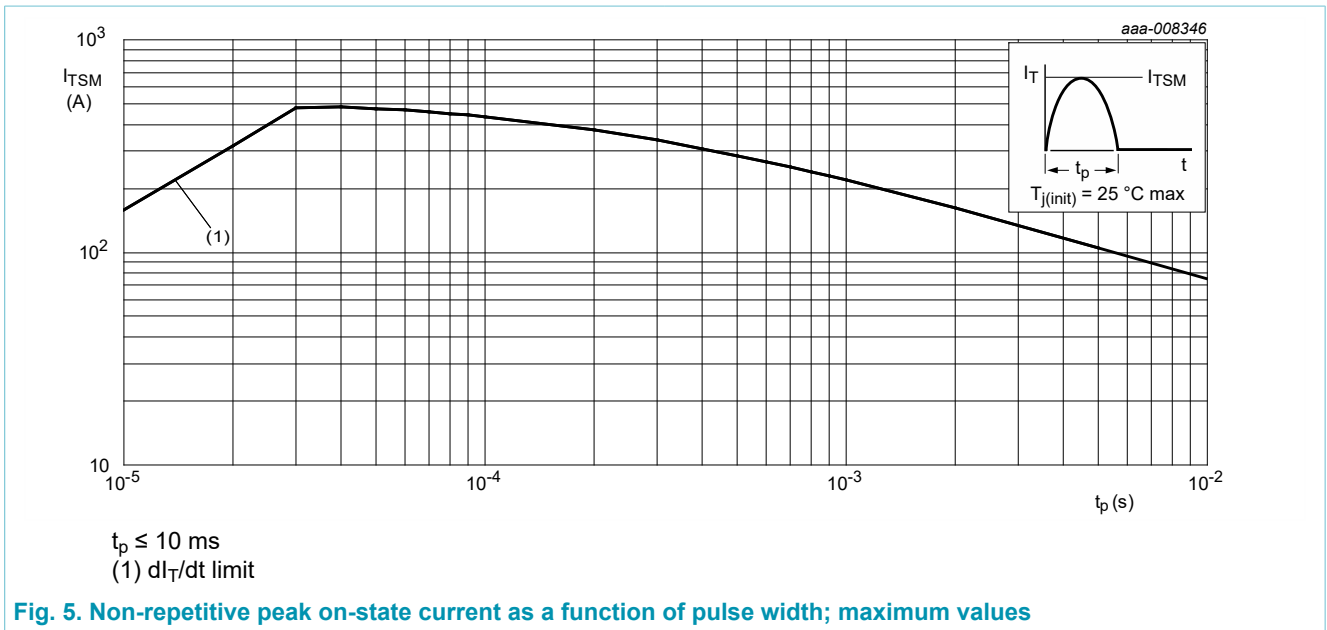
$f = 50 \text{ Hz}; T_{mb} = 135 \text{ °C}$

Fig. 3. RMS on-state current as a function of surge duration; maximum values



$f = 50 \text{ Hz}$

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6	-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	Device mounted on a FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint; Fig. 7	-	75	-	K/W

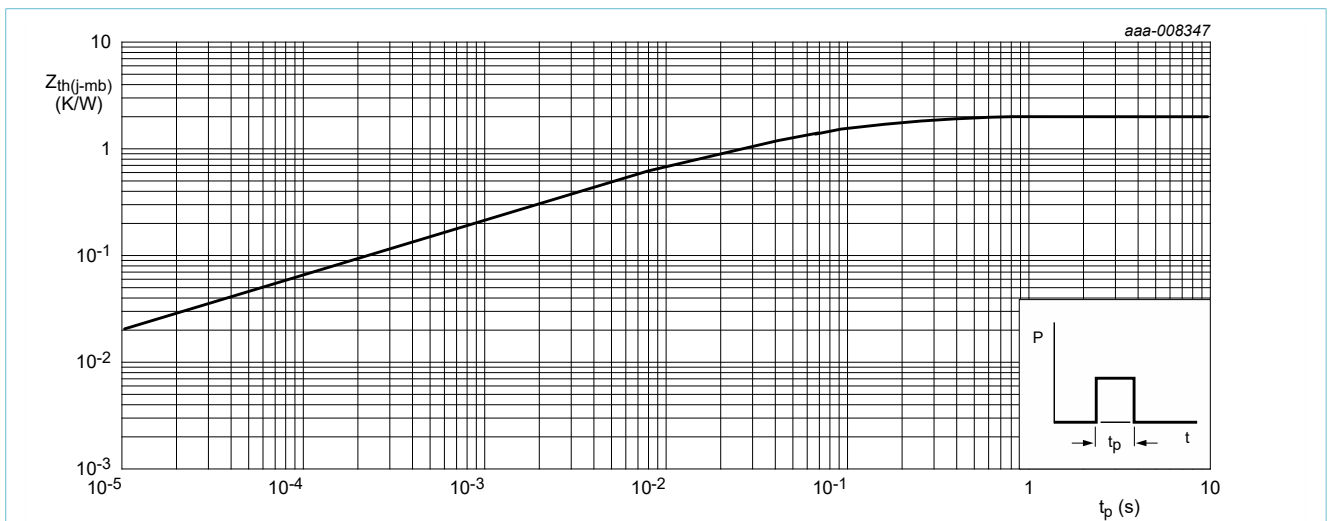


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

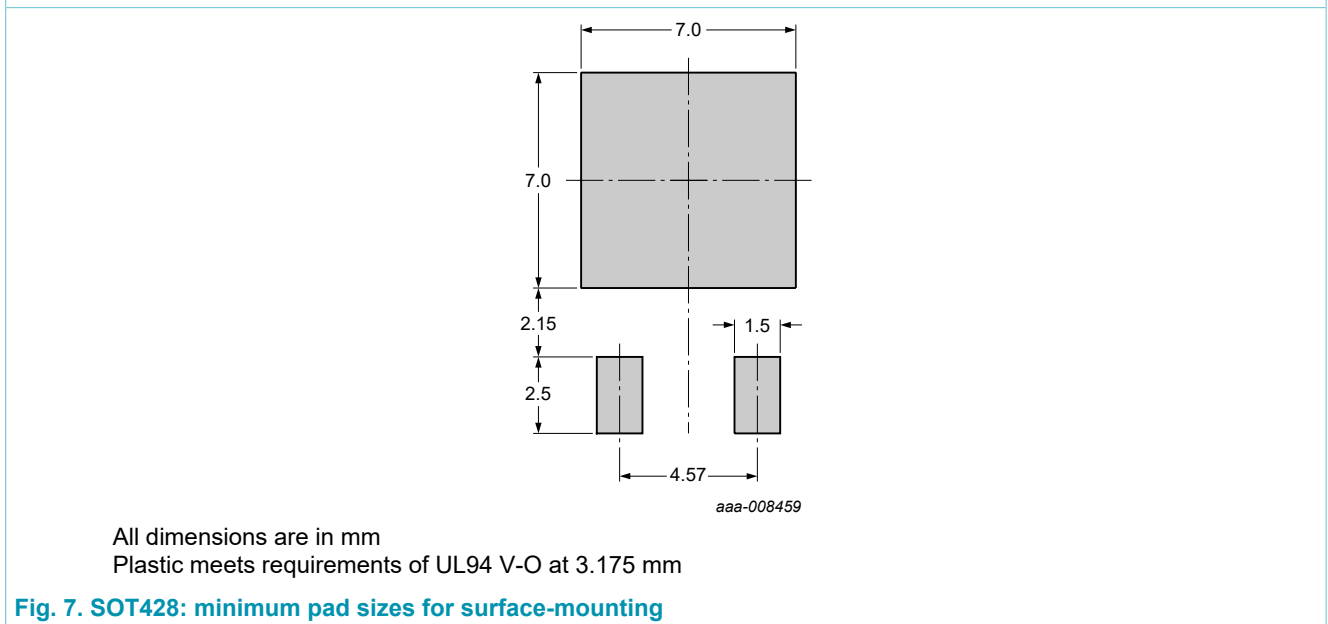
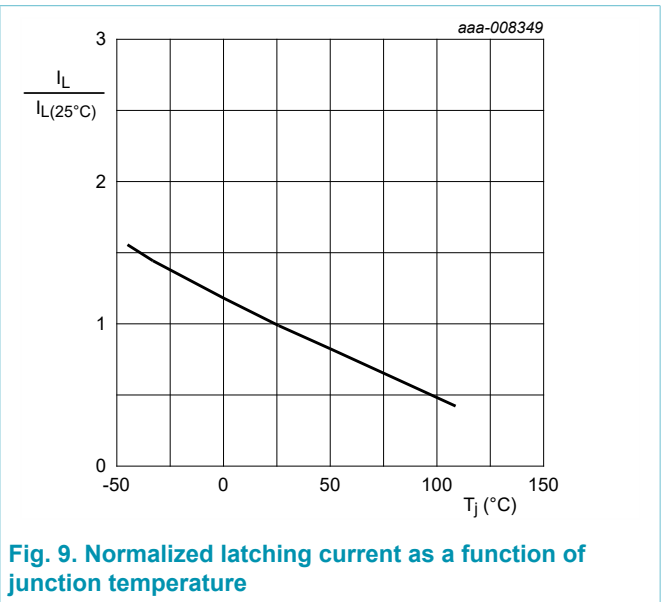
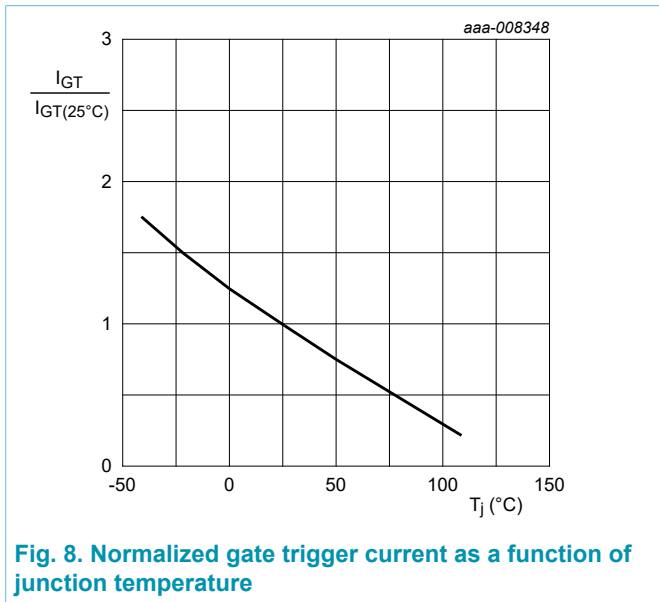


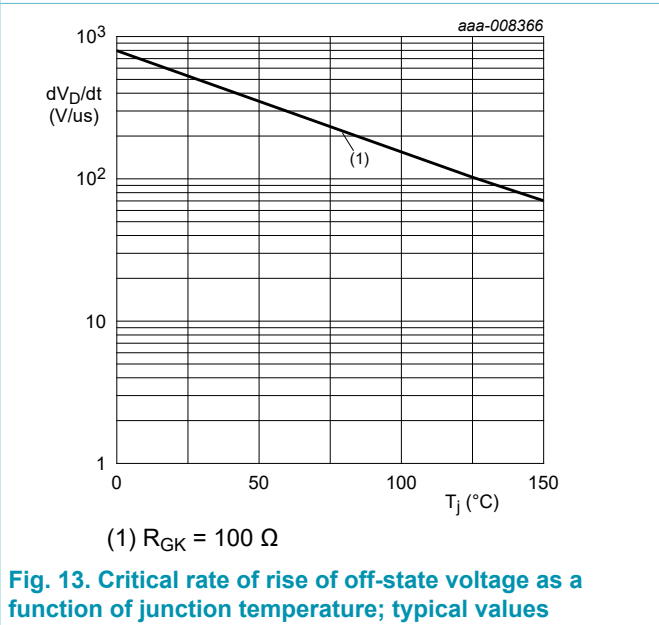
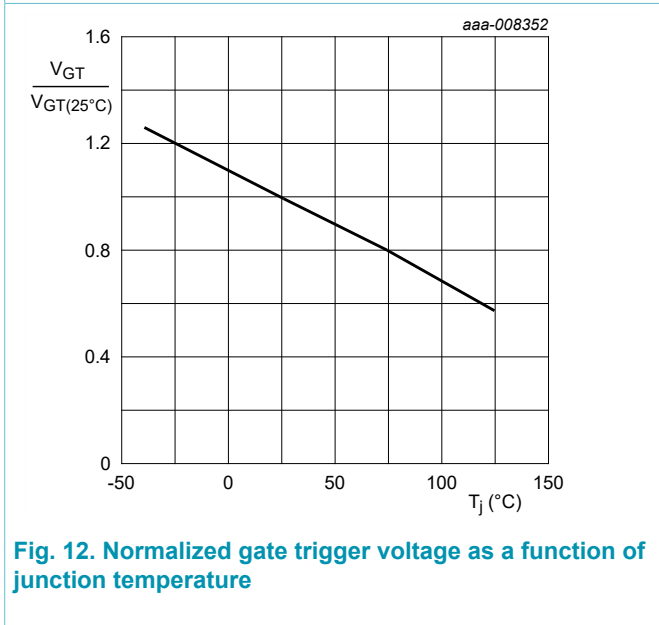
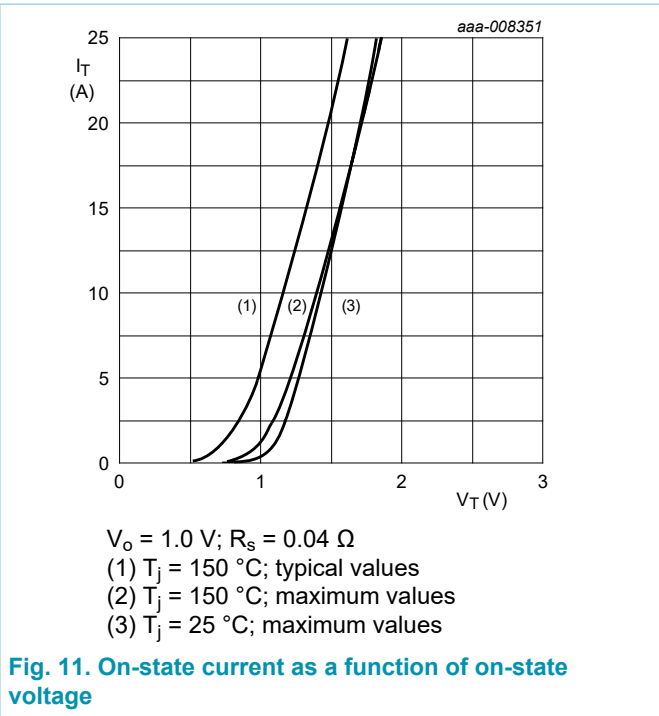
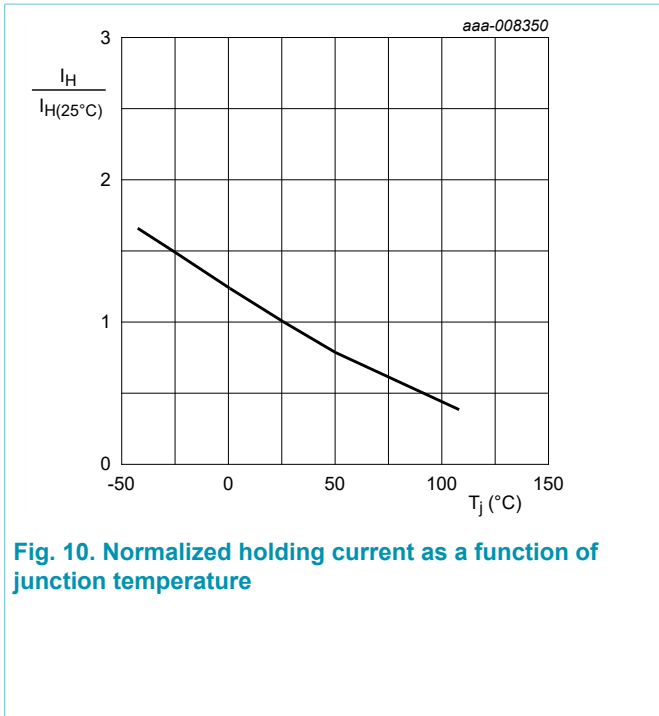
Fig. 7. SOT428: minimum pad sizes for surface-mounting

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 8	20	-	50	μA
I_L	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 9	-	0.4	10	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 10	-	0.3	6	mA
V_T	on-state voltage	$I_T = 16\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 11	-	1.3	1.6	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 12	-	0.4	1	V
		$V_D = 800\text{ V}; I_T = 0.1\text{ A}; T_j = 110\text{ }^\circ\text{C};$ Fig. 12	0.1	0.2	-	V
I_D	off-state current	$V_D = 800\text{ V}; T_j = 150\text{ }^\circ\text{C}$	-	0.5	2.5	mA
I_R	reverse current	$V_R = 800\text{ V}; T_j = 150\text{ }^\circ\text{C}$	-	0.5	2.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 150\text{ }^\circ\text{C}; R_{GK} = 100\ \Omega;$ ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 13	35	70	-	$\text{V}/\mu\text{s}$
t_{gt}	gate-controlled turn-on time	$I_{TM} = 10\text{ A}; V_D = 800\text{ V}; I_G = 5\text{ mA}; dI_G/dt = 0.2\text{ A}/\mu\text{s}; T_j = 25\text{ }^\circ\text{C}$	-	2	-	μs

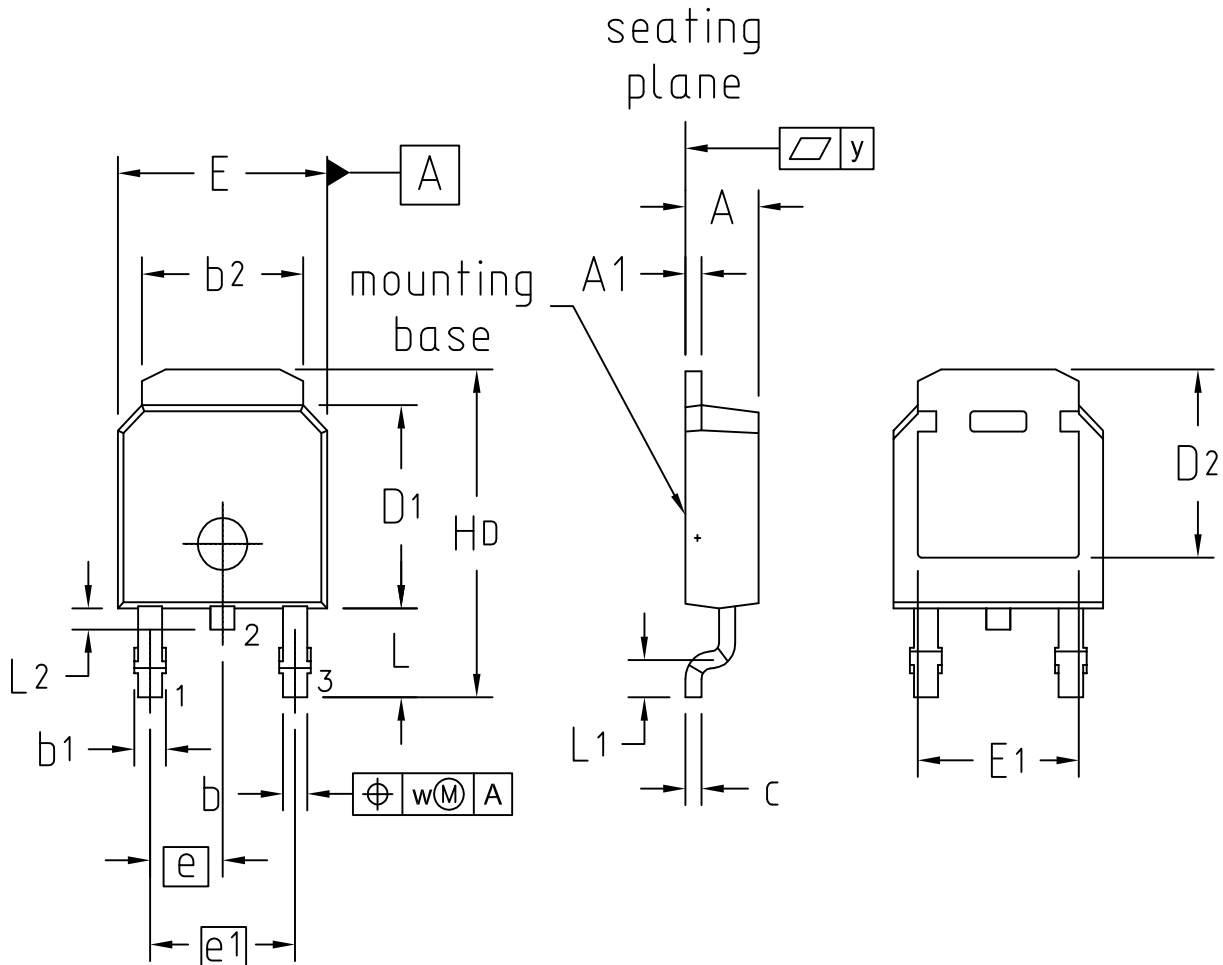




10. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428



UNIT	A	A ₁	b	b ₁	b ₂	c	D ₁	D ₂	E	E ₁	e	e ₁	H _b	L	L ₁	L ₂	w	y
mm	2.38	0.93	0.89	1.1	5.46	0.56	6.22	4.00	6.73	4.45	2.285	4.57	10.40	2.95	0.5	0.90	0.2	0.20
	2.22	0.46	0.71	0.9	5.00	0.20	5.98	min.	6.47	min.			9.60	2.55	min.	0.50	0.2	max.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428		TO-252				

Fig. 14. Package outline DPAK (SOT428)

11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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