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# Bluetooth v4.0 Dual-Mode USB HCI Module

## Hardware Integration Guide

*Version 1.5*

BT800-ST

global solutions: local support

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# REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| 1.0 | 04 Sept 2013 | Initial Release – Preliminary ST HIG |
| 1.1 | 30 Sept 2014 | Updated certification information (FCC, IC, CE, BT SIG) |
| 1.2 | 07 Oct 2014 | Updated Declaration of Conformity |
| 1.3 | 14 Oct 2014 | Removed X +/-1.3mm references |
| 1.4 | 03 Dec 2014 | Updated the Power Control and Regulation section. |
| 1.5 | 02 July 2015 | Added Tape/Reel (T/R) information |

# CONTENTS

# 1 SCOPE

This document describes key hardware aspects of the Laird BT800 Bluetooth HCI/HID module. This document is intended to assist device manufacturers and related parties with the integration of this module into their host devices. Data in this document are drawn from a number of sources including data sheets for the CSR8510.

# 2 OPERATIONAL DESCRIPTION

*BT800 module*


*BT820 USB dongle*

The BT800 series of USB HCI devices are designed to meet the needs of OEMs adding robust Bluetooth connectivity and using embedded Bluetooth stacks within these products.

Leveraging the market-leading CSR8510 chipset, the BT800 series provides exceptionally low power consumption with outstanding range. Supporting the latest Bluetooth v4.0 Specification with EDR (Enhanced Data Rate), the Laird BT800 series enables OEMs to accelerate their development time for leveraging either Classic Bluetooth or Bluetooth Low Energy (BLE) into their operating system based devices.

With a tiny footprint as small as 8.5 x 13 mm, yet output power at 8 dBm, these modules are ideal for applications where designers need high performance in minimal size. For maximum flexibility in systems integration, the modules are designed to support a full speed USB interface plus GPIO and additionally I2S and PCM audio interfaces.

These modules present an HCI interface and have native support for Windows and Linux Bluetooth software stacks. All BT800 series devices are fully qualified as Bluetooth Controller Subsystem products. This also allows designers to integrate their existing pre-approved Bluetooth Host and Profile subsystem stacks to gain a Bluetooth END product approval for their products.

The BT800 series is engineered to provide excellent RF performance with integrated antenna and additional band pass filters. It further reduces regulatory and testing requirements for OEMs and ensures a hassle free development cycle. As an additional benefit of the BT800 series, Laird has implemented CSR's HID (Human Interface Device) Proxy Mode enabling out of the box HID connectivity for pointing devices and / or keyboard functionality, requiring zero host device software or configuration.

A fully featured, low-cost developer's kit is available for prototyping, debug, and integration testing of the BT800 series modules and further reduces risk and time in development cycles.

Note: Laird also offers a **BT800-ST version** which is a trace pin variant of the BT800 for use with an external antenna.

### Features and Benefits

- Bluetooth v4.0 - Dual mode (Classic Bluetooth and BLE)
- Compact footprint
- 2-wire and 3-wire Wi-Fi coexistence scheme
- High antenna radiation gain and efficiency
- Good interference rejection for multi-com system (GSM/WCDMA)
- Class 1 output – 8 dBm
- USB, GPIO, I2S, and PCM
- Industrial Temperature Range
- 64 k EEPROM support for HID Proxy mode
- Bluetooth Controller subsystem
- FCC, IC, CE, and MIC approvals

### Application Areas

- Medical devices
- ePOS terminals
- Barcode scanners
- Industrial Cable Replacement
- M2M Connectivity
- Automotive Diagnostic Equipment
- Personal Digital Assistants (PDA)
- Bluetooth HID device (keyboard, mouse, joystick)

# 3 Block Diagram and Descriptions

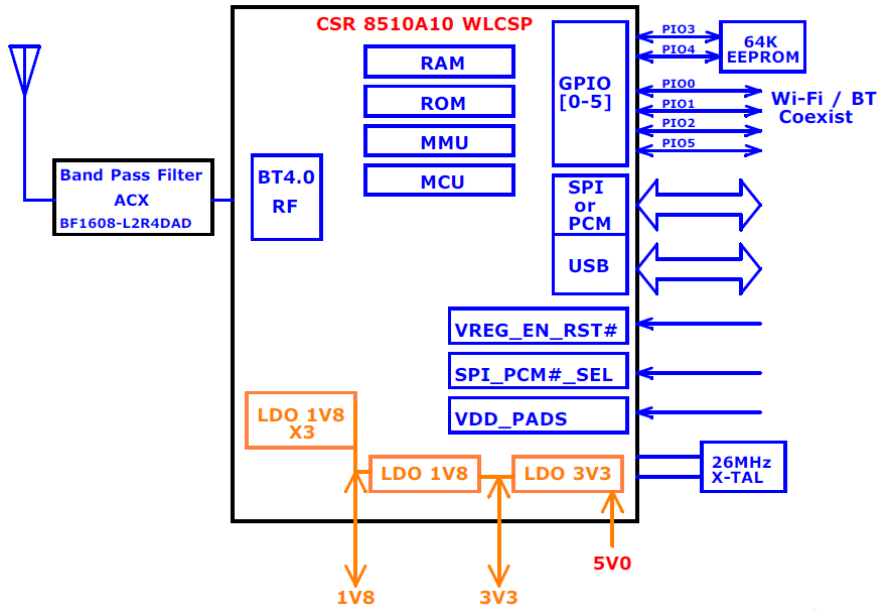



*Figure 1: BT800 module block diagram*

| | |
|---|---|
| CS8510A10 (Main chip) | The BT800 is based on CSR8510A10 dual mode chip. The chip is a single-chip radio with on-chip LDO regulators and baseband IC for Bluetooth 2.4 GHz systems including EDR to 3 Mbps. Dedicated signal and baseband processing is included for full Bluetooth operation. The chip provides SPI/PCM and USB interfaces. Up to four general purpose I/Os are available for general use such as Wi-Fi coexistence or general indicators.<br><br>**Note:** The purpose of the SPI interface is to access the module's inner settings such as selecting different WLAN CO-EXIST scheme and enabling HID proxy mode. The SPI interface can also be used to put the module in RF test mode. You cannot use the module over the SPI interface for normal operation as the main host interface. |
| Antenna Options | BT800 The antenna is a ceramic monopole chip antenna.<br>BT800-ST A trace pin variant of the BT800 for use with an external antenna. |
| Band Pass Filter | The band pass filter filters the out-of-band emissions from the transmitter to meet the specific regulations for type approvals of various countries. |
| EEPROM | There are 64 k bits EEPROM embedded on the BT800 module which can be used to store customizable parameters, such as maximum TX power, PCM configuration, USB product ID, USB vendor ID, and USB product description. With that, the BT800 module can support HID/HCI Proxy mode. |
| Crystal | The embedded 26 MHz crystal is used for generating the clock for the entire module. |

# 4 SPECIFICATIONS

*Table 1: BT800 specifications*

| CATEGORIES | FEATURE | IMPLEMENTATION |
|---|---|---|
| Wireless Specification | Bluetooth® | V4.0 Dual Mode |
| | Frequency | 2.402 - 2.480 GHz |
| | Maximum Transmit Power | Class 1<br>+8 dBm from antenna |
| | Receive Sensitivity | -89 dBm |
| | Range | Circa 100 meters |
| | Data Rates | Up to 3 Mbps (over the air) |
| Host Interface | USB | Full Speed USB 2.0 |
| | GPIO | Four configurable lines<br>(1.8V/3.3V configurable by VDD_PADS) |
| Operational Modes | HCI | Host Controller Interface over USB |
| | HID Proxy Mode | Human Interface Device |
| EEPROM | 2-wire | 64 K bits |
| Coexistence | 802.11 (Wi-Fi) | 3 wire CSR schemes supported<br>(Unity-3;Unity-3e, and Unity+) |
| Supply Voltage | Supply | 5V +/-10%<br>**Note:** See *Implementation Note* for details on different DC power selections on the BT800. |
| Power Consumption | Current | Idle Mode ~5 mA<br>File Transfer ~58 mA |
| Antenna Option | Internal (BT800)<br>External (BT800-ST) | Multilayer ceramic antenna with up to 41% efficiency.<br>A trace pin variant of the BT800 for use with an external antenna. |
| Physical | Dimensions | 8.5 x 13 x 1.75 mm (BT800 ) +/- 1.3mm (L/W) |
| | | 8.5 x 13 x 1.7 mm (BT800-ST ) |
| | | 16 x 43 x 11 (BT820 – USB Dongle) |
| Environmental | Operating | -30C to +85C |
| | Storage | -40C to +85C |
| Miscellaneous | Lead Free | Lead-free and RoHS compliant |
| | Warranty | 1 Year |
| Approvals | Bluetooth® | Controller Subsystem Approved |
| | FCC / IC / CE | All BT800 series (BT800; BT800-ST) |

# 5 PIN DEFINITIONS

*Table 2: BT800 pin definitions*

| # | Pin Name | I/O | Supply Domain | Description | If Unused |
|---|---|---|---|---|---|
| 1 | SPI_PCM#_SEL | Input with weak internal pull-down | VDD_PADS | High switches SPI/PCM lines to SPI,<br>Low switches SPI/PCM lines to PCM/PIO<br>*See Note 1. | NC |
| 2 | VDD_HOST | Power supply | (3.1V-3.6V) | USB system positive supply | N/A |
| 3 | GND | GND | - | Ground | GND |
| 4 | USB+ | Bidirectional | VDD_HOST | USB data plus with selectable internal 1.5kΩ pull-up resistor | NC |
| 5 | USB- | Bidirectional | VDD_HOST | | NC |
| 6 | GND | GND | - | Ground | GND |
| 7 | VREG_IN_USB | Power supply | Analogue regulator input | Input to USB regulator. Connect to external USB bus supply (USB_VBUS) | N/A |
| 8 | VREG_EN_RST# | Input with strong internal pull-down | VDD_PADS | Take high to enable internal regulators. Also acts as active low reset. Maximum voltage is VDD_PADS.<br>Note: *USB regulator is always enabled and not controlled by this pin.* | NC |
| 9 | VREG_IN_HV | Analogue regulator input / output | 3.3V | Input to internal high-voltage regulator to 1.8V regulator, 3.3V output from USB regulator. | N/A |
| 10 | VREG_OUT_HV | Analogue regulator input / output | 1.8V | Output from internal high-voltage to 1.8V regulator. Input to second stage internal regulators. | N/A |
| 11 | GND | GND | - | Ground | GND |
| 12 | GND | GND | - | Ground | GND |
| 13 | GND | GND | - | Ground | GND |
| 14 | GND | GND | - | Ground | GND |
| 15 | GND | GND | - | Ground | GND |
| 16 | GND | GND | - | Ground | GND |
| 17 | RF | - | - | BT800- No connection<br>BT800-ST – Configured as RF signal output (50 ohm) | - |
| 18 | GND | GND | - | Ground | GND |

| # | Pin Name | I/O | Supply Domain | Description | If Unused |
|---|---|---|---|---|---|
| 19 | PCM_SYNC/<br>SPI_CS#/<br>PIO23 | Bidirectional, tri-state, with weak internal pull-down | VDD_PADS | PCM synchronous data sync SPI chip select, active low<br>Programmable input/output line<br>*See Note 1. | NC |
| 20 | PCM_CLK/<br>SPI_CLK/<br>PIO24 | Bidirectional, tri-state, with weak internal pull-down | VDD_PADS | PCM synchronous data clock<br>SPI clock<br>Programmable input/output line<br>*See Note 1. | NC |
| 21 | PCM_IN/<br>SPI_MOSI/<br>PIO21 | Input, tri-state, with weak internal pull-down | VDD_PADS | PCM synchronous data input<br>SPI data input<br>Programmable input/output line<br>*See Note 1. | NC |
| 22 | PCM_OUT/<br>SPI_MISO/<br>PIO22 | Output, tri-state, with weak internal pull-down | VDD_PADS | PCM synchronous data output<br>SPI data output<br>Programmable input/output line<br>*See Note 1. | NC |
| 23 | PIO0/<br>WLAN_ACTIVE | Bidirectional, tri-state, with weak internal pull- down | VDD_PADS | Programmable input/output line | NC |
| 24 | GND | GND | - | Ground | GND |
| 25 | PIO1/<br>BT_PIRORITY | Bidirectional, tri-state, with weak internal pull- down | VDD_PADS | Programmable input/output line | NC |
| 26 | PIO2/<br>BT_ACTIVE | Bidirectional, tri-state, with weak internal pull- down | VDD_PADS | Programmable input/output line | NC |
| 27 | VDD_PADS | Power supply | (1.7V-3.6V) | Positive supply for digital I/O pads | N/A |
| 28 | PIO5 | Bidirectional, tri-state, with weak internal pull- down | VDD_PADS | Programmable input/output line | NC |

**Note 1:** The purpose of the SPI interface is to access the module's inner settings such as selecting different WLAN CO-EXIST scheme and enabling HID proxy mode. The SPI interface can also be used to put the module in RF test mode. You cannot use the module over the SPI interface for normal operation as the main host interface.

# 6 DC Electrical Characteristic

*Table 3: Absolute maximum ratings*

| Rating | Min | Max | Unit |
|---|---|---|---|
| Storage temperature | -40 | +85 | $^0$C |
| VREG_IN_USB | -0.2 | 5.75 | V |
| VREG_IN_HV | -0.2 | 4.9 | V |
| VDD_HOST | -0.2 | 3.7 | V |
| VDD_PADS | -0.2 | 3.7 | V |
| Other terminal voltages | VSS - 0.4V | VDD + 0.4 V | V |

*Table 4: Recommended operating conditions*

| Rating | Min | Max | Unit |
|---|---|---|---|
| Operating temperature | -30 | +85 | $^0$C |
| VREG_IN_USB | 4.5 | 5.5 | V |
| VREG_IN_HV | 3.1 | 3.6 | V |
| VDD_HOST | 3.1 | 3.6 | V |
| VDD_PADS | 1.7 | 3.6 | V |

*Table 5: USB Linear Regulator*

| Rating | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input voltage (VREG_IN_USB) | 4.5 | 5.0 | 5.5 | V |
| Output voltage (VREG_IN_HV) | 3.2 | 3.3 | 3.4 | V |
| Output current | - | - | 150 | mA |

*Table 6: High-voltage Linear Regulator*

| Normal Operation | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input voltage (VREG_IN_HV) | 3.1 | 3.3 | 3.6 | V |
| Output voltage (VREG_OUT_HV) | 1.75 | 1.85 | 1.95 | V |
| Temperature coefficient | -200 | - | 200 | ppm/$^0$C |
| Output noise (frequency range 100Hz to100kHz) | - | - | 0.4 | mV rms |
| Settling time (settling time within 10% of final value) | - | - | 5 | µs |
| Output current | - | - | 100 | mA |
| Quiescent current (excluding load, load <1mA) | 30 | 40 | 60 | µA |
| Low-power Mode | | | | |
| Quiescent current (excluding load, load <100µA) | 14 | 18 | 23 | µA |

*Table 7: Digital I/O Characteristics*

| Normal Operation | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **Input Voltage** | | | | |
| VIL input logic level low | -0.4 | - | 0.4 | V |
| VIH input logic level high | 0.7 x VDD | - | VDD + 0.4 | V |
| **Output Voltage** | | | | |
| VOL output logic level low, IOL = 4.0 mA | - | - | 0.4 | V |
| VOH output logic level high, IOL = 4.0 mA | 0.75 x VDD | - | - | V |
| **Input and Tristate Currents** | | | | |
| Strong pull-up | -150 | -40 | -10 | µA |
| Strong pull-down | 10 | 40 | 150 | µA |
| Weak pull-up | -5 | -1.0 | -0.33 | µA |
| Weak pull-down | 0.33 | 1.0 | 5.0 | µA |
| CI input capacitance | 1.0 | - | 5.0 | pF |

*Table 8: Current Consumption*

| Normal Operation | Peak (8 dBm) | AVG | Unit |
|---|---|---|---|
| Idle | | 5 | mA |
| USB Suspend | | 200 | µA |
| Inquiry | 73 | 51 | mA |
| File Transfer | 73 | 58 | mA |
| LE Connected (Master) | 74 | | mA |
| LE Scan (Master) | 48 | | mA |

# 7 RF CHARACTERISTICS

*Table 9: Receiver Characteristics*

| **RF Characteristics,** VDD = 3.3V @ room temperature unless otherwise specified | | Min | Typ. | Max | BT. Spec. | Unit |
|---|---|---|---|---|---|---|
| Maximum RF Transmit Power | | | 8 | 10 | 20 | dBm |
| RF power variation over temperature range | | | 1.5 | | - | dB |
| RF power variation over supply voltage range | | | | 0.2 | - | dB |
| RF power variation over BT band | | | 2 | | - | dB |
| RF power control range | | -21 | | 8 | - | dBm |
| 20 dB band width for modulated carrier | | | | | 1000 | kHz |
| ACP | $F = F_0 \pm 2MHz$ | | | | -20 | |
| | $F = F_0 \pm 3MHz$ | | | | -40 | |

| RF Characteristics, VDD = 3.3V @ room temperature unless otherwise specified | Min | Typ. | Max | BT. Spec. | Unit |
|---|---|---|---|---|---|
| F = $F_0$ > 3MHz | | | | -40 | |
| Drift rate | | 10 | | +/-25 | kHz |
| $\Delta F_{1avg}$ | | 165 | | 140<175 | kHz |
| $\Delta F1_{max}$ | | 168 | | 140<175 | kHz |
| $\Delta F_{2avg}$ / $\Delta F_{1avg}$ | | 0.9 | | >=0.8 | |

*Table 10: BDR and EDR receiver sensitivity*

| RF Characteristics, VDD = 3.3V @ room temp. | Packet Type | Min | Typ | Max | BT. Spec. | Unit |
|---|---|---|---|---|---|---|
| Sensitivity for 0.1% BER | DH1 | | -89 | | -70 | dBm |
| | DH3 | | -89 | | | dBm |
| | DH5 | | -89 | | | dBm |
| | 2-DH5 | | -92 | | | dBm |
| | 3-DH5 | | -85 | | | dBm |
| Sensitivity variation over BT band | All | | 2 | | | dB |
| Sensitivity variation over temperature range | All | | TBD | | | dB |

# 8 INTERFACE

## 8.1 PIO

See the Device Terminal Functions section for the list of supplies to the PIOs (Programmable I/O ports).

PIO lines are configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset and have additional individual bus-keeper configuration.

## 8.2 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of WLAN coexistence schemes. There is support for:

- Channel skipping AFH
- Priority signaling
- Channel signaling
- Host passing of channel instructions

The BT800 supports the WLAN coexistence schemes:

- Unity-3
- Unity-3e
- Unity+

For more information see *BT800 WLAN Coexistence Schemes and LED Indication*.

## 8.3 USB Interface

BT800 has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices. The USB interface on the BT800 acts as a USB peripheral, responding to requests from a master host controller.

BT800 supports the Universal Serial Bus Specification (USB v2.0 Specification) and USB Battery Charging Specification, available from http://www.usb.org. For more information on how to integrate the USB interface on BT800, see Figure 19 located in the following section: USB Dongle Design Example Using BT800.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for power supply and data lines, as well as PCB tracks and effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes
- Global suspend
- Selective suspend, includes remote wake
- Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
- Suspend mode current draw
- PIO status in suspend mode
- Resume, detach, and wake PIOs
- Battery charging from USB: dead battery provision, charge currents, charging in suspend modes and USB
- VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

## 8.4 PCM Interface

The audio PCM interface on the BT800 supports:

- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data.
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
- Hardware on the BT800 for sending data to and from a SCO connection.
- Up to three SCO connections on the PCM interface at any one time.
- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
  - Long Frame Sync
  - Short Frame Sync
- GCI timing environments.
- 13-bit or 16-bit linear, 8-bit µ-law, or A-law companded sample formats.
- Receives and transmits on any selection of three of the first four slots following PCM_SYNC.

The PCM configuration options are enabled by setting PSKEY_PCM_CONFIG32.

### 8.4.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, the BT800 generates PCM_CLK and PCM_SYNC.

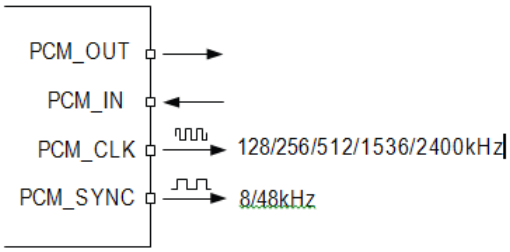



*Figure 2: PCM Interface Master*

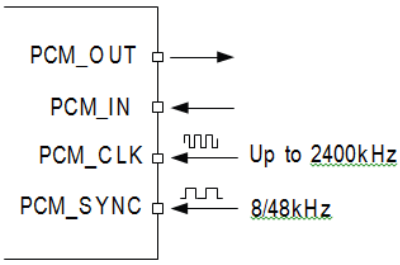



*Figure 3: PCM Interface Slave*

### 8.4.2 Long Frame Sync

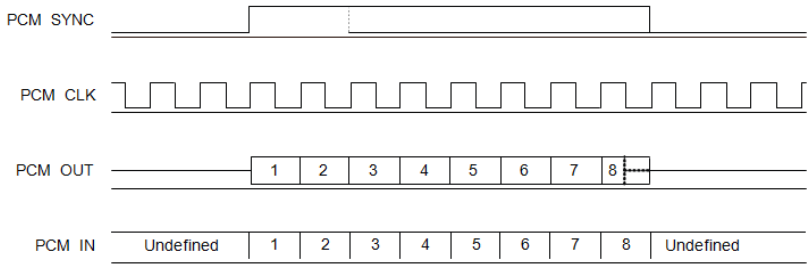



*Figure 4: Long Frame Sync (shown with 8-bit Companded Sample)*

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When the BT800 is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is eight bits long. When the BT800 is configured as PCM Slave, PCM_SYNC is from one cycle PCM_CLK to half the PCM_SYNC rate.

BT800 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

### 8.4.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

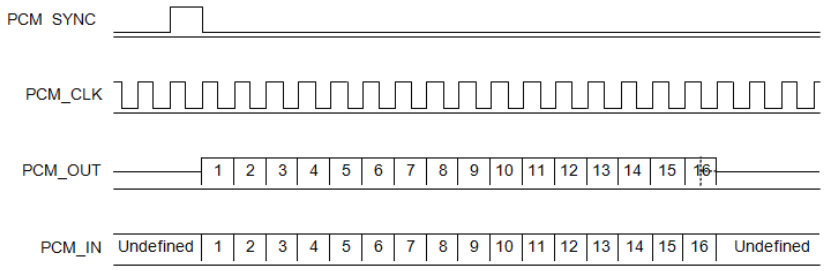



*Figure 5: Short Frame Sync (Shown with 16-bit Sample)*

As with Long Frame Sync, BT800 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

### 8.4.4 Multi-Slot Operation

More than 1 SCO connection over the PCM interface is supported using multiple slots. Up to 3 SCO connections are carried over any of the first 4 slots.

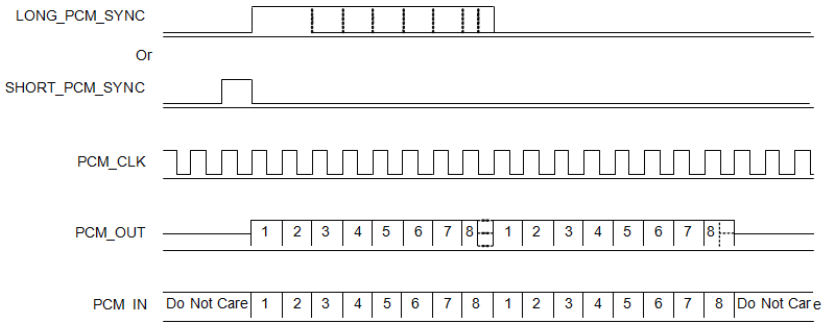



*Figure 6: Multi-slot Operation with 2 Slots and 8-bit Companded Samples*

## 8.5 GCI Interface

BT800 is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The two 64 kbps B channels are accessed when this mode is configured.

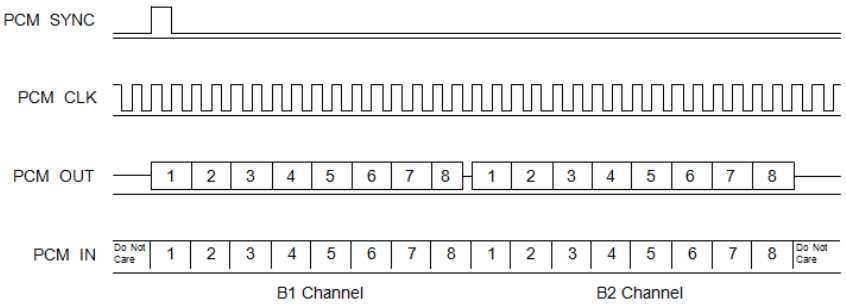



*Figure 7: Multi-slot Operation*

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8 kHz.

## 8.6 Slots and Sample Formats

BT800 receives and transmits on any selection of the first four slots following each sync pulse. Slot durations are either 8 or 16 clock cycles:

- 8 clock cycles for 8-bit sample formats.
- 16 clock cycles for 8-bit, 13-bit, or 16-bit sample formats.

BT800 supports:

- 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats
- A sample rate of 8 ksps
- Little or big endian bit order
- For 16-bit slots, the three or eight unused bits in each slot are filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some codecs.

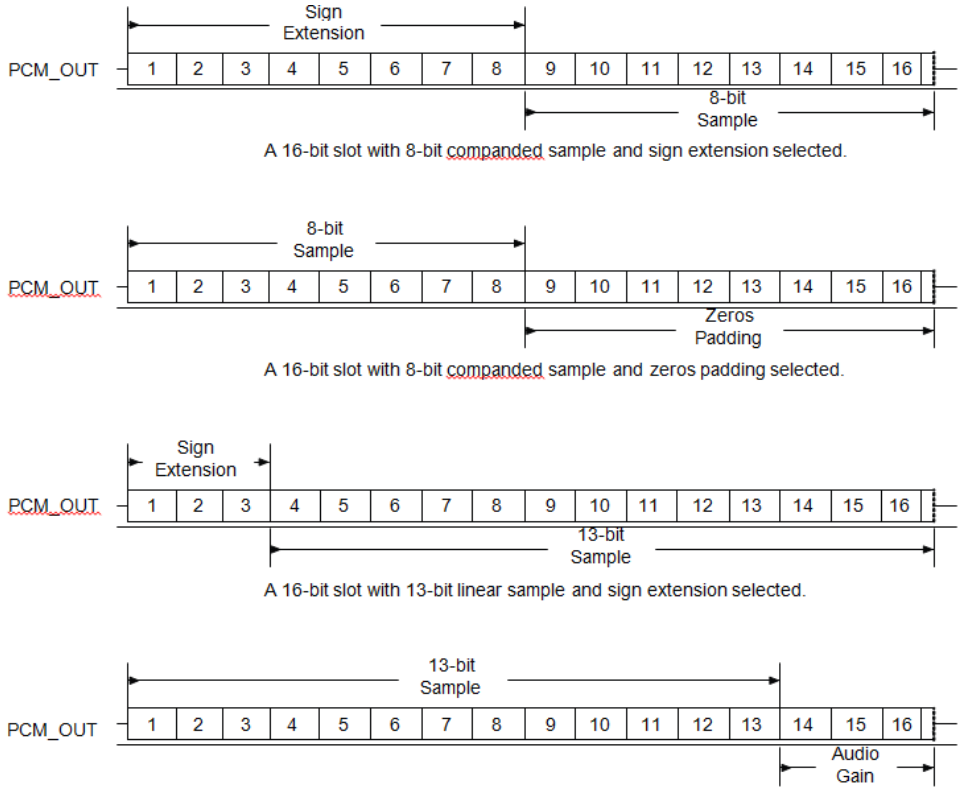



*Figure 8: 16-bit Slot Length and Sample Formats*

## 8.7 PCM Timing Information

*Table 11: PCM Timing information*

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{mclk}$ | PCM_CLK frequency | 4MHz DDS generation. Frequency selection is programmable. | - | 128<br>256<br>512 | - | kHz |
| | | 48MHz DDS generation. Frequency selection is programmable. | 2.9 | - | - | kHz |
| - | PCM_SYNC frequency for SCO connection | | - | 8 | - | kHz |
| $t_{mclkh}$ (a) | PCM_CLK high | 4MHz DDS generation | 980 | - | - | ns |
| $t_{mclkl}$ a) | PCM_CLK low | 4MHz DDS generation | 730 | - | - | ns |
| - | PCM_CLK jitter | 48MHz DDS generation | - | - | 21 | ns pk-pk |
| $t_{dmclksynch}$ | Delay time from PCM_CLK high to PCM_SYNC high | 4MHz DDS generation | - | - | 20 | ns |
| | | 48MHz DDS generation | - | - | 40.83 | ns |
| $t_{dmclkpout}$ | Delay time from PCM_CLK high to valid PCM_OUT | | - | - | 20 | ns |
| $t_{dmclklsyncl}$ | Delay time from PCM_CLK low to PCM_SYNC low (long frame sync only) | 4MHz DDS generation | - | - | 20 | ns |
| | | 48MHz DDS generation | - | - | 40.83 | ns |

(a) Assumes normal system clock operation. Figures vary during low-power modes, when system clock speeds are reduced.

*Table 12: PCM Master Mode Timing Parameters*

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{dmclkhsyncl}$ | Delay time from PCM_CLK high to PCM_SYNC low | 4MHz DDS generation | - | - | 20 | ns |
| | | 48MHz DDS generation | - | - | 40.83 | ns |
| $t_{dmclklpoutz}$ | Delay time from PCM_CLK low to PCM_OUT high impedance | | - | - | 20 | ns |
| $t_{dmclkhpoutz}$ | Delay time from PCM_CLK high to PCM_OUT high impedance | | - | - | 20 | ns |
| $t_{supinclkl}$ | Set-up time for PCM_IN valid to PCM_CLK low | | 20 | - | - | ns |
| $t_{hpinclkl}$ | Hold time for PCM_CLK low to PCM_IN invalid | | 0 | - | - | ns |

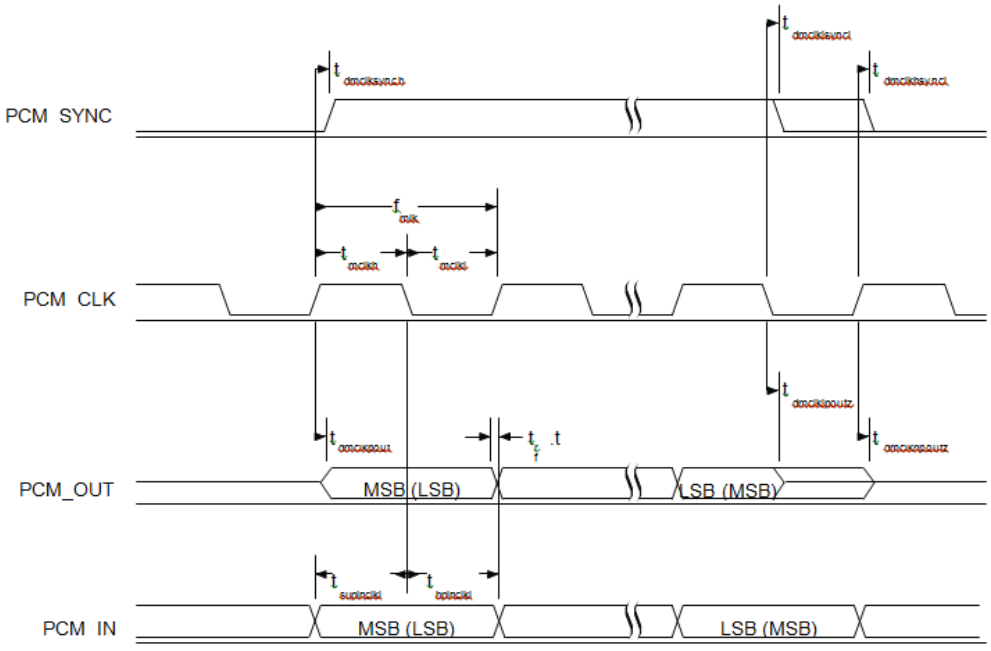



*Figure 9: PCM Master Timing Long Frame Sync*

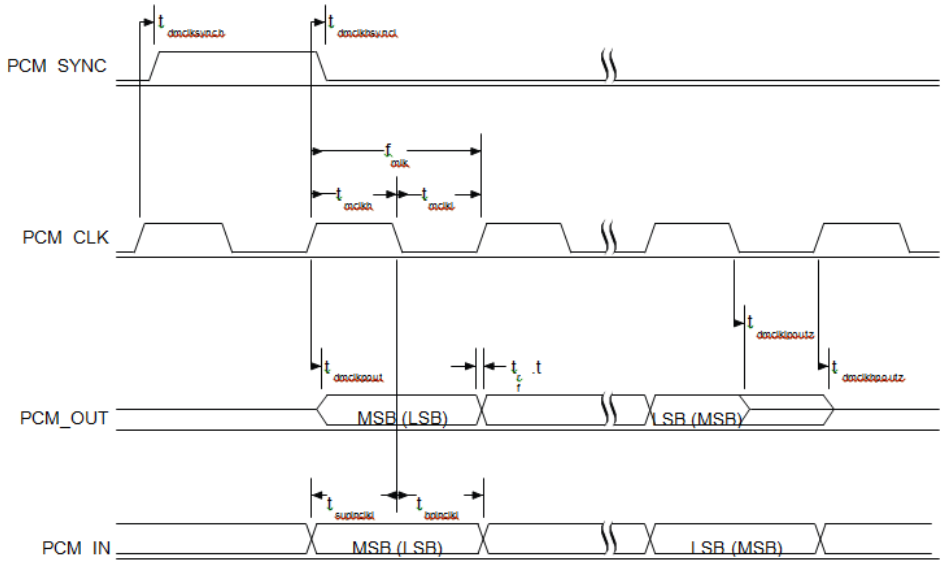



*Figure 10: PCM Master Timing Short Frame Sync*

## 8.8 PCM Slave Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{sclk}$ | PCM clock frequency (Slave mode: input) | 64 | - | 2048 | kHz |
| $f_{sclk}$ | PCM clock frequency (GCI mode) | 128 | - | 4096 | kHz |

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{sclkl}$ | PCM_CLK low time | 200 | - | - | ns |
| $t_{sclkh}$ | PCM_CLK high time | 200 | - | - | ns |

## 8.9 PCM Slave Mode Timing Parameters

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{hsclksynch}$ | Hold time from PCM_CLK low to PCM_SYNC high | 2 | - | - | ns |
| $t_{susclksynch}$ | Set-up time for PCM_SYNC high to PCM_CLK low | 20 | - | - | ns |
| $t_{dpout}$ | Delay time from PCM_SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (long frame sync only) | - | - | 15 | ns |
| $t_{dsclkhpout}$ | Delay time from CLK high to PCM_OUT valid data | - | - | 15 | ns |
| $t_{dpoutz}$ | Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance | - | - | 20 | ns |
| $t_{supinsclkl}$ | Set-up time for PCM_IN valid to CLK low | 20 | - | - | ns |
| $t_{hpinsclkl}$ | Hold time for PCM_CLK low to PCM_IN invalid | 2 | - | - | ns |

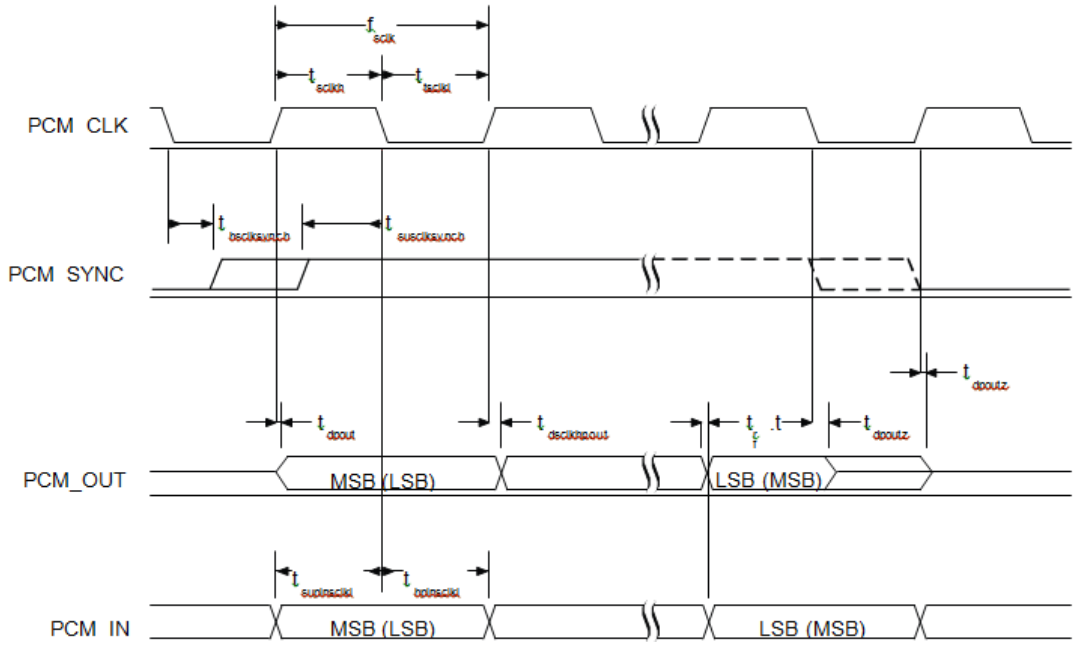



*Figure 11: PCM Slave Timing Long Frame Sync*

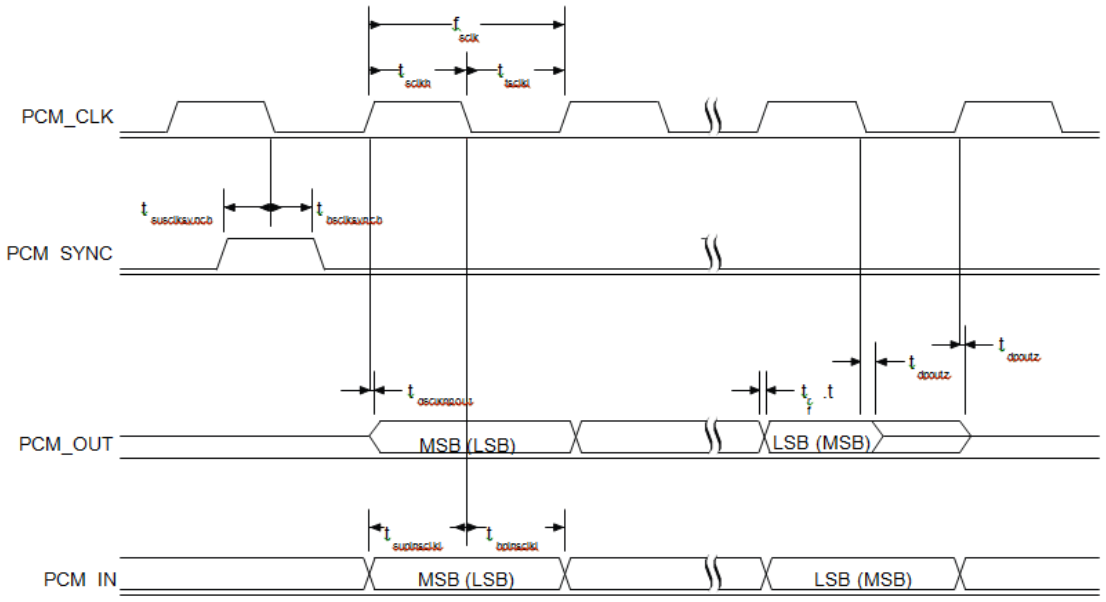



*Figure 12: PCM Slave Timing Short Frame Sync*

## 8.10 PCM_CLK and PCM_SYNC Generation

BT800 has two methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from BT800internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512 kHz and PCM_SYNC to 8 kHz.
- Generating these signals by DDS from an internal 48MHz clock, which enables a greater range of frequencies to be generated with low jitter but consumes more power. To select this second method set bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC is either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 8.1 describes PCM_CLK frequency when generated from the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

*Equation 8.1: PCM_CLK Frequency Generated Using the Internal 48MHz Clock*

Set the frequency of PCM_SYNC relative to PCM_CLK using Equation 8.2:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

*Equation 8.2: PCM_SYNC Frequency Relative to PCM_CLK*

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set SKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

## 8.11 PCM Configuration

Configure the PCM by using PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG (See your PSKey file). The default for PSKEY_PCM_CONFIG32 is 0x00800000 (for example: first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT).

## 8.12 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 13 lists these alternative functions. Figure 11 shows the timing diagram.

*Table 13: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface.*

| PCM Interface | I²S Interface |
|---|---|
| PCM_OUT | SD_OUT |
| PCM_IN | SD_IN |
| PCM_SYNC | WS |
| PCM_CLK | SCK |

Configure the digital audio interface using PSKEY_DIGITAL_AUDIO_CONFIG, see BlueCore Audio API Specification and the PS Key file.

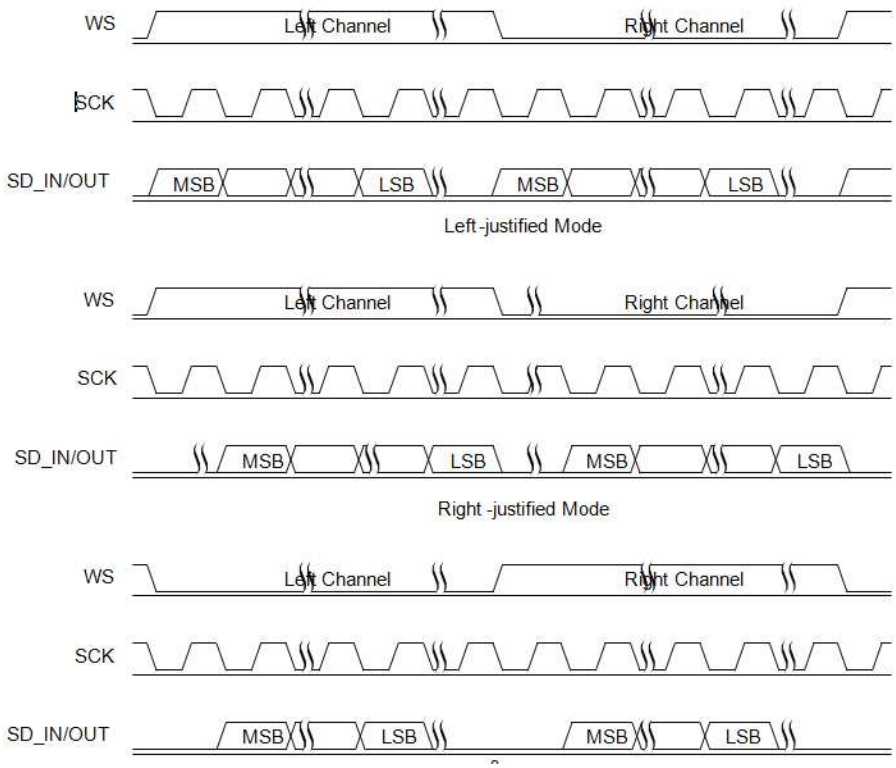



*Figure 13: PCM Configuration*

The internal representation of audio samples within BT800is 16-bit and data on SD_OUT is limited to 16-bit per channel.

*Table 14: Digital Audio Interface Slave Timing*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| - | SCK Frequency | - | - | 6.2 | MHz |
| - | WS Frequency | - | - | 96 | kHz |
| $t_{ch}$ | SCK high time | 80 | - | - | ns |
| $t_{cl}$ | SCK low time | 80 | - | - | ns |

*Table 15: I²S Slave Mode Timing*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{ssu}$ | WS valid to SCK high set-up time | 20 | - | - | ns |
| $t_{sh}$ | SCK high to WS invalid hold time | 2.5 | - | - | ns |
| $t_{opd}$ | SCK low to SD_OUT valid delay time | - | - | 20 | ns |
| $t_{isu}$ | SD_IN valid to SCK high set-up time | 20 | - | - | ns |
| $t_{ih}$ | SCK high to SD_IN invalid hold time | 2.5 | - | - | ns |

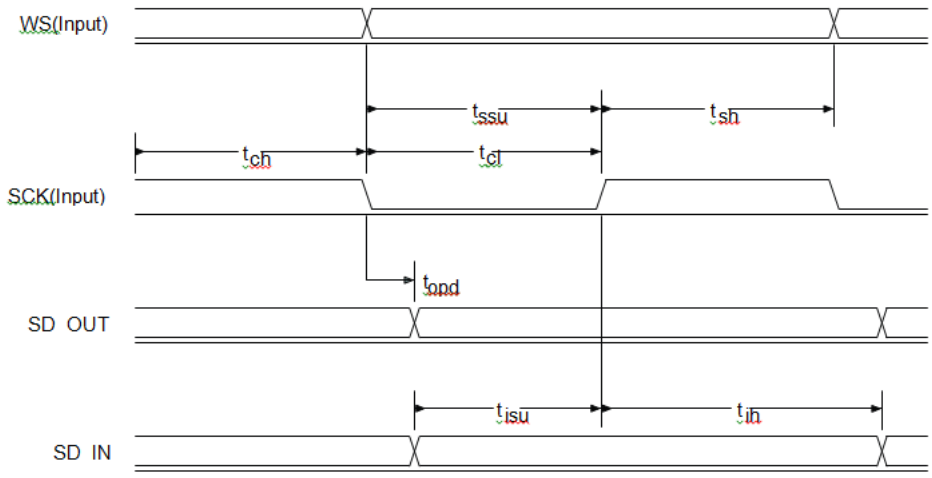



*Figure 14: Digital Audio Interface Slave Timing*

*Table 16: Digital Audio Interface Master Timing*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| - | SCK Frequency | - | - | 6.2 | MHz |
| - | WS Frequency | - | - | 96 | kHz |

*Table 17: I²S Master Mode Timing Parameters, WS and SCK as Outputs*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{spd}$ | SCK low to WS valid delay time | - | - | 39.27 | ns |

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{opd}$ | SCK low to SD_OUT valid delay time | - | - | 18.44 | ns |
| $t_{isu}$ | SD_IN valid to SCK high set-up time | 18.44 | - | - | ns |
| $t_{ih}$ | SCK high to SD_IN invalid hold time | 0 | - | - | ns |

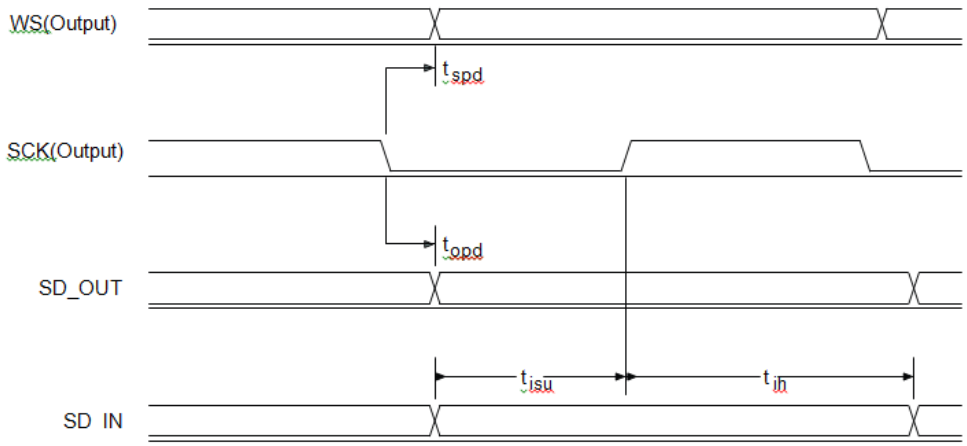



*Figure 15: Digital Audio Interface Master Timing*

# 9 Power Control and Regulation

See the Example Application Schematic (Figure 19) for the regulator configuration. BT800 contains three regulators:

- USB linear regulator, to generate the 3.3 V from the USB bus power and the input to the high-voltage linear regulator.
- High-voltage linear regulator, to generate the main 1.8 V from the USB linear regulator or an external 3.3 V.

  This regulator then feeds the three low-voltage regulators:
  - Low-voltage VDD_DIG linear regulator, a programmable low-voltage regulator to supply a 0.90 V to1.25 V digital supply, VDD_DIG.
  - Low-voltage VDD_ANA linear regulator, to supply the radio supply, VDD_RADIO.
  - Low-voltage VDD_AUX linear regulator, to supply the auxiliary supply, VDD_AUX.

## 9.1 USB Linear Regulator

The integrated USB LDO linear regulator is available as a 3.3 V supply rail and is intended to supply the USB interface and the high-voltage linear regulator. The input voltage range is between 4.25 V and 5.75 V. The maximum current from this regulator is 150 mA, of which 50 mA is available for external use (for example EEPROM/LED). Internally decouple the output of this regulator using a low ESR MLC capacitor to the VREG_IN_HV pin. No externally decouple capacitor is required. For hassle environment, an output capacitor of 1µF to 4.7µF (±20%) is preferred.

This regulator is enabled by default. If the USB linear regulator is not required, leave its input (VREG_IN_USB) unconnected.

## 9.2 High-voltage Linear Regulator

The integrated high-voltage linear regulator is available to power the main 1.8 V supply rail. The input voltage range is between 2.3 V and 4.8 V. The maximum current from this regulator is 100 mA. Internally decouple the output of this regulator using a low ESR MLC capacitor of a 2.2 µF to the VREG_OUT_HV pin. No externally decouple capacitor is required. For hassle environment, an output capacitor of 1 µF to 4.7 µF (±20%) is preferred. Take VREG_EN_RST# high to enable this regulator. If this regulator is not required, then leave VREG_IN_HV unconnected or tied to VREG_OUT_HV.

## 9.3 Voltage Regulator Enable and Reset

A single pin, VREG_EN_RST#, controls both the regulator enables and the digital reset function. All the regulators are enabled, except the USB linear regulator, by taking the VREG_EN_RST# pin above 1 volt. Software also controls the regulators. The VREG_EN_RST# pin is connected internally to the reset function and is powered from VDD_HOST, so do not apply voltages above VDD_HOST to the VREG_EN_RST# pin. The REG_EN_RST# pin is pulled down internally before the software starts. The VREG_EN_RST# pin is an active low reset. Assert the reset signal for a period >5 ms to ensure a full reset.

---

**Note:** The regulator enables are released as soon as VREG_EN_RST# is low, so the regulators shut down. Therefore do not take VREG_EN_RST# low for less than 5 ms, as a full reset is not guaranteed.

Other reset sources are:

Power-on reset
Via a software-configured watchdog timer

A warm reset function is also available under software control. After a warm reset the RAM data remains available.

---

## 9.4 Power Sequencing

CSR recommends that all power supplies are powered at the same time. The order of powering the supplies relative to the I/O supply, VDD_PADS to VDD_HOST, is not important. If the I/O supply is powered before VDD_DIG, all digital I/Os are weak pull-downs regardless of the reset state.

# 10 ANTENNA PERFORMANCE ON BT800

Figure 16 illustrates antenna performance.

Gain Table

| Unit in dBi @2.44GHz | XY-plane | | XZ-plane | | YZ-plane | | Efficiency |
|---|---|---|---|---|---|---|---|
| | Peak | Avg. | Peak | Avg. | Peak | Avg. | |
| A1 | -3.5 | -4.2 | 3.8 | -5.3 | 3.2 | -4.7 | 41.0% |

*Figure 16: BT800 Gain Table*

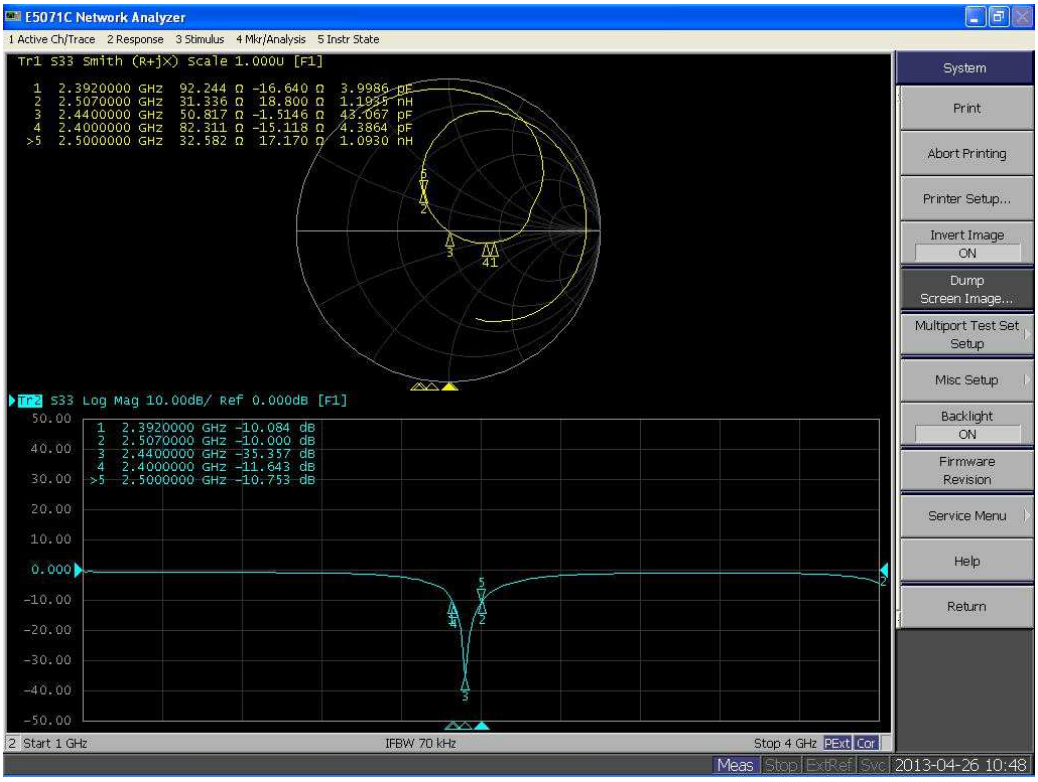
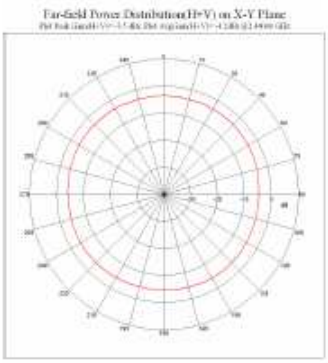



*Figure 17: Network Analyzer output*

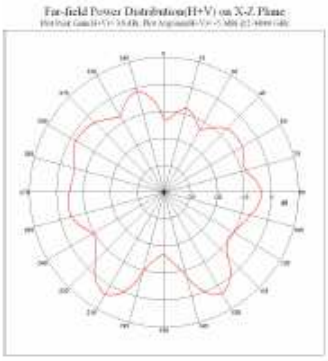
◆XY-plane



Unit : dBi

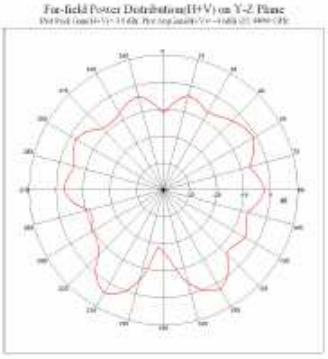
| | Peak gain | Avg. gain |
|---|---|---|
| XY-plane | -3.5 | -4.2 |

◆XZ-plane



| | Peak gain | Avg. gain |
|---|---|---|
| XZ-plane | 3.8 | -5.3 |

◆YZ-plane



| | Peak gain | Avg. gain |
|---|---|---|
| YZ-plane | 3.2 | -4.7 |