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Datasheet

BT830 Bluetooth v4.0 Dual-Mode UART HCI Module

Version 1.7

BT830 - SA

BT830 - ST

REVISION HISTORY

Revision	Date	Changes	Approved By
1.0	23 July 2014	Initial Version	Jonathan Kaye
1.1	10 Nov 2014	Updated pin definitions	Jonathan Kaye
1.2	10 Aug 2015	Added Tape/Reel information	Jonathan Kaye
1.3	30 Sept 2015	Added additional antenna information	Andrew Chen
1.4	15 Dec 2015	Replaced tray image with new one	Maggie Teng
1.5	17 Aug 2016	Changed *Hardware Integration Guide* to *Datasheet*.	Sue White
1.6	31 Aug 2016	Updated Declaration of Conformity	Tom Smith
1.7	16 May 2016	Updated Declaration of Conformity for RED standards	Tom Smith

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CONTENTS

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1 Scope

This document describes key hardware aspects of the Laird BT830 Bluetooth HCI modules. This document is intended to assist device manufacturers and related parties, with the integration of this module into their host devices. Data in this document are drawn from a number of sources including data sheets for the CSR8811. Because the BT830 is currently in development stage, this document is preliminary and the information in this document is subject to change. Visit www.lairdtech.com to obtain the most recent version of this document.

2 Operational Description

The BT830 series of UART HCI devices are designed to meet the needs of OEMs adding robust Bluetooth connectivity and using embedded Bluetooth stacks within their products.

BT830-SA module

Leveraging the market-leading CSR8811 chipset, the BT830 series provides exceptionally low power consumption with outstanding range. Supporting the latest Bluetooth v4.0 specification with EDR (Enhanced Data Rate), the Laird BT830 series enables OEMs to accelerate their development time for leveraging either Classic Bluetooth or Bluetooth Low Energy (BLE) into their operating system-based devices.

BT830 –ST module

With a footprint as small as 8.5 x 13 mm, yet output power at 7 dBm, these modules are ideal for applications where designers need high performance in minimal size. For maximum flexibility in systems integration, the modules are designed to support a UART interface plus GPIO and additionally I2S and PCM audio interfaces.

These modules present an HCI interface and have native support for Windows and Linux Bluetooth software stacks. All BT830 series devices are fully qualified as Bluetooth Hardware Controller Subsystem products. This allows designers to integrate their existing pre-approved Bluetooth host and profile subsystem stacks to gain a Bluetooth END product approval for their products.

The BT830 series is engineered to provide excellent RF performance with integrated antenna and additional band pass filters. It further reduces regulatory and testing requirements for OEMs and ensures a hassle free development cycle.

A fully featured, low-cost developer's kit is available for prototyping, debug, and integration testing of the BT830 series modules and further reduces risk and time in development cycles.

BT830-SA	BTv4.0 Dual Mode UART HCI Module (Integrated Antenna)
BT830-ST	BTv4.0 Dual Mode UART HCI Module (SMT Pad for External Antenna)

2.1 Features and Bene

- Bluetooth v4.0 - dual mode (Classic Bluetooth and BLE)
- Compact footprint
- 3-wire Wi-Fi coexistence scheme
- High antenna radiation gain and efficiency
- Good interference rejection for multi-com system (GSM/WCDMA)
- Class 1 output – 7 dBm
- UART, GPIO, I2S, and PCM
- Industrial temperature range
- Bluetooth hardware controller subsystem
- FCC, IC, and CE approvals
- Host Wake up

2.2 Application Areas

- Medical devices
- ePOS terminals
- Barcode scanners
- Industrial cable replacement
- M2M connectivity
- Automotive Diagnostic Equipment
- Personal Digital Assistants (PDA)
- Bluetooth HID device (keyboard, mouse, and joystick)

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3 Block Diagram and Descriptions

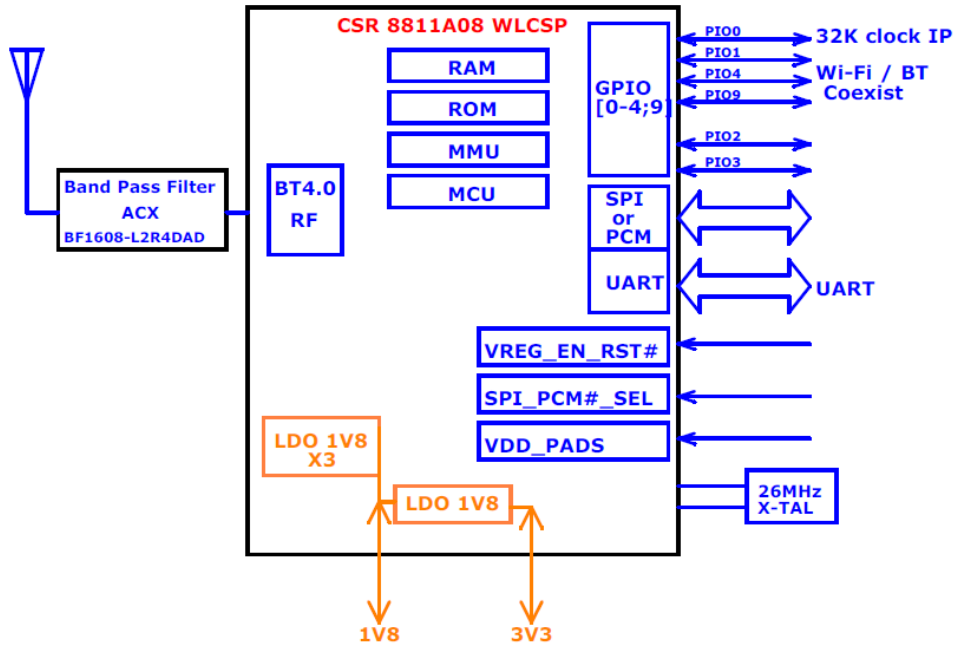

Figure 2: BT830 module block diagram

CS8811A08 (Main chip)

The BT830 is based on the CSR8811A08 dual mode chip. The chip is a single-chip radio with on-chip LDO regulators and baseband IC for Bluetooth 2.4 GHz systems including EDR to 3 Mbps.

Dedicated signal and baseband processing is included for full Bluetooth operation. The chip provides PCM/I2S and UART interfaces. Up to four general purpose I/Os are available for general use such as Wi-Fi coexistence or general indicators.

Note: The purpose of the SPI interface is to access the module's inner settings such as selecting different WLAN CO-EXIST scheme. The SPI interface can also be used to place the module in RF test mode. You cannot use the module over the SPI interface for normal operation as the main host interface.

Antenna Options	BT830-SA – The antenna is a ceramic monopole chip antenna. BT830-ST – Provides a SMT pad for connecting an external antenna.
Band Pass Filter	The band pass filter filters the out-of-band emissions from the transmitter to meet the specific regulations for type approvals of various countries.
Crystal	The embedded 26 MHz crystal is used for generating the clock for the entire module.

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4 SPECIFICATIONS

Table 1: BT830 specifications

Categories	Feature	Implementation
Wireless Specification	Bluetooth®	V4.0 Dual Mode
	Frequency	2.402 - 2.480 GHz
	Maximum Transmit Power	Class 1 +7 dBm from antenna
	Receive Sensitivity	-89 dBm
	Range	Circa 100 meters
	Data Rates	Up to 3 Mbps (over the air)
Host Interface	UART	RX, TX, CTS, RTS
	GPIO	Six configurable lines (1.8V/3.3V configurable by VDD_PADS)
Operational Modes	HCI	Host Controller Interface over UART
Coexistence	802.11 (Wi-Fi)	3 wire CSR schemes supported (Unity-3 and Unity-3e)
Supply Voltage	Supply	3.3V +/-10% **Note:** See *Implementation Note* for details on different DC power selections on the BT830.
Power Consumption	Current	Idle Mode ~4.3 mA (Master; ACL link; No traffic) File Transfer ~7.1 mA (Master; ACL link; Transmit)
Antenna Option	Internal (BT830-SA) External (BT830-ST)	Multilayer ceramic antenna with up to 40% efficiency. SMT pad for external antenna
Physical	Dimensions	8.5 x 13 x 1.6 mm (BT830 - module)
Environmental	Operating	-30°C to +85°C
	Storage	-40°C to +85°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	1-Year Warranty
Approvals	Bluetooth®	Hardware Controller Subsystem Approved
	FCC / IC / CE	All BT830 series (BT830-SA; BT830-ST)

5 Pin Definitions

Table 2: BT830 pin definitions

#	Pin Name	I/O	Supply Domain	Description	If Unused…
1	VDD_PADS	DC voltage input	(1.75V-3.6V)	Positive DC supply for configuring digital I/O level.	N/A
2	GND	GND	-	Ground	GND
3	PIO2	Bidirectional, tri-state, with weak internal pull-down	VDD_PADS	Programmable input/output line	NC
4	UART_RTS	Bidirectional, tri-state, with weak internal pull-up	VDD_PADS	UART request to send, active low	NC
5	UART_TX	Bidirectional, tri-state, with weak internal pull-up	VDD_PADS	UART data output, active high	NC
6	UART_CTS	Bidirectional, tri-state, with weak internal pull-up	VDD_PADS	UART clear to send, active low	NC
7	UART_RX	Bidirectional, tri-state, with weak internal pull-up	VDD_PADS	UART data input, active high	NC
8	VREG_EN_RST#	Input with strong internal pull-down	VDD_PADS	Take high to enable internal regulators. Also acts as active low reset. Maximum voltage is VDD_PADS.	N/A
9	VREG_IN_HV	Analogue regulator input	3.3V	Module main DC power supply; Input to internal high-voltage regulator	N/A
10	VREG_OUT_HV	Analogue regulator input/output	1.8V	Output from internal high-voltage regulator and input to low-voltage internal regulators.	N/C
11	GND	GND	-	Ground	GND
12	GND	GND	-	Ground	GND
13	GND	GND	-	Ground	GND
14	GND	GND	-	Ground	GND
15	GND	GND	-	Ground	GND
16	GND	GND	-	Ground	GND
17	RF			BT830-ST – RF signal out (50 ohm) BT830-SA – No connection	

#	Pin Name	I/O	Supply Domain	Description	If Unused…
18	GND	GND	-	Ground	GND
19	PCM_SYNC/ SPI_CS#/ PIO23	Bidirectional, tri-state, with weak internal pull-down	VDD_PADS	PCM synchronous data sync SPI chip select, active low programmable input/output line *See Note 1.	NC
20	PCM_CLK/ SPI_CLK/ PIO24	Bidirectional, tri-state, with weak internal pull-down	VDD_PADS	PCM synchronous data clock SPI clock Programmable input/output line *See Note 1.	NC
21	PCM_IN/ SPI_MOSI/ PIO21	Input, tri-state, with weak internal pull-down	VDD_PADS	PCM synchronous data input SPI data input Programmable input/output line *See Note 1.	NC
22	PCM_OUT/ SPI_MISO/ PIO22	Output, tri-state, with weak internal pull-down	VDD_PADS	PCM synchronous data output SPI data output Programmable input/output line *See Note 1.	NC
23	GND	GND	-	Ground	GND
24	PIO0/ 32K_CLK_IN	Bidirectional, tri-state, with weak internal pull-down	VDD_PADS	Programmable input/output line and 32kHz sleep clock input	NC
25	PIO1/ BT_ACTIVE	Bidirectional, tri-state, with weak internal pull-down	VDD_PADS	Programmable input/output line; Wi-Fi and BT 3-wire coexistance	NC
26	PIO9/ BT_PRIORITY	Bidirectional, tri-state, with weak internal pull-down	VDD_PADS	Programmable input/output line; Wi-Fi and BT 3-wire coexistance	NC
27	PIO4/ WLAN_ACTIVE	Bidirectional, tri-state, with weak internal pull-down	VDD_PADS	Programmable input/output line; Wi-Fi and BT 3-wire coexistance	NC
28	SPI_PCM#_SEL	Input with weak internal pull-down	VDD_PADS	Control line to select SPI or PCM interface, high = SPI, low = PCM *See Note 1.	NC
29	PIO3/ Host Wake up	Bidirectional, tri-state, with weak internal pull-down	VDD_PADS	Programmable input/output line; Host wake up from BT, active High.	NC
30	GND	GND	-	Ground	GND

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Note 1: The purpose of the SPI interface is to access the module's inner settings such as selecting different WLAN CO-EXIST scheme. The SPI interface can also be used to put the module in RF test mode. You cannot use the module over the SPI interface for normal operation as the main host interface.

6 DC Electrical Characteristic

Table 3: Absolute maximum ratings

Rating	Min	Max	Unit
Storage temperature	-40	+85	^{0}C
VREG_IN_HV	2.3	4.8	V
VREG_OUT_HV	1.7	2.0	V
VDD_PADS	-0.4	3.6	V
Other terminal voltages	-0.4	VDD_PADS + 0.4 V	V

Table 4: Recommended operating conditions

Rating	Min	Max	Unit
Operating temperature	-30	+85	^{0}C
VREG_IN_HV	3.0	3.6	V
VREG_OUT_HV	1.75	1.95	V
VDD_PADS	1.75	3.6	V
VREG_EN_RST#	VDD_PADS	VDD_PADS	V

Table 5: High-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage (VREG_IN_HV)	3.0	3.3	3.6	V
Output voltage (VREG_OUT_HV)	1.75	1.85	1.95	V
Temperature coefficient	-200	-	200	ppm/^{0}C
Output noise (frequency range 100Hz to100kHz)	-	-	0.4	mV rms
Settling time (settling time within 10% of final value)	-	-	5	µs
Output current	-	-	100	mA

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Table 6: Digital I/O Characteristics

Normal Operation	Min	Typ	Max	Unit
Input Voltage				
VIL input logic level low	-0.4	-	0.4	V
VIH input logic level high	0.7 x VDD_PADS	-	VDD_PADS + 0.4	V
Output Voltage				
VOL output logic level low, IOL = 4.0 mA	-	-	0.4	V
VOH output logic level high, IOL = 4.0 mA	0.75 x VDD_PADS	-	-	V
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	µA
Strong pull-down	10	40	150	µA
Weak pull-up	-5	-1.0	-0.33	µA
Weak pull-down	0.33	1.0	5.0	µA
CI input capacitance	1.0	-	5.0	pF

Table 7: Current Consumption

Normal Operation		**Avg.**	**Unit**
Idle		5	mA
Inquiry		891	µA
File Transfer (ACL)	Transmit (Master)	7.1	mA
	Receive (Slave)	11.5	mA
LE Connected (Master)		292	µA
LE Scan (Master)		448	µA

Current consumption values are taken with:

- VREG_IN_HV pin = 3.15V
- RF TX power set to 0dBm
- XTAL used with PSKEY_LP_XTAL_LVL = 8
- LEDs disconnected

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7 RF CHARACTERISTICS

Table 8: RF Characteristics

RF Characteristics, VREG_IN_HV/VDD_PADS = 3.3V @ room temperature unless otherwise specified		Min	Typ.	Max	BT. Spec.	Unit
Maximum RF Transmit Power			7	8	20	dBm
RF power variation over temperature range			1.5		-	dB
RF power variation over supply voltage range				0.2	-	dB
RF power variation over BT band			3		-	dB
RF power control range		-21		8	-	dBm
20 dB band width for modulated carrier					1000	kHz
ACP	$F = F_0 \pm 2MHz$				-20	
	$F = F_0 \pm 3MHz$				-40	
	$F = F_0 > 3MHz$				-40	
Drift rate			5		≤20	kHz
ΔF_{1avg}			165		140<175	kHz
$\Delta F1_{max}$			168		140<175	kHz
ΔF_{2avg} / ΔF_{1avg}			0.9		>=0.8	

Table 9: BDR and EDR receiver sensitivity

RF Characteristics, VREG_IN_HV/VDD_PADS = 3.3V @ room temp.	Packet Type	Min	Typ	Max	BT. Spec.	Unit
Sensitivity for 0.1% BER	DH1		-87		-70	dBm
	DH3		-87			dBm
	DH5		-87			dBm
	2-DH5		-91			dBm
	3-DH5		-85			dBm
Sensitivity variation over BT band	All		3			dB
Sensitivity variation over temperature range	All		TBD			dB

8 INTERFACE

8.1 PIO

PIO lines are configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset and have additional individual bus-keeper configuration.

8.2 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of WLAN coexistence schemes. The following are supported:

- Channel skipping AFH
- Priority signaling

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- Channel signaling
- Host passing of channel instructions

The BT830 supports the following WLAN coexistence schemes:

- Unity-3
- Unity-3e

More information is available in the BT830 Configuration File application note, available on the documentation tab of the BT830 Product Page at Lairdtech.com.

8.3 UART Interface

This is a standard UART interface for communicating with other serial devices. The CSR8811 UART interface provides a simple mechanism for communicating with other serial devices using the RS-232 protocol.

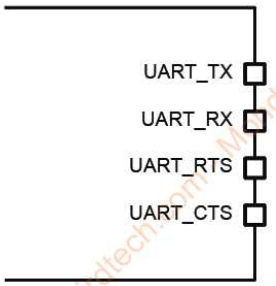

Figure 1: Signals that implement the UART function

The above figure shows the four signals that implement the UART function. When BT830 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, implement RS232 hardware flow control where both are active low indicators. The default configuration of UART is 115200 bauds; None parity check; 1 stop bit; 8 bits per byte.

Note: With a standard PC, an accelerated serial port adapter card is required to communicate with the UART at its maximum data rate.

8.4 PCM Interface

The audio PCM interface on the BT830 supports the following:

- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data.
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
- Hardware on the BT830 for sending data to and from a SCO connection.
- Up to three SCO connections on the PCM interface at any one time.
- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
  - Long Frame Sync
  - Short Frame Sync
- GCI timing environments.

- 13-bit or 16-bit linear, 8-bit µ-law, or A-law companded sample formats.
- Receives and transmits on any selection of three of the first four slots following PCM_SYNC.

The PCM configuration options are enabled by setting PSKEY_PCM_CONFIG32.

8.4.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, the BT830 generates PCM_CLK and PCM_SYNC.

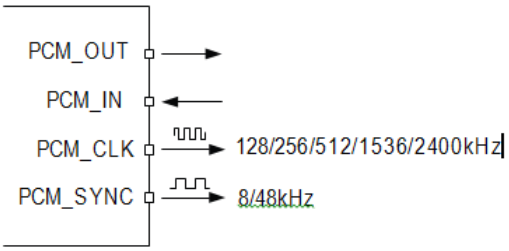

Figure 2: PCM Interface Master

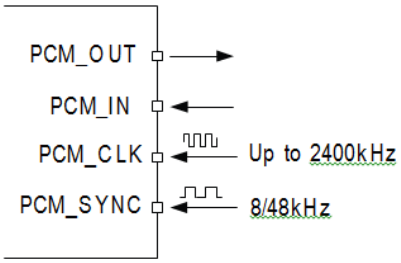

Figure 3: PCM Interface Slave

8.4.2 Long Frame Sync

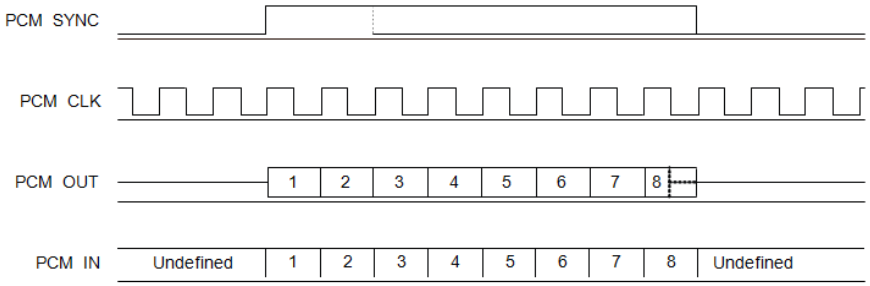

Figure 4: Long Frame Sync (shown with 8-bit Companded Sample)

Long Frame Sync indicates a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When the BT830 is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is eight bits long. When the BT830 is configured as PCM Slave, PCM_SYNC is from one cycle PCM_CLK to half the PCM_SYNC rate.

BT830 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

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8.4.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

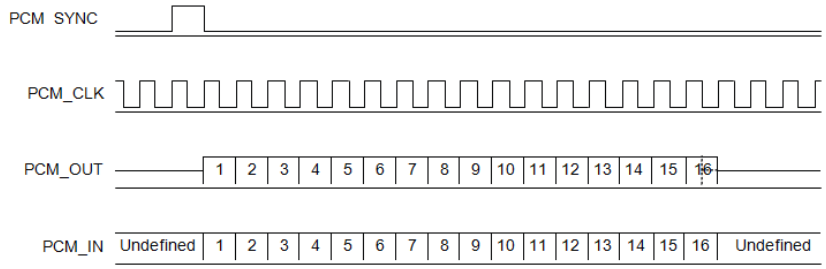

Figure 5: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BT830 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

8.4.4 Multi-Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections are carried over any of the first four slots.

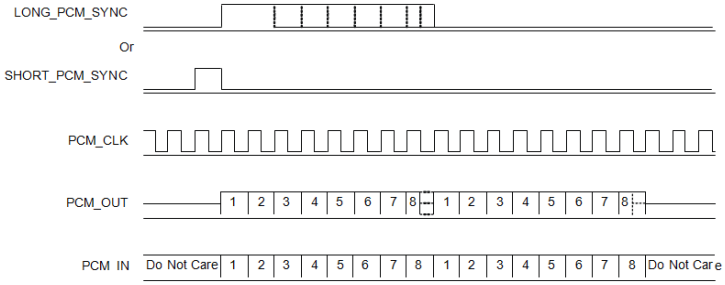

Figure 6: Multi-slot operation with 2 Slots and 8-bit companded samples

8.5 GCI Interface

BT830 is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The two 64 kbps B channels are accessed when this mode is configured.

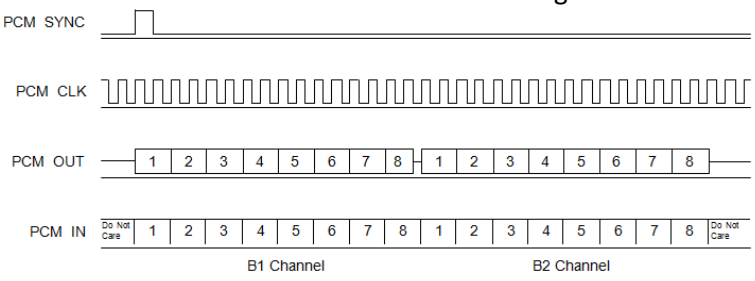

Figure 7: Multi-slot operation

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8 kHz.

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8.6 Slots and Sample Formats

BT830 receives and transmits on any selection of the first four slots following each sync pulse. Slot durations are either 8 or 16 clock cycles:

- 8 clock cycles for 8-bit sample formats
- 16 clock cycles for 8-bit, 13-bit, or 16-bit sample formats

BT830 supports:

- 13-bit linear, 16-bit linear, and 8-bit µ-law or A-law sample formats
- A sample rate of 8 ksps
- Little or big endian bit order
- For 16-bit slots, the three or eight unused bits in each slot are filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some codecs.

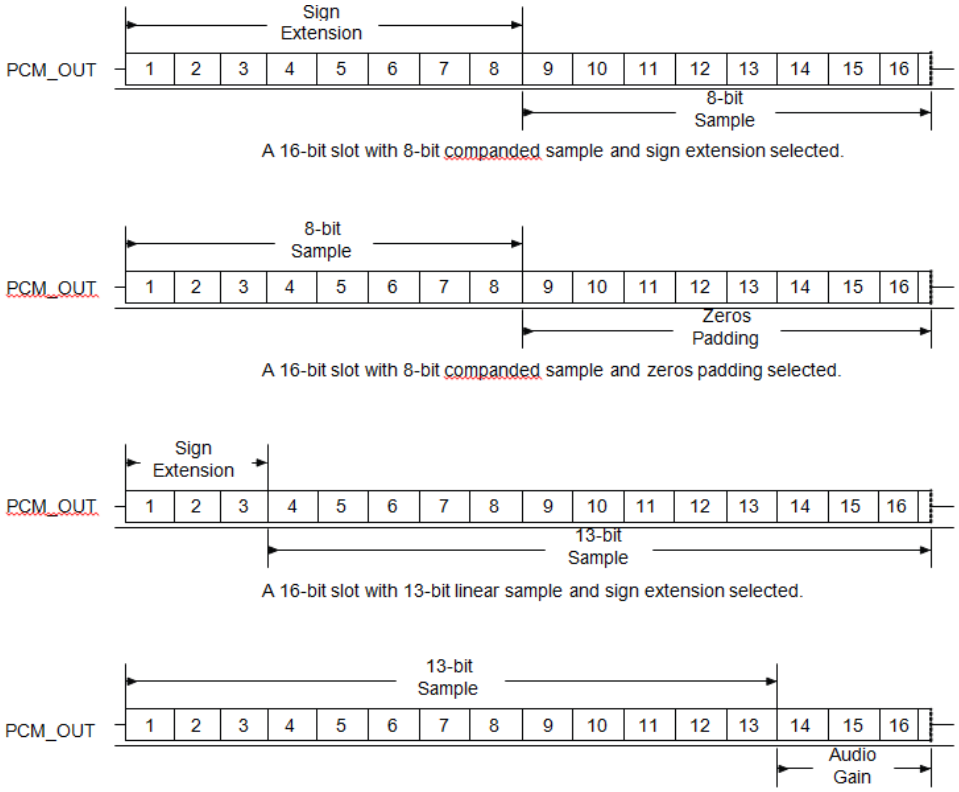

Figure 8: 16-bit slot Length and sample formats

8.7 PCM Timing Information

Table 10: PCM Timing information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Frequency selection is programmable.	-	128	-	kHz
				256		
				512		
		48MHz DDS generation. Frequency selection is programmable.	2.9	-	-	kHz

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Symbol	Parameter		Min	Typ	Max	Unit
-	PCM_SYNC frequency for SCO connection		-	8	-	kHz
t_{mclkh} (a)	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} a)	PCM_CLK low	4MHz DDS generation	730	-	-	ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high	4MHz DDS generation	-	-	20	ns
		48MHz DDS generation	-	-	40.83	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (long frame sync only)	4MHz DDS generation	-	-	20	ns
		48MHz DDS generation	-	-	40.83	ns

(a) Assumes normal system clock operation. Figures vary during low-power modes, when system clock speeds are reduced.

Table 11: PCM Master Mode Timing Parameters

Symbol	Parameter		Min	Typ	Max	Unit
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low	4MHz DDS generation	-	-	20	ns
		48MHz DDS generation	-	-	40.83	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		20	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		0	-	-	ns

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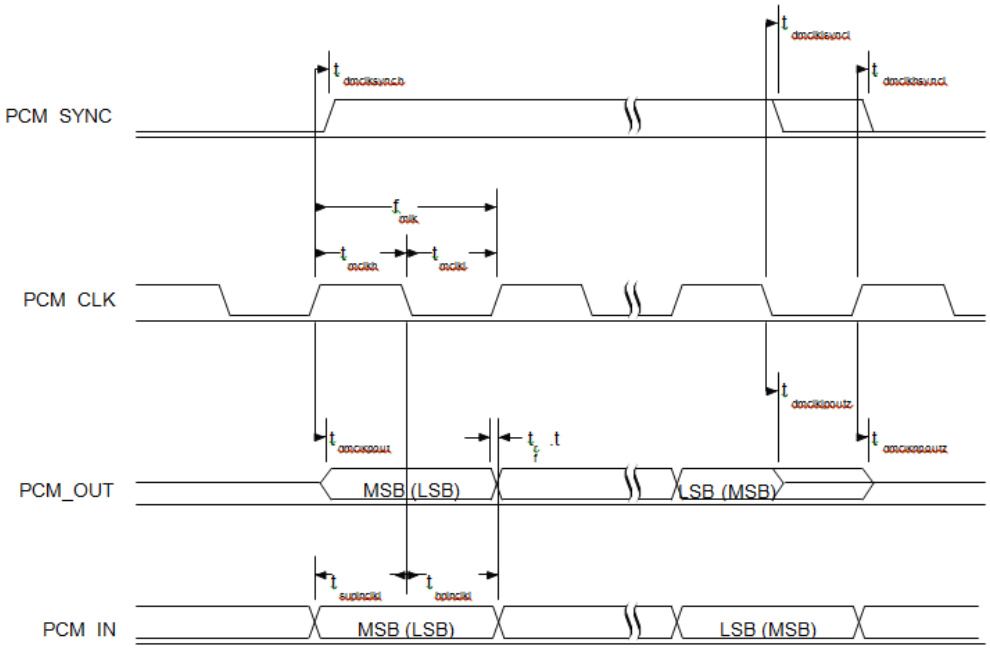

Figure 9: PCM Master Timing Long Frame Sync

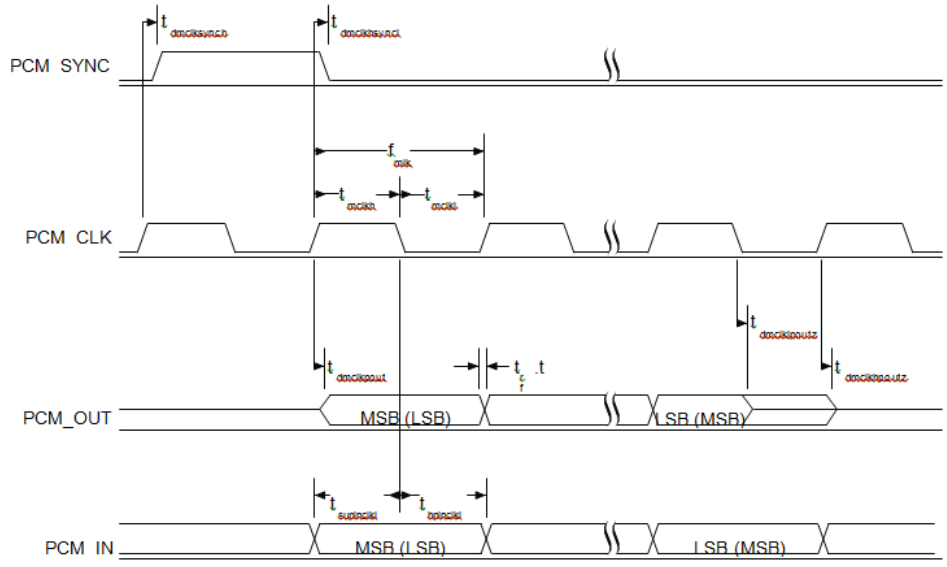

Figure 10: PCM Master Timing Short Frame Sync

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8.8 PCM Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns

8.9 PCM Slave Mode Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	2	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	20	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (long frame sync only)	-	-	15	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	15	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	20	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	2	-	-	ns

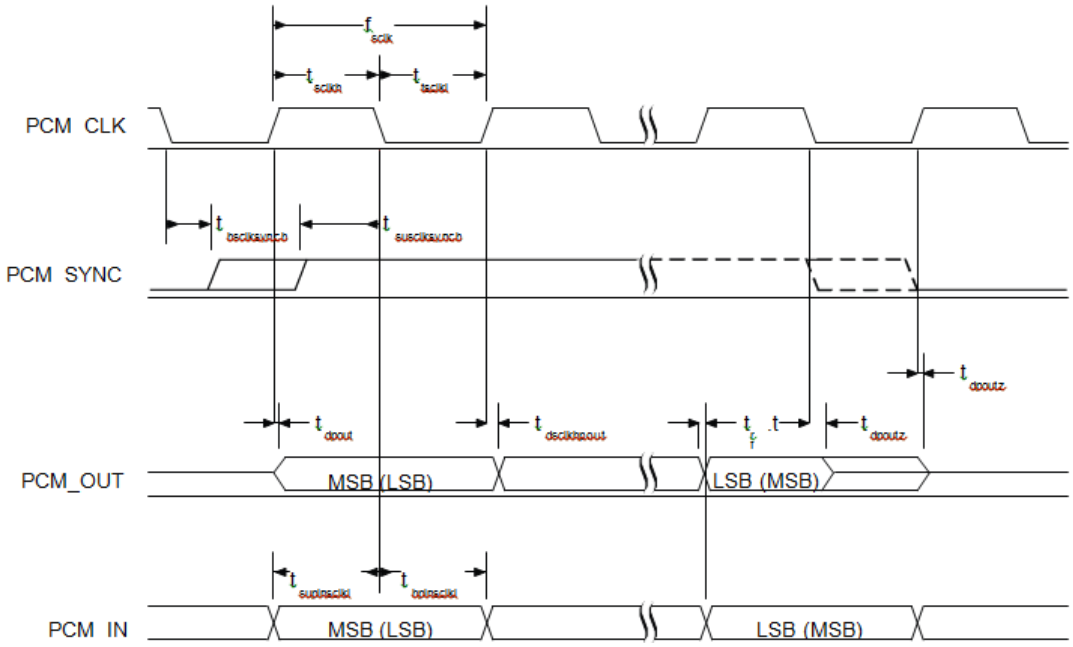

Figure 11: PCM Slave Timing Long Frame Sync

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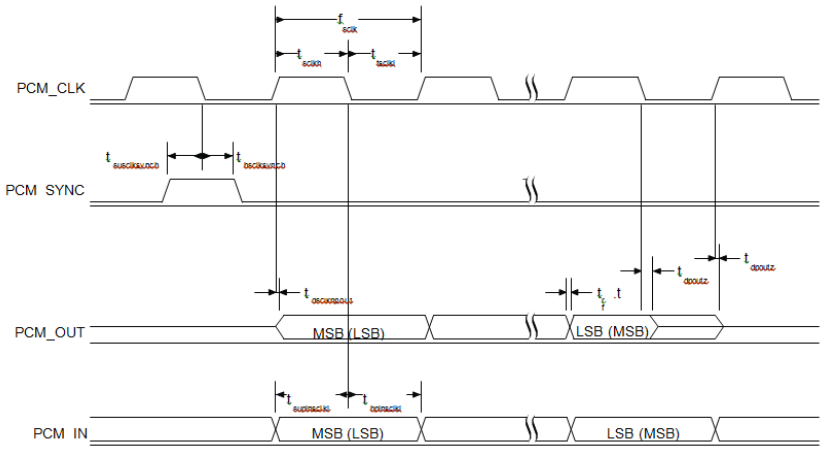

Figure 12: PCM Slave Timing Short Frame Sync

8.10 PCM_CLK and PCM_SYNC Generation

BT830 has two methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from BT830internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512 kHz and PCM_SYNC to 8 kHz.
- Generating these signals by DDS from an internal 48MHz clock enables a greater range of frequencies to be generated with low jitter but consumes more power. To select this second method, set bit to 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC is either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 8.1 describes PCM_CLK frequency when generated from the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 8.1: PCM_CLK Frequency Generated Using the Internal 48MHz Clock

Set the frequency of PCM_SYNC relative to PCM_CLK using Equation 8.2:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 8.2: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set SKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

8.11 PCM Configuration

Configure the PCM by using PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG (see your PSKey file). The default for PSKEY_PCM_CONFIG32 is 0x00800000.

For example: First slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT).

8.12 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface which means each audio bus is mutually exclusive in its usage. Table 12 lists these alternative functions. Figure 11 shows the timing diagram.

Table 12: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

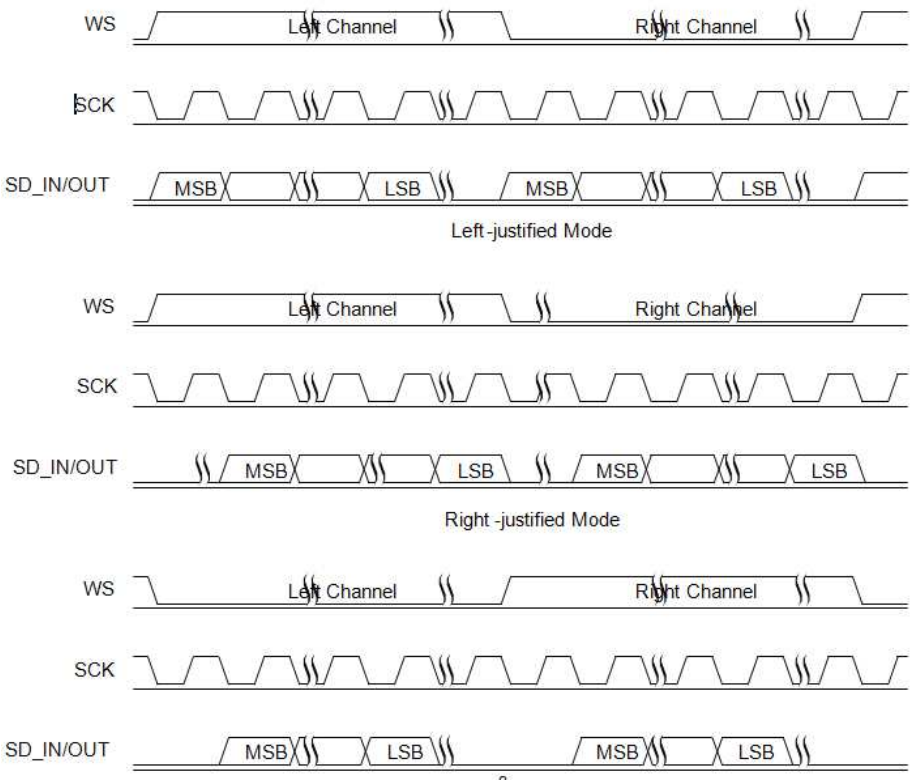

Figure 13: PCM Configuration

The internal representation of audio samples within BT830is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Table 13: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns

Table 14: I²S Slave Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{ssu}	WS valid to SCK high set-up time	20	-	-	ns
t_{sh}	SCK high to WS invalid hold time	2.5	-	-	ns
t_{opd}	SCK low to SD_OUT valid delay time	-	-	20	ns
t_{isu}	SD_IN valid to SCK high set-up time	20	-	-	ns
t_{ih}	SCK high to SD_IN invalid hold time	2.5	-	-	ns

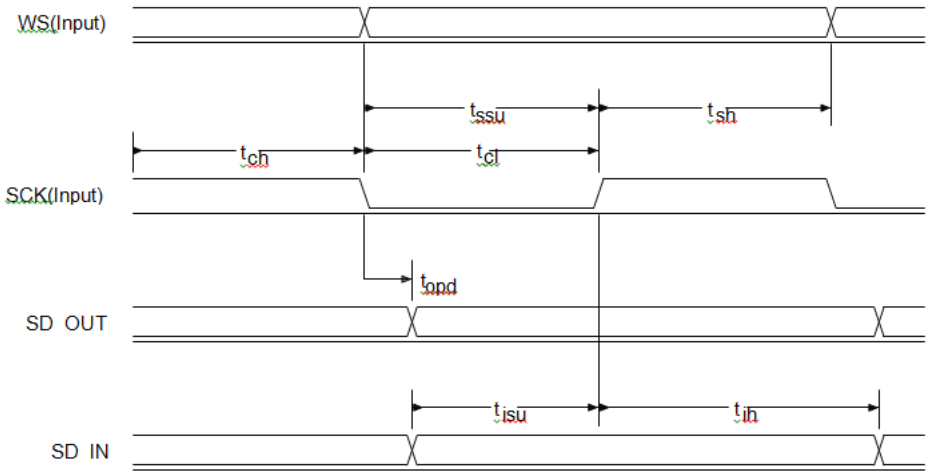

Figure 14: Digital Audio Interface Slave Timing

Table 15: Digital Audio Interface Master Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz

Table 16: I²S Master Mode Timing Parameters, WS and SCK as Outputs

Symbol	Parameter	Min	Typ	Max	Unit
t_{spd}	SCK low to WS valid delay time	-	-	39.27	ns
t_{opd}	SCK low to SD_OUT valid delay time	-	-	18.44	ns
t_{isu}	SD_IN valid to SCK high set-up time	18.44	-	-	ns
t_{ih}	SCK high to SD_IN invalid hold time	0	-	-	ns

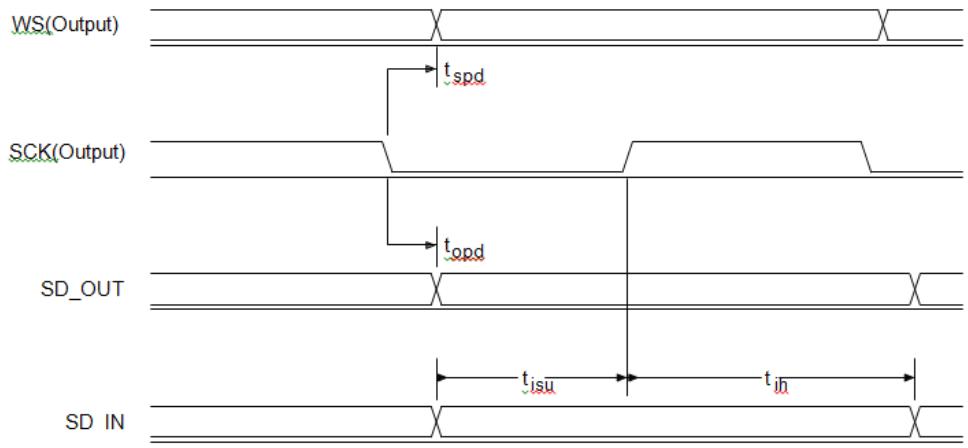

Figure 15: Digital Audio Interface Master Timing

9 Power Supply and Regulation

BT830 can be powered by either of the two sources listed below:

Method #1 – Apply 3.3 V on pin-9, High-voltage linear regulator input (VREG_IN_HV), to generate the main 1.8 V out put on pin-10 (VREG_OUT_HV).

> A minimum 1.5 μ F capacitor must be connected to the Pin-10 (VREG_OUT_HV). Low ESR capacitors such as multilayer ceramic types should be used. In this case, the VDD_PADS can be either 3.3V or 1.8V.

Method #2 – Apply 1.8V on pin-10 High-voltage linear regulator output (VREG_OUT_HV), to generate the internal voltage for the system. Be sure to left Pin-9 un-connected in this method. In this case, the VDD_PADS can only be set at 1.8V.

Note: The I/O signal voltage level (VDD_PADS) should be equal or less than the power supply mentioned voltage above.

9.1 Voltage Regulator Enable and Reset

A single pin, VREG_EN_RST#, controls both the high-voltage linear regulator enables and the digital reset function. The VREG_EN_RST# pin remains active controlling the reset function if the HV linear regulator is not used; the pin must be driven high to take the device out of reset.

The regulator is enabled by taking the VREG_EN_RST# pin above 1.0V. The regulator can also be controlled by the software.

The VREG_EN_RST# is also connected internally to the reset function, and is powered from the VDD_PADS supply, so voltages above VDD_PADS must not be applied to this pin. The VREG_EN_RST# pin is pulled down internally.

The VREG_EN_RST# pin is an active low reset. Assert the reset signal for a period greater than five milliseconds to ensure a full reset.

Note: The regulator enables are released as soon as VREG_EN_RST# is low, so the regulators shut down. Therefore do not take VREG_EN_RST# low for less than five millilseconds, as a full reset is not guaranteed.

Other reset sources are:

- Power-on reset
- Via a software-configured watchdog timer

A warm reset function is also available under software control. After a warm reset the RAM data remains available.

9.2 Power Sequencing

CSR recommends that all power supplies are powered at the same time. The order of powering the supplies relative to the I/O supply, VDD_PADS to VREG_IN_HV or VREG_OUT_HV, is not important.

10 Antenna Performance

10.1 Multilayer Chip Antenna

Figure 16 illustrates this antenna's performance.

Unit in dBi @2.44GHz	XY-plane		XZ-plane		YZ-plane		Efficiency
	Peak	Avg.	Peak	Avg.	Peak	Avg.	
AT3216-B2R7HAA	-2.2	-5.9	-0.7	-5.0	-1.3	-3.7	40%

Figure 16: BT830 gain table for the multilayer chip antenna

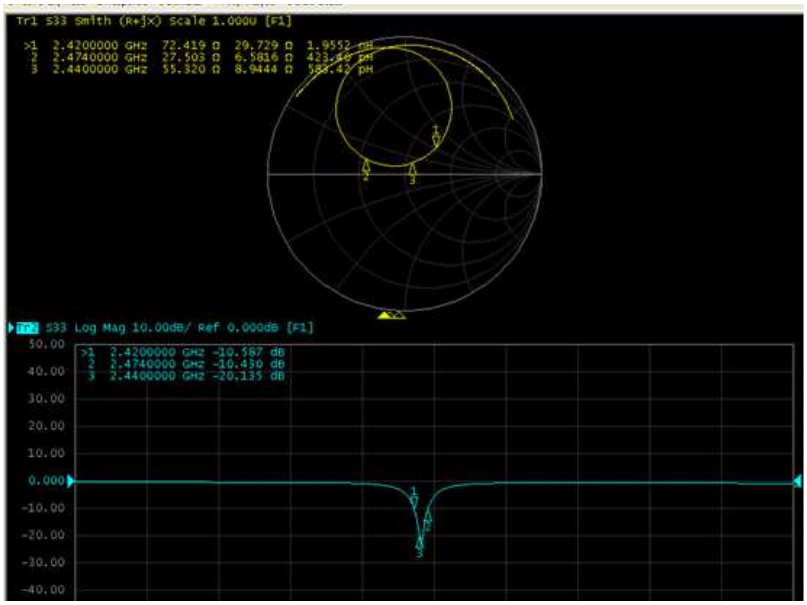

Figure 17: Network Analyzer output

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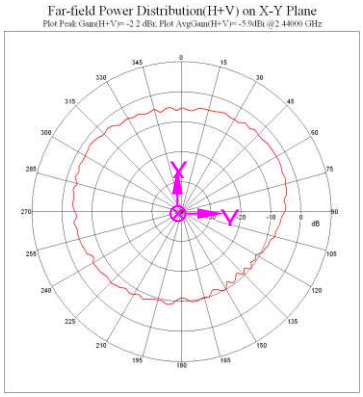
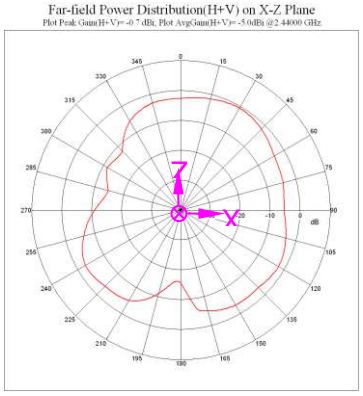
XY-plane



Unit : dBi

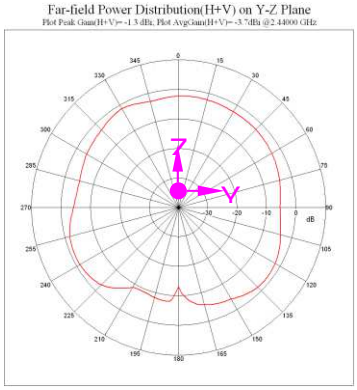
	Peak gain	Avg. gain
XY-plane	-2.2	-5.9

XZ-plane



	Peak gain	Avg. gain
XZ-plane	-0.7	-5.0

YZ-plane



	Peak gain	Avg. gain
YZ-plane	-1.3	-3.7

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