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IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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Thank you for your cooperation and understanding,

WeEn Semiconductors

BTA202X-800E

3Q Hi-Com Triac

22 May 2014 Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT186A (TO-220F) "full pack" plastic package. This "series E" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers including microcontrollers.

2. Features and benefits

- 3Q technology for improved noise immunity
- Direct interfacing with low power drivers and microcontrollers
- Good immunity to false turn-on by dV/dt
- High commutation capability with sensitive gate
- High voltage capability
- Isolated mounting base package
- Planar technology for voltage ruggedness and reliability
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only

3. Applications

- General purpose motor controls
- Large and small appliances (White Goods)
- Loads such as contactors, circuit breakers, valves, dispensers and door locks
- Lower-power highly inductive, resistive and safety loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	-	14	A
T_j	junction temperature			-	-	125	°C
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 110$ °C; Fig. 1; Fig. 2; Fig. 3		-	-	2	A

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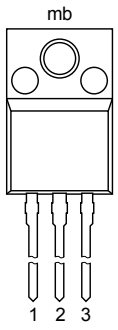
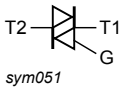
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		0.5	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		0.5	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		0.5	-	10	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; R_{GT1} = 220 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform		-	500	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit		2	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 **TO-220F (SOT186A)**	 *sym051*
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

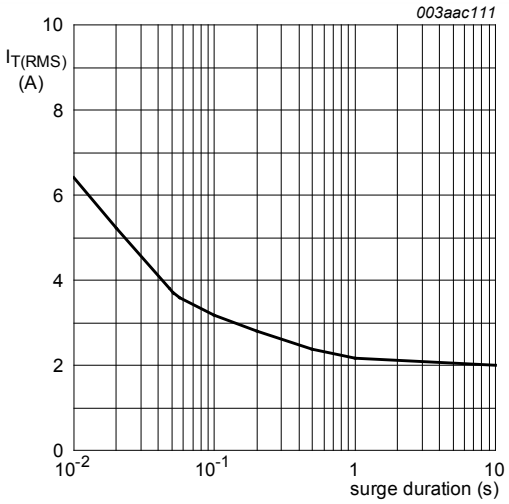
Type number	Package		
	Name	Description	Version
BTA202X-800E	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A
BTA202X-800E/L01	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 110$ °C; Fig. 1; Fig. 2; Fig. 3		-	2	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		-	14	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	15.4	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse		-	0.98	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 1.5$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs		-	100	A/µs
I_{GM}	peak gate current			-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C



f = 50 Hz; $T_h = 110$ °C

Fig. 1. RMS on-state current as a function of surge duration; maximum values

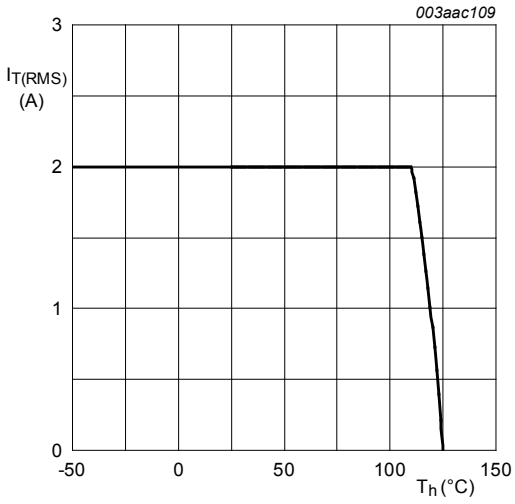
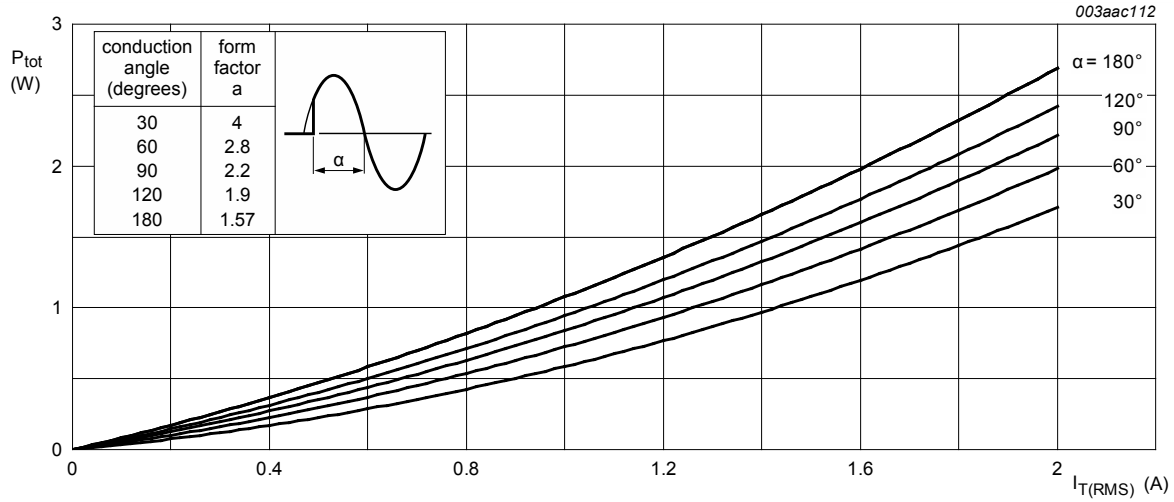


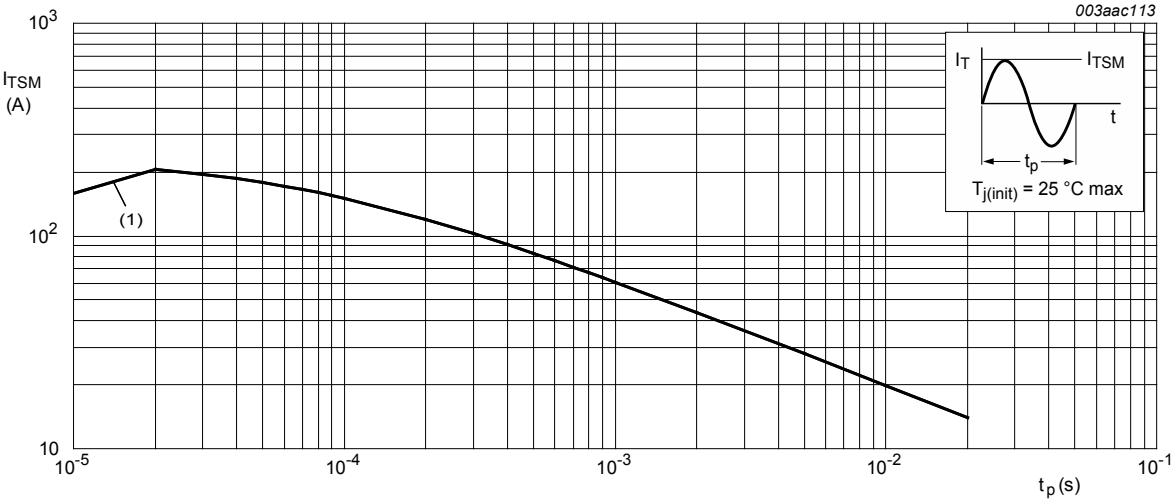
Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values



α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

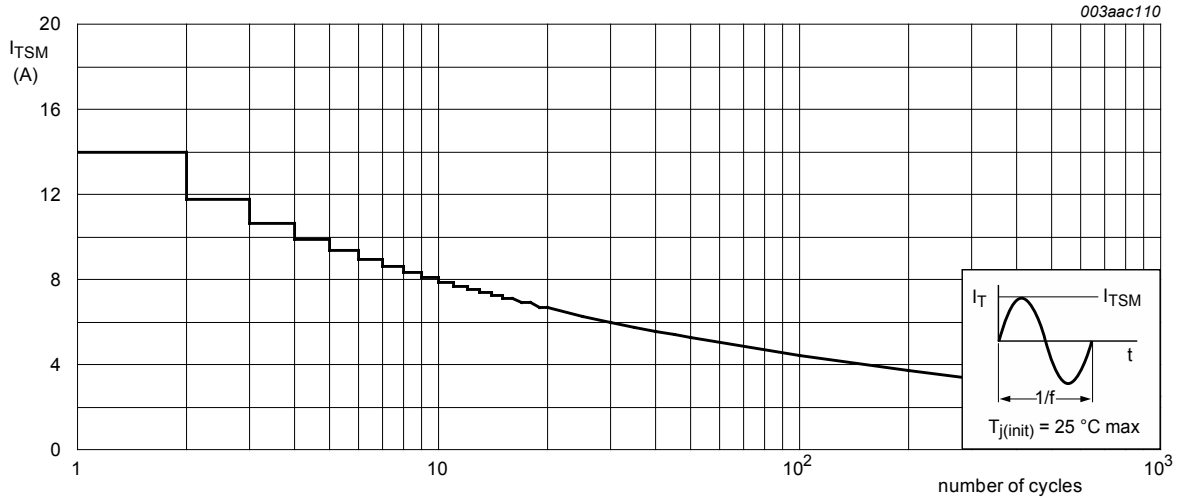
Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



t_p ≤ 20 ms

(1) dI_T/dt limit

Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values



f = 50 Hz

Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle; with heatsink compound; Fig. 6		-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	55	-	K/W

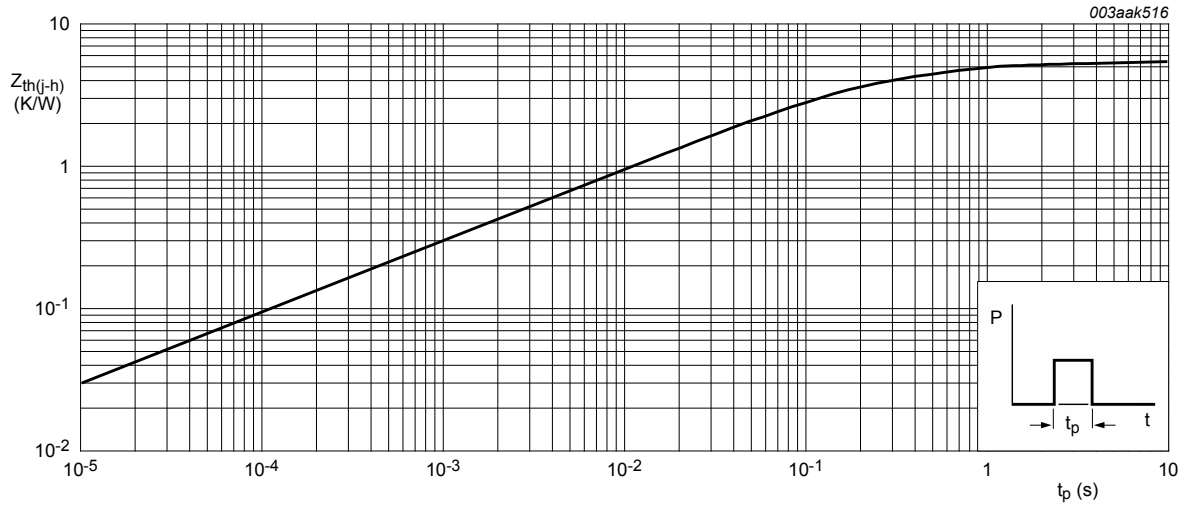


Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse width

9. Isolation characteristics

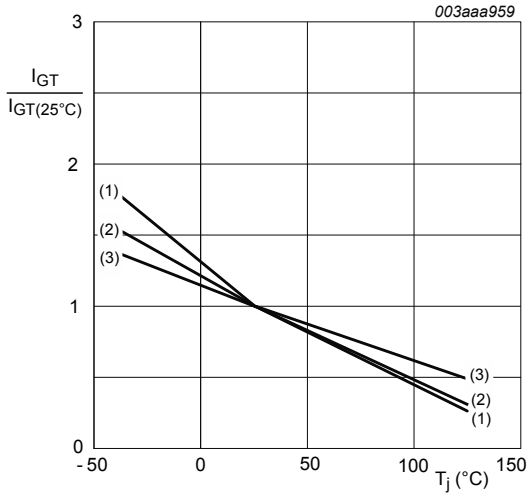
Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C		-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz		-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		0.5	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		0.5	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		0.5	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 8		-	-	12	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 8		-	-	20	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; Fig. 8		-	-	12	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	-	12	mA
V_T	on-state voltage	I_T = 3 A; T_j = 25 °C; Fig. 10		-	1.63	2	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.7	1	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C; Fig. 11		0.2	0.3	-	V
I_D	off-state current	V_D = 800 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; R_{GT1} = 220 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform		-	500	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit		2	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 2 A; dV_{com}/dt = 10 V/µs; gate open circuit		2.3	-	-	A/ms



(1) T2- G-
(2) T2+ G-
(3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

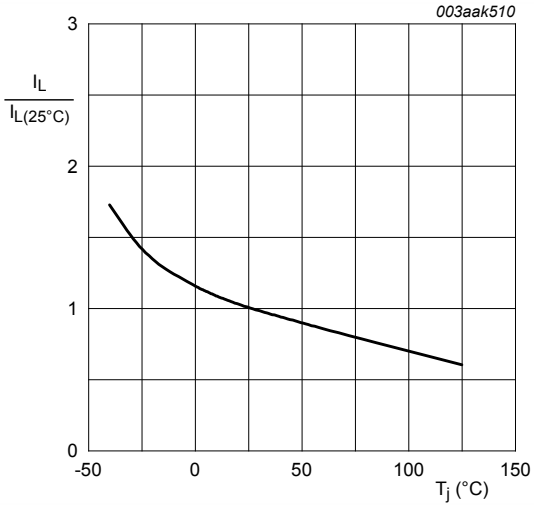


Fig. 8. Normalized latching current as a function of junction temperature

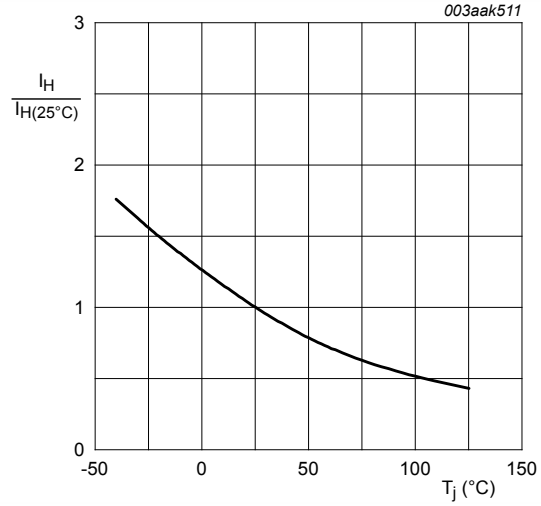
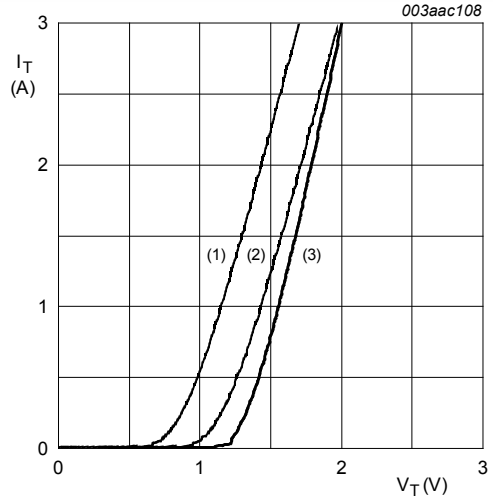


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 0.9 V; R_s = 0.267 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

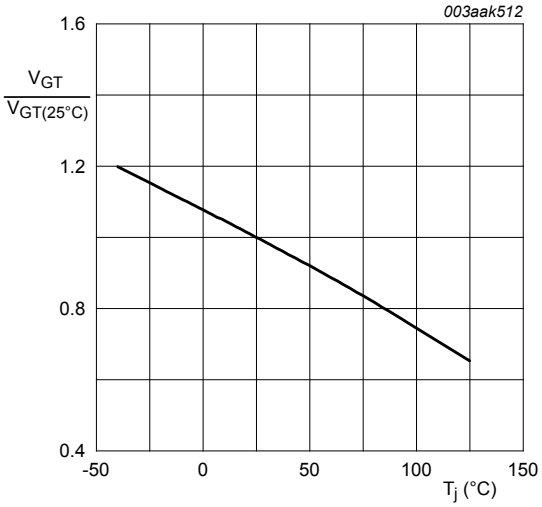
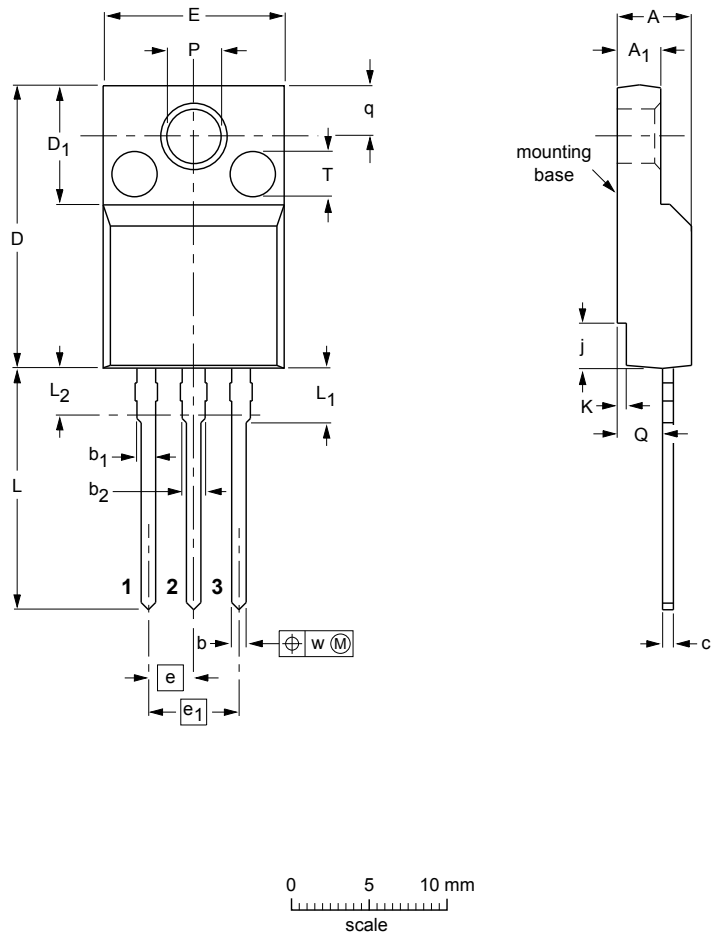


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2 (1) max.	P	Q	q	T (2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are # 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				~~02-04-09~~ 06-02-14

Fig. 12. Package outline TO-220F (SOT186A)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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Date of release: 22 May 2014