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HITFET™ +

BTF3050TE

Smart Low-Side Power Switch

Single channel, 50 mΩ

Datasheet

Rev. 1.0, 2014-07-21

Automotive Power

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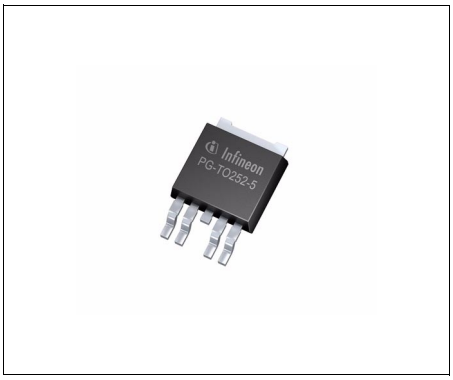
1 Overview



PG-TO252-5

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for inductive loads as well as loads with inrush currents

Features

- Single channel device
- Very low power DMOS leakage current in OFF state
- 3.3 V and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Adjustable switching speed
- Digital Feedback
- Green Product (RoHS compliant)
- AEC Qualified

Description

The BTF3050TE is a 50 mΩ single channel Smart Low-Side Power Switch in a PG-TO252-5 package providing embedded protective functions. The power transistor is built by a N-channel vertical power MOSFET.
The device is monolithically integrated. The BTF3050TE is automotive qualified and is optimized for 12V automotive and industrial applications.

Table 1 Product Summary

Operating voltage range	V_{OUT}	3 .. 28 V
Maximum load voltage	$V_{BAT(LD)}$	40 V
Operating supply voltage range	V_{DD}	3.0 .. 5.5 V
Maximum input voltage	V_{IN}	5.5 V
Maximum On-State resistance at T_J = 150°C, V_{DD} = 5V	$R_{DS(ON)}$	100 mΩ
Nominal load current	$I_{L(NOM)}$	3.0 A
Minimum current limitation trigger level	$I_{L(LIM)\_TRIGGER}$	30 A
Maximum OFF state load current at T_J ≤ 85 °C	$I_{L(OFF)}$	2 µA
Maximum stand-by supply current at T_J = 25 °C	$I_{DD(OFF)}$	6 µA

Type	Package	Marking
BTF3050TE	PG-TO252-5	

Diagnostic Functions

- Short circuit to battery
- Over temperature
- Stable latching diagnostic signal

Protection Functions

- Over temperature shutdown with auto-restart
- Active clamp over voltage protection of the output
- Current limitation
- Enhanced short circuit protection

Detailed Description

The device is able to switch all kind of resistive, inductive and capacitive loads, limited by clamping energy (E_{AS}) and maximum current capabilities.

The BTF3050TE offers dedicated ESD protection on the IN, VDD and SRP pins which refers to the Ground pin, as well as an over voltage clamping of the output to Source/GND.

The over voltage protection gets activated during inductive turn off conditions or other over voltage events (e.g. load dump). The power MOSFET is limiting the drain-source voltage, if it rises above the $V_{OUT(CLAMP)}$.

The over temperature protection prevents the device from overheating due to overload and/or bad cooling conditions.

The BTF3050TE has a thermal-restart function. The device will turn on again, if input is still high, after the measured temperature has dropped below the thermal hysteresis.

2 Block Diagram

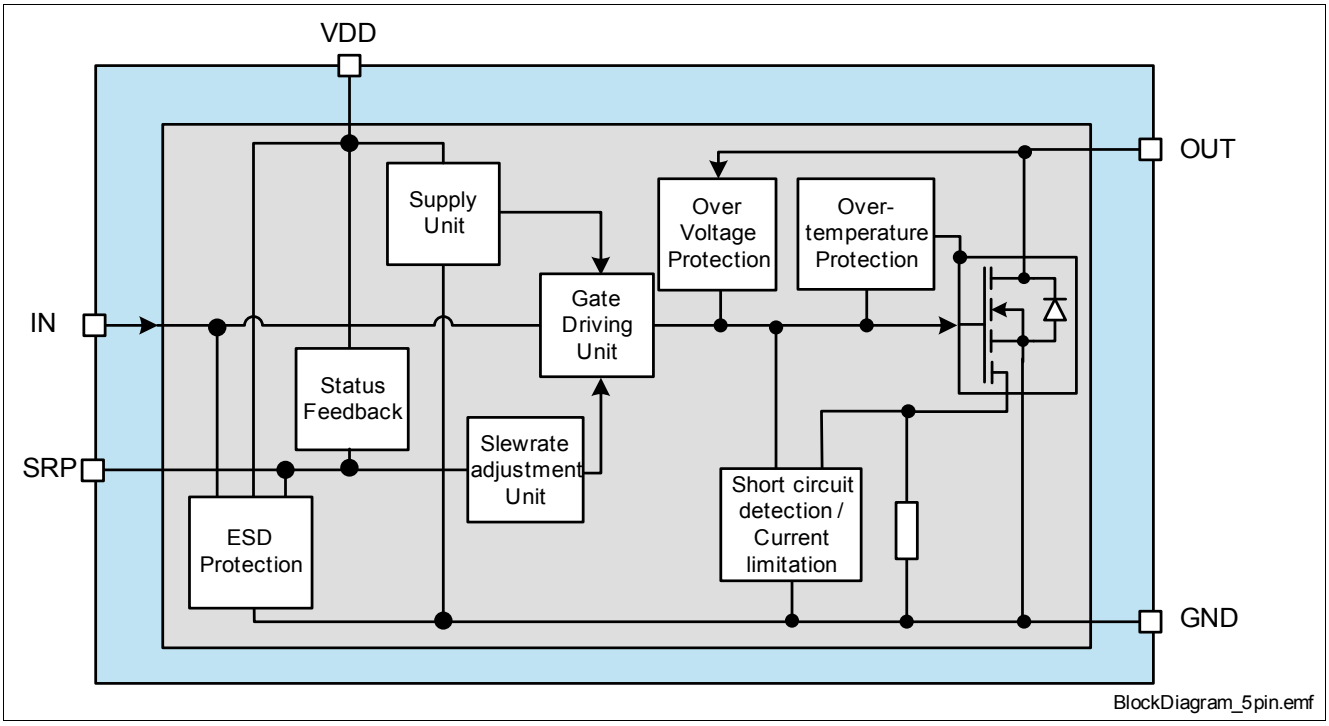


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment BTF3050TE

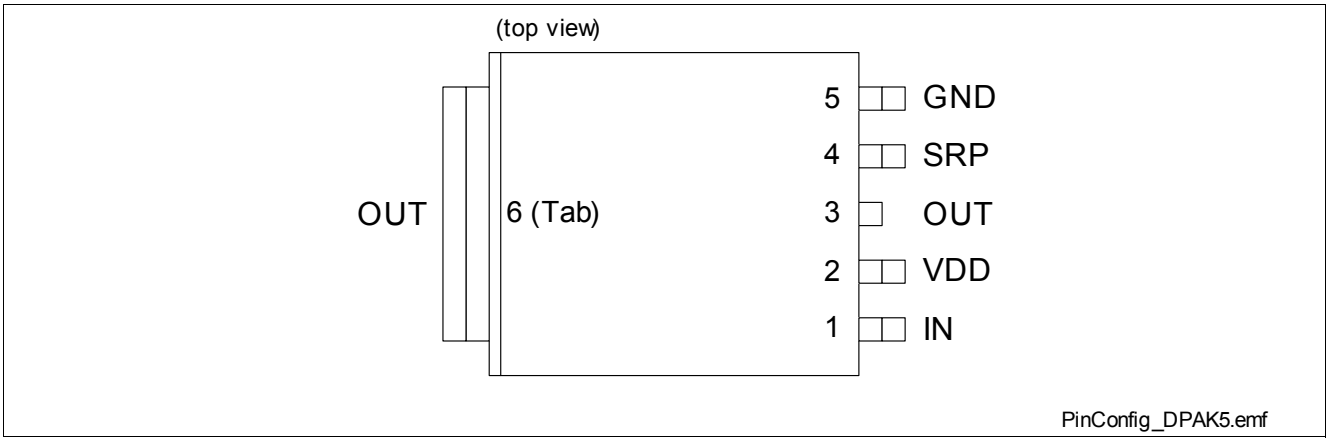


Figure 2 Pin Configuration PG-TO252-5

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	IN	Input pin
2	VDD	5V supply pin
3,6	OUT	Drain, Load connection for power DMOS
4	SRP	Slew rate adjustment and digital status feedback
5	GND	Ground, Source of power DMOS

3.3 Voltage and Current Definition

Figure 3 shows all external terms used in this data sheet, with associated convention for positive values.

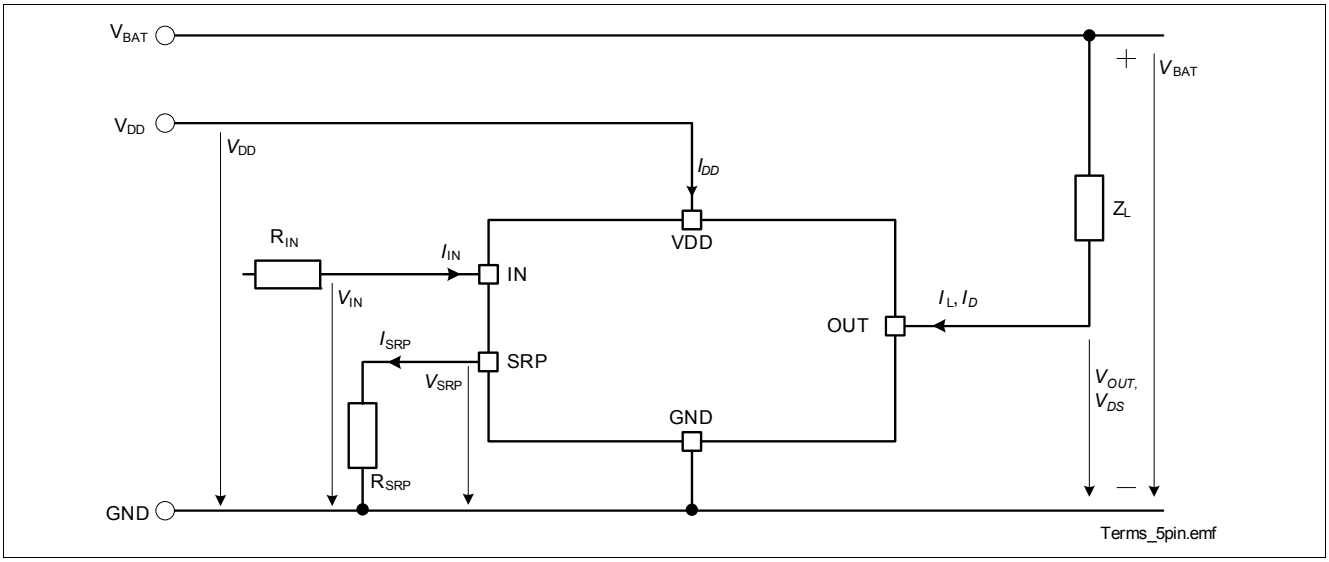


Figure 3 Naming Definition of electrical parameters

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1)]

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Note / Test Condition
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.2	Output voltage	V_{OUT}	-0.3	40	V	internally clamped
4.1.3	Battery voltage for short circuit protection	$V_{BAT(SC)}$	–	28	V	1) l = 0 ... 5m R_{SC} = 30 mΩ + R_{CABLE} R_{CABLE} = l * 16 mΩ/m L_{SC} = 5 µH + L_{CABLE} L_{CABLE} = l * 1 µH/m
4.1.4	Battery voltage for load dump protection ($V_{BAT(LD)}$ = V_A + V_S with V_A = 13.5V)	$V_{BAT(LD)}$	–	40	V	2) R_I = 2 Ω, R_L = 4.5 Ω, t_D = 400 ms, suppressed pulse
Input and SRP Pins						
4.1.5	Input Voltage	V_{IN}	-0.3	5.5	V	–
4.1.6	SRP pin Voltage	V_{SRP}	-0.3	5.5	V	$V_{SRP} < V_{DD}$
Power Stage						
4.1.7	Load current	$\|I_L\|$	–	$I_{L(LIM)\_TRIGGER}$	A	T_J < 150 °C
Energies						
4.1.8	Unclamped single inductive energy single pulse	E_{AS}	–	120	mJ	$I_{L(0)} = I_{L(NOM)}$ V_{BAT} = 13.5 V $T_{J(0)}$ = 150 °C
4.1.9	Unclamped repetitive inductive energy pulse with 100k cycles	$E_{AR(100k)}$	–	80	mJ	$I_{L(0)}$ = 4.5A V_{BAT} = 13.5 V $T_{J(0)}$ = 105 °C
Temperatures						
4.1.10	Operating temperature	T_J	-40	+150	°C	–
4.1.11	Storage temperature	T_{STG}	-55	+150	°C	–
ESD Susceptibility						
4.1.12	ESD susceptibility (all pins)	V_{ESD}	-2	2	kV	HBM[3)]
4.1.13	ESD susceptibility OUT pin vs. GND	V_{ESD}	-4	4	kV	HBM[3)]
4.1.14	ESD susceptibility	V_{ESD}	-750	750	V	CDM[4)]

1) Not subject to production test, specified by design.

2) $V_{BAT(LD)}$ is setup without the DUT connected to the generator per ISO7637-1;
R_I is the internal resistance of the load dump test pulse generator;
t_D is the pulse duration time for load dump pulse (pulse 5) according ISO 7637-1, -2.
3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF)
4) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation

4.2 Functional Range

Table 3 Functional Range[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
4.2.1	Supply Voltage Range for Normal Operation	$V_{DD(NOR)}$	3.0	5.0	5.5	V	–
4.2.2	Supply current continuous ON operation	I_{DD}	–	2.5	6	mA	–
4.2.3	Standby supply current (ambient)	$I_{DD(OFF)\_25}$	–	1.5	6	µA	T_J = 25 °C
4.2.4	Maximum standby supply current (hot)	$I_{DD(OFF)\_150}$	–	6	14	µA	T_J = 150°C
4.2.5	Battery Voltage Range for Nominal Operation	$V_{BAT(NOR)}$	8	13.5	18	V	–
4.2.6	Extended Battery Voltage Range for Operation	$V_{BAT(EXT)}$	3	–	28	V	parameter deviations possible
4.2.7	SRP pin resistor for normal operation	$R_{SRP(NOR)}$	5	–	70	kΩ	–
4.2.8	SRP pin resistor for extended operation	$R_{SRP(EXT)}$	0	–	600	Ω	no latched fault available

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards.
*For more information, go to **www.jedec.org**.*

Table 4 Thermal resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
4.3.1	Junction to Case	R_{thJC}	–	1.9	–	K/W	1) 2)
4.3.2	Junction to Ambient (2s2p)	$R_{thJA(2s2p)}$	–	25	–	K/W	1) 3)
4.3.3	Junction to Ambient (1s0p+600mm^2 Cu)	$R_{thJA(1s0p)}$	–	38	–	K/W	1) 4)

1) Not subject to production test, specified by design
2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature). T_C = 85 °C. Device is loaded with 1W power.
3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. T_a = 85 °C, Device is loaded with 1W power.
4) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm^2 and 70 µm thickness. T_a = 85°C, Device is loaded with 1W power.

4.3.1 PCB set up

The following PCB set up was implemented to determine the transient thermal impedance.

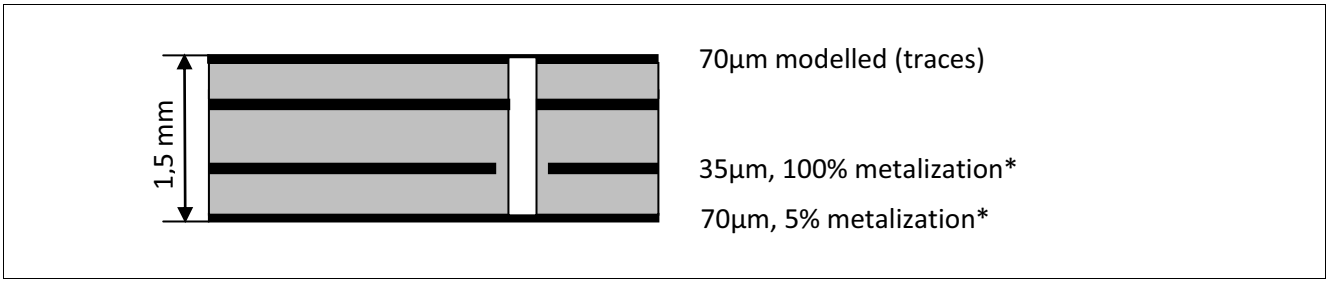


Figure 4 Cross section JEDEC2s2p.

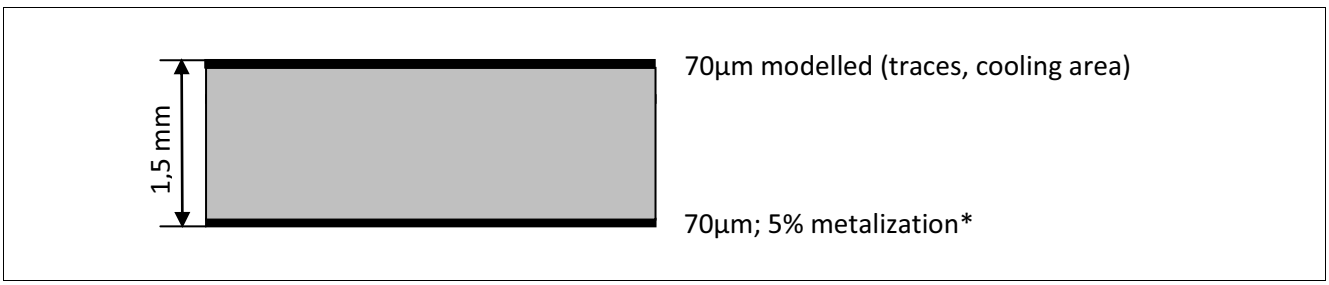


Figure 5 Cross section JEDEC1s0p.

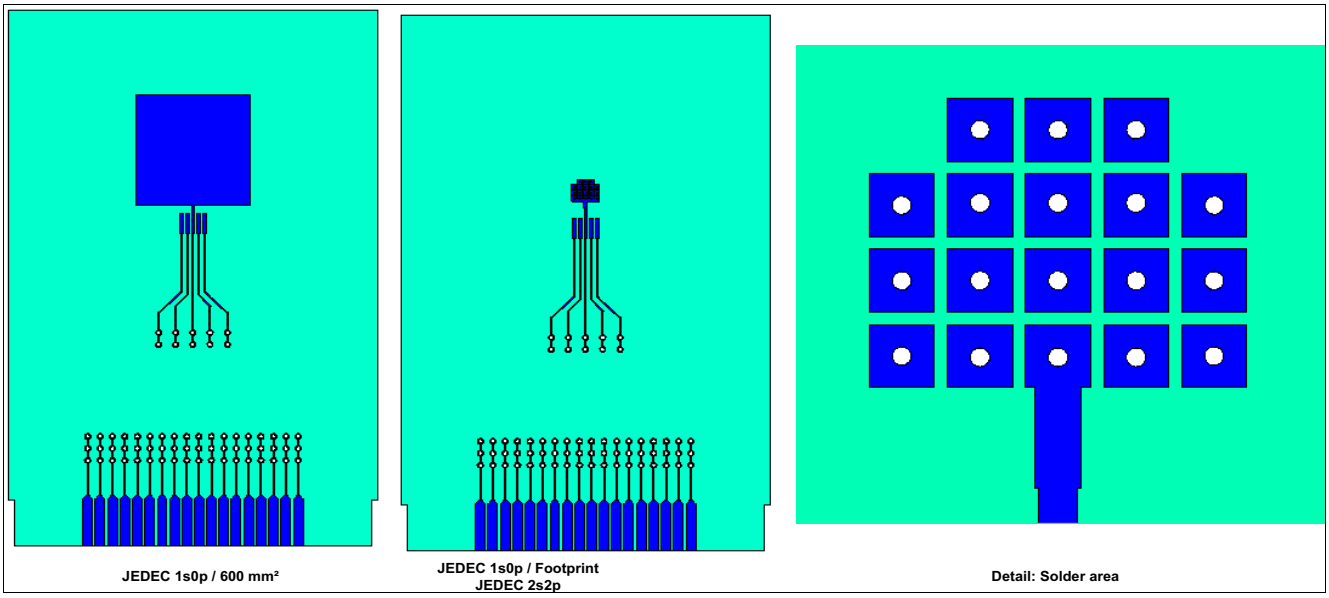


Figure 6 PCB layout

4.3.2 Transient Thermal Impedance

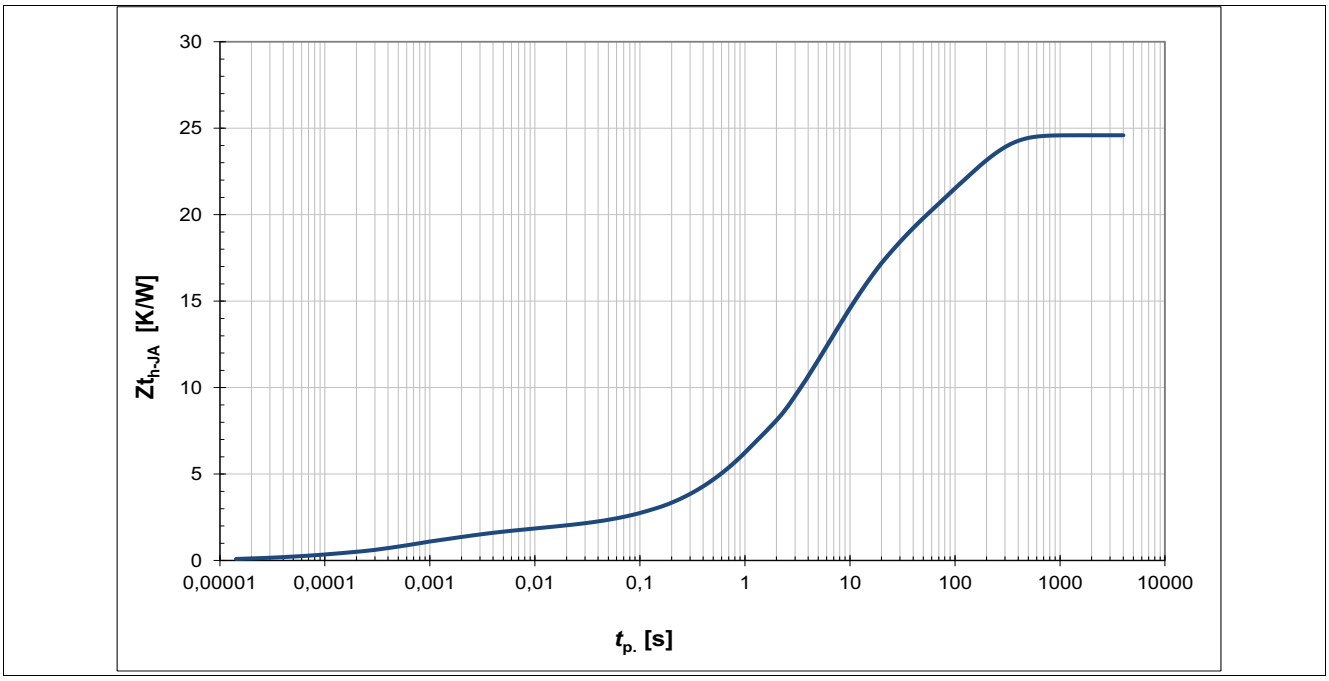


Figure 7 Typical transient thermal impedance Z_{thJA} = f(t_p), T_a = 85 °C
Value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70 mm Cu, 2 x 35 mm Cu). Where applicable a thermal via array under the ex posed pad contacted the first inner copper layer. Device is dissipating 1 W power.

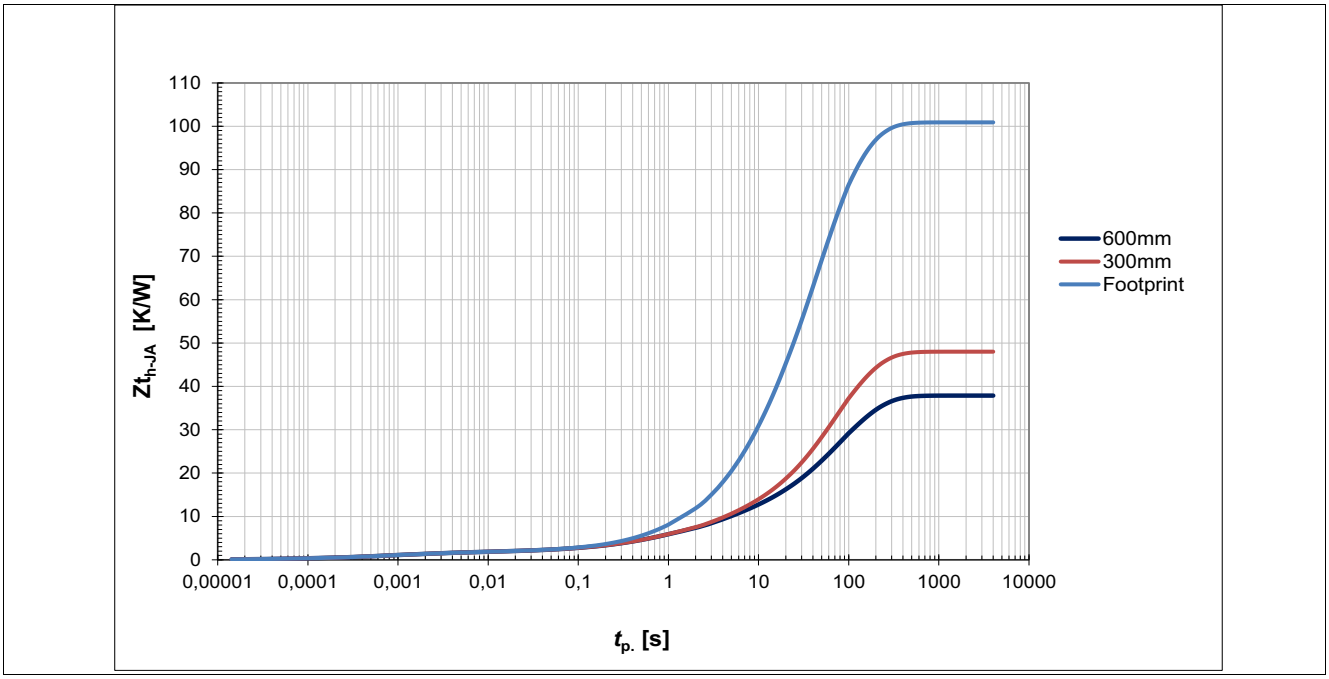


Figure 8 **Typical transient thermal impedance Z_{thJA} = f(t_p), T_a = 85 °C**
Value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board. Device is dissipating 1 W power.

5 Power Stage

5.1 Output On-state Resistance

The on-state resistance depends on the supply voltage as well as on the junction temperature T_J. **Figure 9** shows this dependencies in terms of temperature and voltage for the typical on-state resistance $R_{DS(ON)}$. The behavior in reverse polarity is described in chapter**"Reverse/Inverse Current Capability" on Page 15**.

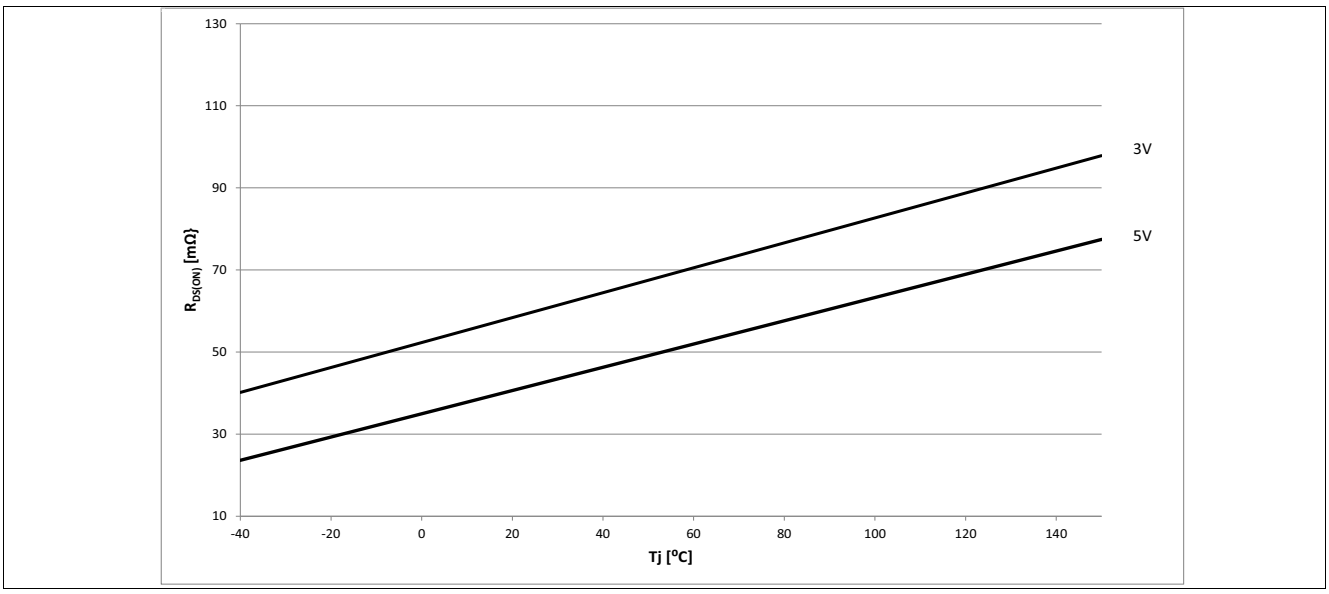


Figure 9 Typical On-State Resistance, $R_{DS(ON)}$ = f(T_J), V_{DD} = 5 V, V_{DD} = 3V, V_{IN} = high

A high signal at the input pin causes the power DMOS to switch ON with a dedicated slope.

To achieve a reasonable $R_{DS(ON)}$ and the specified switching speed a 5V supply is required.

5.2 Resistive Load Output Timing

Figure 10 shows the typical timing when switching a resistive load.

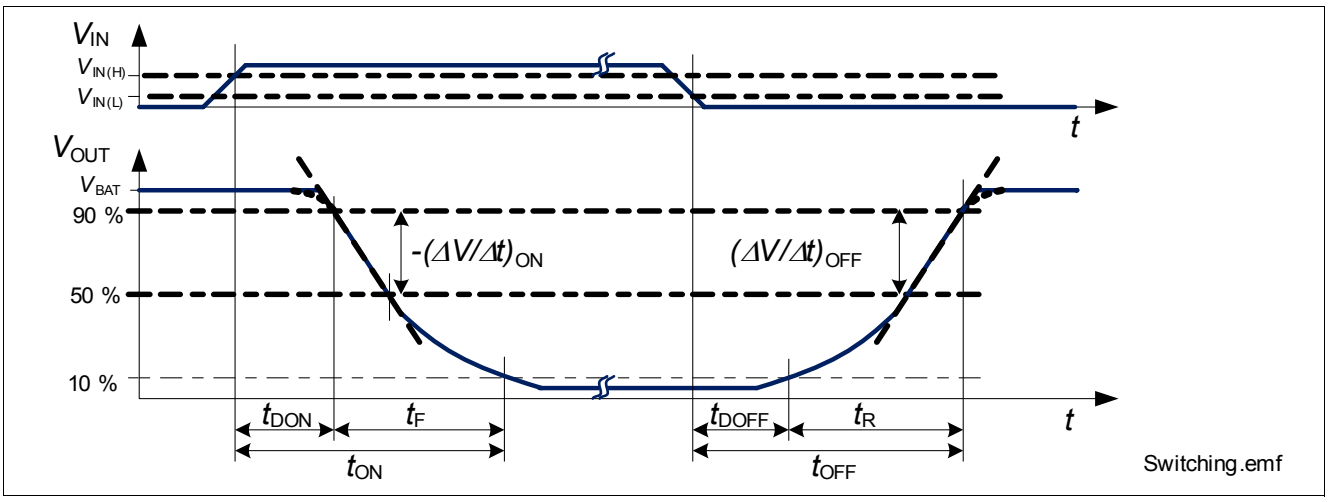


Figure 10 Definition of Power Output Timing for Resistive Load

5.3 Inductive Load

5.3.1 Output Clamping

When switching off inductive loads with low side switches, the drain-source voltage V_{OUT} rises above battery potential, because the inductance intends to continue driving the current. To prevent unwanted high voltages the device has a voltage clamping mechanism to keep the voltage at $V_{OUT(CLAMP)}$. During this clamping operation mode the device heats up as it dissipates the energy from the inductance. Therefore the maximum allowed load inductance is limited. See **Figure 11** and **Figure 12** for more details.

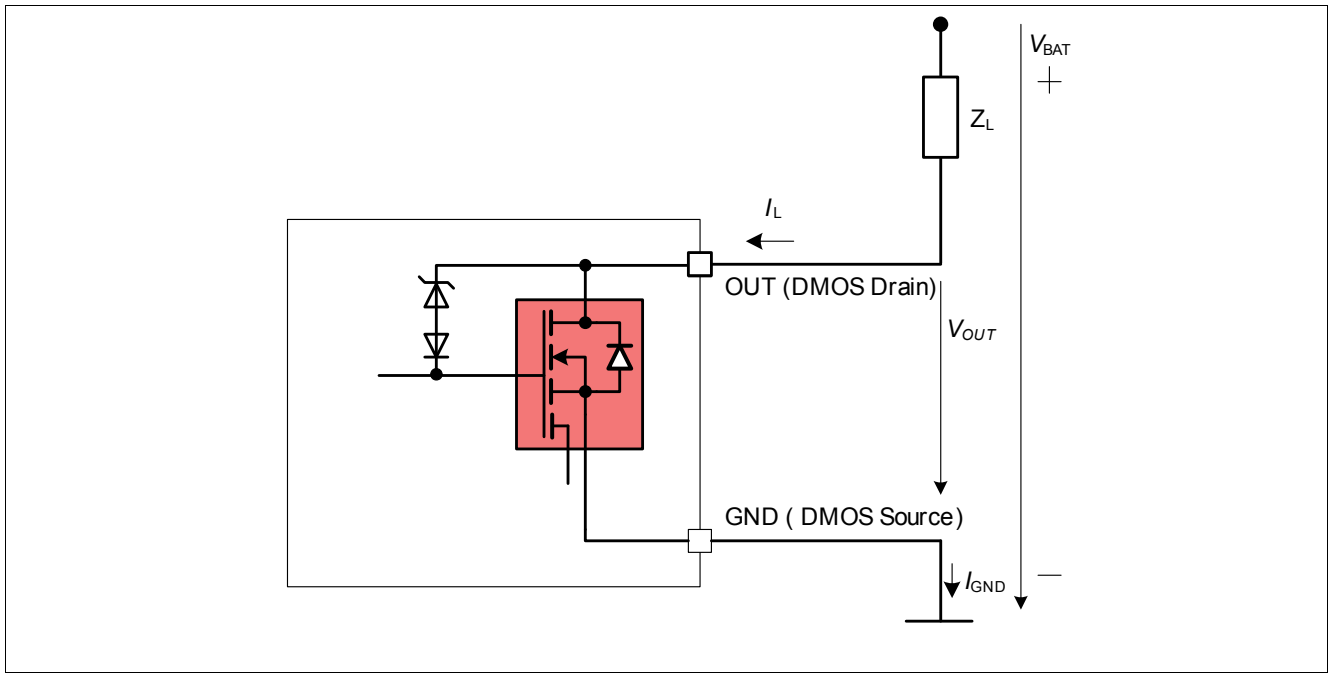


Figure 11 Output Clamp Circuitry

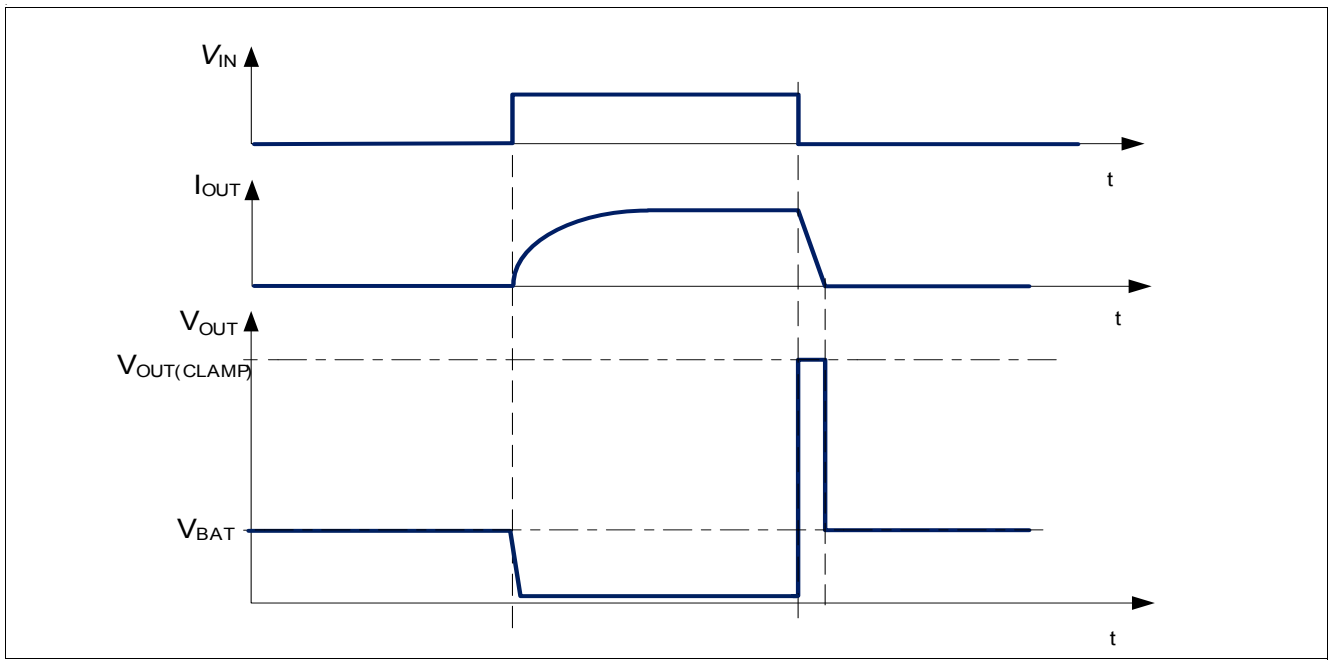


Figure 12 Switching an Inductive Load

Note: Repetitive switching of inductive load by V_{DD} instead of using the input is a not recommended operation and may affect the device reliability and reduce the lifetime.

5.3.2 Maximum Load Inductance

While demagnetization of inductive loads, energy has to be dissipated in the BTF3050TE.
This energy can be calculated by the following equation:

$$E = V_{OUT(CLAMP)} \cdot \left[\frac{V_{BAT} - V_{OUT(CLAMP)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_{BAT} - V_{OUT(CLAMP)}}\right) + I_L \right] \cdot \frac{L}{R_L}$$

Following equation simplifies under assumption of R_L = 0

$$E = \frac{1}{2} L I_L^2 \cdot \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CLAMP)}}\right)$$

Figure 13 shows the inductance / current combination the BTF3050TE can handle.
For maximum single avalanche energy please also refer to E_{AS} value in **"Energies" on Page 8**

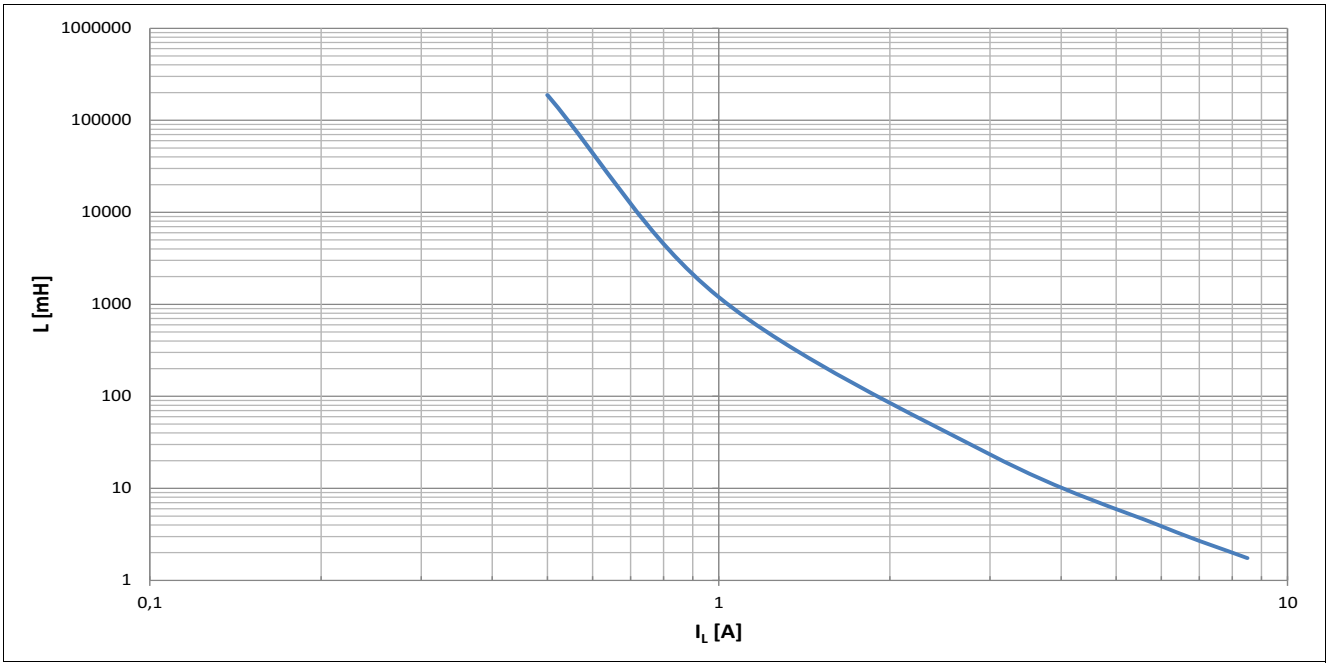


Figure 13 Maximum load inductance for single pulse
$L = f(I_L)$, $T_{J,start}$ = 150 °C, V_{BAT} = 13.5 V

5.4 Reverse/Inverse Current Capability

A reverse battery situation means the OUT pin is pulled below GND potential to $-V_{BAT}$ via the load Z_L.

In this situation the load is driven by a current through the intrinsic body diode of the BTF3050TE and all protection, such as current limitation, over temperature or over voltage clamping, are inactive.

In certain application cases (for example, usage in a bridge or half-bridge configuration) the intrinsic reverse body diode is used for freewheeling of an inductive load. In this case the device is still supplied but an inverse current is flowing from GND to OUT(drain) and the OUT will be pulled below GND.

In inverse or reverse operation via the reverse body diode, the device is dissipating a power loss which is defined by the driven current and the voltage drop on the body diode $-V_{DS}$.

During inverse current, an increased supply current I_{DD} flowing into V_{DD} needs to be considered . The device might be reset by inverse current.

5.5 Adjustable Swtiching Speed / Slew Rate

In order to optimize electromagnetic emission, the switching speed of the MOSFET can be adjusted by connecting an external resistor between SRP pin and GND. This allows for balancing between electromagnetic emissions and power dissipation. Shorting the SRP pin to GND represents the fastest switching speed. Open SRP pin represents the slowest switching speed. It is recommended to put a high ohmic resistor like 200kΩ on this SRP pin to GND.

The accuracy of the switching speed adjustment is dependent on the precision of the external resistor used. It's recommended to use accurate resistors.

Figure 14 shows the simplified relation between the resistor value and the switching times.

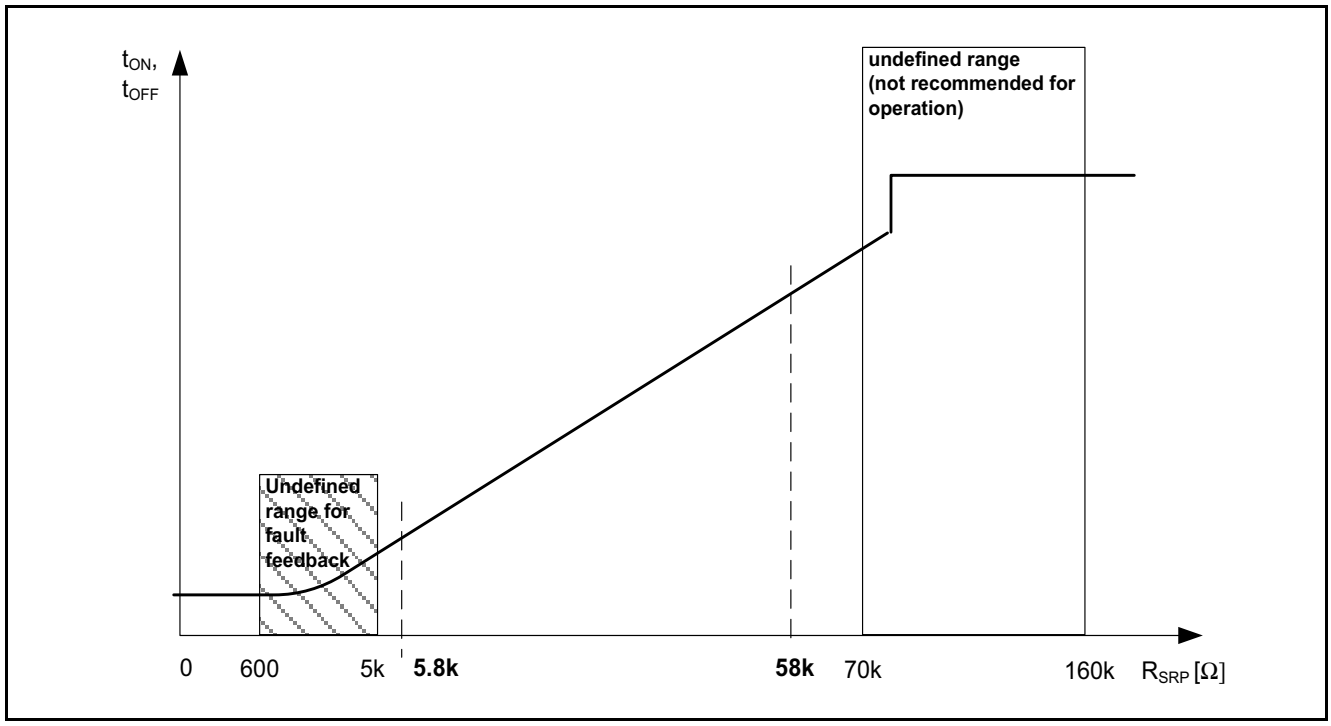


Figure 14 Typical simplified relation between switching time and R_{SRP} resistor values used on SRP pin (V_{BAT} = 13.5V)

It is not recommended to change the slew rate resistance during switching (supplied device, $V_{DD} > V_{DD(UV\_ON)}$). Otherwise undefined switching behavior can occur.

Slew Rate in Fault mode (fault signal set):

Beside the normal slew rate function the SRP pin is also used as fault feedback output. In case of a latched fault caused by over temperature detection the SRP pin will be internally pulled to V_{DD}. For details please refer to **"Functional Description of the SRP Pin" on Page 22**. In this operation mode (latched fault signal) the slew rate control by R_{SRP} will be ignored and the switching speed (dynamic characteristics) will be set to fault mode default values . As long as the fault signal is set and the SRP-pin is not shorted to GND a fast default slew rate adjustment (like for R_{SRP} = 5.8kΩ) will be applied to the device.

If the SRP pin will be externally pulled up above the normal SRP pin voltage $V_{SRP(NOR)}$ (e.g. to V_{DD}) the slowest slew rate settings will be applied.

5.6 Characteristics

Please see **“Power Stage” on Page 26** for electrical characteristic table.

6 Protection Functions

The device provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not to be used for continuous or repetitive operation. Over temperature is indicated by a high-logic active fault signal on the SRP pin.

6.1 Over Voltage Clamping on OUTput

The BTF3050TE is equipped with a voltage clamp circuitry that keeps the drain-source voltage V_{DS} at a certain level $V_{OUT(CLAMP)}$. The over voltage clamping is overruling the other protection functions. Power dissipation has to be limited to keep the maximum allowed junction temperature.

This function is also used in terms of inductive clamping. Please see also **“Output Clamping” on Page 14** for more details.

6.2 Thermal Protection with Latched Fault Signal

The device is protected against over temperature due to overload and/or bad cooling conditions by an integrated temperature sensor. The thermal protection is available if the device is active. .

The device incorporates an absolute ($T_{J(SD)}$) and a dynamic temperature limitation ($\Delta T_{J(SW)}$). Triggering one of them will cause the output to switch off.

The switch off will be done with the fastest possible slew rate. The BTF3050TE has a thermal-restart function. If input (IN) is still high the device will turn on again after the junction temperature has dropped below the thermal hysteresis.

In case of detected over temperature the fault signal will be set and the SRP pin will be internally pulled up to V_{DD}. This state is latched independent on the IN signal, providing a stable fault signal to be read out by a micro controller. The latched fault signal needs to be reset by low signal ($V_{SRP} < V_{SRP(RESET)\_MIN}$) at the SRP pin, provided that the junction temperature has decreased at least below the thermal hysteresis in the meantime. To reliably reset the latch the SRP pin needs to be pulled down with a minimum length of t_{RESET}.

As long as the fault signal is set and the SRP-pin is not shorted to GND a fast default slew rate adjustment (like for R_{SRP} = 5.8kΩ) will be applied to the device.

If the latched fault signal is not reset, the device logic stays active (also if IN = low) not entering the quiescent current mode and therefore reaching upper limits of normal supply current I_{DD}.

Please see **“Diagnostics” on Page 22** for details on the feedback and reset function.

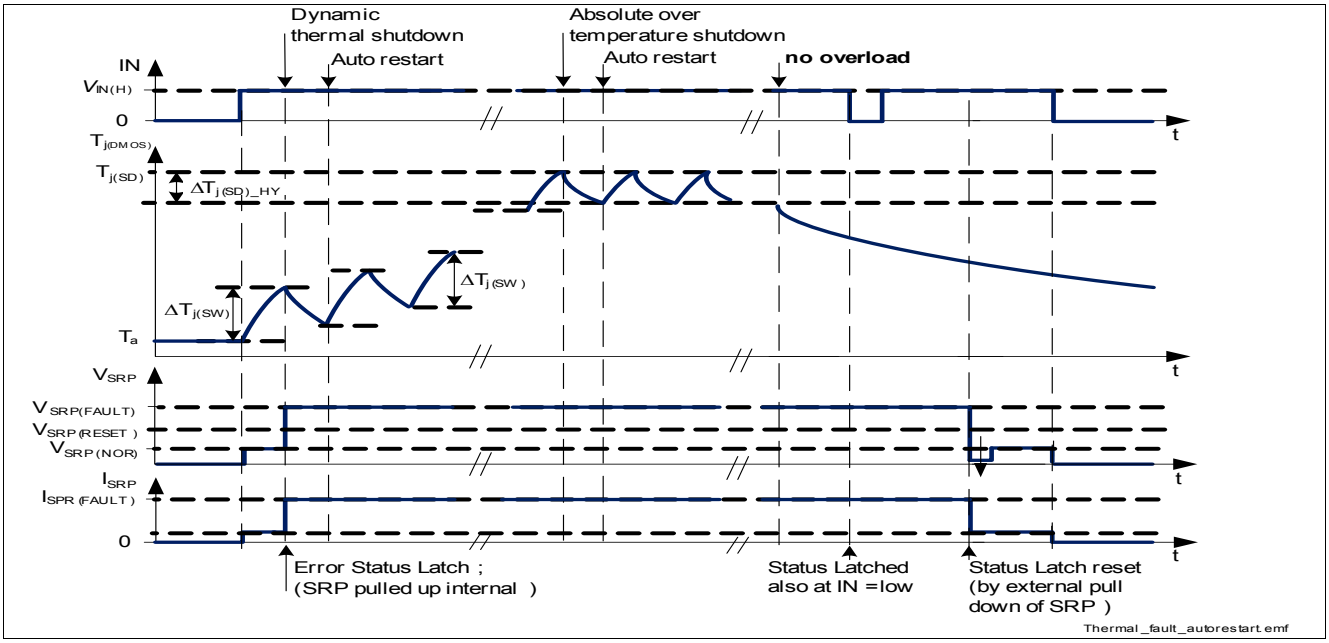


Figure 15 Thermal protective switch OFF scenario for case of overload or short circuit

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant.

6.3 Overcurrent Limitation / Short Circuit Behavior

This device is providing a smart overcurrent limitation which provides protection against short circuit conditions while allowing also load inrush currents higher than the current limitation level. To achieve this the device has a current limitation level $I_{L(LIM)}$ which is triggered by a higher trigger level $I_{L(LIM)\_TRIGGER}$.

The condition short circuit is an overload condition to the device.

If the load current I_L reaches the current limitation trigger level $I_{L(LIM)\_TRIGGER}$ the internal current limitation will be activated and the device limits the current to a lower value $I_{L(LIM)}$. The device starts heating up. When the thermal shutdown temperature $T_{J(SD)}$ is reached, the device turns off. The time from the beginning of current limitation until the over temperature switch off depends strongly on the cooling conditions.

If input is still high the device will turn on again after the measured temperature has dropped below the thermal hysteresis. The current limitation trigger is a latched signal. It will be only reset by input (IN) pin low and resetting the fault latch (SRP-pin = low (below reset threshold)) at the same time. This means if the input stays high all the time during short circuit the current will be limited to $I_{L(LIM)}$ the following pulses (during thermal restart). It also means that the output current is limited to the current limitation level $I_{L(LIM)}$ until the current limitation trigger is not reset.

Figure 16 shows this behavior.

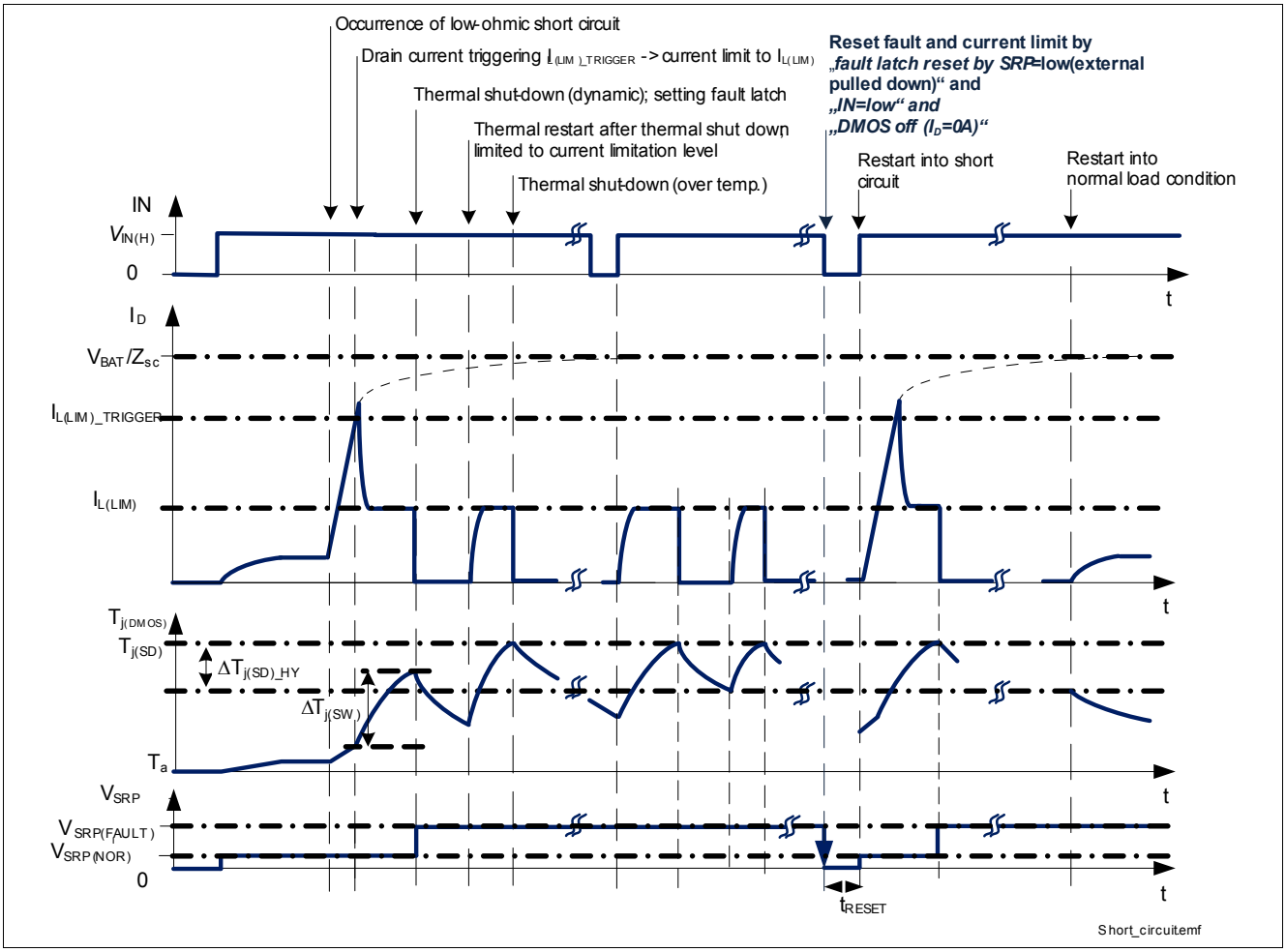


Figure 16 Short circuit protection via current limitation and thermal switch off , with latched fault signal on SRP (valid for R_{SRP} = 5...70 kOhm)

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant.

Behavior with overload current below current limitation trigger level

The lower current limitation level $I_{L(LIM)}$ will be also triggered by an thermal shutdown. This could be the case in terms of overload with a current still below the overcurrent limitation trigger level ($I_L < I_{L(LIM)\_TRIGGER}$).

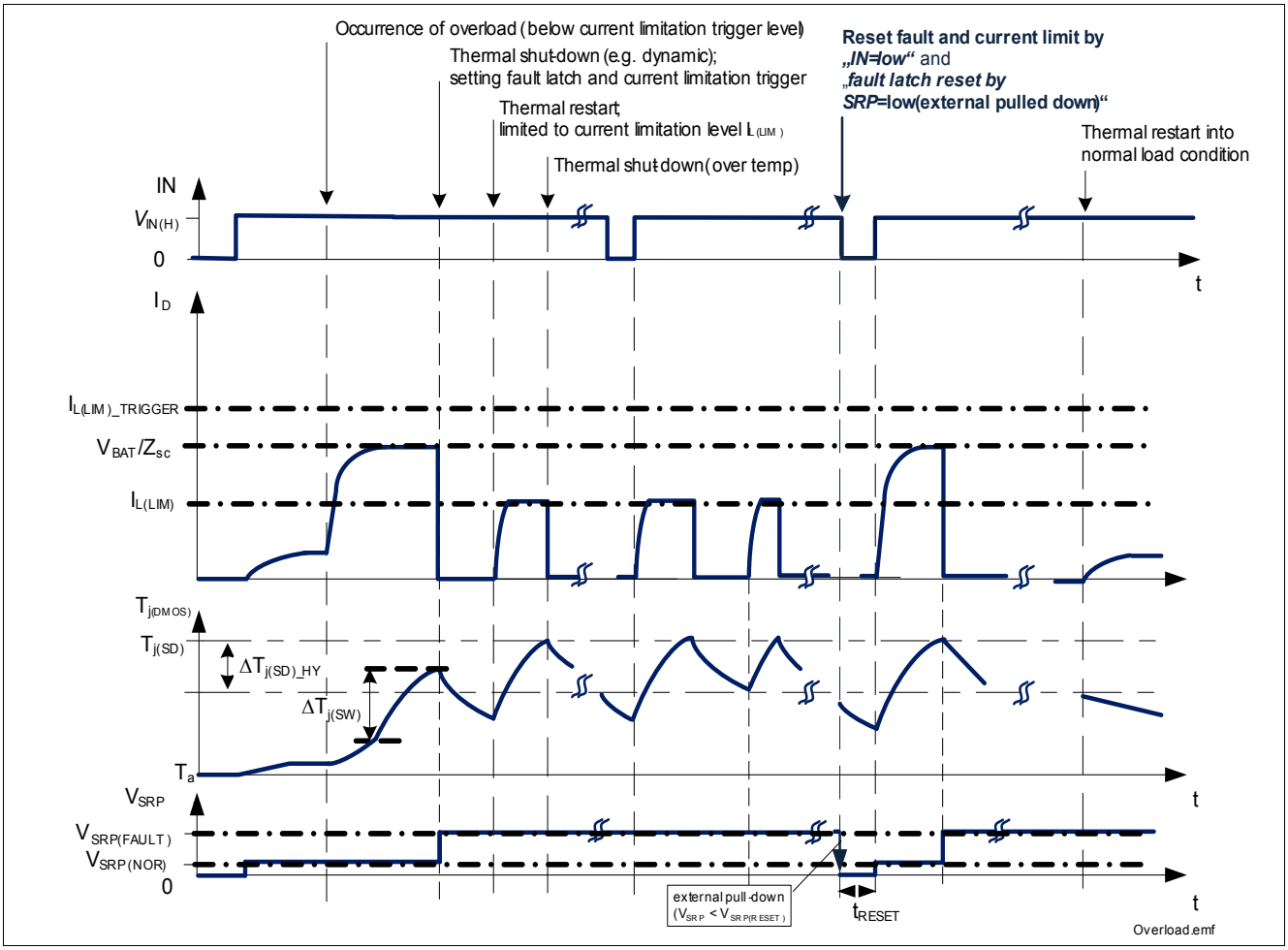


Figure 17 Example of overload behavior with thermal shutdown

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant.

6.4 Characteristics

Figure 18 Please see **“Protection” on Page 27** for electrical characteristic table.

7 Diagnostics

The BTF3050TE provides a latching digital fault feedback signal on the SRP pin triggered by an over temperature shutdown.

Additionally the device features an adjustable slew rate via the SRP pin.

7.1 Functional Description of the SRP Pin

The BTF3050TE provides digital status information via the combined status and Slew-Rate-Preset pin (SRP). This pin has three modes of operation:

Normal operation mode (slew rate mode; low signal)

The pin is used to define the switching speed of the BTF3050TE.
A resistor to ground defines the strength of the gate driver stage used to switch the power DMOS. The SRP pin works as a controlled low voltage output with a normal voltage up to $V_{SRP(NOR)}$, driving from V_{DD} a current out of the SRP-pin through the slew rate adjustment resistor.
For details on this function please refer to **"Adjustable Swtiching Speed / Slew Rate" on Page 16**.

The voltage on the SRP pin in normal operation mode is $V_{SRP(NOR)}$, signaling a low signal to the micro controller.

Latched Feedback mode (internal pull-up to V_{DD}; high signal)

The pin is used to give an alarming feedback to the micro controller after an over temperature shut down.
The SRP pin is pulled to V_{DD} by an active internal pull-up source providing typical a current $I_{SRP(FAULT)}$, intend to signal a logic high to the micro controller. This mode stays active independent from the input pin state or internal restarts until it will be reset (see below).

During this mode the slew rate of the device is set to a fast "fault" mode slew rate (similar to the switching times at R_{SRP} = 5.8kΩ.)The latched fault/feedback mode and signal is available at slew rate resistors of 5kΩ < R_{SRP} < 70kΩ. (please see also **Figure 21 "Availability of latched fault/feedback mode in dependency of slew rate resistor R_{SRP}" on Page 23**)

Reset Latch (external pull-down)

The pin is used as an input pin to set the device back to normal mode and reset the fault latch.
To reset the device the voltage on the SRP pin needs to be forced below the reset threshold $V_{SRP(RESET)}$ by an external pull down (e.g. using the micro controller I/O as pull-down).
If the SRP pin will be pulled down below $V_{SRP(RESET)}$ for a minimum time of t_{RESET} the logic resets the feedback latch, provided that its temperature has decreased at least the thermal hysteresis $\Delta T_{j(SW)\_HYS}$ in the meantime.

If INput is pulled down as well the current limitation trigger level will be also reset (enabling high peak currents again).
Figure 19 is showing the simplified circuitry used.

As long as the latched fault signal is not reset, the device logic stays active (also if IN = low) not entering the quiescent current mode.

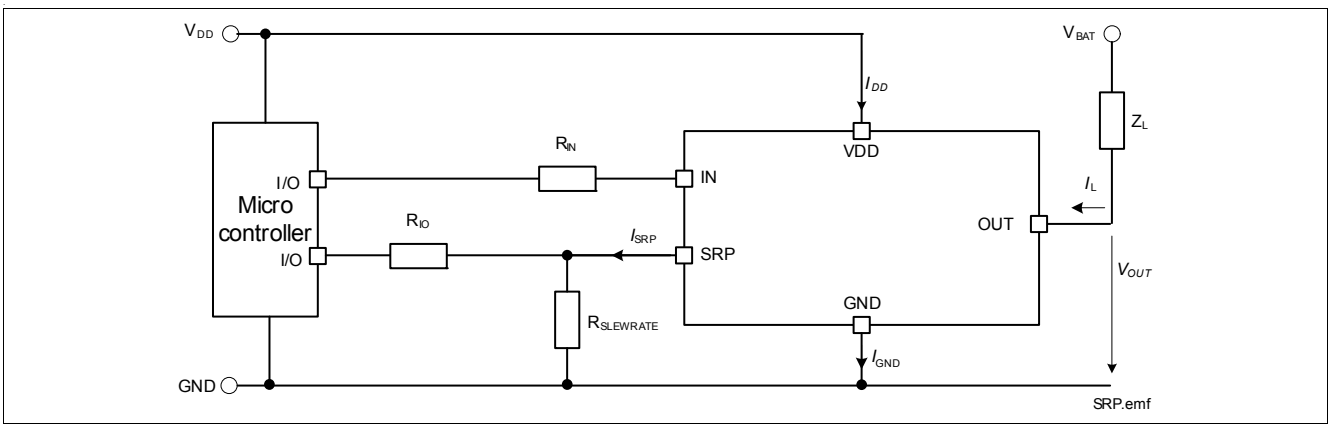


Figure 19 Feedback and control of BTF3050TE

Alternatively to a bidirectional pin, the micro controller can use a input and a output in parallel to drive the SRP pin.

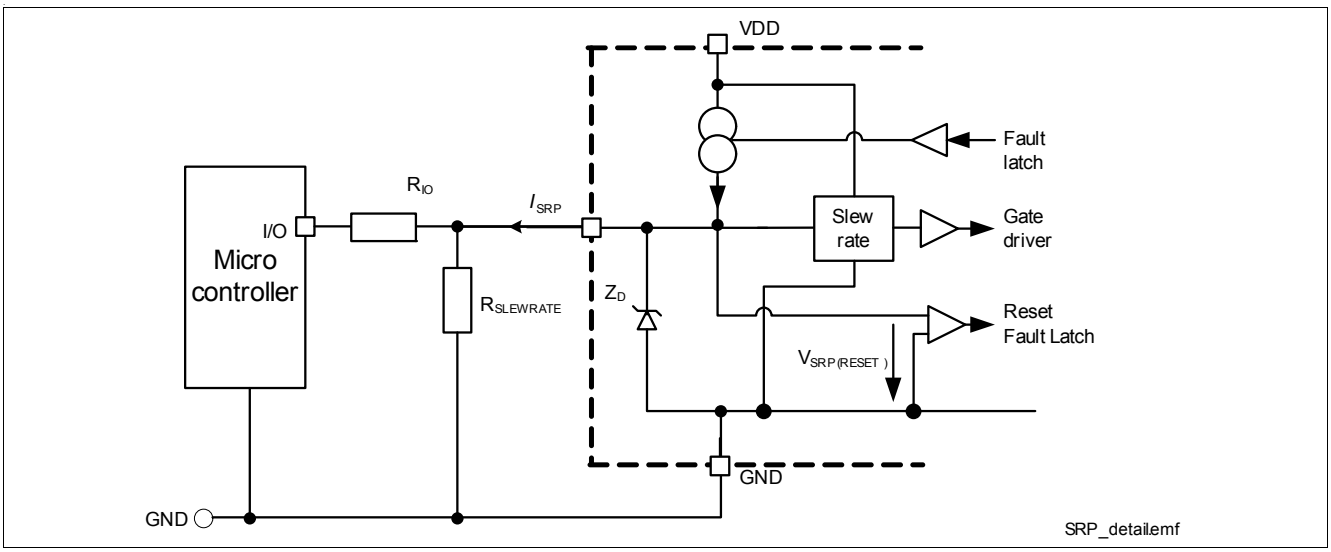


Figure 20 Simplified functional block diagram of SRP pin

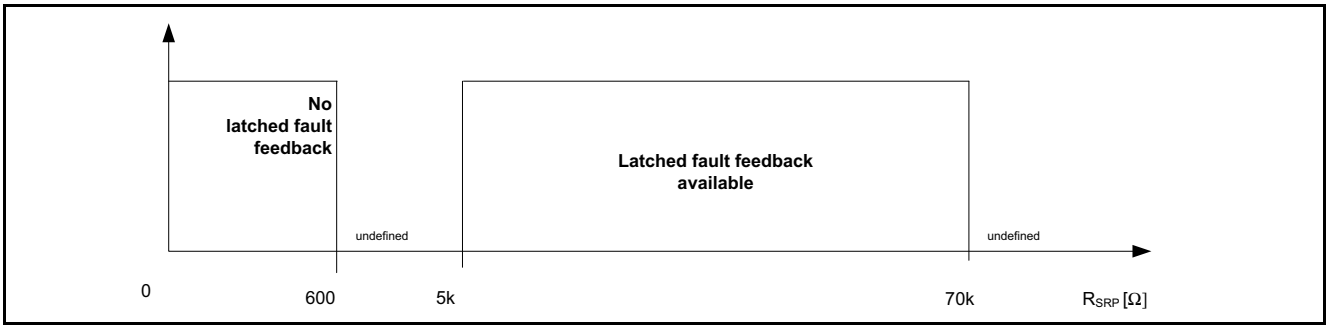


Figure 21 Availability of latched fault/feedback mode in dependency of slew rate resistor R_{SRP}

7.2 Characteristics

Please see **"Diagnostics" on Page 28** for electrical characteristic table.

8 Supply and Input Stage

8.1 Supply Circuit

The supply pin V_{DD} is protected against ESD pulses as shown in **Figure 22**.

The device supply is not internal regulated but directly taken from a external supply. Therefore a reverse polarity protected and buffered 5V (or 3.3V) voltage supply is required. To achieve a reasonable $R_{DS(ON)}$ and the specified switching speed, a 5V (or 3.3V) supply is required.

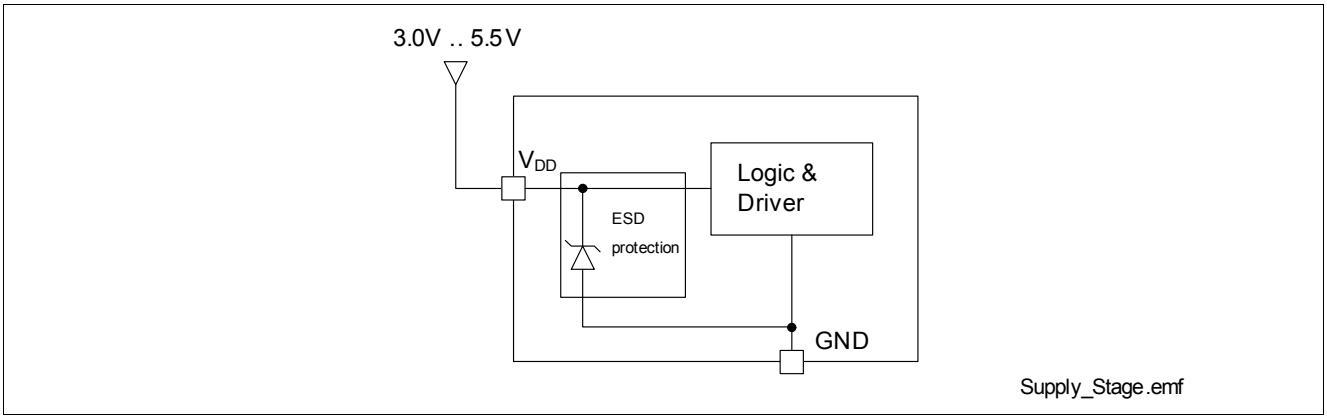


Figure 22 Supply Circuit

8.1.1 Undervoltage Shutdown

In order to ensure a stable and defined device behavior under all allowed conditions the supply voltage V_{DD} is monitored.

The output switches off, if the supply voltage V_{DD} drops below the switch-off threshold $V_{DD(TH)}$. In this case also all latches will be reset. The device functions are only given for supply voltages above the supply voltage threshold $V_{DD(TH)}$. There is no failure feedback ensured for $V_{DD} < V_{DD(TH)}$.

8.2 Input Circuit

Figure 23 shows the input circuit of the BTF3050TE. Due to an internal pull-down it is ensured that the device switches off in case of open input pin. A Zener structure protects the input circuit against ESD pulses. As the BTF3050TE has a supply pin, the $R_{DS(ON)}$ of the power MOS is independent of the voltage on the IN pin (assumed V_{DD} is sufficient).

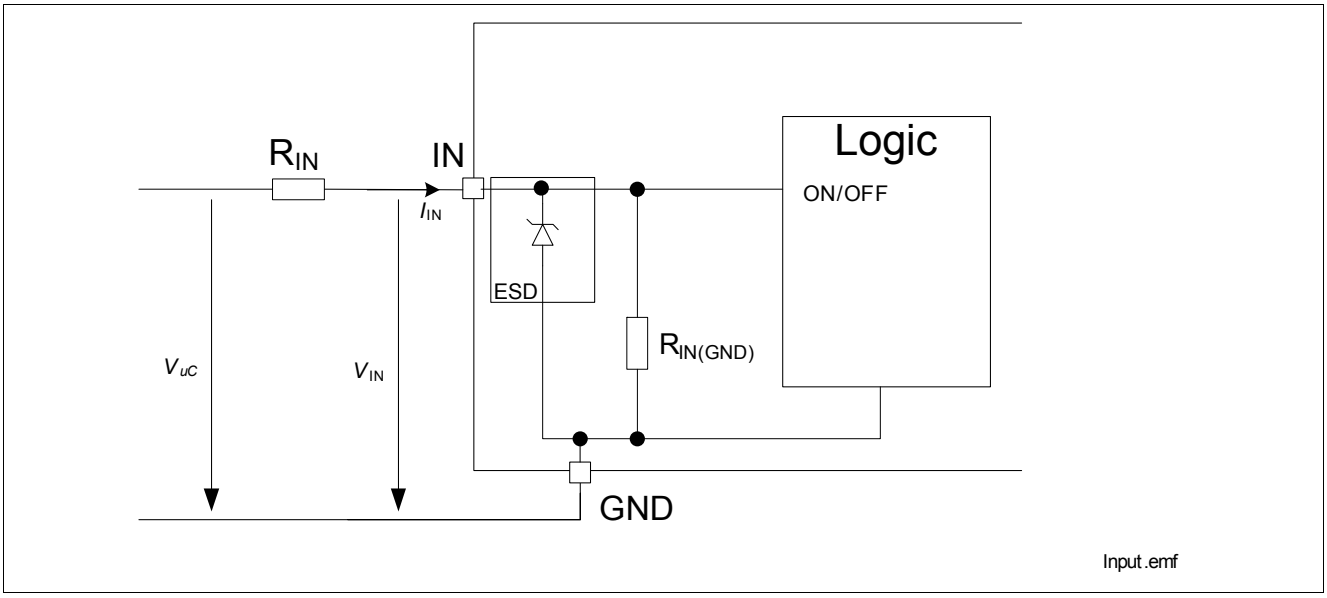


Figure 23 Simplified input circuitry

8.3 Characteristics

Please see **"Supply and Input Stage" on Page 30** for electrical characteristic table.