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Never stop thinking

Speed PROFET™

BTF50060-1TEA

Smart High-Side Power Switch, One Channel
High PWM Frequencies

Datasheet

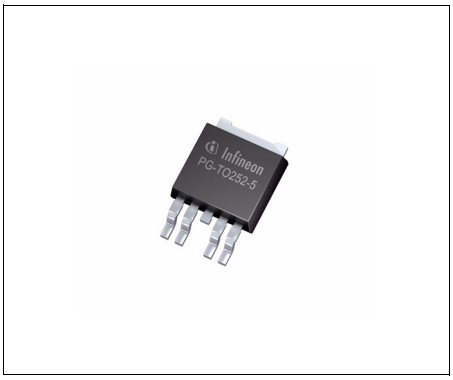
Rev. 1.2, 2011-09-01

Automotive

Smart High-Side Power Switch, One Channel High PWM Frequencies **BTF50060-1TEA**

AEC Qualified RoHS

1 Overview



PG-TO252-5-11

Application

- Driving all types of resistive, inductive and capacitive loads
- Most suitable for driving loads with PWM frequency from 0Hz (DC operation) up to 33kHz and above
- Drives valves, coils, and motors, with inrush currents up to 60 A

Features

- Optimized for PWM frequencies of approx. 25 kHz
- 3.3V and 5V compatible logic inputs
- Advanced analog load current sense signal
- Designed for easy current sense calibration
- Embedded diagnosis features (e.g. open load in ON and OFF state)
- Embedded protection functions (e.g. over current shutdown, over temperature shutdown)
- Infineon® INTELLIGENT LATCH
- Infineon® SMART CLAMPING
- Green Product (RoHS compliant)
- AEC Qualified

Description

Embedded in a PG-TO252-5-11 package, the BTF50060-1TEA is a 6mΩ single channel Smart High-Side Power Switch. It is based on Smart power chip on chip technology with a P-channel vertical power MOSFET, providing protective and diagnostic functions. It is specially designed to drive loads in the harsh automotive environment.

Table 1 Product Summary

Parameter	Symbol	Values
Range of typical PWM frequencies	f_{PWM}	0 Hz ... 33 kHz
Maximum On-state Resistance at T_j = 150 °C	$R_{DS(ON)\_150}$	12 mΩ
Nominal Supply Voltage Range for Operation	$V_{S(NOM)}$	6 V … 19 V
Nominal Load Current (DC operation)	$I_{L(NOM)}$	16.5 A
Typical Stand-by Current at T_j = 25 °C	$I_{S(OFF)}$	5 µA
Minimum short circuit current shutdown threshold	$I_{L(SC)}$	60 A
Maximum reverse battery voltage	$-V_{S(REV)}$	16 V

Type	Package	Marking
BTF50060-1TEA	PG-TO252-5-11	F50060A

Embedded Protection Functions

- Infineon® INTELLIGENT LATCH - resettable latch resulting from protective switch OFF
- Over current protection by short-circuit shutdown
- Overload protection by over-temperature shutdown
- Infineon® SMART CLAMPING

Embedded Diagnosis Functions

- Advanced analog load current sense signal with defined positive offset current; enabling load diagnosis like Open Load in ON state, overload
- Providing defined fault signal
- Open Load detection in OFF state
- Short-to-battery detection

2 Block Diagram

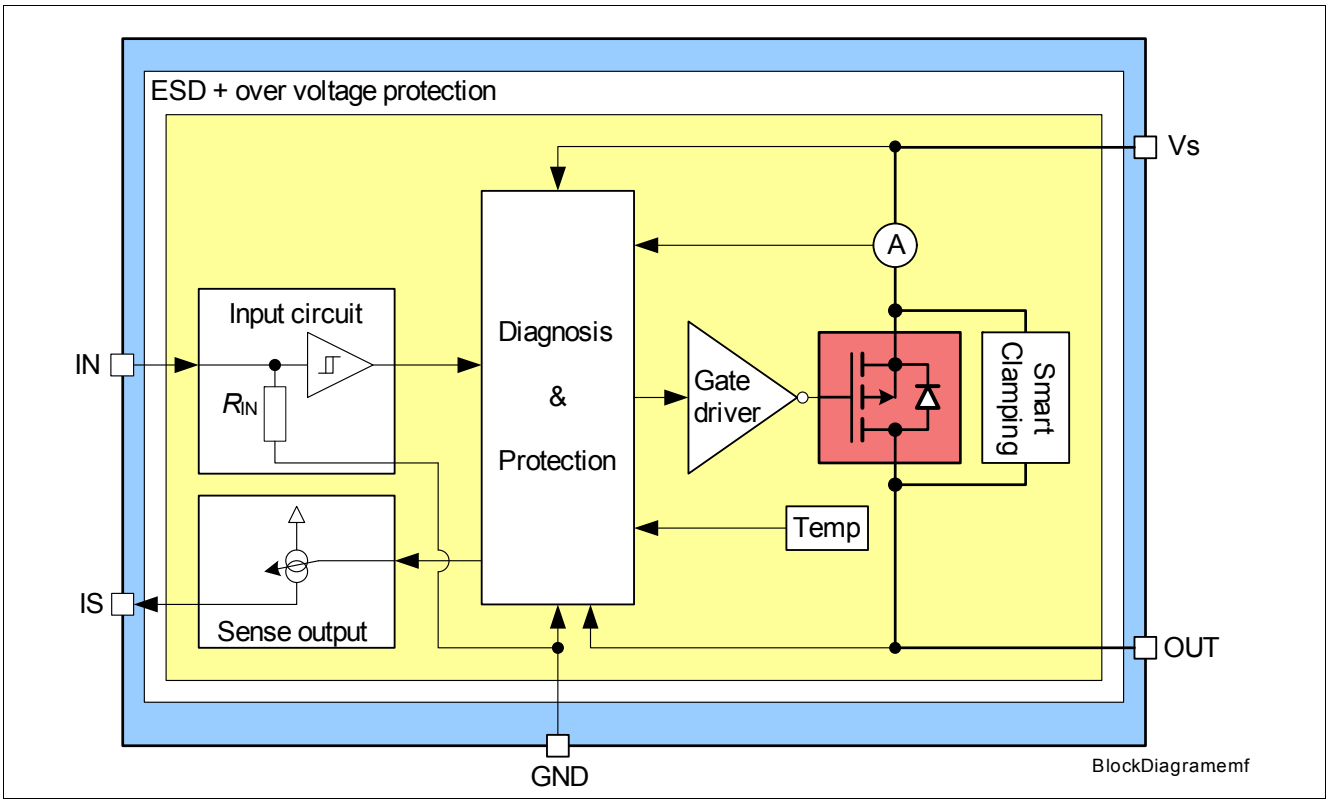


Figure 1 Block Diagram of BTF50060-1TEA

For a **Diagram of Diagnosis & Protection block**, please see **Figure 15**.

3 Pin Configuration

3.1 Pin Assignment

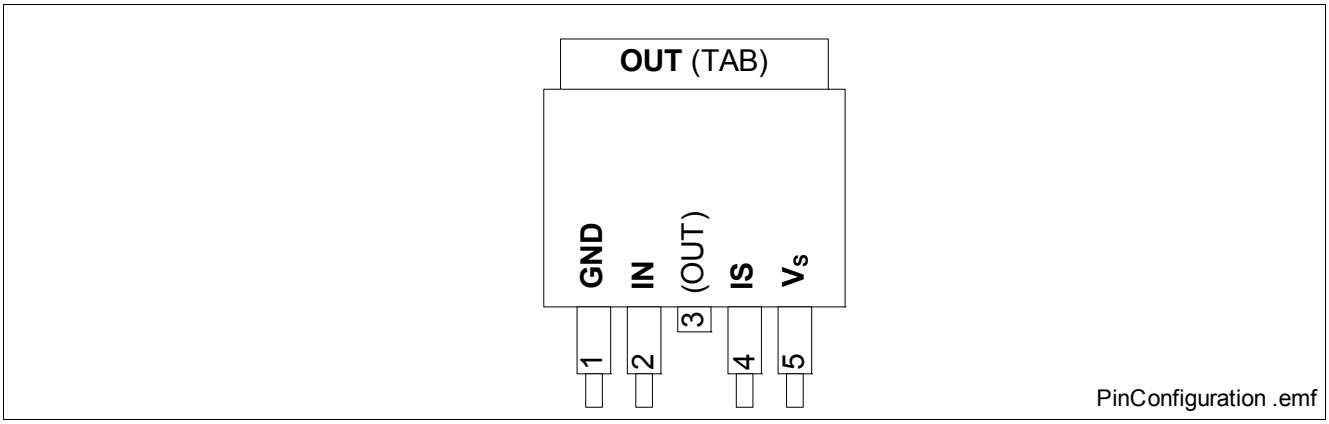


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**Ground;** Ground connection for control chip.
2	IN	**Input;** Digital 3.3 V and 5 V compatible logic input; activates power switch if set to HIGH level; Includes internal pull-down resistor R_{IN}.
Tab; 3[1)]	OUT	**Output;** Protected high side power output
4	IS	**Sense;** Provides analog sense current signal and defined fault signal.
5	Vs	**Supply Voltage;** Positive supply voltage for Logic and Power Stage[2)]

1) Tab and pin 3 are internally connected. Pin 3 is cut.

2) PCB traces have to be designed to withstand maximum current occuring in the application.

3.3 Definition of Terms

Figure 3 shows all terms used for currents and voltages in this data sheet, with associated convention for positive values.

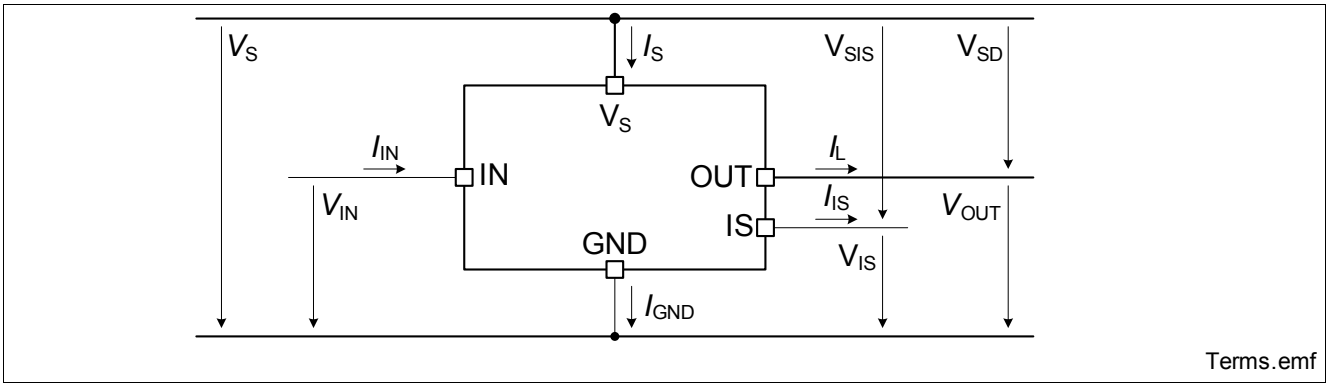


Figure 3 Definition of currents and voltages

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values		Unit	Note / Test Condition	Number
		Min.	Max.			
Supply voltages						
Supply Voltage	V_S	-0.3	28	V	–	P_4.1
Reverse Polarity Voltage on pin GND, IS	$\|-V_{S(REV)}\|$	0	16	V	[2)], [3)]	P_4.2
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0	28	V	[4)] R_{ECU} = 20mΩ, R_{Cable} = 6mΩ/m, L_{Cable} = 1µH/m, l = 0 or 5m, see **Chapter 5.3.1**	P_4.3
Supply voltage for load dump protection	$V_{S(LD)}$	–	45	V	R_I = 2 Ω [5)], R_L = 1.0 Ω, t_d = 400ms	P_4.4
Short Circuit Capability						
Short circuit cycle capability	n_{RSC1}	–	1 E6 (Grade A)	–	[4)6)]	P_4.21
IN + IS + GND pin						
Voltage at IN pin	V_{IN}	-0.3	6	V	–	P_4.5
Current through IN pin	I_{IN}	-2	2	mA	t < 2min	P_4.6
Voltage at IS pin	V_{IS}	-0.3	V_S	V	–	P_4.7
Current through IS pin	I_{IS}	-2	10	mA	–	P_4.8
Current through GND pin	I_{GND}	-2	10	mA	–	P_4.9
Power stage						
Load current	I_L	$-I_{L(SC)}$	$I_{L(SC)}$	A	–	P_4.10
Maximum energy dissipation for switching OFF an inductive load - single pulse	E_{AS}	–	280	mJ	V_S = 13.5V $I_{L(0)}$ = 20A $T_{j(0)}$ = 150°C See **Figure 4** and **Chapter 5.1.2**	P_4.11
Maximum energy dissipation for switching OFF an inductive load - repetitive pulse	E_{AR}	–	84	mJ	V_S = 13.5V $I_{L(0)}$ = 20A $T_{j(0)}$ = 105°C See **Figure 4** and **Chapter 5.1.2**	P_4.13
Temperatures						
Junction Temperature	T_j	-40	150	°C	–	P_4.14

Table 2 Absolute Maximum Ratings (cont'd)[1)]

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values		Unit	Note / Test Condition	Number
		Min.	Max.			
Dynamic temperature increase while switching	ΔT_j	–	60	K	–	P_4.15
Storage Temperature	T_{stg}	-55	150	°C	–	P_4.16
ESD Susceptibility						
ESD Resistivity HBM all Pins to GND	V_{ESD1}	-2	2	kV	HBM[7)]	P_4.17
ESD Resistivity HBM V_S vs. GND, V_S vs. OUT, OUT vs. GND	V_{ESD2}	-4	4	kV	HBM[7)]	P_4.18
ESD Resistivity CDM all pins to GND	V_{ESD3}	-500	500	V	CDM[8)]	P_4.19
ESD Resistivity CDM corner pins	V_{ESD4}	-750	750	V	CDM[8)]	P_4.20

1) Not subject to production test, specified by design.

2) In case of reverse polarity voltage on pin IN, I_{IN} needs to be limited (see P_4.6) by external resistor R_{INPUT}, see **Figure 45**.

3) In case of reverse polarity voltage, current through the OUT pin needs to be limited by external circuitry to prevent over heating (see P_4.14). Power dissipation during reverse polarity voltage can be calculated by **Equation (3)**. Please note, build-in protection functions are not available during reverse polarity condition.

4) In accordance to AEC Q100-012 and AEC Q101-006.

5) $V_{S(LD)}$ is set up without the DUT connected to the generator per ISO 7637-1.

6) Test aborted after 1 E6 cycles.

7) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001-2010

8) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

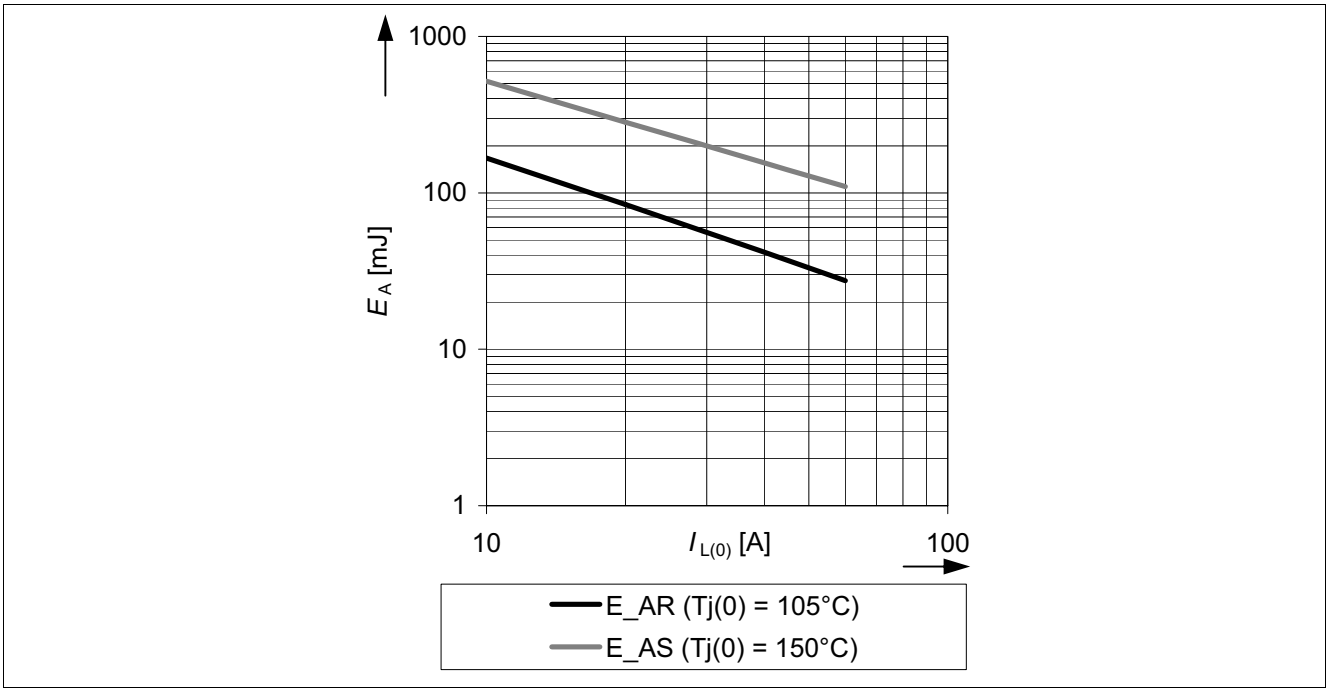


Figure 4 Maximum energy dissipation for switching OFF an inductive load E_A vs. load current

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values		Unit	Note / Test Condition	Number
		Min.	Max.			
Nominal Supply Voltage Range for Operation	$V_{S(NOM)}$	6	19	V	–	P_4.23
Extended Supply Voltage Range for Operation	$V_{S(EXT)}$	$V_{S(UV)ON}$	28	V	1)2)	P_4.24
Extended Supply Voltage Range for short dynamic undervoltage swings	$V_{S(DYN)}$	$V_{S(UV)OFF}$	$V_{S(UV)ON}$	V	1)2)3)	P_4.25
Junction Temperature	T_j	-40	150	°C	–	P_4.26

1) see **Chapter 5.5**, **Undervoltage turn ON voltage** and **Undervoltage turn OFF voltage**

2) In extended supply voltage range, the device is functional but electrical parameters are not specified.

3) Operation only if supply voltage was in range of $V_{S(EXT)}$ before undervoltage swing. Otherwise, device will stay OFF.

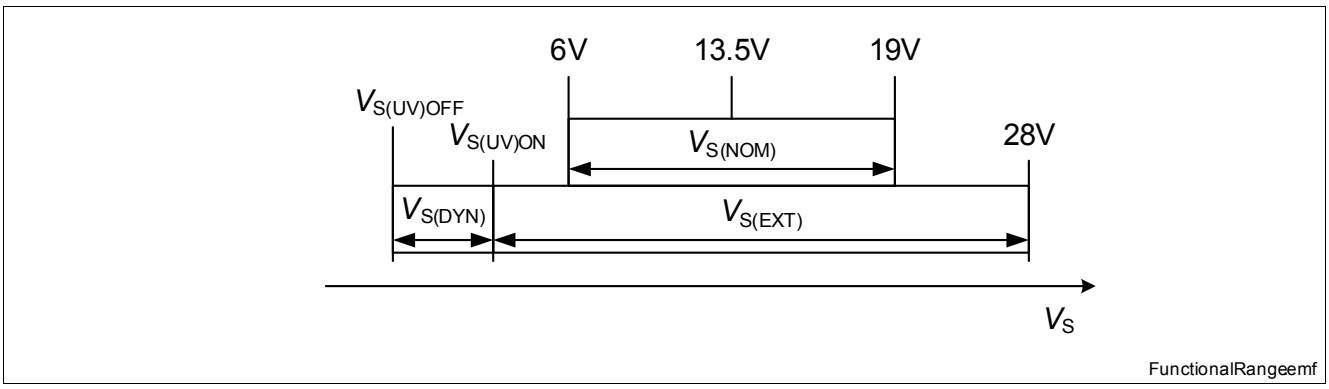


Figure 5 Overview of functional ranges

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance - Junction to Case	R_{thJC} [1]	–	1	1.1	K/W	–	P_4.27
Thermal Resistance - Junction to Ambient - 2s2p	R_{thJA_2s2p} [1]	–	22	–	K/W	[2]	P_4.29

1) Not subject to production test, specified by design.

2) Specified RthJA value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

Figure 6 and **Figure 7** are showing the typical thermal impedance of BTF50060-1TEA mounted according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s and 2s2p board. The product (chip + package) was simulated on a 76.4 × 114.3 × 1.5 mm board with 2 inner copper layers (2× 70µm Cu, 2× 35µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer. The PCB layer structure is shown in **Figure 8**. The PCB layout is shown in **Figure 9**.

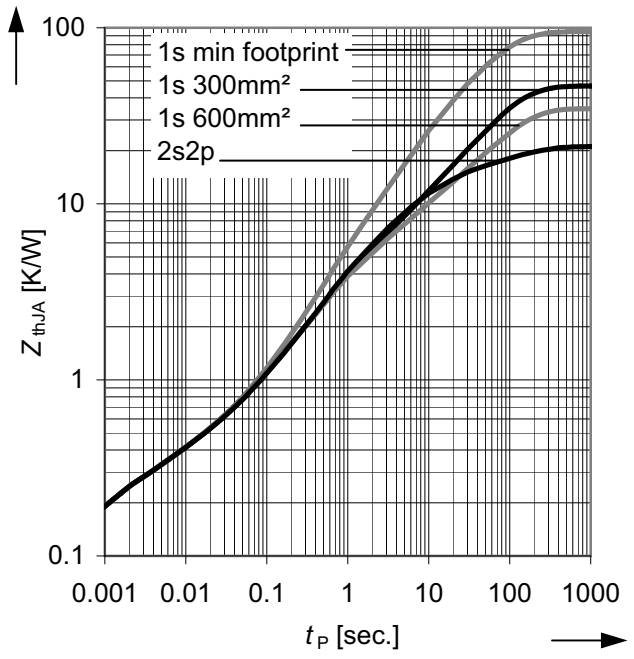


Figure 6 Typical Transient Thermal Impedance $Z_{th(JA)} = f(t_P)$ for different cooling areas

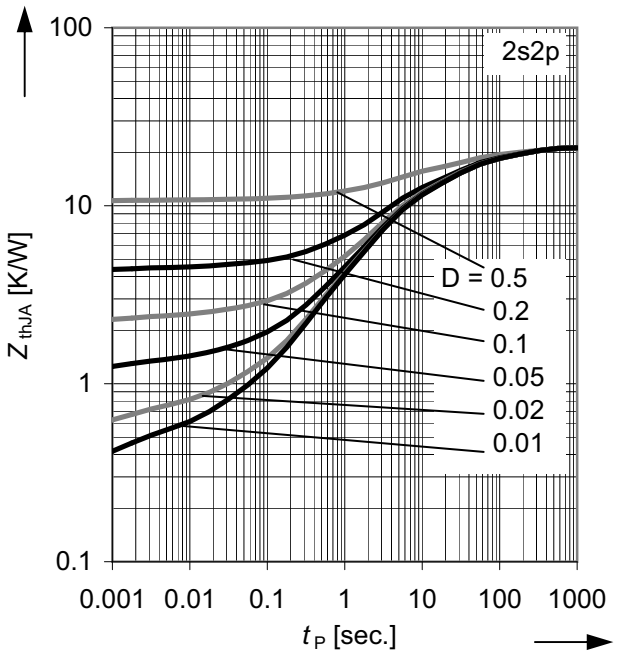


Figure 7 Typical Transient Thermal Impedance $Z_{th(JA)} = f(t_P)$ for PWM operation with duty cycles D = t / t_{period} on a 2s2p PCB

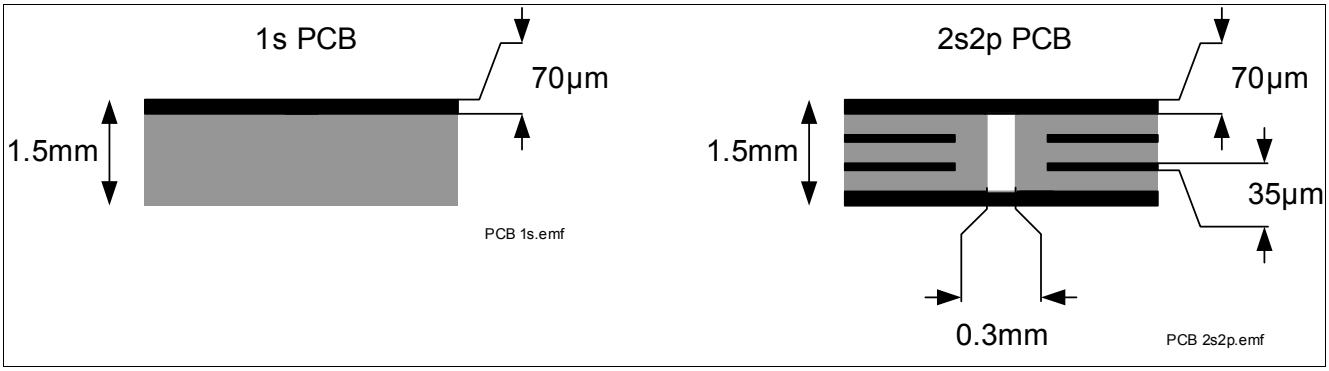


Figure 8 Cross section of 1s and 2s2p PCB used for Z_{thJA} simulation

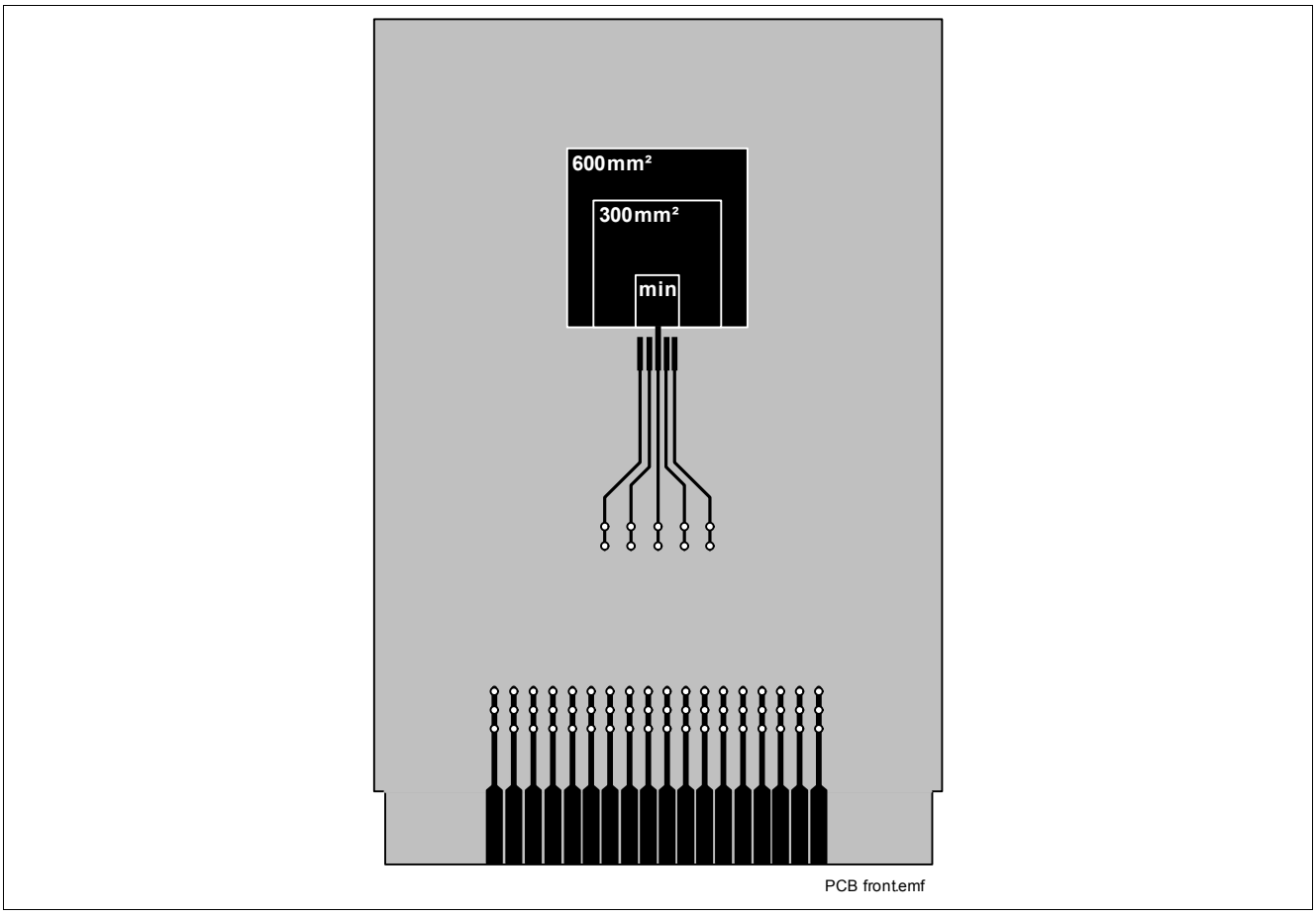


Figure 9 Front view of PCB layout used for Z_{thJA} simulation

5 Functional Description

5.1 Power Stage

The power stage is built by a P-channel vertical power MOSFET (DMOS). The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage V_S as well as the junction temperature T_j. **Figure 26** shows the dependencies for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 5.3.4**. A HIGH signal at the input pin (see **Chapter 5.2**) causes the power DMOS to switch ON. A LOW signal at the input pin causes the power DMOS to switch OFF.

5.1.1 Switching a Resisitve Load

Defined slew rates for turn ON and OFF as well as edge shaping support PWM'ing of the load while achieving lowest EMC emission at minimum switching losses. **Figure 10** shows the typical timing when switching a resistive load. Please note: if the devices logic is inactive, e.g. because the IN signal was LOW for $t > t_{RESET}$, the logic of the device needs a wake-up time of t_{wake} for turning the output ON in addition to the turn ON time t_{ON}. See also **Figure 11**.

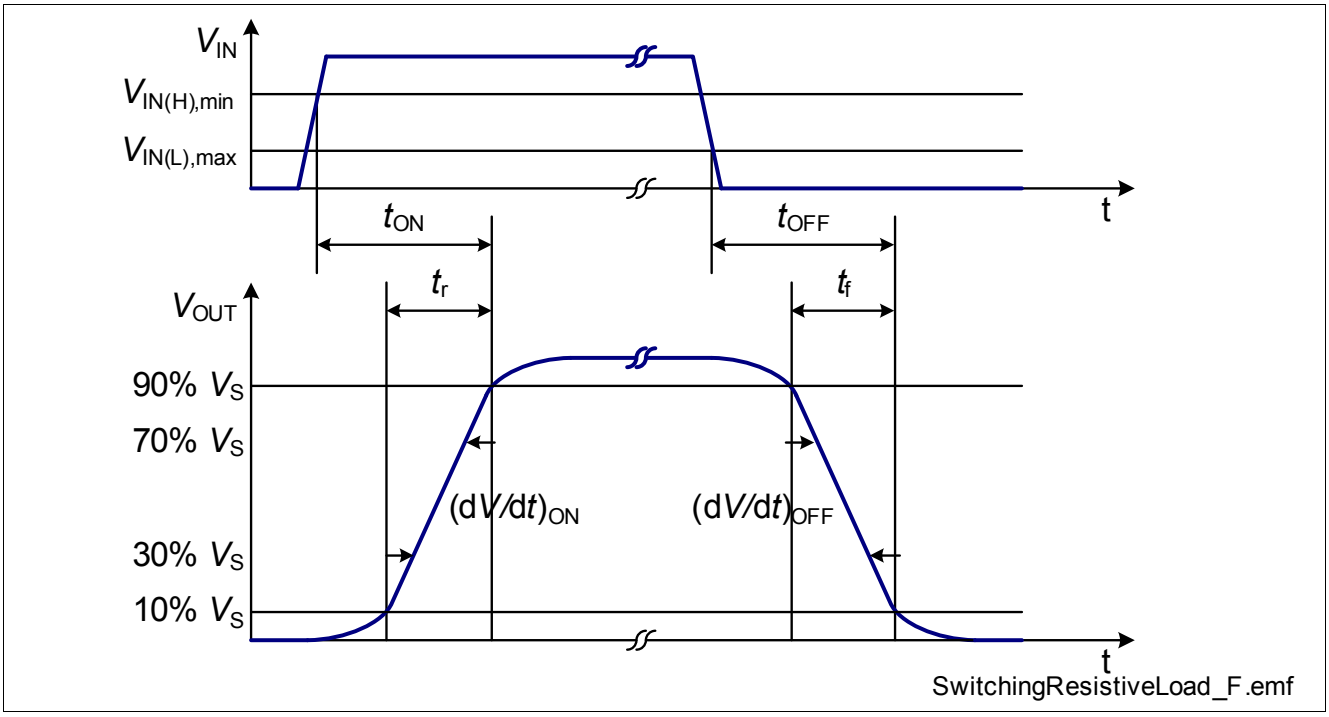


Figure 10 Switching a resistive load

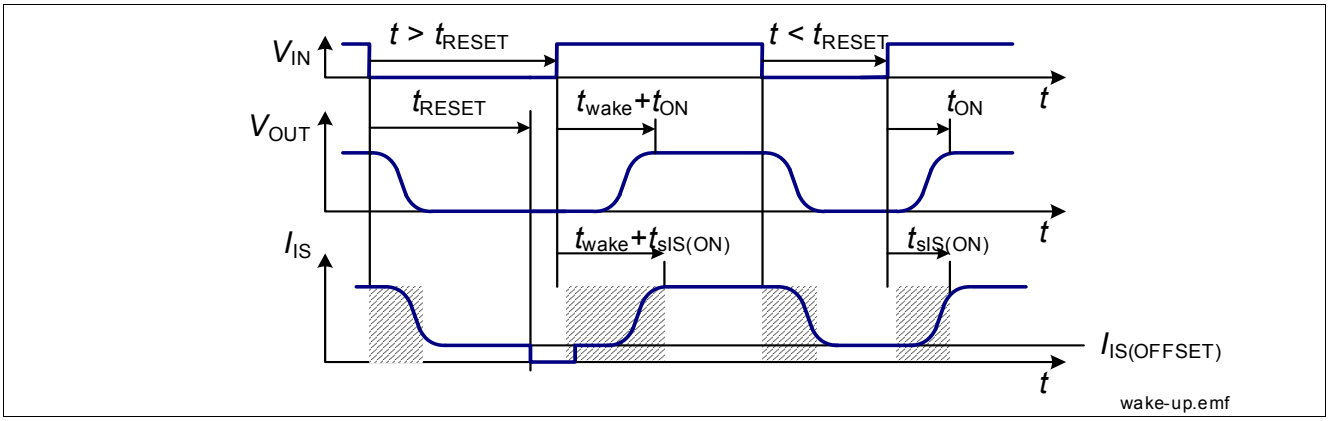


Figure 11 Wake up timing

5.1.2 Switching an Inductive Load - Infineon® SMART CLAMPING

When switching OFF inductive loads with no path for load current freewheeling available, the output voltage V_{OUT} drops below ground potential due to the involved inductance ($-di_L/dt = -v_L/L$; $-V_{OUT} \cong -V_L$). To prevent the destruction of the device due to high voltages, there is a voltage clamp mechanism implemented that keeps the negative output voltage at a certain level ($-V_{OUT}=V_S-V_{SD(CL)}$). Please refer to **Figure 1** and **Figure 12** for details.

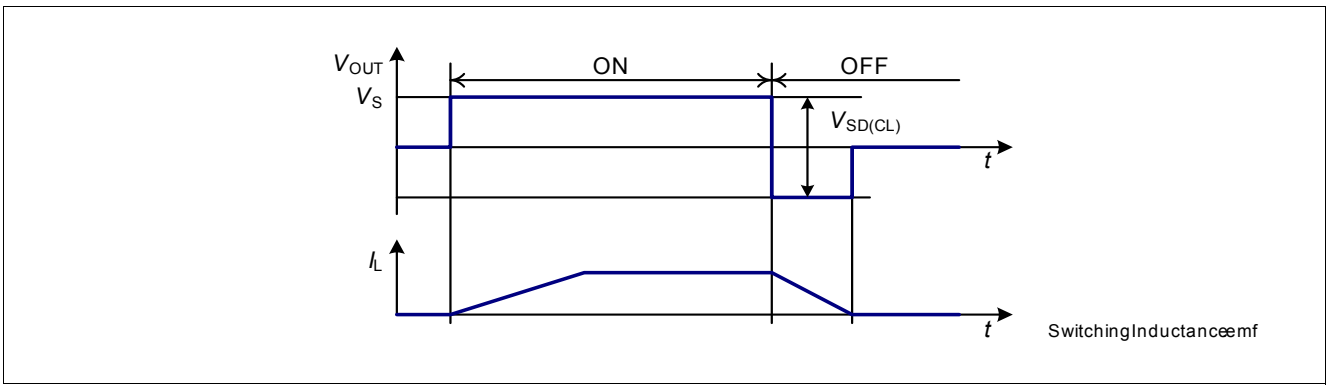


Figure 12 Switching an inductance

Nevertheless, the energy capability of the device is limited because the energy is converted into heat. That's why the maximum allowed load inductance is limited as well. Please see **Figure 4** for limitations of energy and load inductance.

For calculationg the demagnization energy, **Equation (1)** may be used:

$$E_A = V_{SD(CL)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{SD(CL)}}{R_L} \times \ln\left(1 + \frac{R_L \times I_L}{V_{SD(CL)} - V_S}\right) + I_L \right] \quad (1)$$

The equation can be simplified under the assumption of R_L = 0 Ω to:

$$E_A = \frac{1}{2} \times L \times I_L^2 \times \frac{V_{SD(CL)}}{V_{SD(CL)} - V_S} \quad (2)$$

The BTF50060-1TEA provides Infineon® SMART CLAMPING functionality. To optimize the energy capability for single and parallel operation, the clamp voltage $V_{SD(CL)}$ increases over the junction temperature T_j and load current I_L. **Figure 33** shows the dependency from T_j for the typical $V_{SD(CL)}$. Please refer also to **Figure 15**.

5.1.3 Switching a Capacitive Load

A capacitive load's dominant characteristic is it's inrush current. The BTF50060-1TEA can support inrush currents up to $I_{L(SC)}$. If the inrush current reaches $I_{L(SC)}$, the device may detect a short circuit condition and switches OFF. For a description of the short circuit protection mechanism, please refer to **Chapter 5.3.1**.

5.1.4 Inverse Load Current Operation

In case of a negative load current, e.g. caused by load operating as a generator, the device can not block a current flowing through the intrinsic body diode. See **Figure 13**. The power stage of the device can be switched ON or stays ON as long as V_{IN} = HIGH, reaching the same $R_{DS(ON)}$ as for positive load currents, if no fault condition is detected. In case of fault condition, the logic of the device will switch OFF the power stage and supply a fault signal $I_{IS(fault)}$. Since the device can not block a negative load current (even under fault conditions), it can not protect itself from overload condition. In the application, overload conditions, e.g. over temperature, must not occur during inverse load current operation.

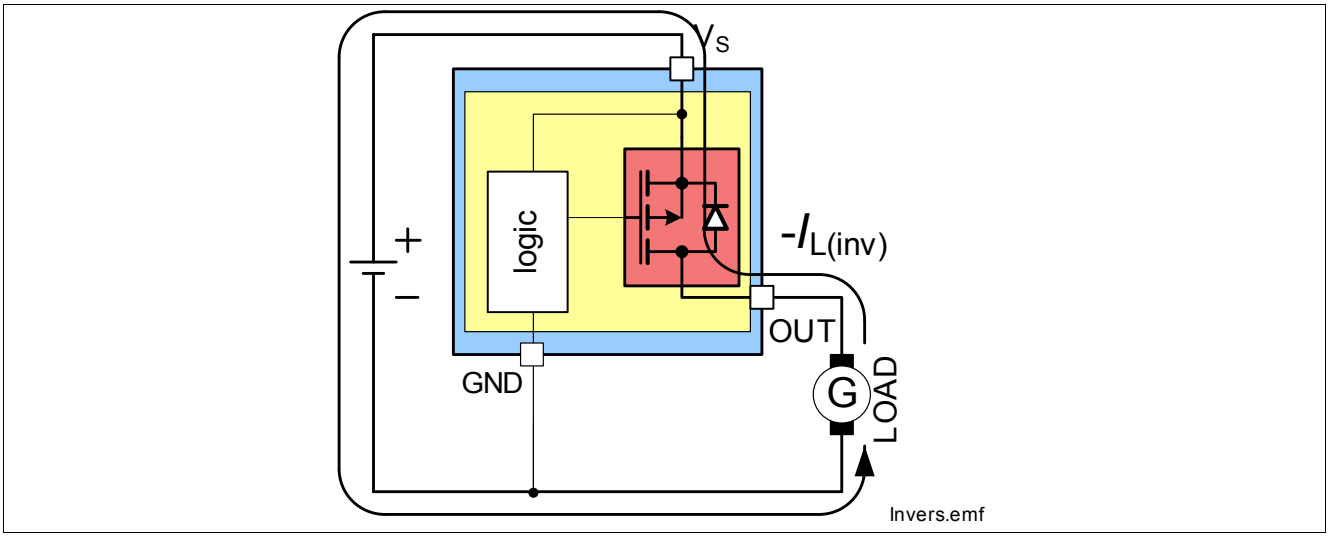


Figure 13 Inverse load current operation

5.2 Input Circuit

The input circuitry is compatible with 3.3 and 5V micro controllers. If V_{IN} is set to V_{IN} = $V_{IN(H)}$ (V_{IN} = HIGH), the device will turn ON. See **Figure 10** for the timings. If V_{IN} is set to V_{IN} = $V_{IN(L)}$ (V_{IN} = LOW), the power stage of the device will be turned OFF. The input circuitry has a hysteresis ΔV_{IN}. The input circuitry is compatible with PWM applications. **Figure 14** shows the electrical equivalent input circuitry. The logic of the BTF50060-1TEA stays active for a delay time t_{RESET} after the switch OFF signal.

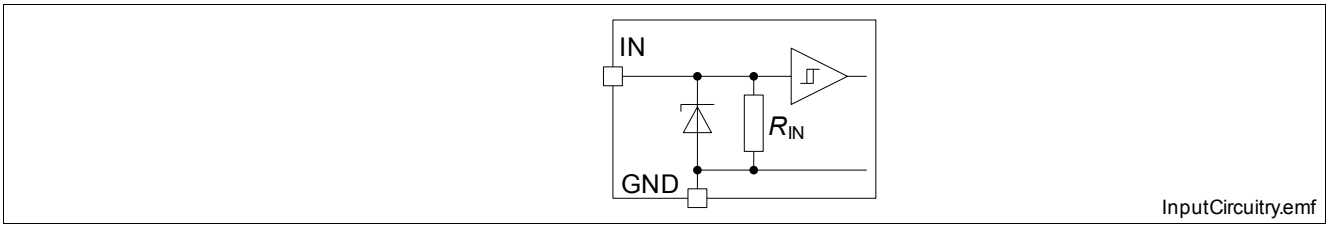


Figure 14 Input pin circuitry

Applying an input voltage of V_{IN} > 20V (absolute maximum ratings exceeded!) may force the BTF50060-1TEA to deactivate parts of the logic circuitry. This includes the undervoltage shutdown, the undervoltage restart delay, and the analog sense function. In this case, also the short circuit shutdown threshold $I_{L(SC)}$ is set to typically 50A, and

the latch reset time t_{RESET} is reduced to typically 200µs. To reset this behavior, set input voltage to V_{IN} = LOW for t>300µs.

5.3 Protection Functions

The BTF50060-1TEA provides embedded protective functions. Integrated protection functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

In case of overload, high inrush currents, or short circuit to ground, the BTF50060-1TEA offers several protection mechanisms. **Figure 15** describes the functionality of the diagnosis and protection block.

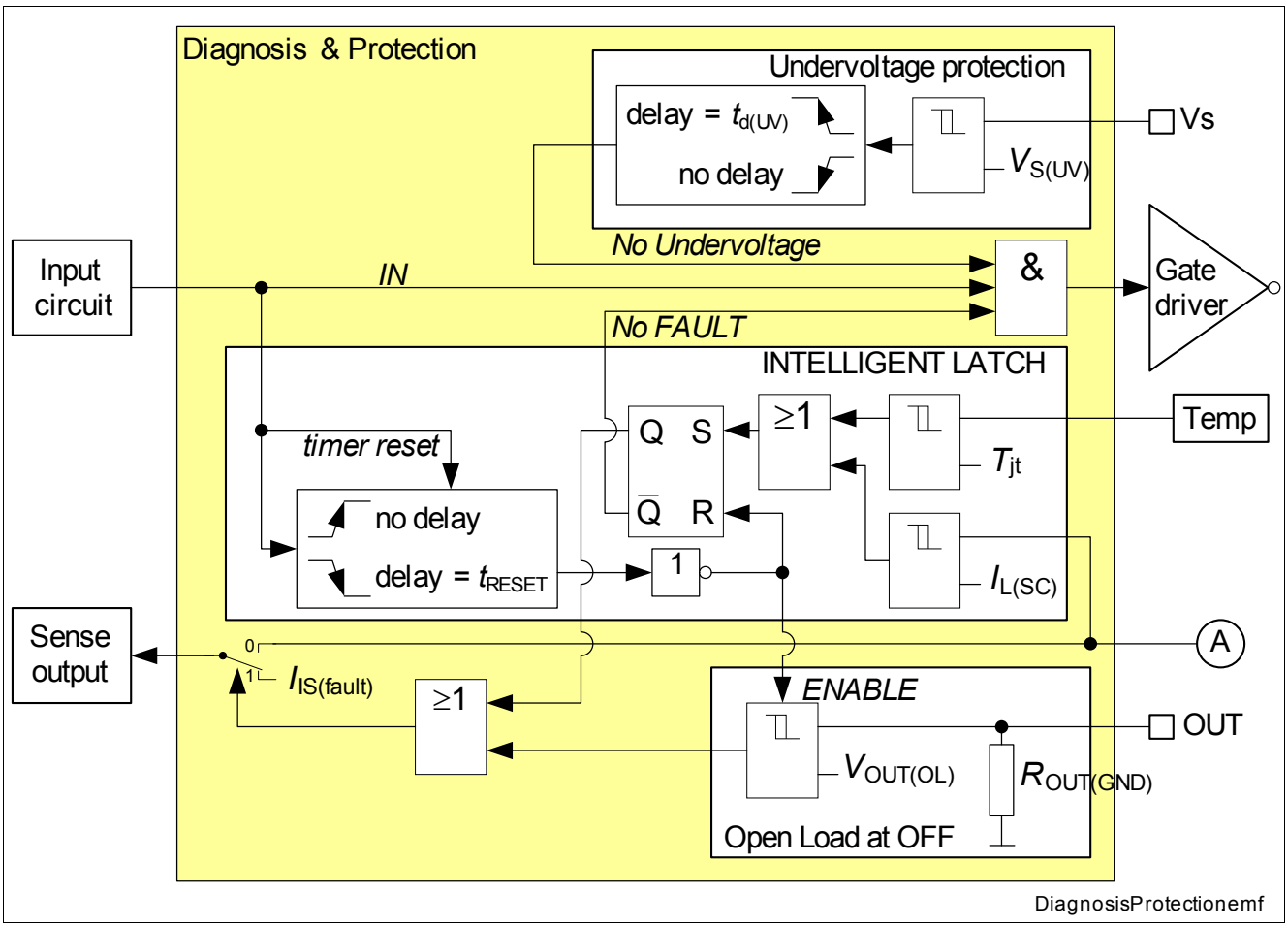


Figure 15 Diagram of Diagnosis & Protection block

5.3.1 Protection by Over Current Shutdown

The internal logic permanently monitors the load current I_L. In the event of a load current exceeding the short circuit shutdown threshold ($I_L > I_{L(SC)}$), the output will switch OFF with a latching behavior. During an over current shutdown, an overshooting $I_{L(SC)peak}$ may occur, depending on the short circuit impedances. For the case the device is in ON state while short circuit appears, the typical overshooting $I_{L(SC)peak}$ as a function of the steepness of the short circuit current dI_{SC}/dt, see **Chapter 6.2.3**.

For a detailed description of the latching behavior, please see **Chapter 5.3.3**.

At lower supply voltages the current tripping level $I_{L(SC)}$ will decrease depending on the supply voltage. At V_S = 4.7V, the current tripping level will be reduced to $I_{L(SC)LV}$. Please refer to **Figure 35** for typical current tripping level $I_{L(SC)}$ as a function of the supply voltage V_S.

5.3.2 Protection by Over Temperature Shutdown

The internal logic permanently monitors the junction temperature of the output stage. In the event of an over temperature ($T_j > T_{jt}$) the output will immediately switch OFF with a latching behavior, see **Chapter 5.3.3** for details.

5.3.3 Infineon® INTELLIGENT LATCH

The BTF50060-1TEA provides Infineon® INTELLIGENT LATCH to avoid permanent resetting of a protective, latched switch OFF caused by over current shutdown or over temperature shutdown) in PWM applications. To reset a latched protective switch OFF the fault has to be acknowledged by commanding the input LOW for a minimum duration of t_{reset}. See **Figure 16** for details.

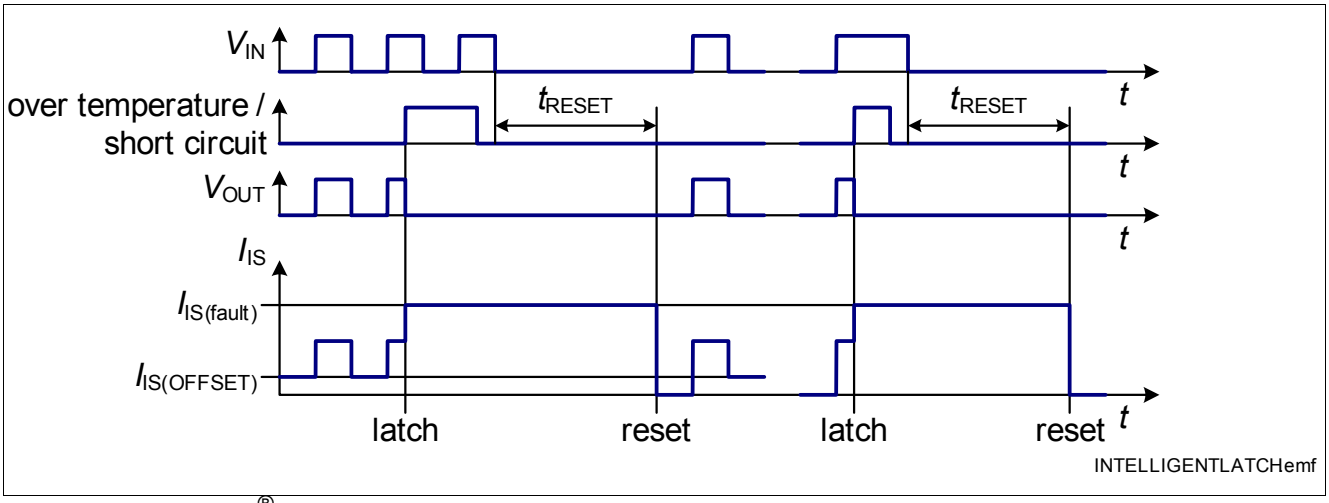


Figure 16 Infineon® INTELLIGENT LATCH - fault acknowledge and latch reset

5.3.4 Reverse Polarity Protection

Reverse polarity condition is the mix-up of the power supply connections of the entire application. This means, application GND connector is connected to positive supply voltage, while Vs pin is connected to negative supply voltage or ground potential. See **Figure 17** and **Figure 45**.

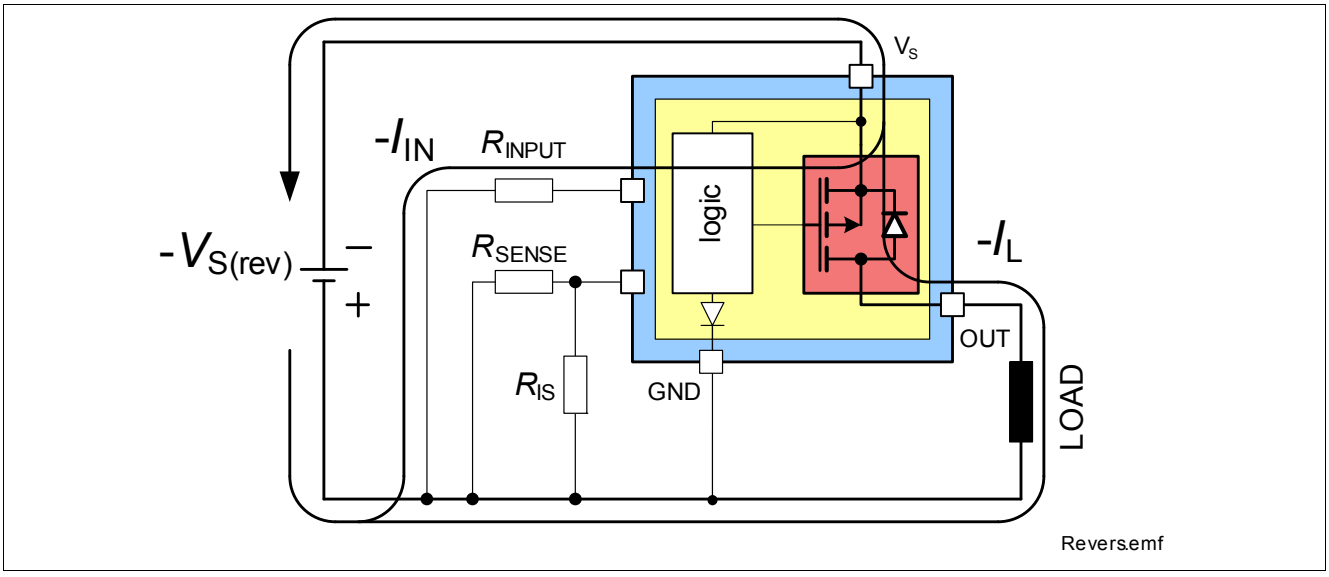


Figure 17 Reverse polarity condition

Under reverse polarity condition, the output stage can not block a current flow. It will conduct a load current via the intrinsic body diode. The current through the output stage has to be limited either by the load itself or by external circuitry, to avoid over heating of the power stage. Power losses in the power stage during reverse polarity condition can be calculated by **Equation (3)**:

$$P_{rev} = (-I_{L(rev)}) \times (-V_{SD(rev)}) \quad (3)$$

Additionally, the current into the logic pins has to be limited to the maximum current described in **Chapter 4.1** with an external resistors. **Figure 46** shows a typical application. Resistors R_{INPUT} and R_{SENSE} are used to limit the current in the logic of the device and in the ESD protection stage. The recommended value for R_{INPUT} = R_{SENSE} = 10kΩ. As long as $|-V_{S(rev)}|$ < 16V, the current through the GND pin of the device is blocked by an internal diode.

5.3.5 Protection during Loss of Ground

In case of loss of the module ground or device ground connection (GND pin) the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF (even if the load remains connected to ground), regardless if the input is driven HIGH or LOW. In case GND recovers the device may need a reset via the IN pin to return to normal operation.

5.3.6 Protection during Loss of Load or Loss of V_S Condition

In case of loss of load with charged primary inductances the maximum supply voltage has to be limited. It is recommended to use a Z-diode, a varistor (V_{Za} < 40V) or V_S clamping power switches with connected loads in parallel.

In case of loss of a charged inductive load, disturbances on pin OUT may require a reset on IN pin for the device to regain normal operation.

In case of loss of V_S connection with charged inductive loads, a current path with load current capability has to be provided, to demagnetize the charged inductances. It is recommended to use a diode, a Z-diode or a varistor (V_{Zb} < 16V, V_{ZL} + V_D < 16V).

For higher clamp voltages currents through all pins have to be limited according to the maximum ratings. Please see **Figure 18** and **Figure 19** for details.

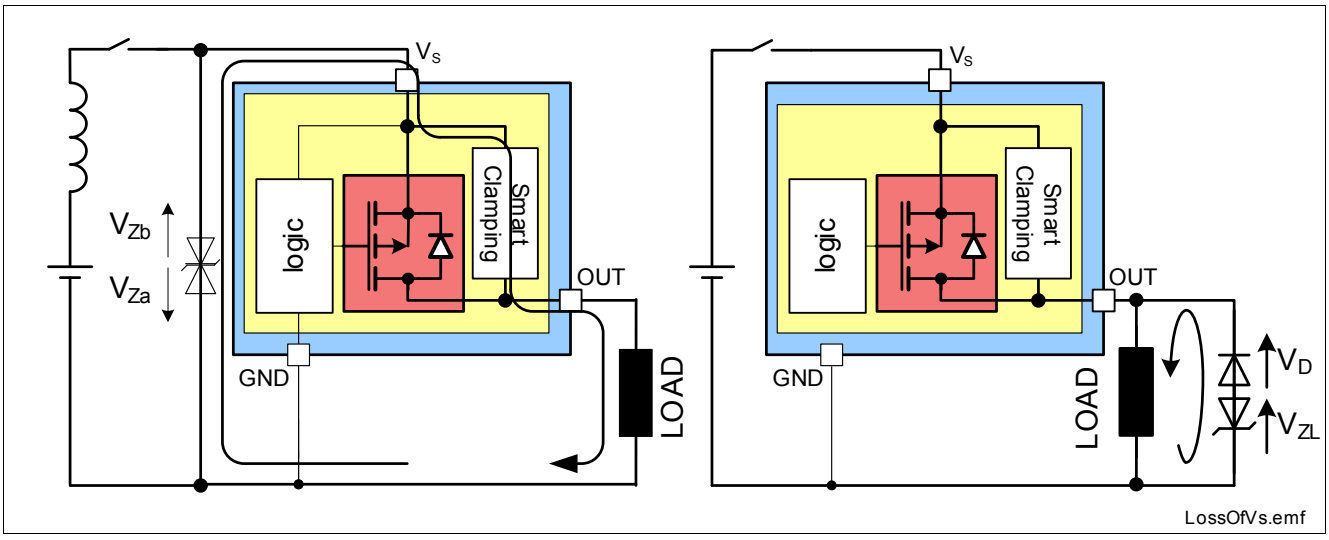


Figure 18 Loss of V_S

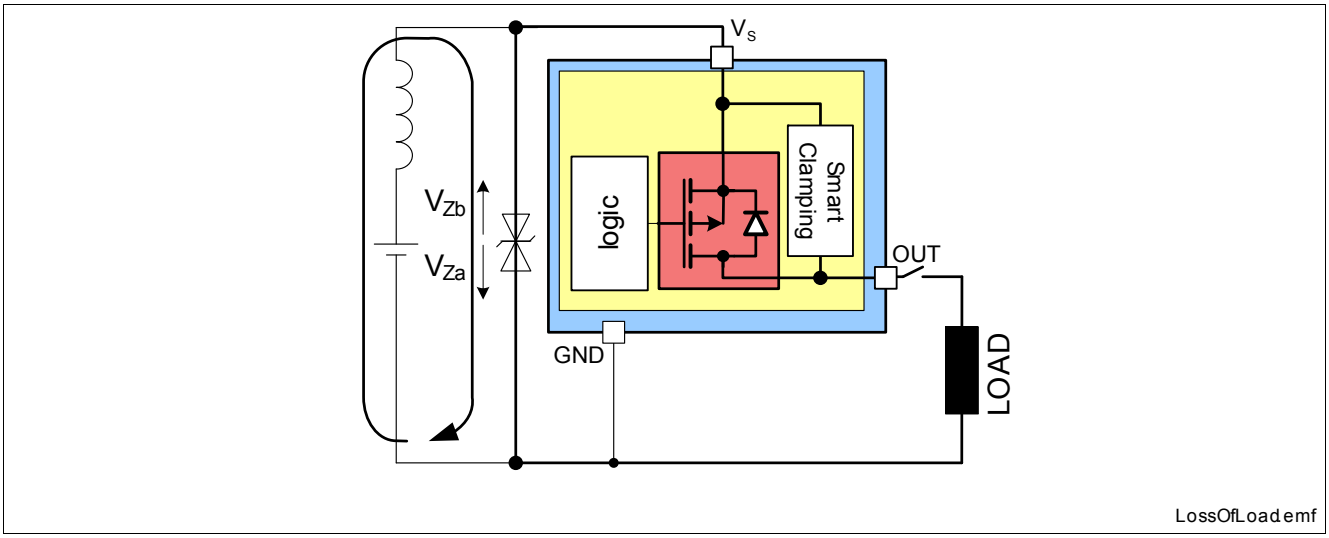


Figure 19 Loss of load

5.3.7 Protection during ESD or Over Voltage Condition

All logic pins have ESD protection. A dedicated clamp mechanism protects the logic IC against transient over voltages. See **Figure 20** for details.

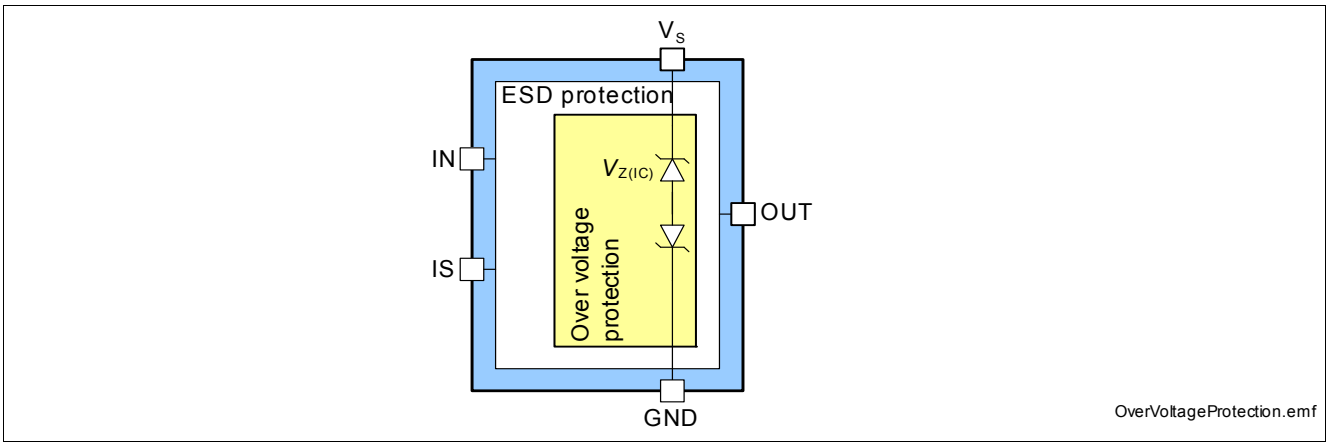


Figure 20 Over voltage protection

In the case (V_S > max $V_{S(SC)}$)&(V_S < $V_{SD(CL)}$), the output transistor is still operational and follows the input. Parameters are no longer warranted and lifetime is reduced compared to normal mode. This specially impacts the short circuit robustness, as well as the maximum energy E_{AS} the device can handle.

The BTF50060-1TEA provides Infineon® SMART CLAMPING functionality, which suppresses non nominal over voltages by actively clamping the over voltage across the power stage and the load. This is achieved by controlling the clamp voltage $V_{SD(CL)}$ depending on the junction temperature T_j and the load current I_L. See **Figure 15** for details. Please refer also to **Chapter 5.1.2**.

5.4 Diagnosis Functions

For diagnosis purpose, the BTF50060-1TEA provides an enhanced analog sense signal at the pin IS. For an overview of the diagnosis functions, you may have a look at **Figure 15** "**Diagram of Diagnosis & Protection block**".

5.4.1 Sense Output

The current sense output is a current source driving a signal I_{IS} proportional to the load current (see **Equation (5)**) as long as no "hard" failure mode occurs (short circuit to GND / over temperature) and $V_{SIS} = V_S - V_{IS} > 3V$. It is activated and deactivated by the input signal. Usually, in the application a pull-down resistor R_{IS} is connected between the current sense pin IS and GND pin. A typical value is $R_{IS} = 1.0\ k\Omega$. **Figure 46** shows a simplified application setup.

Table 5 is giving a quick reference for the logic / analog state of the IS pin during device operation.

In case a short circuit or an over temperature condition is detected, the sense output is supplying a fault signal $I_{IS(fault)}$. The fault signal is reset by an input signal being LOW for t > t_{RESET}. As long as an open load, short-to-V_S or inverse operation is detected while the device is in OFF state, the sense output also supplies the fault signal $I_{IS(fault)}$. The timings and logic of the IS pin are described in **Figure 21**. During output turning ON or OFF, the sense signal is invalid. Please note: if the devices logic is inactive, e.g. because the IN signal was LOW for $t > t_{RESET}$, the logic of the device needs a wake-up time of t_{wake} for activating the sense output in addition to the current sense settling time for turn ON $t_{sIS(ON)}$. See also **Figure 11**.

Table 5 Truth Table for Sense Signal

Operation mode	Input level	Output level	Sense output
Normal operation	**HIGH**[1]	$V_{OUT} = V_S - R_{DS(ON)} * I_L$	$I_{IS} = (I_L / k_{IS}) + I_{IS(OFFSET)}$
	LOW [2] for t < t_{RESET}	V_{OUT} ~ GND ($V_{OUT} < V_{OUT(OLL)}$)	$I_{IS} = I_{IS(OFFSET)}$
	LOW for t > t_{RESET}		Z[3] ($I_{IS} = I_{IS(LL)}$)
Inverse operation	**HIGH**	$V_{OUT} > V_S$	$I_{IS} \leq I_{IS(OFFSET)}$
	LOW for t < t_{RESET}		$I_{IS} = I_{IS(OFFSET)}$
	LOW for t > t_{RESET}		$I_{IS} = I_{IS(FAULT)}$
After short circuit to GND or over temperature detection	**HIGH** or **LOW for t < t_{RESET}**	V_{OUT} ~ GND	$I_{IS} = I_{IS(FAULT)}$
	LOW for t > t_{RESET}		Z ($I_{IS} = I_{IS(LL)}$)
Short circuit to V_S	**HIGH**	$V_{OUT} = V_S$	$I_{IS} \leq I_{IS(OFFSET)}$
	LOW for t < t_{RESET}		$I_{IS} = I_{IS(OFFSET)}$
	LOW for t > t_{RESET}		$I_{IS} = I_{IS(FAULT)}$
Open load	**HIGH**	$V_{OUT} = V_S$	$I_{IS} \leq I_{IS(OFFSET)}$
	LOW for t < t_{RESET}	$V_{OUT} > V_{OUT(OLH)}$[4]	$I_{IS} = I_{IS(OFFSET)}$
	LOW for t > t_{RESET}		$I_{IS} = I_{IS(FAULT)}$

1) HIGH: $V_{IN} = V_{IN(H)}$
2) LOW: $V_{IN} = V_{IN(L)}$
3) Z: High impedance
4) Can be achieved e.g. with external pull up resistor R_{OL}, see **Figure 46**.

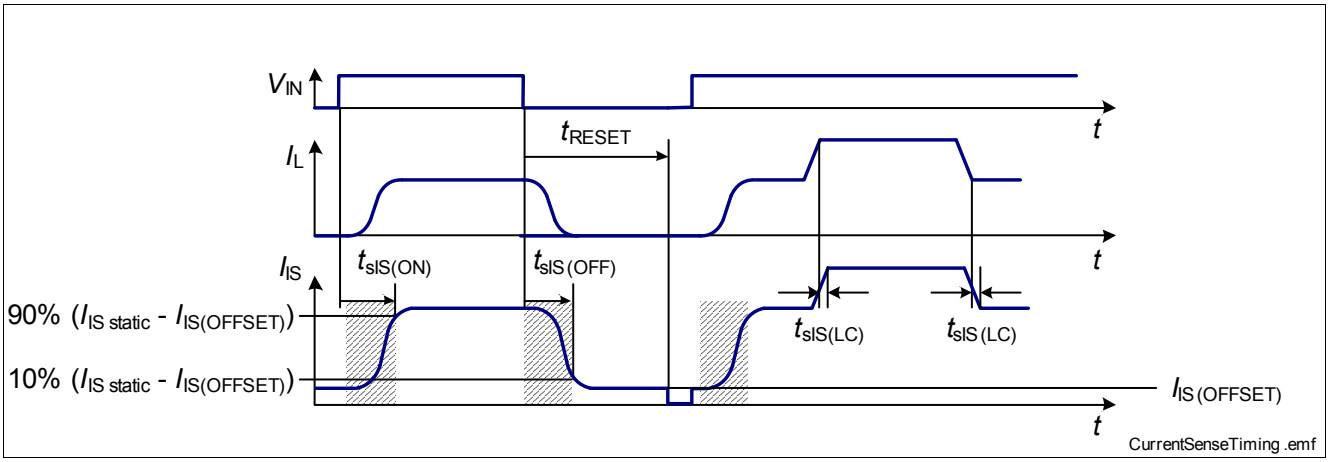


Figure 21 Sense output timing

Figure 22 shows the current sense as a function of the load current in the power DMOS. The curves represent the minimum and maximum values for the sense current, as well as the ideal sense current, assuming an ideal k_{IS} factor value as well as an ideal $I_{IS(OFFSET)}$.

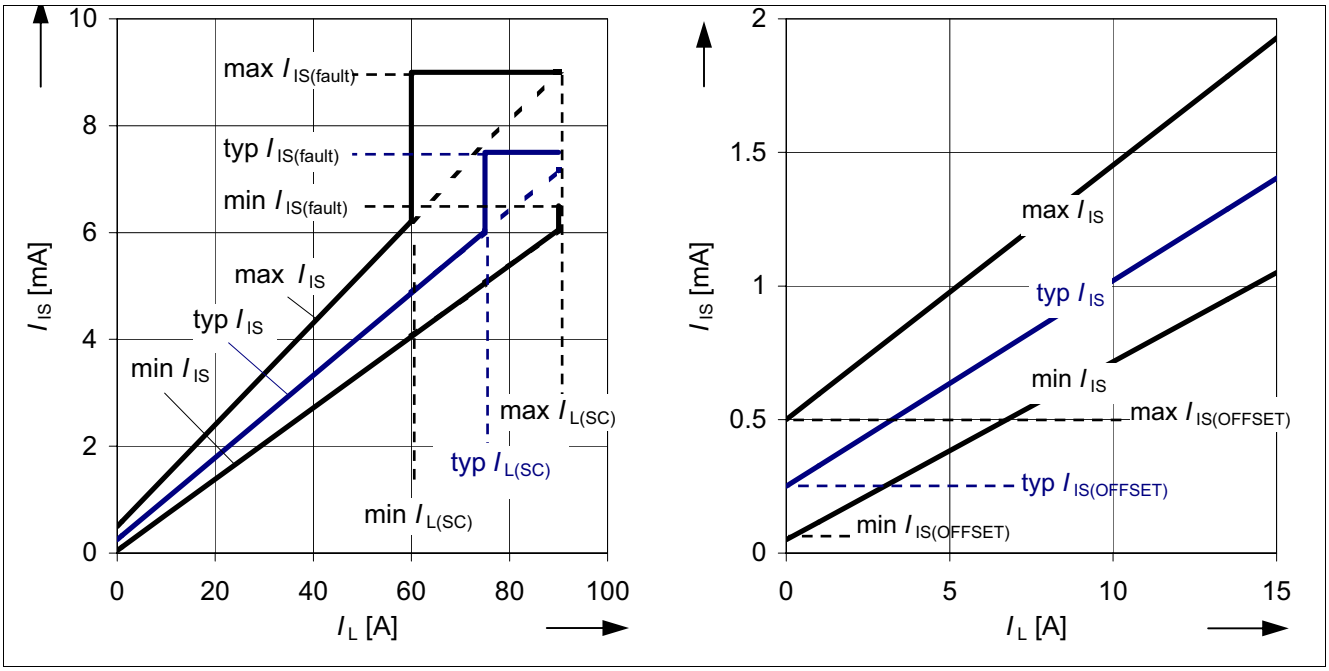


Figure 22 Sense current as a function of the load current (V_{SIS} > 3V)

The sense current can be calculated out of the load current by the following **Equation (4)**:

$$I_{IS} = \frac{1}{k_{IS}} \times I_L + I_{IS(OFFSET)} \quad (4)$$

Or, vice versa, the load current can be calculated out of the sense current by following **Equation (5)**:

$$I_L = k_{IS} \times (I_{IS} - I_{IS(OFFSET)}) \quad (5)$$

For definition of k_{IS}, the following **Equation (6)** is used:

$$k_{IS} = \frac{I_{L1} - I_{L2}}{I_{IS}(I_{L1}) - I_{IS}(I_{L2})} \quad (6)$$

I_{L1} and I_{L2} are two different load currents, $I_{IS(IL1)}$ and $I_{IS(IL2)}$ are the corresponding sense currents.

5.4.2 Enhancing Accuracy of the Sense Output by End of Line Calibration

For some applications it may be necessary to measure the load current with very high accuracy. To increase the device accuracy, different methods can be used, e.g. single point calibration or dual point calibration.

The variance of the sense current at a certain load current depends on the variance of the factor k_{IS} as well as on the variance of the offset current $I_{IS(OFFSET)}$. The temperature variance of the factor k_{IS} over the temperature range is described with the parameter $\Delta k_{IS,Temp}$.

$$\Delta k_{IS(Temp)} = \max[|k_{IS}(-40°C) - k_{IS}(25°C)|; |k_{IS}(150°C) - k_{IS}(25°C)|] \quad (7)$$

The variance of the sense current offset over the temperature range is defined as shown in **Equation (8)**:

$$\Delta I_{IS(OFFSET)} = \max[|I_{IS(OFFSET)}(-40°C) - I_{IS(OFFSET)}(25°C)|; |I_{IS(OFFSET)}(150°C) - I_{IS(OFFSET)}(25°C)|] \quad (8)$$

5.4.3 Short-to-Battery detection / Open Load Detection in OFF state

The BTF50060-1TEA provides open load diagnosis in OFF state. This is achieved by monitoring the OUT voltage. The open load at OFF diagnosis is activated if V_{IN} = LOW for t > t_{RESET}. An open load or short-to-battery is detected if $V_{OUT} > V_{OUT(OLH)}$. To provoke this condition during Open Load, it may be necessary to use an external pull up resistor R_{OL} (see **Figure 46**). In case of detecting a shorted load to battery, open load, or inverse operation in OFF state, the pin IS provides a defined fault current $I_{IS(fault)}$. If V_{OUT} drops below $V_{OUT(OLL)}$, or V_{IN} is set to HIGH, the fault signal is removed. **Figure 23** shows the behavior of the open load at OFF diagnosis. **Figure 43** and **Figure 44** provide the typical behavior of $V_{OUT(OLH)}$ and $V_{OUT(OLL)}$ as a function of the supply voltage and junction temperature. The device internally connects OUT with GND pin with an effective resistor $R_{OUT(GND)}$. In case the application provides high leakage current outside of the BTF50060-1TEA between Vs and OUT, it may be necessary to use an external resistor R_{L_OL} to disable open load detection. **Figure 46** gives an example of external circuitry for enabling / disabling open load detection in OFF state.

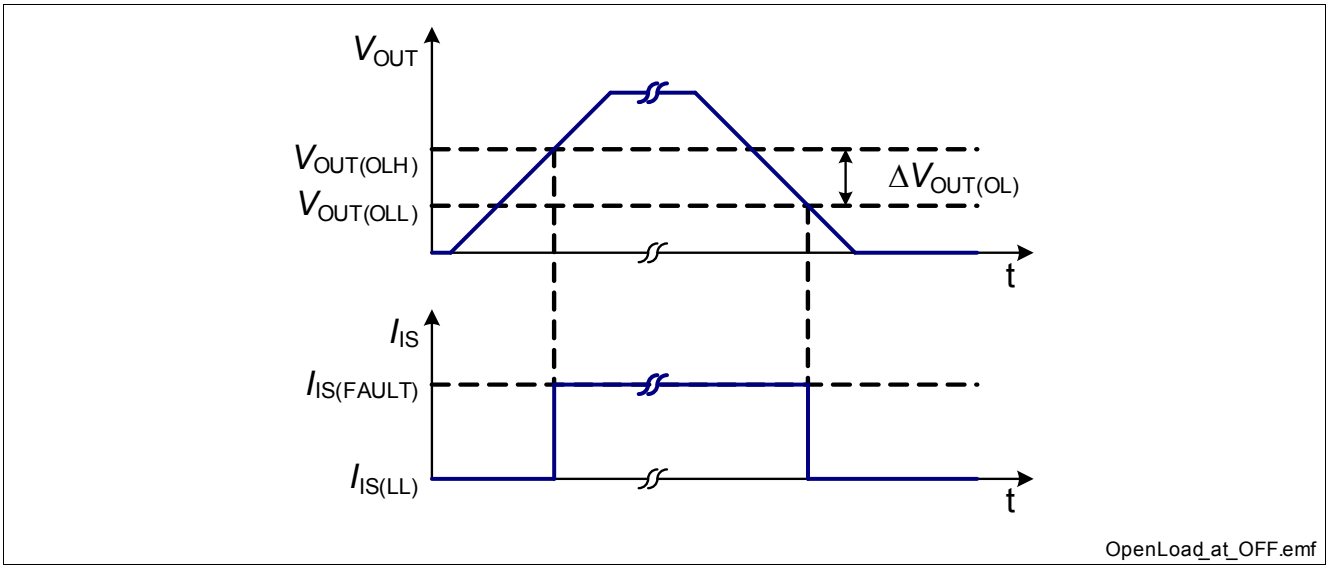


Figure 23 Open load detection in OFF state

5.5 Undervoltage Shutdown & Restart

The BTF50060-1TEA switches OFF whenever V_S drops below $V_{S(UV)OFF}$. The device restarts automatically after the supply voltage increases to a sufficient level (V_S > $V_{S(UV)ON}$) and a delay time of $t_{delay(UV)}$, if the input pin IN is HIGH. Please see **Figure 24** for details. The fault signal is reset if V_S is below $V_{S(UV)}$ for more than typ. 70µs.

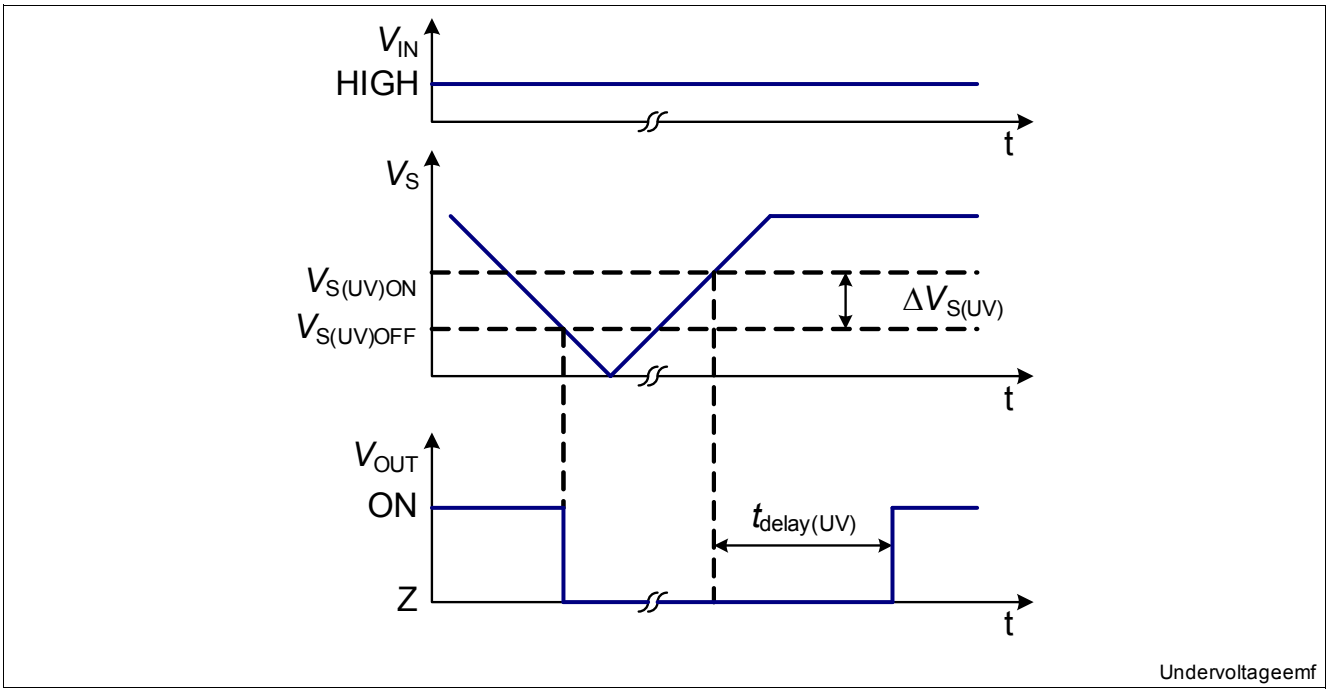


Figure 24 Undervoltage shutdown and restart

6 Electrical Characteristics BTF50060-1TEA

6.1 Electrical Characteristics Table

Table 6 Electrical Characteristics: BTF50060-1TEA

V_S = 6V to 19V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Operating currents							
Standby current for whole device with load T_j = 25°C	$I_{S(OFF)\_25}$ [1]	–	5	8	µA	V_{IN} = LOW for t > t_{RESET}, V_S = 13.5V, T_j = 25°C V_{OUT} < $V_{OUT(OLL)}$	P_6.1
Standby current for whole device with load T_j = 85°C	$I_{S(OFF)\_85}$ [1]	–	5	8	µA	V_{IN} = LOW for t > t_{RESET}, V_S = 13.5V, T_j = 85°C V_{OUT} < $V_{OUT(OLL)}$	P_6.2
Standby current for whole device with load T_j = 150°C	$I_{S(OFF)\_150}$	–	20	60	µA	V_{IN} = LOW for t > t_{RESET}, V_S = 13.5V, T_j = 150°C V_{OUT} < $V_{OUT(OLL)}$	P_6.3
Ground current during ON	$I_{GND(ON)}$	–	3	5	mA	V_{IN} = HIGH, t > t_{ON}	P_6.4
Supply current during open load detection in OFF state	$I_{S(OL)}$ [1]	–	12	15	mA	V_{IN} = LOW for t > t_{RESET}, V_{OUT} > $V_{OUT(OLH)}$	P_6.5
Power stage							
On-State Resistance	$R_{DS(ON)\_25}$ [1]	–	6.8	–	mΩ	V_{IN} = HIGH, T_j = 25 °C, V_S = 13.5V, I_L = +/-13.5A	P_6.6
On-State Resistance	$R_{DS(ON)\_150}$	–	10	12	mΩ	V_{IN} = HIGH, T_j = 150 °C, V_S = 13.5V, I_L = +/-13.5A	P_6.7
On-State Resistance	$R_{DS(8V)\_25}$ [1]	–	8	–	mΩ	V_{IN} = HIGH, T_j = 25 °C, V_S = 8V, I_L = +/-13.5A	P_6.8
On-State Resistance	$R_{DS(8V)\_150}$ [1]	–	11.5	15	mΩ	V_{IN} = HIGH, T_j = 150 °C, V_S = 8V, I_L = +/-13.5A	P_6.9

Table 6 Electrical Characteristics: BTF50060-1TEA (cont'd)

V_S = 6V to 19V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
On-State Resistance at low supply voltage	$R_{DS(UV)\_25}$ [1]	–	10.5	–	mΩ	V_{IN} = HIGH, T_j = 25 °C, V_S = 4.7V, I_L = +/-13.5A	P_6.10
On-State Resistance at low supply voltage	$R_{DS(UV)\_150}$	–	19	25	mΩ	V_{IN} = HIGH, T_j = 150°C, V_S = 4.7V, I_L = +/-13.5A	P_6.11
Body diode forward voltage drop[2]	$-V_{SD(rev)}$ [1]	300	700	1000	mV	V_{IN} = 0V, I_L = -13.5A (see Figure 13 and Figure 17)	P_6.12
Output leakage current[3]	$I_{L(OFF)\_25}$ [1]	–	0.1	1	µA	T_j = 25°C, V_{IN} = LOW, V_{OUT} = 0V	P_6.13
Output leakage current	$I_{L(OFF)\_85}$ [1]	–	0.1	1	µA	T_j = 85°C, V_{IN} = LOW, V_{OUT} = 0V	P_6.14
Output leakage current	$I_{L(OFF)\_150}$	–	1	60	µA	T_j = 150°C, V_{IN} = LOW, V_{OUT} = 0V	P_6.15
Switching a resistive load							
Slew rate 30% to 70% V_S	$(dV/dt)_{ON}$ [1]	22	43	108	V/µs	R_L = 1Ω, V_S = 13.5V (see Figure 10 and Figure 11 for definitions)	P_6.16
Slew rate 70% to 30% V_S	$(dV/dt)_{OFF}$ [1]	-90	-31	-13	V/µs		P_6.17
Slew rate matching $(dV/dt)_{ON}$ - $\|(dV/dt)_{OFF}\|$	$\Delta dV/dt$ [1]	-5	12	30	V/µs		P_6.18
Turn ON time to 90% V_S	t_{ON}	–	0.35	1.0	µs		P_6.19
Turn OFF time to 10% V_S	t_{OFF}	–	0.85	1.5	µs		P_6.20
Turn ON/OFF matching	t_{ON}-t_{OFF}	-1.15	-0.5	-0.25	µs		P_6.21
Wake up delay time	t_{wake} [1]	–	2	–	µs		P_6.62
Turn ON rise time 10% to 90% V_S	t_r	0.1	0.25	0.49	µs		P_6.22
Turn OFF fall time 90% to 10% V_S	t_f	0.12	0.35	0.83	µs		P_6.23
Switching an inductive load							
Source to Drain Smart Clamping voltage[4]	$V_{SD(CL)\_25}$ [1]	32	40	–	V	T_j = 25°C, I_L = 40mA,	P_6.26
Source to Drain Smart Clamping voltage	$V_{SD(CL)\_150}$ [1]	40	48	–	V	T_j = 150°C, I_L = 13.5A,	P_6.27
Input circuitry							
LOW level input voltage	$V_{IN(L)}$	-0.3	–	0.8	V	–	P_6.28