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BTN7973B

High Current PN Half Bridge NovalithIC™

Automotive Power

Never stop thinking

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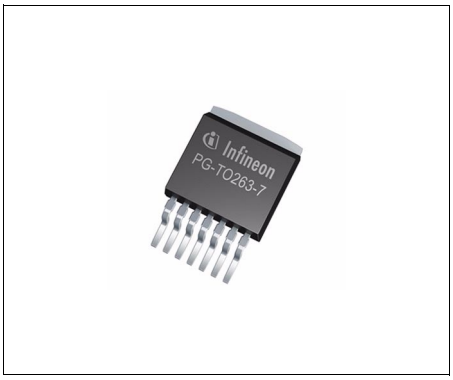
High Current PN Half Bridge NovalithIC™ **BTN7973B**

1 Overview



PG-TO263-7-1

Features

- Path resistance of max. 30.5 mΩ @ 150 °C (typ. 16 mΩ @ 25 °C)
  High Side: max. 12.8 mΩ @ 150 °C (typ. 7 mΩ @ 25 °C)
  Low Side: max. 17.7 mΩ @ 150 °C (typ. 9 mΩ @ 25 °C)
- Enhanced switching speed for reduced switching losses (rise/fall times down to typ. 550ns)
- Extended operating voltage range down to 4.5 V (high side switch)
- Low quiescent current of typ. 7 µA @ 25 °C
- PWM capability of up to 25 kHz combined with active freewheeling
- Switched mode current limitation for reduced power dissipation in overcurrent
- Current limitation level of 50 A min. / 70 A typ. (low side)
- Status flag diagnosis with current sense capability
- Overtemperature shut down with latch behaviour
- Smart clamping in overvoltage
- Undervoltage shut down
- Driver circuit with logic level inputs
- Adjustable slew rates for optimized EMI
- Operation up to 28V
- Green Product (RoHS compliant)
- AEC Qualified

Description

The BTN7973B is an integrated high current half bridge for motor drive applications. It is part of the NovalithIC™ family containing one p-channel highside MOSFET and one n-channel lowside MOSFET with an integrated driver IC in one package. Due to the p-channel highside switch the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation, smart clamping in overvoltage, and protection against overtemperature, undervoltage, overcurrent and short circuit.

The BTN7973B provides a cost optimized solution for protected high current PWM motor drives with very low board space consumption.

Type	Package	Marking
BTN7973B	PG-TO263-7-1	BTN7973B

2 Block Diagram

The BTN7973B is part of the NovalithIC™ family containing three separate chips in one package: One p-channel highside MOSFET and one n-channel lowside MOSFET together with a driver IC, forming an integrated high current half-bridge. All three chips are mounted on one common lead frame, using the chip on chip and chip by chip technology. The power switches utilize vertical MOS technologies to ensure optimum on state resistance. Due to the p-channel highside switch the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation, smart clamping in overvoltage and protection against overtemperature, undervoltage, overcurrent and short circuit. The BTN7973B can be combined with other BTN7973B to form H-bridge and 3-phase drive configurations.

2.1 Block Diagram

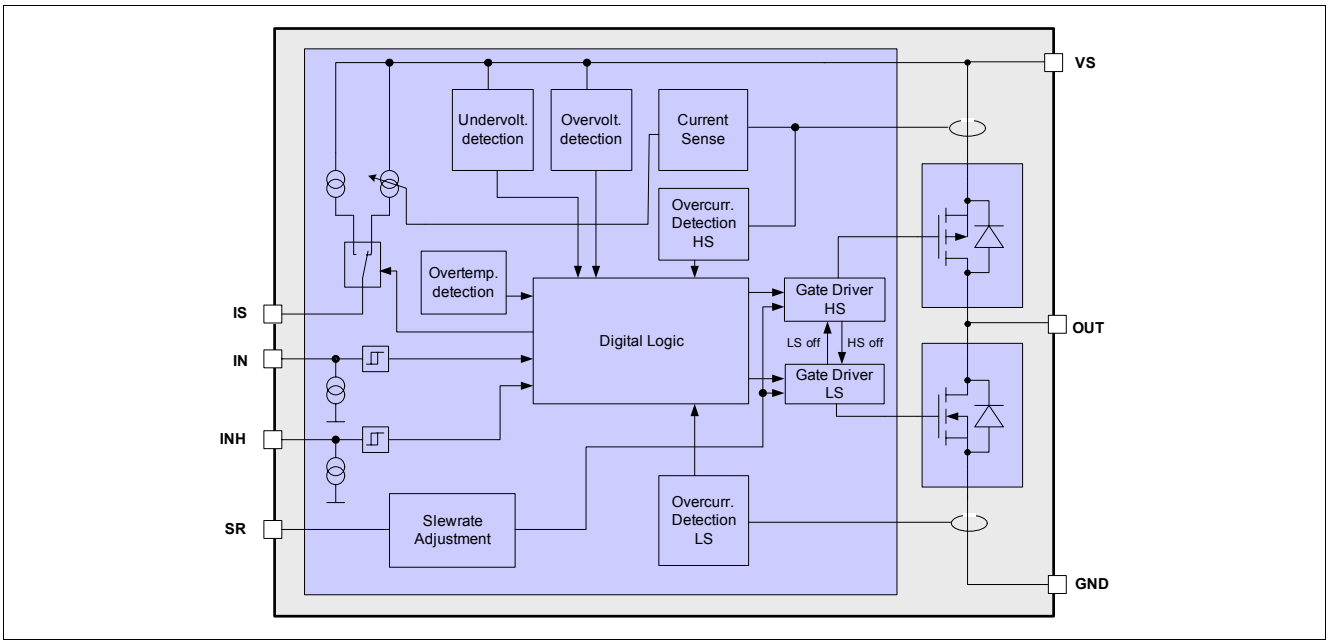


Figure 1 Block Diagram

2.2 Terms

Following figure shows the terms used in this data sheet.

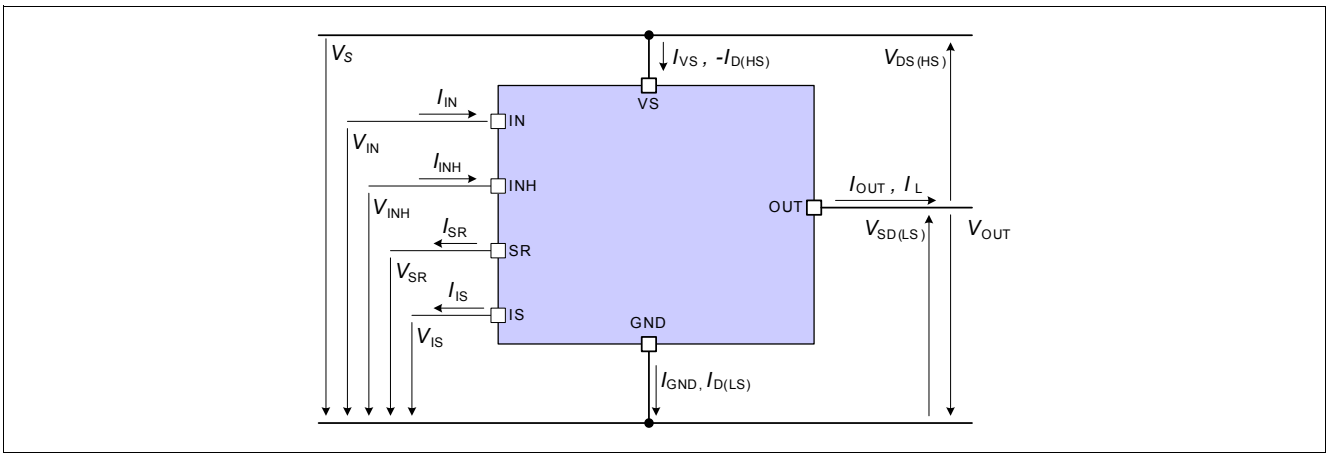


Figure 2 Terms

3 Pin Configuration

3.1 Pin Assignment

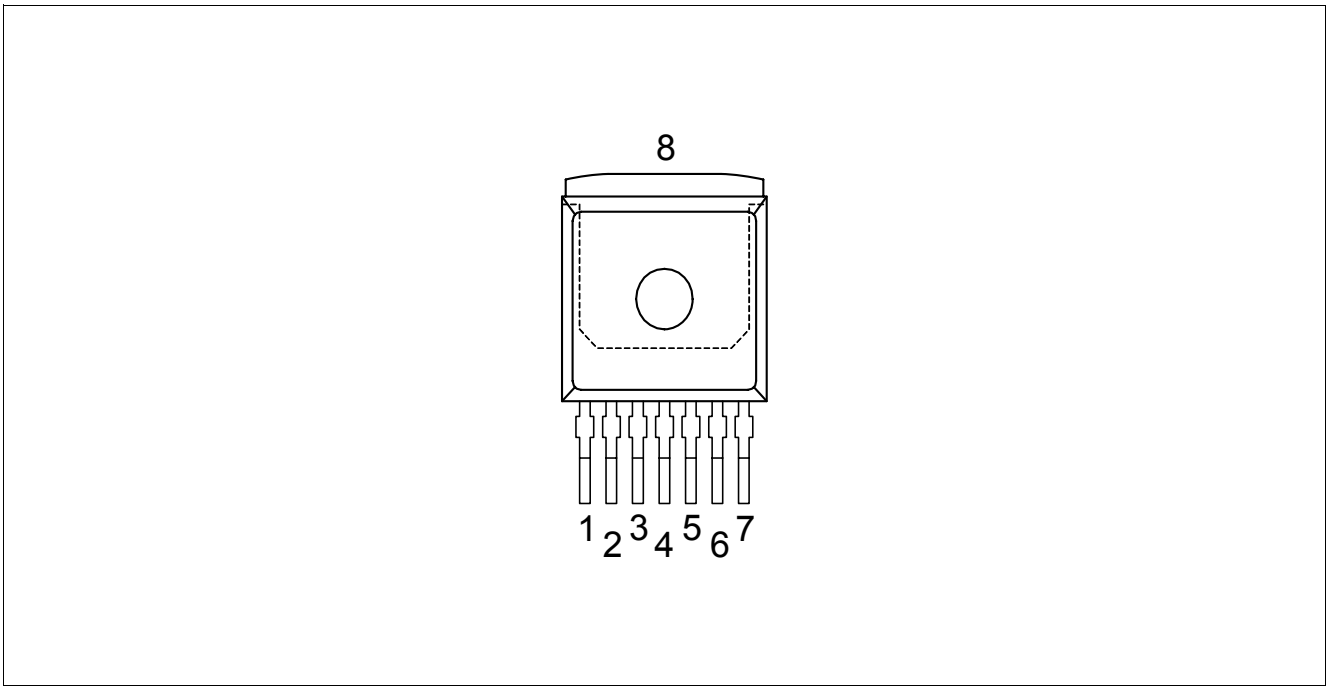


Figure 3 Pin Assignment BTN7973B (top view)

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
1	**GND**	**-**	**Ground**
2	IN	I	Input Defines whether high- or lowside switch is activated
3	INH	I	Inhibit When set to low device goes in sleep mode
4,8	**OUT**	**O**	**Power output of the bridge**
5	SR	I	Slew Rate The slew rate of the power switches can be adjusted by connecting a resistor between SR and GND
6	IS	O	Current Sense and Diagnostics
7	**VS**	**-**	**Supply**

Bold type: pin needs power wiring

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply Voltage	V_S	-0.3	28	V	–
4.1.2	Supply Voltage for Load Dump Protection ($V_{S(LD)}$= V_A + V_S with V_A = 13.5V)	$V_{S(LD)}$	–	40	V	[2)] R_i = 2 Ω R_L = 0.5 Ω t_d = 400ms suppressed pulse
4.1.3	Logic Input Voltage	V_{IN} V_{INH}	-0.3	5.3	V	–
4.1.4	Voltage at SR Pin	V_{SR}	-0.3	1.0	V	–
4.1.5	Voltage between VS and IS Pin	V_S -V_{IS}	-0.3	45	V	–
4.1.6	Voltage at IS Pin	V_{IS}	-20	28	V	–
Currents						
4.1.7	HS/LS Continuous Drain Current[3)]	$I_{D(HS)}$ $I_{D(LS)}$	-44	44	A	T_C < 85°C switch active
			-40	40	A	T_C < 125°C switch active
4.1.8	HS/LS Pulsed Drain Current[3)]	$I_{D(HS)}$ $I_{D(LS)}$	-90	90	A	T_C < 85°C t_{pulse} = 10ms single pulse
			-85	85	A	T_C < 125°C t_{pulse} = 10ms single pulse
4.1.9	HS/LS PWM Current[3)]	$I_{D(HS)}$ $I_{D(LS)}$	-55	55	A	T_C < 85°C f = 1kHz, DC = 50%
			-50	50	A	T_C < 125°C f = 1kHz, DC = 50%
			-60	60	A	T_C < 85°C f = 20kHz, DC = 50%
			-54	54	A	T_C < 125°C f = 20kHz, DC = 50%
Temperatures						
4.1.10	Junction Temperature	T_j	-40	150	°C	–
4.1.11	Storage Temperature	T_{stg}	-55	150	°C	–

Absolute Maximum Ratings (cont'd)[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
ESD Susceptibility						
4.1.12	ESD Resistivity HBM IN, INH, SR, IS OUT, GND, VS	V_{ESD}	 -2 -6	 2 6	kV	HBM[4)]

1) Not subject to production test, specified by design

2) $V_{S(LD)}$ is setup without the DUT connected to the generator per ISO7637-1; R_i is the internal resistance of the load dump test pulse generator; t_d is the pulse duration time for load dump pulse (pulse 5) according ISO 7637-1, -2.

3) Maximum reachable current may be smaller depending on current limitation level

4) ESD susceptibility, HBM according to EIA/JESD22-A114-B (1.5 kΩ, 100 pF)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

Maximum Single Pulse Current

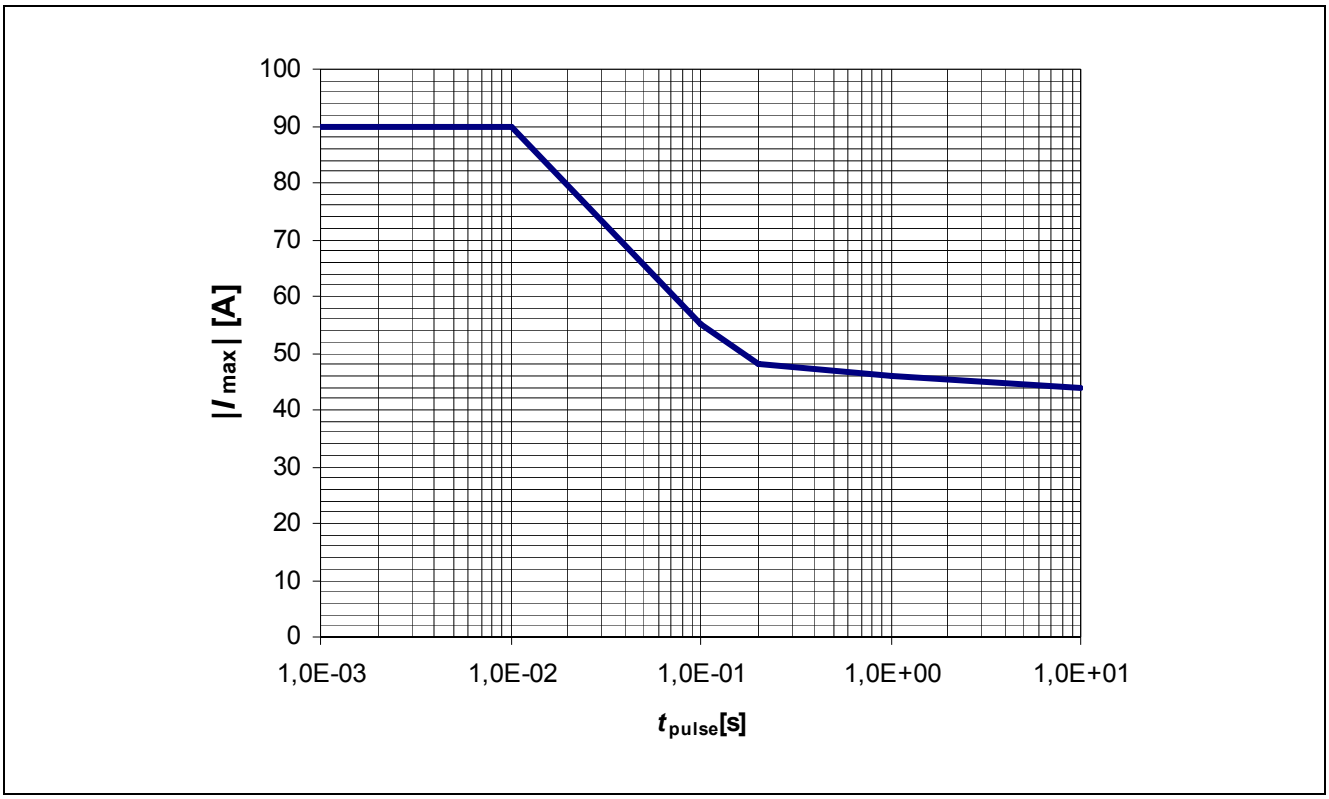


Figure 4 BTN7973B Maximum Single Pulse Current (T_C < 85°C)

This diagram shows the maximum single pulse current that can be driven for a given pulse time t_{pulse}. The maximum reachable current may be smaller depending on the current limitation level. Pulse time may be limited due to thermal protection of the device.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Range for Normal Operation	$V_{S(nor)}$	8	18	V	–
4.2.2	Extended Supply Voltage Range for Operation	$V_{S(ext)}$	$V_{UV(OFF)max}$	28	V	Parameter Deviations possible
4.2.3	Junction Temperature	T_j	-40	150	°C	–

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Thermal Resistance Junction-Case, Low Side Switch[1)] $R_{thjc(LS)} = \Delta T_{j(LS)} / P_{v(LS)}$	$R_{thJC(LS)}$	–	1.3	1.8	K/W	–
4.3.2	Thermal Resistance Junction-Case, High Side Switch[1)] $R_{thjc(HS)} = \Delta T_{j(HS)} / P_{v(HS)}$	$R_{thJC(HS)}$	–	0.6	0.9	K/W	–
4.3.3	Thermal Resistance Junction-Case, both Switches[1)] $R_{thjc} = \max[\Delta T_{j(HS)}, \Delta T_{j(LS)}] / (P_{v(HS)} + P_{v(LS)})$	R_{thJC}	–	0.7	1.0	K/W	–
4.3.4	Thermal Resistance Junction-Ambient[1)]	R_{thJA}	–	20	–	K/W	[2)]

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

5 Block Description and Characteristics

5.1 Supply Characteristics

V_S = 8 V to 18 V, T_j = -40 °C to +150 °C, I_L = 0 A, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
General							
5.1.1	Supply Current	$I_{VS(on)}$	–	2	3	mA	V_{INH} = 5 V V_{IN} = 0 V or 5 V R_{SR} = 0 Ω DC-mode normal operation (no fault condition)
5.1.2	Quiescent Current	$I_{VS(off)}$	–	7	12	µA	V_{INH} = 0 V V_{IN} = 0 V or 5 V T_j < 85 °C
			–	–	65	µA	V_{INH} = 0 V V_{IN} = 0 V or 5 V

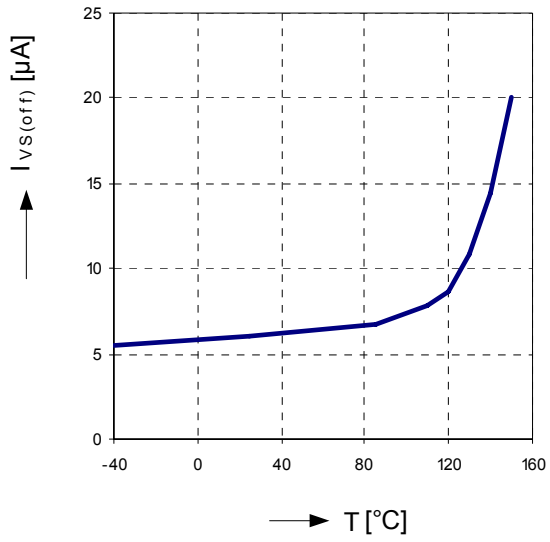


Figure 5 Typical Quiescent Current vs. Junction Temperature

5.2 Power Stages

The power stages of the BTN7973B consist of a p-channel vertical DMOS transistor for the high side switch and a n-channel vertical DMOS transistor for the low side switch. All protection and diagnostic functions are located in a separate top chip. Both switches can be operated up to 25 kHz, allowing active freewheeling and thus minimizing power dissipation in the forward operation of the integrated diodes.

The on state resistance R_{ON} is dependent on the supply voltage V_S as well as on the junction temperature T_j. The typical on state resistance characteristics are shown in **Figure 6**.

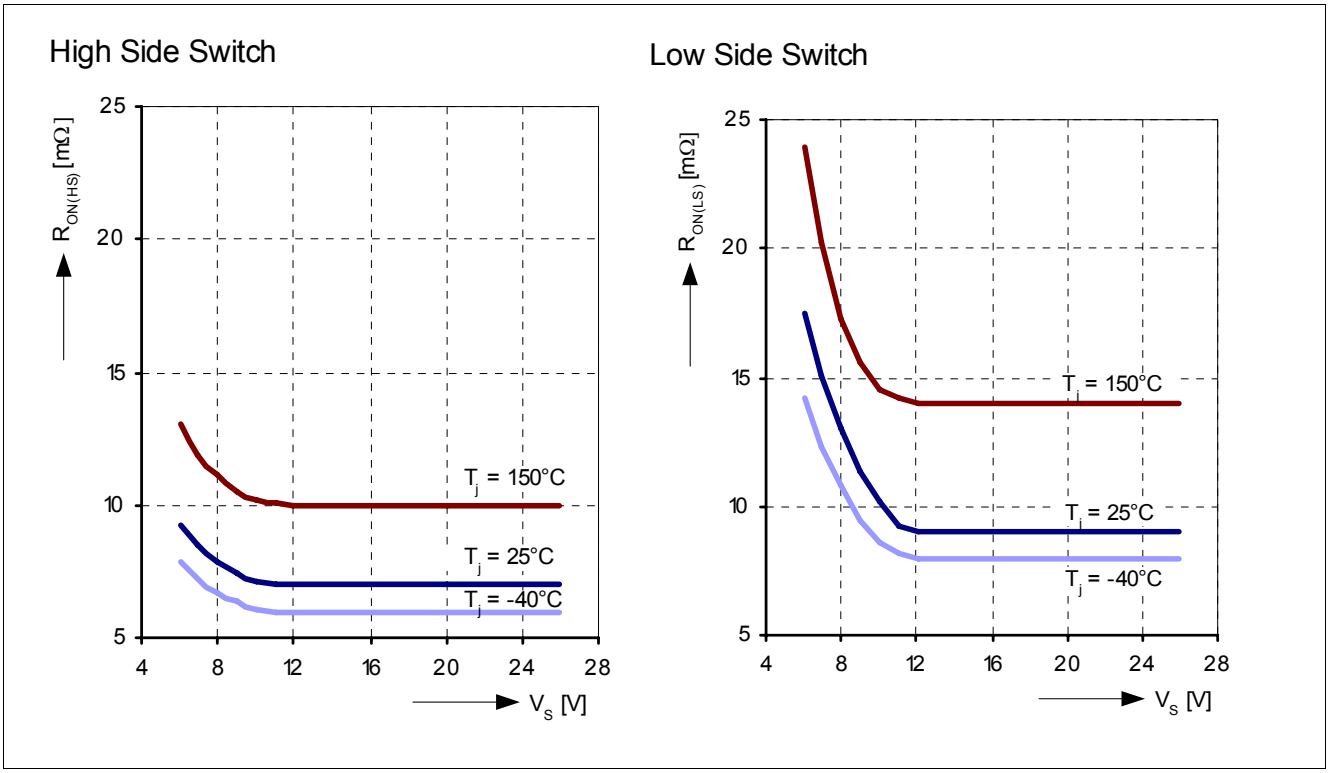


Figure 6 Typical ON State Resistance vs. Supply Voltage

5.2.1 Power Stages - Static Characteristics

V_S = 8 V to 18 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
High Side Switch - Static Characteristics							
5.2.1	ON State High Side Resistance	$R_{ON(HS)}$	–	7	–	mΩ	I_{OUT} = 9 A; V_S = 13.5 V
			–	10	12.8		T_j = 25 °C; 1) T_j = 150 °C
5.2.2	Leakage Current High Side	$I_{L(LKHS)}$	–	–	1	µA	V_{INH} = 0 V; V_{OUT} = 0 V T_j < 85 °C; 1)
			–	–	50	µA	V_{INH} = 0 V; V_{OUT} = 0 V T_j = 150 °C
5.2.3	Reverse Diode Forward-Voltage High Side2)	$V_{DS(HS)}$	–	0.9	–	V	I_{OUT} = -9 A T_j = -40 °C; 1)
			–	0.8	–		T_j = 25 °C; 1)
			–	0.6	0.8		T_j = 150 °C
Low Side Switch - Static Characteristics							
5.2.4	ON State Low Side Resistance	$R_{ON(LS)}$	–	9	–	mΩ	I_{OUT} = -9 A; V_S = 13.5 V
			–	14	17.7		T_j = 25 °C; 1) T_j = 150 °C
5.2.5	Leakage Current Low Side	$I_{L(LKLS)}$	–	–	1	µA	V_{INH} = 0 V; V_{OUT} = V_S T_j < 85 °C; 1)
			–	–	10	µA	V_{INH} = 0 V; V_{OUT} = V_S T_j = 150 °C
5.2.6	Reverse Diode Forward-Voltage Low Side2)	$V_{SD(LS)}$	–	0.9	–	V	I_{OUT} = 9 A T_j = -40 °C; 1)
			–	0.8	–		T_j = 25 °C; 1)
			–	0.7	0.9		T_j = 150 °C

1) Not subject to production test, specified by design

2) Due to active freewheeling, diode is conducting only for a few µs, depending on R_{SR}

5.2.2 Switching Times

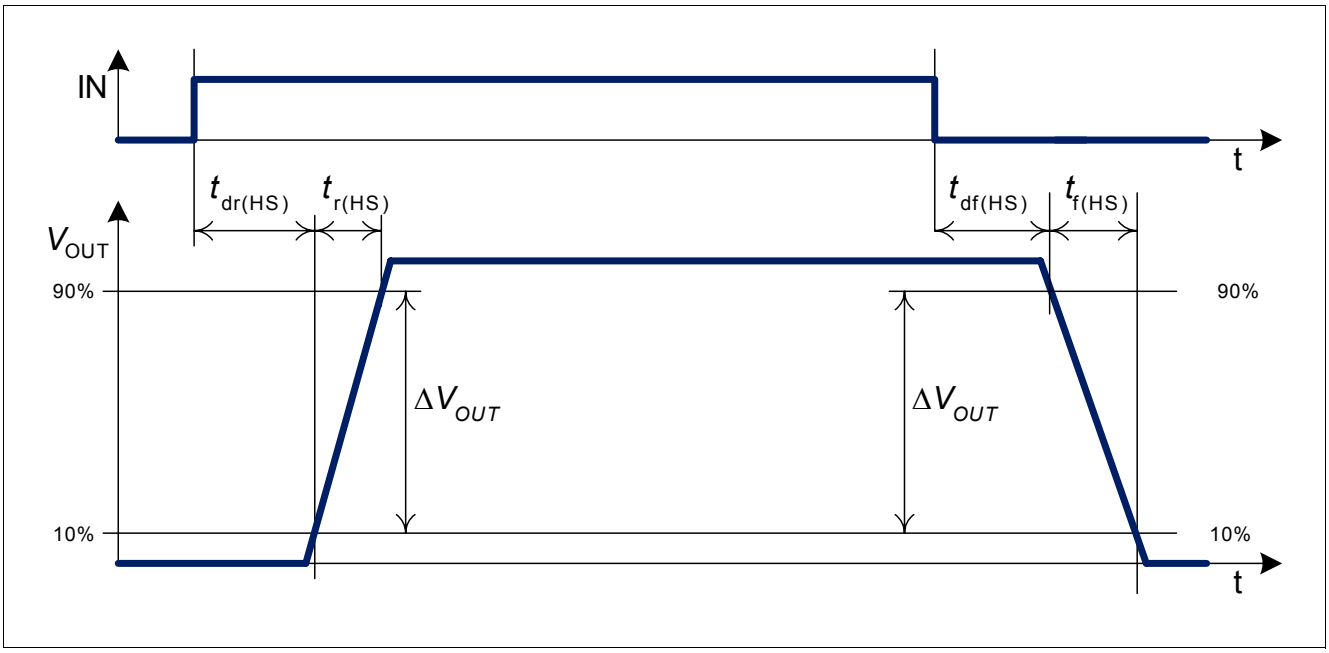


Figure 7 Definition of switching times high side (R_{load} to GND)

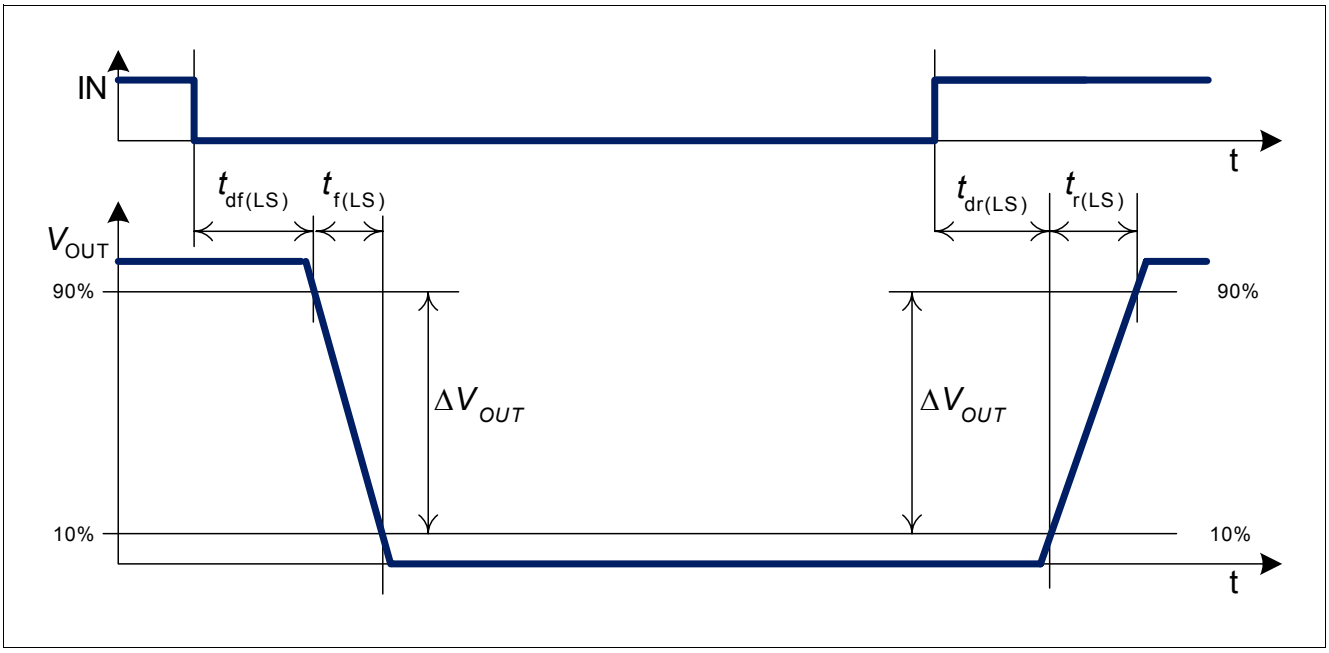


Figure 8 Definition of switching times low side (R_{load} to VS)

Due to the timing differences for the rising and the falling edge there will be a slight difference between the length of the input pulse and the length of the output pulse. It can be calculated using the following formulas:

- $\Delta t_{HS} = (t_{dr(HS)} + 0.5\ t_{r(HS)}) - (t_{df(HS)} + 0.5\ t_{f(HS)})$
- $\Delta t_{LS} = (t_{df(LS)} + 0.5\ t_{f(LS)}) - (t_{dr(LS)} + 0.5\ t_{r(LS)})$.

5.2.3 Power Stages - Dynamic Characteristics

V_S = 13.5 V, T_j = -40 °C to +150 °C, R_{load} = 2 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
High Side Switch Dynamic Characteristics							
5.2.7	Rise-Time of HS	$t_{r(HS)}$	 0.2 – 0.8	 0.6 1 2.7	 1 – 7	µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.8	Slew Rate HS on[1)]	ΔV_{OUT}/ $t_{r(HS)}$	 10.8 – 1.5	 18 10.8 4	 54 – 13.5	V/µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.9	Switch on Delay Time HS	$t_{dr(HS)}$	 1.2 – 2	 2 2.8 7.8	 2.8 – 17	µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.10	Fall-Time of HS	$t_{f(HS)}$	 0.25 – 0.8	 0.65 1 3.6	 1.05 – 8	µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.11	Slew Rate HS off[1)]	-ΔV_{OUT}/ $t_{f(HS)}$	 10.3 – 1.4	 16.6 10.8 3	 43.2 – 13.5	V/µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.12	Switch off Delay Time HS	$t_{df(HS)}$	 1 – 1.5	 1.6 2.3 6	 2.4 – 14	µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ

1) Not subject to production test, calculated value; $|\Delta V_{OUT}|/ t_{r(HS)}$ or $|-\Delta V_{OUT}|/ t_{f(HS)}$

V_S = 13.5 V, T_j = -40 °C to +150 °C, R_{load} = 2 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Low Side Switch Dynamic Characteristics							
5.2.13	Rise-Time of LS	$t_{r(LS)}$	 0.2 – 0.8	 0.55 1 3	 0.9 – 7	µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.14	Slew Rate LS off[1)]	ΔV_{OUT}/ $t_{r(LS)}$	 12 – 1.5	 19.6 10.8 3.6	 54 – 13.5	V/µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.15	Switch off Delay Time LS	$t_{dr(LS)}$	 0.3 – 0.8	 0.8 1.2 3.6	 1.3 – 7	µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.16	Fall-Time of LS	$t_{f(LS)}$	 0.2 – 0.8	 0.55 1 3	 0.9 – 8	µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.17	Slew Rate LS on[1)]	-ΔV_{OUT}/ $t_{f(LS)}$	 12 – 1.4	 19.6 10.8 3.6	 54 – 13.5	V/µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
5.2.18	Switch on Delay Time LS	$t_{df(LS)}$	 1.8 – 3	 2.7 3.8 11	 3.6 – 20	µs	 R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ

1) Not subject to production test, calculated value; $|\Delta V_{OUT}|/ t_{r(LS)}$ or $|-\Delta V_{OUT}|/ t_{f(LS)}$

5.3 Protection Functions

The device provides integrated protection functions. These are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not to be used for continuous or repetitive operation, with the exception of the current limitation (**Chapter 5.3.4**). In case of overtemperature the BTN7973B will apply the slew rate determined by the connected slew rate resistor. In all other fault conditions the highest slew rate possible will be applied independent of the connected slew rate resistor. Overvoltage, overtemperature and overcurrent are indicated by a fault current $I_{IS(LIM)}$ at the IS pin as described in the paragraph **“Status Flag Diagnosis With Current Sense Capability” on Page 19** and **Figure 12**.

In the following the protection functions are listed in order of their priority.

5.3.1 Overvoltage mode (Smart Clamping)

If the supply voltage is exceeding the over voltage level $V_{OVM(ON)}$ the device enters the overvoltage mode. The IC operates in normal mode again with a hysteresis $V_{OVM(HY)}$ if the supply voltage decreases below the Overvoltage Mode OFF voltage level $V_{OVM(off)}$. In case of overvoltage the device shuts the lowside MOSFET off and a fault current $I_{IS(LIM)}$ is provided at the IS pin. The highside MOSFET is still operational and follows the inputs IN and INH. Current Limitation and Overtemperature Protection are still active for the highside switch, and can independently switch off the highside MOSFET, if it was on before.

If the highside MOSFET is off, an implemented voltage clamp mechanism keeps the voltage drop $-V_{DS(HS)}$ over the highside at a certain level $-V_{DS(HS)\_CL}$.

5.3.2 Undervoltage Shut Down

To avoid uncontrolled motion of the driven motor at low voltages the device shuts off (output is tri-state), if the supply voltage drops below the switch-off voltage $V_{UV(OFF)}$. The IC becomes active again with a hysteresis $V_{UV(HY)}$ if the supply voltage rises above the switch-on voltage $V_{UV(ON)}$.

*Note: With decreasing $V_s < V_{UV(OFF)max}$, activation of the Current Limitation mode may occur before Undervoltage Shut Down with ambient temperatures less than 25°C. See **Table “Switch-OFF Voltage” on Page 18**.*

5.3.3 Overtemperature Protection

The BTN7973B is protected against overtemperature by an integrated temperature sensor. Overtemperature leads to a shut down of both output stages. This state is latched until the device is reset by a low signal with a minimum length of t_{reset} at the INH pin, provided that its temperature has decreased at least the thermal hysteresis ΔT in the meantime.

Repetitive use of the overtemperature protection impacts lifetime.

5.3.4 Current Limitation

The current in the bridge is measured in both switches. As soon as the current in forward direction in one switch (high side or low side) is reaching the limit I_{CLx}, this switch is deactivated and the other switch is activated for t_{CLS}. During that time all changes at the IN pin are ignored. However, the INH pin can still be used to switch both MOSFETs off. After t_{CLS} the switches return to their initial setting. The error signal at the IS pin is reset after 2 * t_{CLS}. Unintentional triggering of the current limitation by short current spikes (e.g. inflicted by EMI coming from the motor) is suppressed by internal filter circuitry. Due to thresholds and reaction delay times of the filter circuitry the effective current limitation level I_{CLx} depends on the slew rate of the load current dI/dt as shown in **Figure 10**.

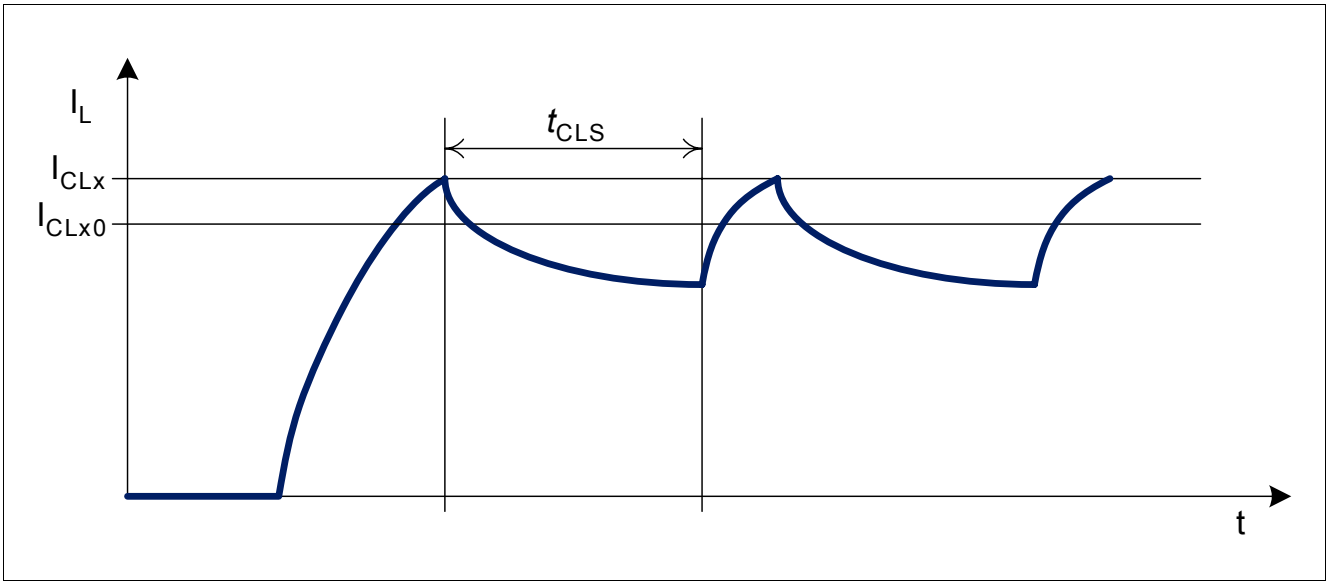


Figure 9 Timing Diagram Current Limitation (Inductive Load)

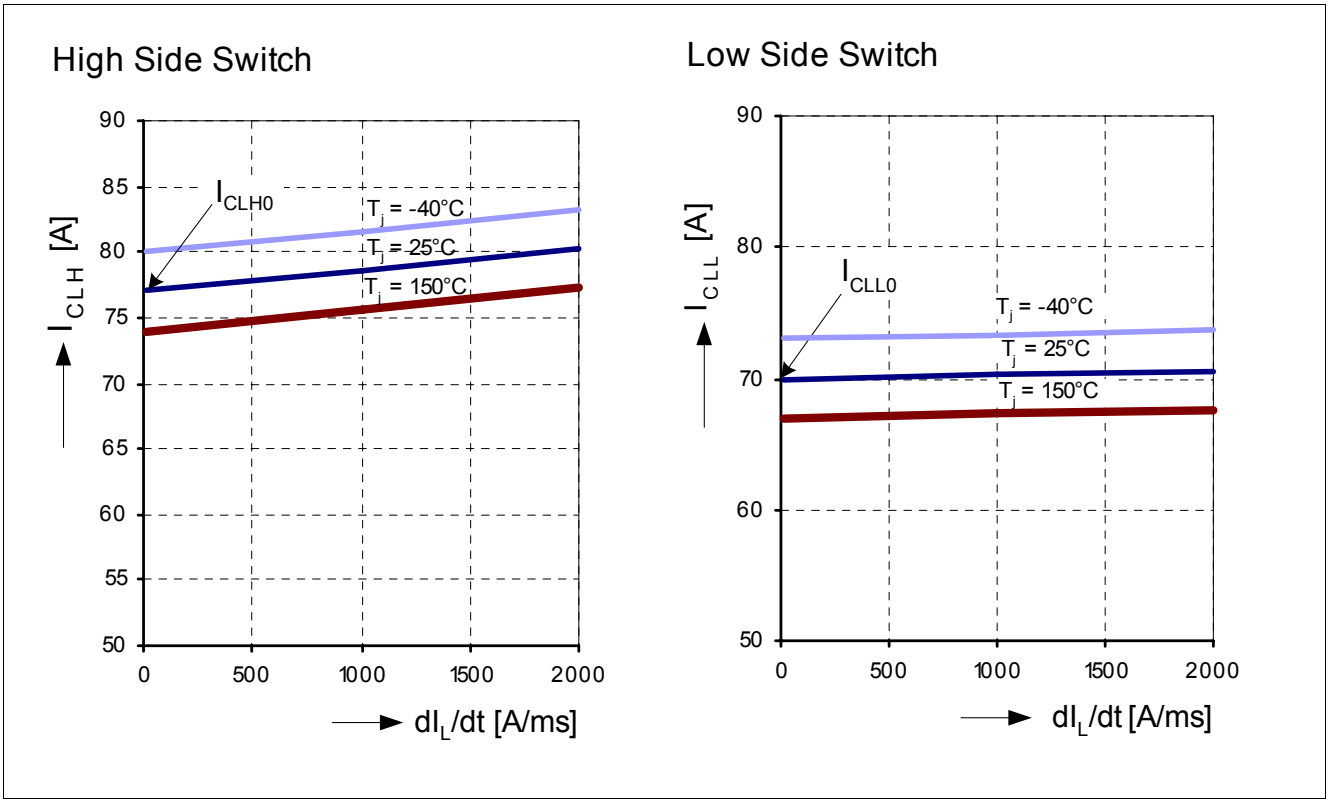


Figure 10 Typical Current Limitation Level vs. Current Slew Rate dI/dt

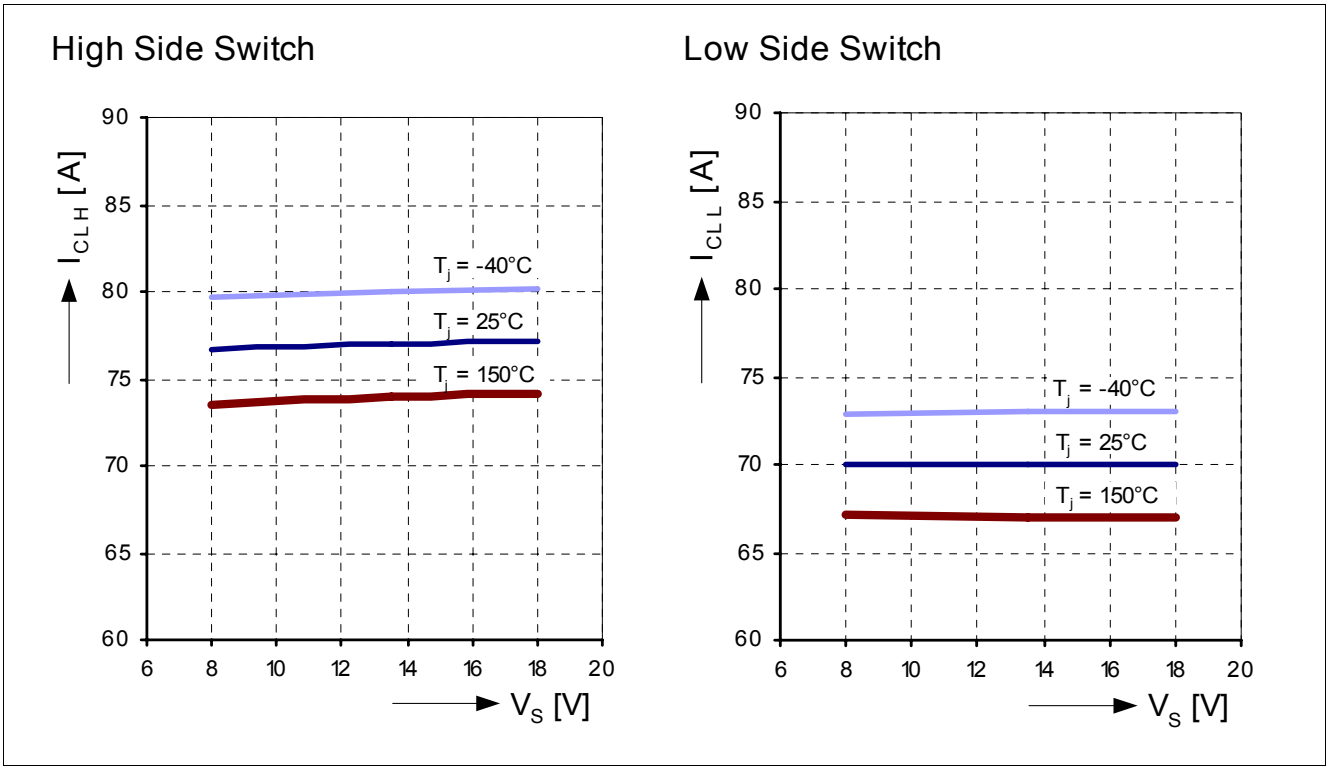


Figure 11 Typical Current Limitation Detection Levels vs. Supply Voltage

In combination with a typical inductive load, such as a motor, this results in a switched mode current limitation. This method of limiting the current has the advantage of greatly reduced power dissipation in the BTN7973B compared to driving the MOSFET in linear mode. Therefore it is possible to use the current limitation for a short time without exceeding the maximum allowed junction temperature (e.g. for limiting the inrush current during motor start up). However, the regular use of the current limitation is allowed as long as the specified maximum junction temperature is not exceeded. Exceeding this temperature can reduce the lifetime of the device.

5.3.5 Short Circuit Protection

The device is short circuit protected against

- output short circuit to ground
- output short circuit to supply voltage
- short circuit of load

The short circuit protection is realized by the previously described current limitation in combination with the over-temperature shut down of the device.

5.3.6 Electrical Characteristics - Protection Functions

V_S = 8 V to 18 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Under Voltage Shut Down							
5.3.1	Switch-ON Voltage	$V_{UV(ON)}$	–	–	5.5	V	V_S increasing
5.3.2	Switch-OFF Voltage[1)]	$V_{UV(OFF)}$	3.0	–	4.5	V	V_S decreasing, IN = 1, INH = 1
			3.0	–	5.5	V	V_S decreasing, IN = 0, INH = 1
5.3.3	ON/OFF hysteresis	$V_{UV(HY)}$	–	0.2	–	V	2)
Over Voltage Mode							
5.3.4	Over voltage Mode OFF Voltage	$V_{OVM(OFF)}$	27.8	–	–	V	V_S decreasing
5.3.5	Over voltage Mode ON Voltage	$V_{OVM(ON)}$	28	–	30	V	V_S increasing
5.3.6	ON/OFF hysteresis	$V_{OVM(HY)}$	–	0.2	–	V	2)
5.3.7	Drain Source Clamp Voltage High Side Switch	$-V_{DS(HS)\_CL}$	30	–	–	V	$I_{D(HS)}$ = -1 mA, HSS off, 2)
Current Limitation							
5.3.8	Current Limitation Detection level High Side	I_{CLH0}	55	77	98	A	V_S = 13.5 V
5.3.9	Current Limitation Detection level Low Side	I_{CLL0}	50	70	90	A	V_S = 13.5 V
Current Limitation Timing							
5.3.10	Shut OFF Time for HS and LS	t_{CLS}	70	115	210	µs	V_S = 13.5 V; 2)
Thermal Shut Down							
5.3.11	Thermal Shut Down Junction Temperature	T_{jSD}	155	175	200	°C	–
5.3.12	Thermal Switch ON Junction Temperature	T_{jSO}	150	–	190	°C	–
5.3.13	Thermal Hysteresis	ΔT	–	7	–	K	2)
5.3.14	Reset Pulse at INH Pin (INH low)	t_{reset}	4	–	–	µs	2)

1) With decreasing $V_s < V_{UV(OFF)max}$, activation of the Current Limitation mode may occur before Undervoltage Shut Down with ambient temperatures less than 25°C.

2) Not subject to production test, specified by design

5.4 Control and Diagnostics

5.4.1 Input Circuit

The control inputs IN and INH consist of TTL/CMOS compatible schmitt triggers with hysteresis which control the integrated gate drivers for the MOSFETs. Setting the INH pin to high enables the device. In this condition one of the two power switches is switched on depending on the status of the IN pin. To deactivate both switches, the INH pin has to be set to low. No external driver is needed. The BTN7973B can be interfaced directly to a microcontroller, as long as the maximum ratings in **Chapter 4.1** are not exceeded.

5.4.2 Dead Time Generation

In bridge applications it has to be assured that the highside and lowside MOSFET are not conducting at the same time, connecting directly the battery voltage to GND. This is assured by a circuit in the driver IC, generating a so called dead time between switching off one MOSFET and switching on the other. The dead time generated in the driver IC is automatically adjusted to the selected slew rate.

5.4.3 Adjustable Slew Rate

In order to optimize electromagnetic emission, the switching speed of the MOSFETs is adjustable by an external resistor. The slew rate pin SR allows the user to optimize the balance between emission and power dissipation within his own application by connecting an external resistor R_{SR} to GND.

5.4.4 Status Flag Diagnosis With Current Sense Capability

The status pin IS is used as a combined current sense and error flag output. In normal operation (current sense mode), a current source is connected to the status pin, which delivers a current proportional to the forward load current flowing through the active high side switch. If the high side switch is inactive or the current is flowing in the reverse direction no current will be driven except for a marginal leakage current $I_{IS(LK)}$. The external resistor R_{IS} determines the voltage per output current. E.g. with the nominal value of **19.5**k for the current sense ratio $k_{ILIS} = I_L / I_{IS}$, a resistor value of R_{IS} = 1 kΩ leads to $V_{IS} = (I_L$ / **19.5** A)V. In case of a fault condition the status output is connected to a current source which is independent of the load current and provides $I_{IS(lim)}$. The maximum voltage at the IS pin is determined by the choice of the external resistor and the supply voltage. In case of current limitation the $I_{IS(lim)}$ is activated for 2 * t_{CLS}.

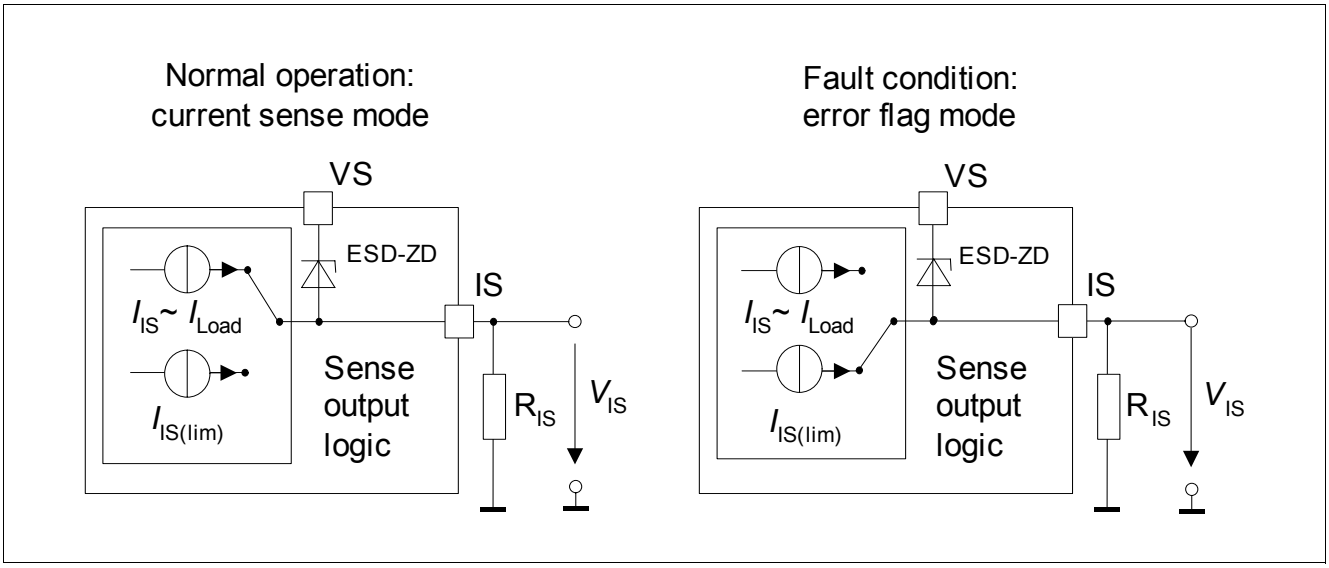


Figure 12 Sense Current and Fault Current

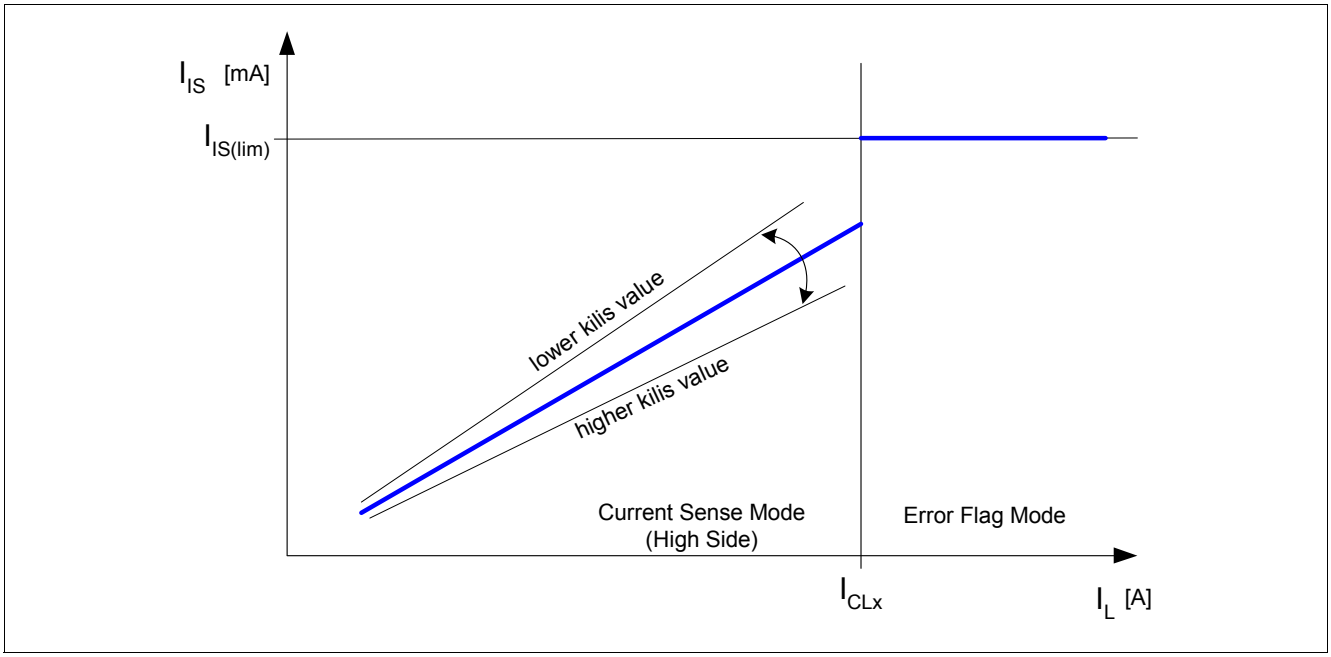


Figure 13 Sense Current vs. Load Current

5.4.5 Truth Table

Device State	Inputs		Outputs			Mode
	INH	IN	HSS	LSS	IS	
Normal Operation	0	X	OFF	OFF	0	Stand-by mode
	1	0	OFF	ON	0	LSS active
	1	1	ON	OFF	CS	HSS active
Over-Voltage Mode (OVM)	0	X	OFF (CL)	OFF	1	HSS possible Smart Clamping; error detected
	1	0	OFF (CL)	OFF	1	Shut-down of LSS, HSS possible Smart Clamping, error detected
	1	1	ON	OFF	1	HSS active (OC and OT still valid), LSS off, error detected
Under-Voltage (UV)	X	X	OFF	OFF	0	UV lockout
Overtemperature (OT) or Short Circuit of HSS or LSS	0	X	OFF	OFF	0	Stand-by mode, reset of latch
	1	X	OFF	OFF	1	Shut-down with latch, error detected
Current Limitation Mode/ Overcurrent (OC)	1	1	OFF	ON	1	Switched mode, error detected[1)]
	1	0	ON	OFF	1	Switched mode, error detected[1)]

1) Will return to normal operation after t_{CLS}; Error signal is reset after 2*t_{CLS} (see **Chapter 5.3.4**)

Inputs	Switches	Status Flag IS
0 = Logic LOW	OFF = switched off	CS = Current sense mode
1 = Logic HIGH	ON = switched on	1 = Logic HIGH (error)
X = 0 or 1	CL = Smart Clamping	

5.4.6 Electrical Characteristics - Control and Diagnostics

V_S = 8 V to 18 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Control Inputs (IN and INH)							
5.4.1	High level Voltage INH, IN	$V_{INH(H)}$ $V_{IN(H)}$	– –	1.75 1.6	2.15 2	V	–
5.4.2	Low level Voltage INH, IN	$V_{INH(L)}$ $V_{IN(L)}$	1.1	1.4	–	V	–
5.4.3	Input Voltage hysteresis	V_{INHHY} V_{INHY}	– –	350 200	– –	mV	1)
5.4.4	Input Current high level	$I_{INH(H)}$ $I_{IN(H)}$	–	30	150	µA	V_{IN} = V_{INH} = 5.3 V
5.4.5	Input Current low level	$I_{INH(L)}$ $I_{IN(L)}$	–	25	125	µA	V_{IN} = V_{INH} = 0.4 V
Current Sense							
5.4.6	Current Sense ratio in static on-condition k_{ILIS} = I_L / I_{IS}	k_{ILIS}	 14 13 11	 19.5 19.5 19.5	 25 26 29	10^3	R_{IS} = 1 kΩ I_L = 40 A I_L = 20 A I_L = 10 A
5.4.7	Maximum analog Sense Current, Sense Current in fault Condition	$I_{IS(lim)}$	4	5	6.5	mA	V_S = 13.5 V R_{IS} = 1kΩ
5.4.8	Isense Leakage current	I_{ISL}	–	–	1	µA	V_{IN} = 0 V or V_{INH} = 0 V
5.4.9	Isense Leakage current, active high side switch	I_{ISH}	–	1	100	µA	V_{IN} = V_{INH} = 5 V I_L = 0 A

1) Not subject to production test, specified by design

6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

6.1 Application Example

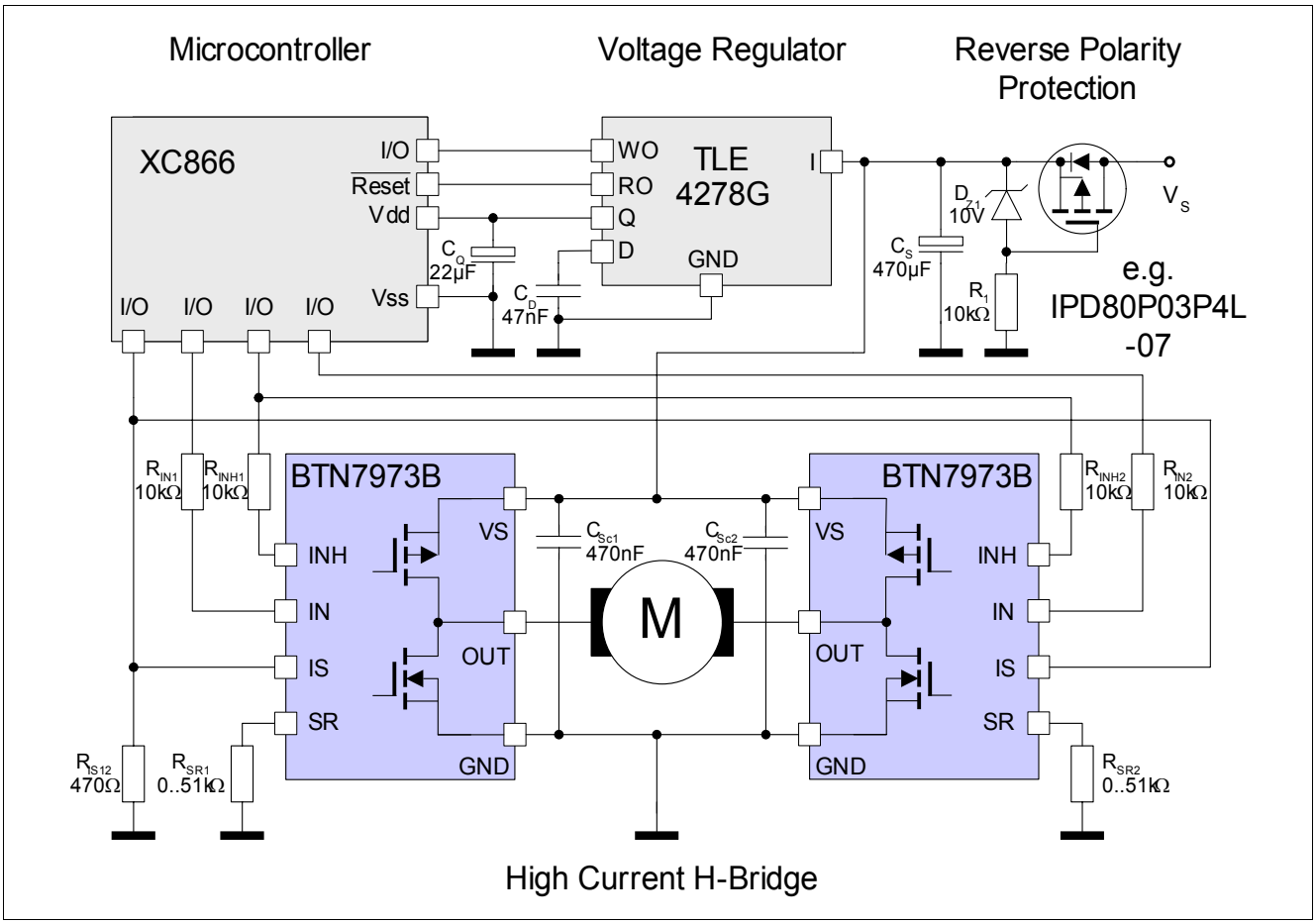


Figure 14 Application Example: H-Bridge with two BTN7973B

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

6.2 Layout Considerations

Due to the fast switching times for high currents, special care has to be taken to the PCB layout. Stray inductances have to be minimized in the power bridge design as it is necessary in all switched high power bridges. The BTN7973B has no separate pin for power ground and logic ground. Therefore it is recommended to assure that the offset between the ground connection of the slew rate resistor, the current sense resistor and ground pin of the device (GND / pin 1) is minimized. If the BTN7973B is used in a H-bridge or B6 bridge design, the voltage offset between the GND pins of the different devices should be small as well.

A ceramic capacitor from VS to GND close to each device is recommended to provide current for the switching phase via a low inductance path and therefore reducing noise and ground bounce. A reasonable value for this capacitor would be about 470 nF.

The digital inputs need to be protected from excess currents (e.g. caused by induced voltage spikes) by series resistors in the range of 10 kΩ.

6.3 Half-bridge Configuration Considerations

If the BTN7973B is used in a half-bridge configuration with the load connected between OUT and VS and the supply voltage is exceeding the Overvoltage Mode ON level $V_{OVM(ON)}$, the implemented "**Overvoltage mode (Smart Clamping)**" feature leads to automatically turning off the low side switch.

If the load is connected between OUT and GND and the supply voltage is exceeding the Overvoltage Mode ON level $V_{OVM(ON)}$ while the high side switch is turned off and low side MOSFET is on, the low side MOSFET will be turned off. If the voltage drop over the high side switch exceeds the high side clamp voltage $-V_{DS(HS)\_CL}$ a current can flow through the high side switch and the load to GND.

It shall be insured that the power dissipated in the NovalithIC™ does not exceed the maximum ratings.

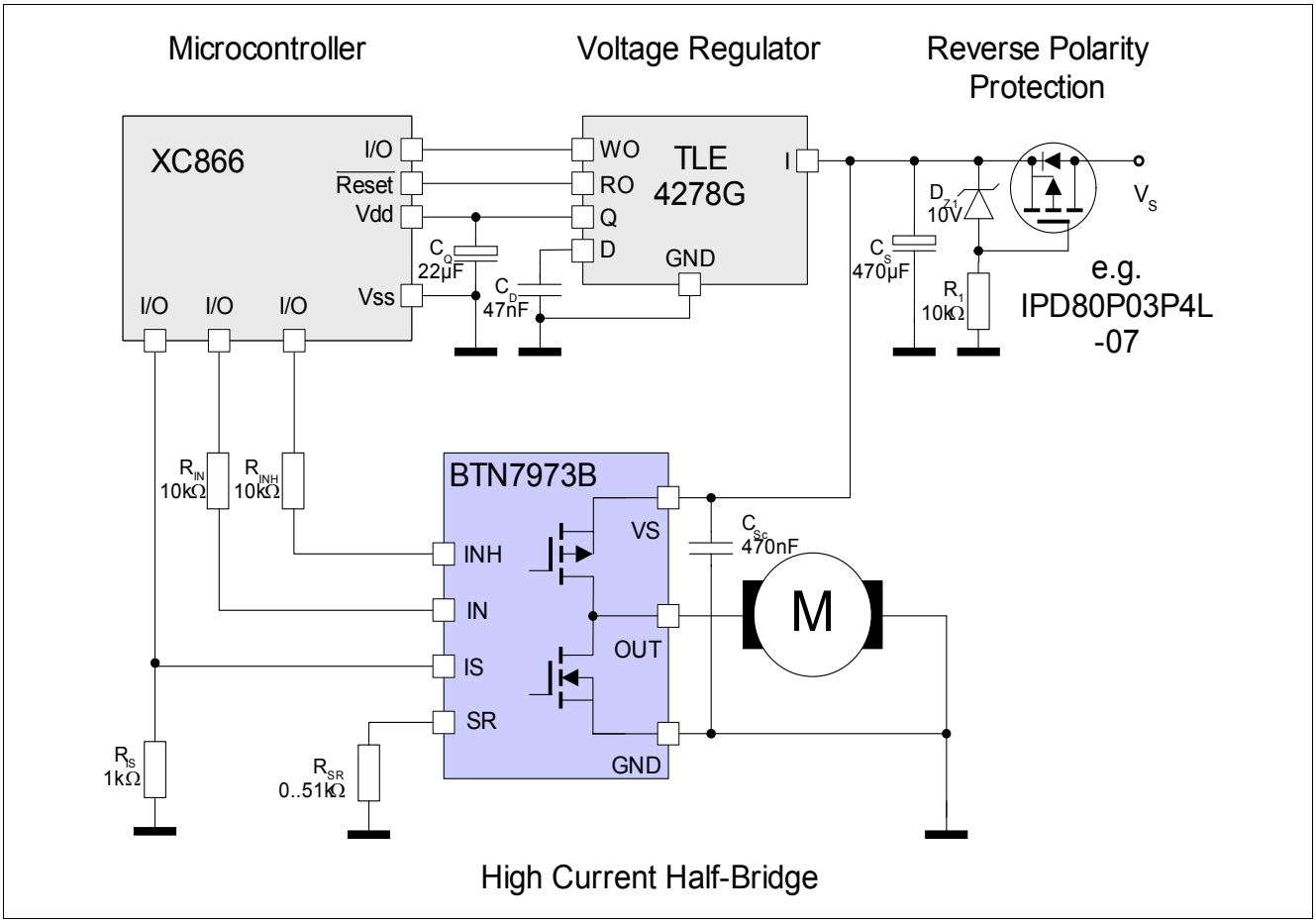
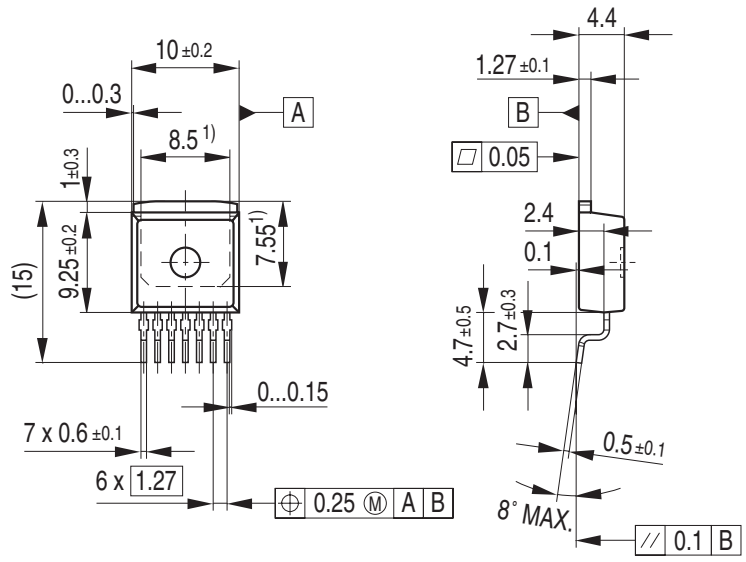


Figure 15 Application Example: Half-Bridge with a BTN7973B (Load to GND)

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

7 Package Outlines



1) Typical
Metal surface min. X = 7.25, Y = 6.9
All metal surfaces tin plated, except area of cut.

GPT09114

Footprint

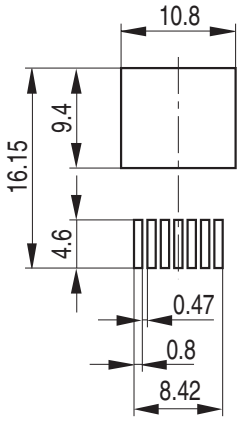


Figure 16 PG-TO263-7-1 (Plastic Green Transistor Single Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision History

Revision	Date	Changes
1.0	2009-09-09	Initial version Data Sheet