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BTN8960 /62 /80 /82

High Current PN Half Bridge

About this document

Scope and purpose

This Application Note is intended to provide information and hints for a high current design, using PWM control with the NovalithIC™ half-bridge family BTN89xy for the automotive environment.

Note: *The following information is only given to help with the implementation of the device and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

1 Abstract

This family contains one P-channel high-side MOSFET and one N-channel low-side MOSFETwith an integrated driver IC in one package. The NovalithIC™ is the interface between the microcontroller and the motor, equipped with diagnostic and protection functions.

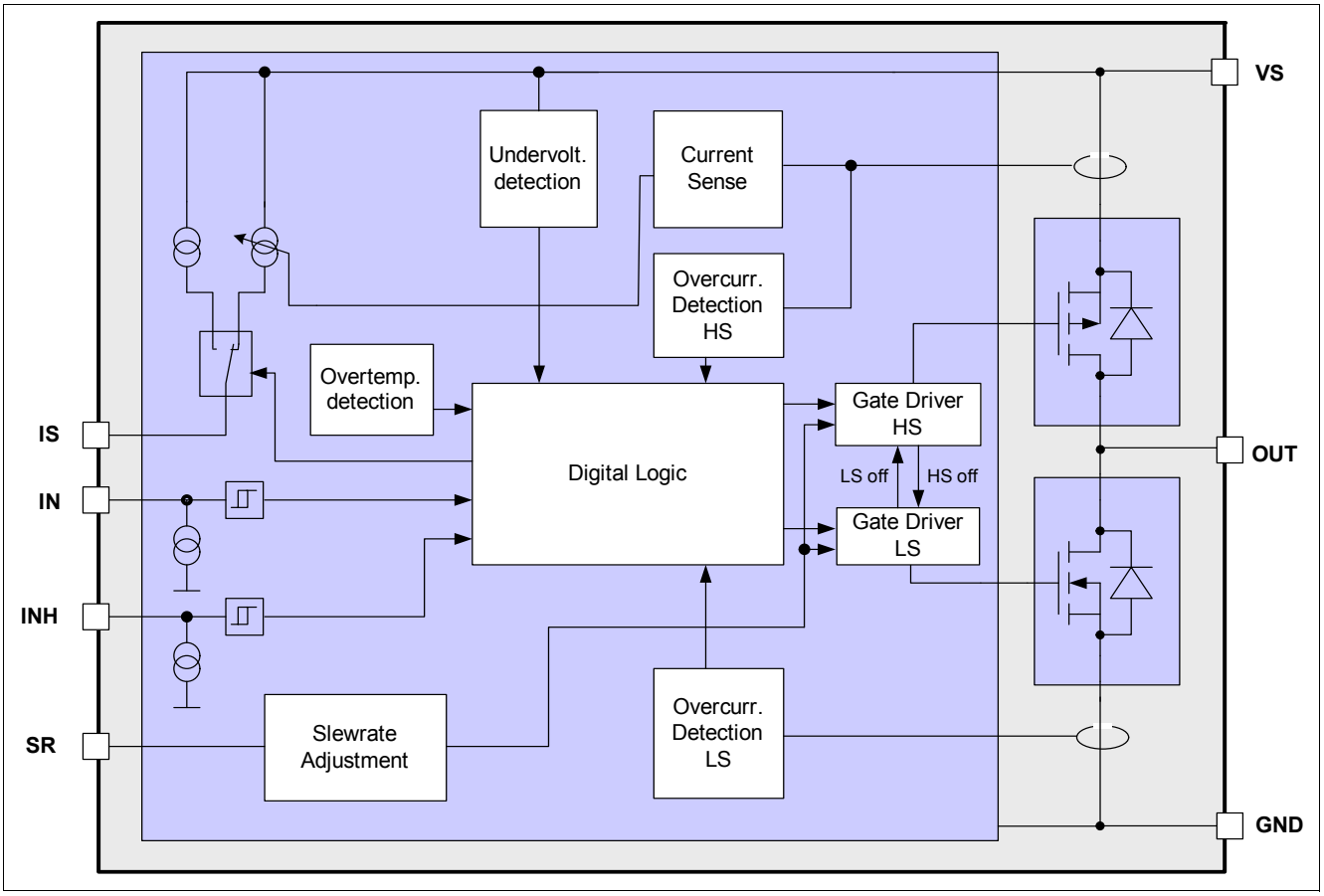

Figure 1 Block Diagram BTN89xy

As both the high-side and low side switch are placed on one single leadframe this results in many system benefits: Resulting from the low distance between the high-side MOSFET and the low-side MOSFETthe stray inductances between them is minimal thus minimizing negative voltage spikes at OUT during switching and improving EMC. As the voltage level of the leadframe is on the output of the half-bridge, only one single cooling

Abstract

area is required (on OUT potential) for the device, thus being used for both a high-side or low-side current switching. For a state of the art N-channel solution, usually two cooling areas are required, each for the high-side and low-side MOSFET.

Due to the p-channel highside switch the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation and protection against overtemperature, undervoltage, overcurrent and short circuit.

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2 Motor Configurations

Electrical motors are built with various architectures. Mechanically commutated motors with brushes, so called DC motors or electrically commutated motors, so called BLDC motors (BrushLess DC motors). The NovalithIC™ family can support all of them due to, the flexibility of the half-bridge concept.

Using NovalithIC™ controlling a DC-motor has the following advantages:

- Extremely low parasitic inductances between high-side and low-side MOSFET.
- Optimized switching performance of the MOSFET's to reduce power losses and EMC emission.
- Driving the motor with PWM for torque and speed control.
- Integrated freewheeling transistor.
- Integrated current measurement.
- Integrated diagnosis and protection.
- Microcontroller -compatible input pins.
- Small and PCB-area saving package.

2.1 Half-bridge configuration for mono-directional motor control

Figure 2 shows the design of a mono-directional motor control with NovalithIC™. In most cases, the motor is connected between "OUT" and "GND". This is because the chassis of a car is "GND", and therefore a short to "GND" is much more probable than a short to "V_S". For this reason it is statistically safer with a motor connected to "GND", because if a short occurs in this case, the motor is not running.

Generally, it is also possible to use the NovalithIC™ to drive the motor between "OUT" and "V_S". The inverted "IN" signal must be respected.

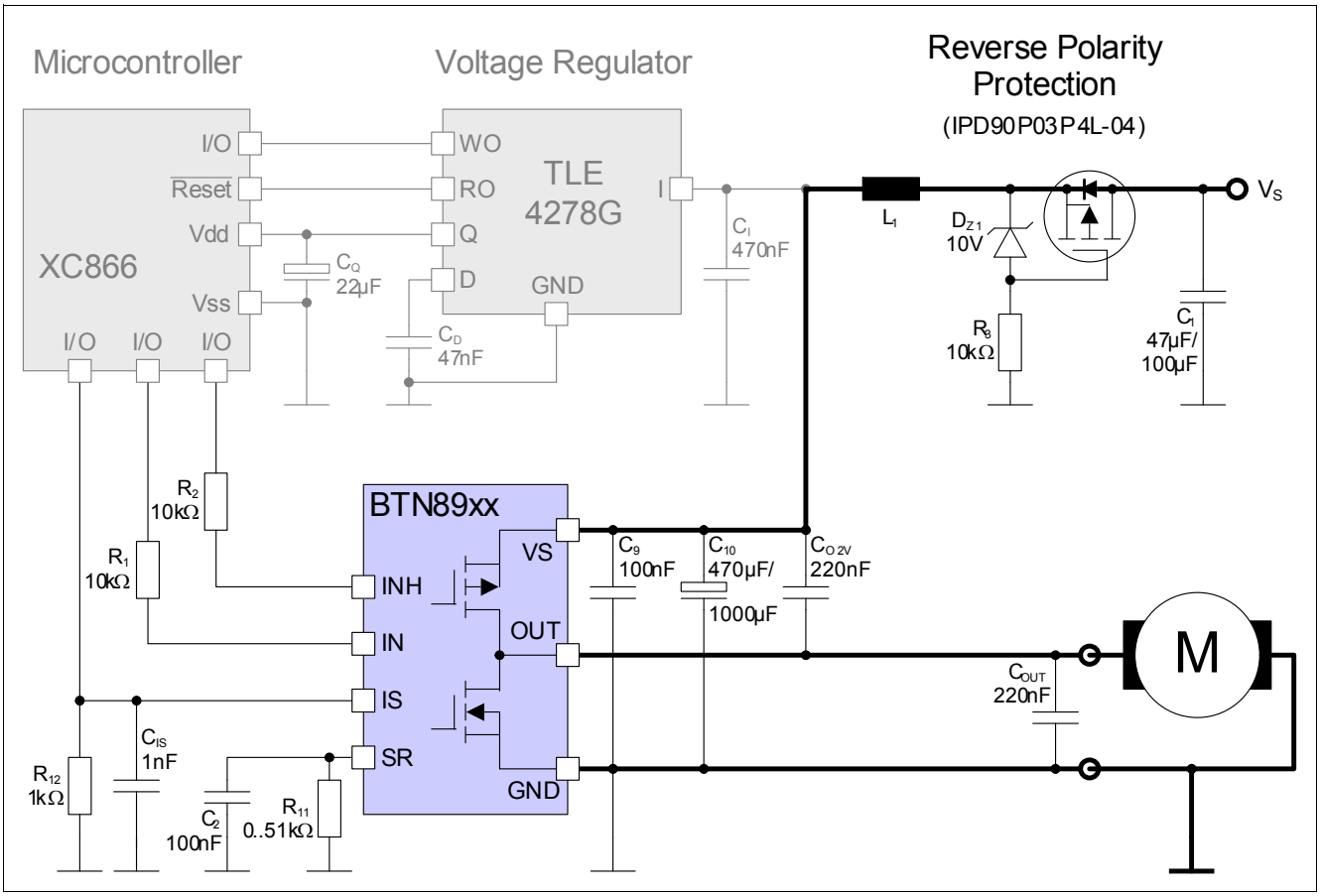

Figure 2 Application circuit for a monodirectional motor with BTN89xy

2.2 H-Bridge configuration for bidirectional motor control

With the NovalithIC™ family it is easy to build an H-bridge for bidirectional DC motor control by simply combining two devices in H-bridge configuration, as it is shown in **Figure 3**.

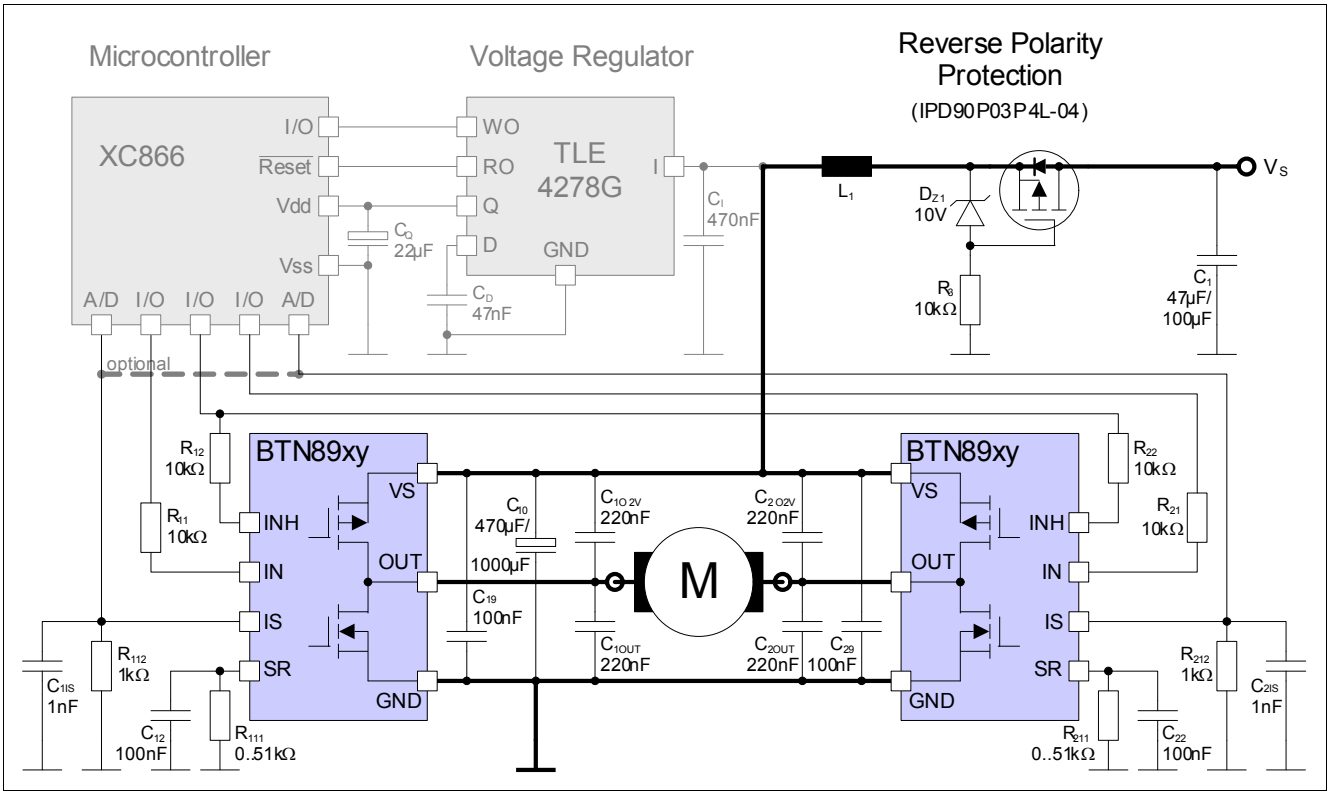

Figure 3 Application circuit for a bidirectional motor with BTN89xy H-bridge

3 Parasitic Inductance

In high-current applications, which the NovalithIC™ family is designed for, special care must be taken for parasitic inductors. The same is valid in case of very high frequencies, which are interesting with regard to EMC considerations.

Each kind of wire in the application is an inductor, e.g. PCB wires, bond wires, etc. The wire inductance can be estimated with

- 1mm PCB wire length approximately 1.2 nH
- 1 PCB via approximately 1 nH

The voltage drop of a wire can be calculated in the following way:

(3.1)

$$U_L = L \cdot \frac{dI}{dt}$$

As can be seen from this equation, care must be taken with the parasitic wire inductors with increasing current and decreasing switching time. The NovalithIC™ is designed to switch high currents very quickly. This means in applications with NovalithIC™, the parasitic inductors are relevant and special care must be taken.

3.1 Measuring signals at NovalithIC™

The parasitic inductance also has an influence on the measurement results. To measure the true signals at the NovalithIC™ it is mandatory to position the measurement probes directly at the device, as it is shown in **Figure 4**. The probe is connected directly to the V_s-pin of the NovalithIC™ and the reference signal directly to the GND-pin of the device.

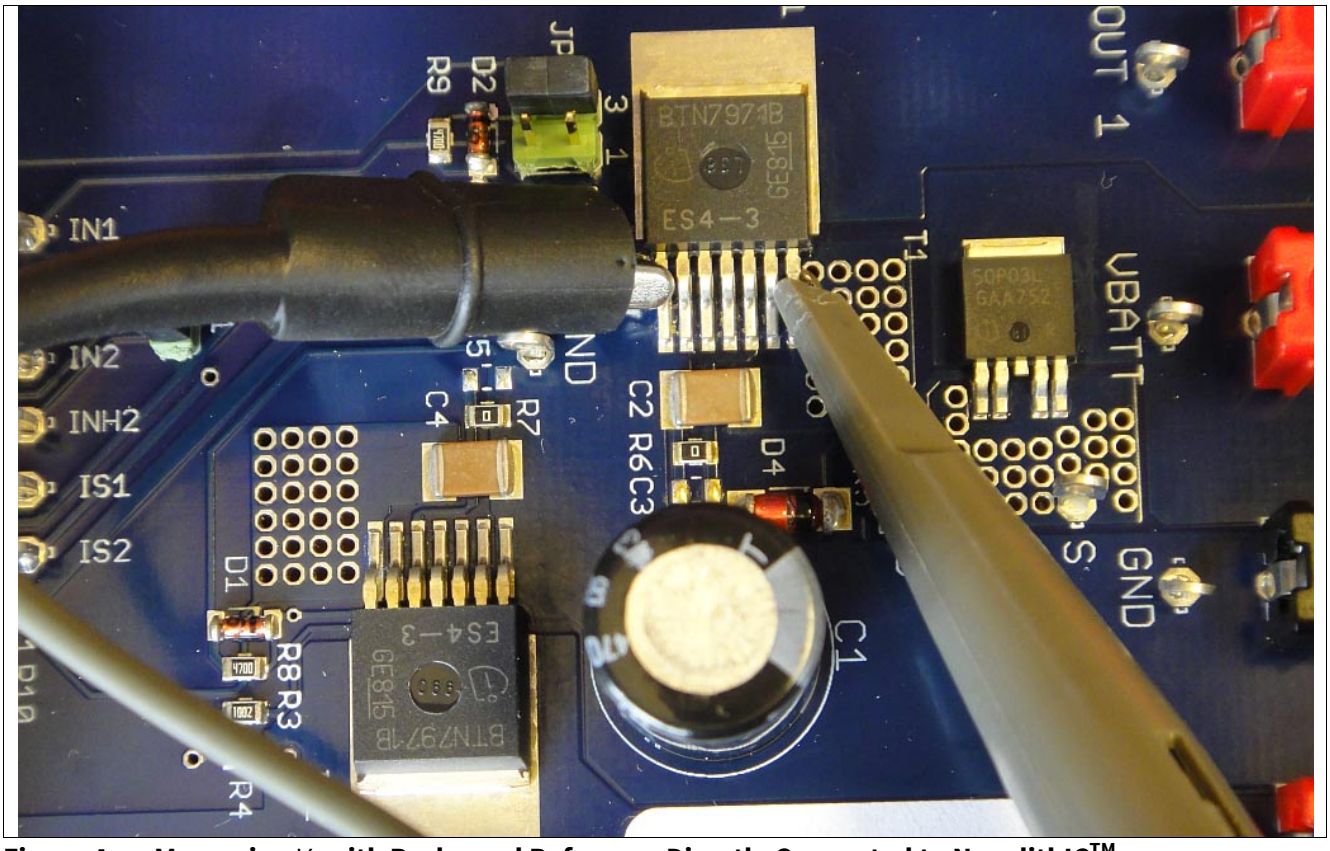

Figure 4 Measuring V_s with Probe and Reference Directly Connected to NovalithIC™

Doing so enables to monitoring of the NovalithIC™ supply voltage when high currents are switched. For example when a short-circuit current is switched, this is the only possibility for measurement if the DC-link capacitor is sufficient to keep the supply voltage above the undervoltage detection threshold (also see **Chapter 4.2**).

4 Design Guideline

For a safe and sufficient motor control design, discrete components are needed. Some of them must be dedicated to the motor application and some to the NovalithIC™.

4.1 Schematic and layout design rules

Figure 5 and **Figure 6** show an example of a schematic plus a corresponding layout for a half-bridge motor control with NovalithIC™.

The best performance in terms of parasitic inductance and EMC can be reached with a GND plane, which we strongly recommend be used.

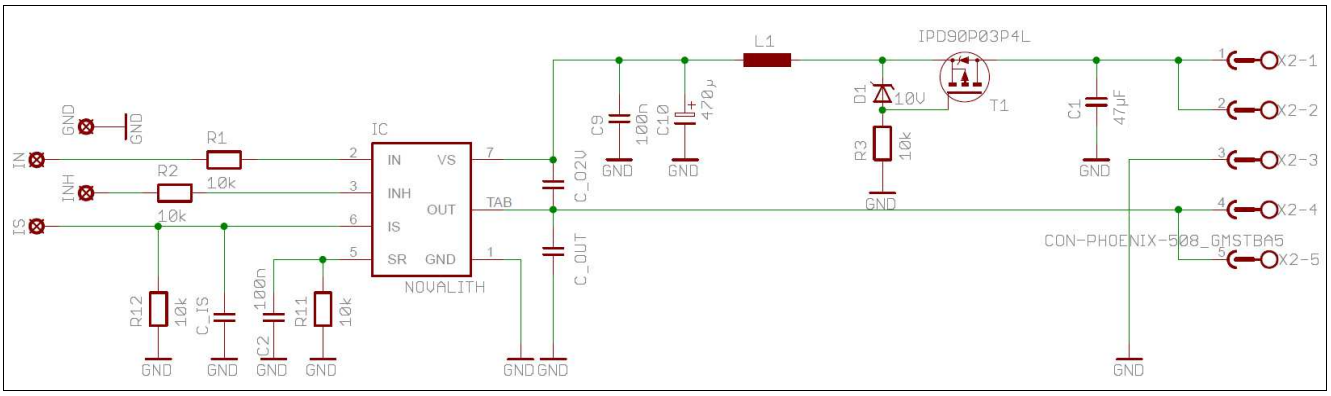

Figure 5 Example of a half-bridge schematic with NovalithIC™

Important design and layout rules:

The basis for the following items is the parasitic inductance of electrical wires, as described in **Chapter 3**.

- C10, so called DC-link capacitor: This electrolytic capacitor is required to keep the voltage ripple at the V_S-pin of the NovalithIC™ low during switching operation (the measurement procedure for the supply voltage is described in **Chapter 3.1**). It is strongly recommended that the voltage ripple at the NovalithIC™ V_s-pin to GND-pin be kept below 1 V peak-to-peak. The value of C10 must be aligned accordingly. See **Equation (4.9)**.
  Most electrolytic capacitors are less effective at cold temperatures. It must be assured that C10 is also effective under the worst case conditions of the application.
  The layout is very important. As shown in **Figure 6**, the capacitor C10 must be positioned with very short wiring at the NovalithIC™. This must be done to keep the parasitic inductors of the PCB-wires as small as possible.
- C9: This ceramic capacitor supports C10 to keep the supply voltage ripple low and covers the fast transients between the V_s-pin and the GND-pin. The value of this ceramic capacitor must be chosen so that fast V_s-ripple at the NovalithIC™ does not exceed 1 V peak-to-peak.
  The layout wiring for C9 must be shorter than for C10 to the NovalithIC™ to keep the parasitic PCB-wire inductance as small as possible. In addition the parasitic inductance could be kept low by placing at least two vias for the connection to the GND-layer.
- C_O2V: This ceramic capacitor is important for EMI in order to avoid entering electromagnetic disturbances into the NovalithIC™ as much as possible. Good results have been achieved with a value of 220 nF.
  In terms of layout, it is important to place this capacitor between “OUT” and “V_s” without significant additional wiring from C_O2V to the V_s- and OUT-line.
- C_OUT: This ceramic capacitor helps improve the EMI and the ESD performance of the application. Good results have been achieved with a value of 220 nF.

To keep the RF and ESD out of the board, the capacitor is most effective when positioned directly on the board connector. In addition, the parasitic inductance could be kept low by placing at least two vias for the connection to the GND-layer.

- C1: This ceramic capacitor helps to improve the EMI and the ESD performance. In combination with L1 and C10 plus C9 a Pi-filter improves the electromagnetic emission on the V_s-line.
  Layout rules are the same as for C_OUT.

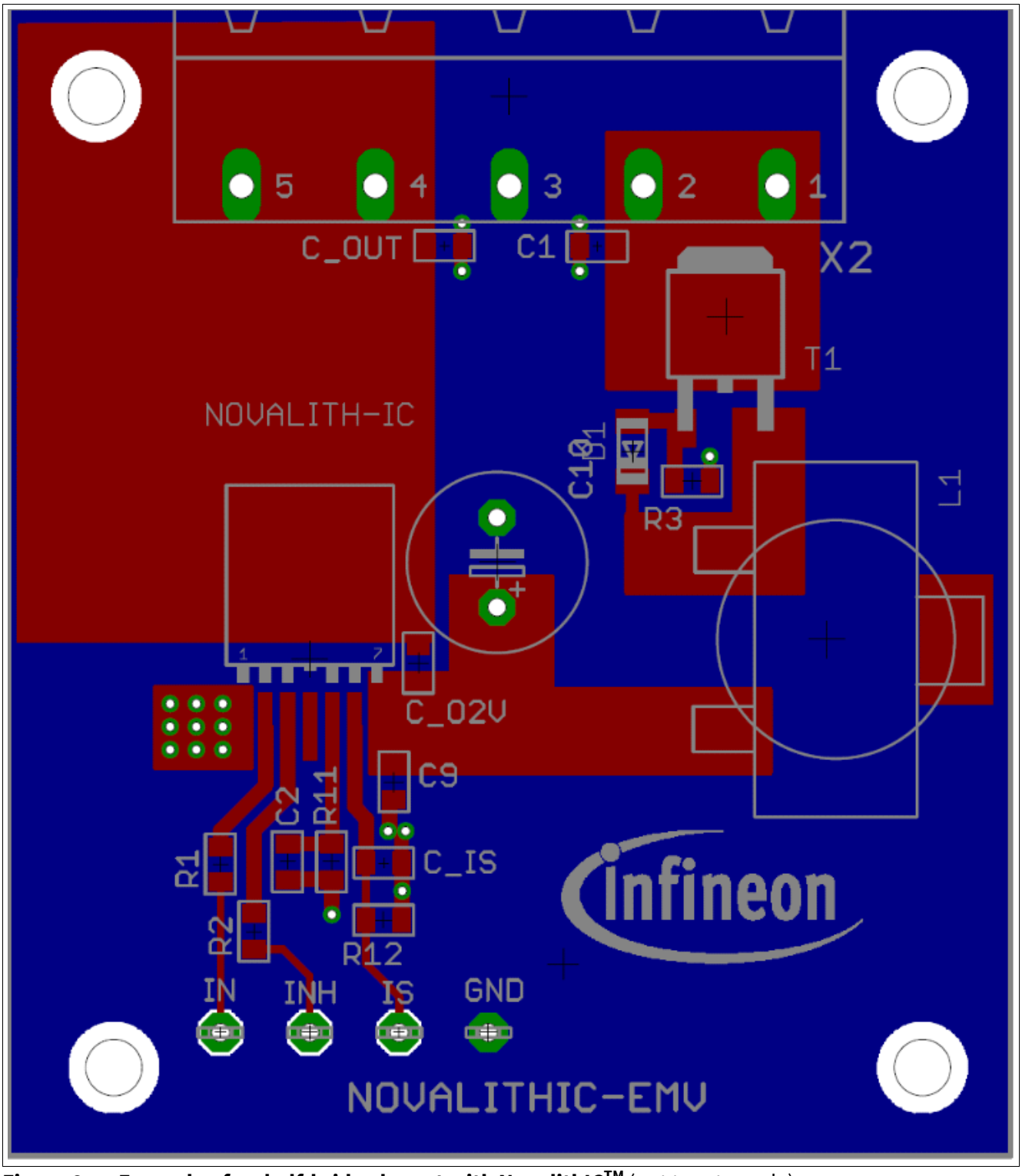

Figure 6 Example of an half-bridge layout with NovalithIC™ (not true to scale)

Other components:

- T1, D1 and R3: Reverse polarity protection. See **Chapter 4.5**.
- R11: Slew rate resistor according to data sheet.
- C2: Stabilization for slew rate resistor (R11).
- R12: Resistor to generate a current sensing voltage from the IS current.
- C_IS: Ceramic capacitor for EMI improvement. GND connection with at least two GND-vias. A good value is 1 nF.
  In case the current should be measured during the PWM-phase, this capacitor must be adapted to the ON-time inside the PWM-phase.
- R1 and R2: Device protection in case of µC pins shorted to V_S.

4.2 DC-link capacitor

For the stability of the DC-link voltage a sufficient capacitor is mandatory (in **Figure 2**, **Figure 3** and **Figure 5** it is C10). This is one of the most important component in a motor design with semiconductor switches.

The DC-link capacitor could be insufficient, because:

- The capacitor value is too small.
- The ESR of the capacitor is too high.
- When cold the capacitor value is too small.
- The distance between the DC-link capacitor and the NovalithIC™ is too large.
- The wiring between the DC-link capacitor and the NovalithIC™ is too long (see **Chapter 3**).

The value must be chosen carefully, taking the undervoltage toggling into account, which is described in **Chapter 4.2.2**.

4.2.1 Calculation of the DC-link capacitor and Pi-filter

As already mentioned in the design- and layout-rules of **Figure 5** the voltage ripple at the NovalithIC™ V_S-pin must not exceed 1 V peak-to-peak. The necessary DC-link capacitor can be estimated in the following way:

Motor control with PWM means for the DC-link voltage to provide energy pulses during the “ON-phase” of the PWM cycle. The DC-link pulses are shown in **Figure 7**.

This energy must be provided by the DC-link capacitor. This can generally be described with

(4.1)

$$E = \frac{1}{2} \cdot C \cdot V^2 = P \cdot T$$

(4.2)

$$C = C_{DC-link}$$

The voltage at the DC-link capacitor consists of the DC-part and the delta voltage from the supply ripple:

(4.3)

$$V = V_{S,DC} + \Delta V_S$$

The total power in this system consists of the DC-power plus the power of the energy pulse (E_{pulse}), which provides the energy to the motor during the ON-phase of the half bridge.

(4.4)

$$P = P_{DC} + \Delta P$$

The maximum pulse length is determined by the PWM frequency, theoretically at a duty cycle of 100%:

(4.5)

$$T = T_{pulse} = T_{PWM} = \frac{1}{f_{PWM}}$$

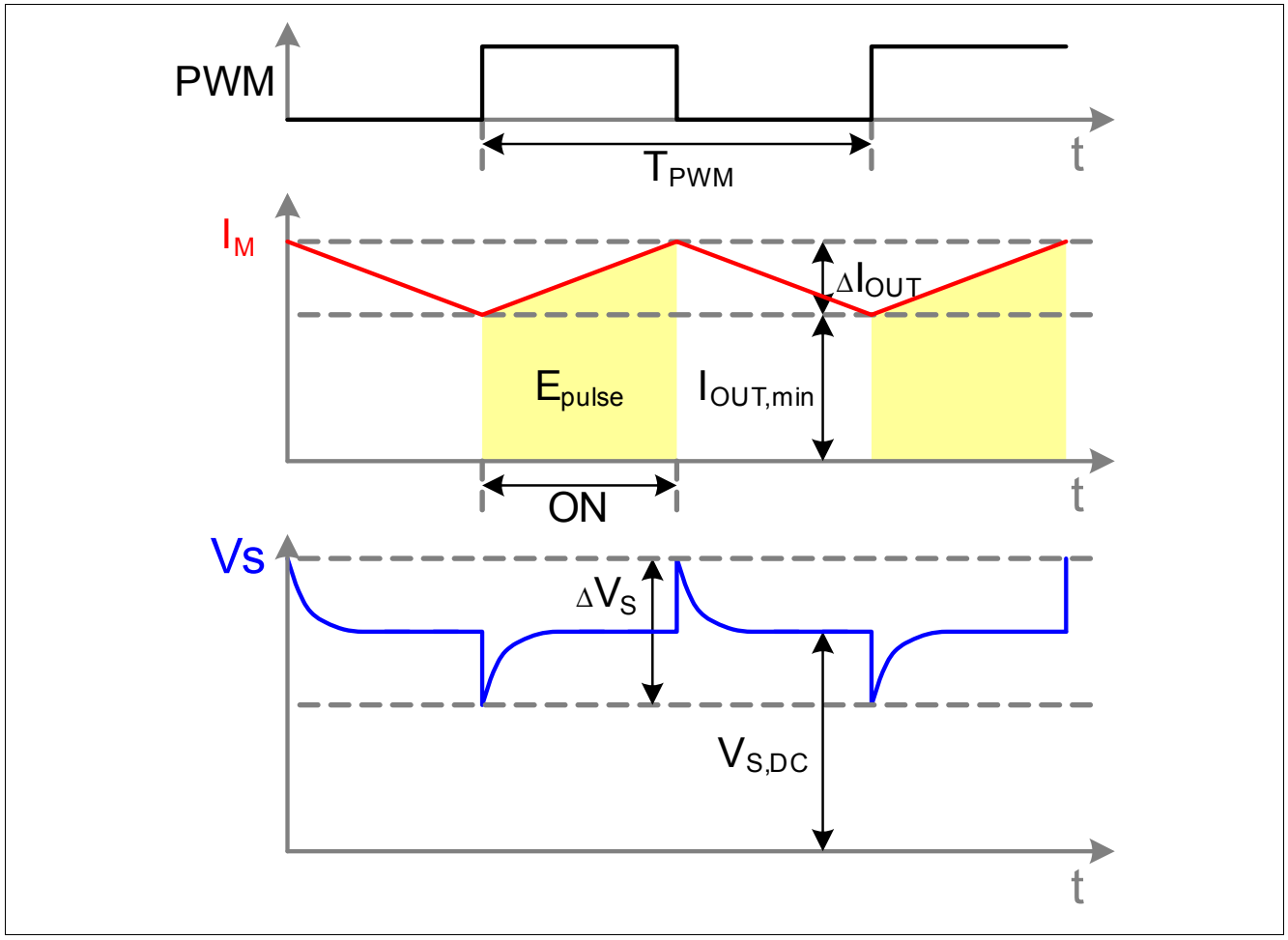

Figure 7 PWM control (PWM = IN-pin-signal, I_M = motor current and V_S = V_S-pin-voltage @ NovalithIC)

Insertion of **Equation (4.2)** to **Equation (4.5)** into **Equation (4.1)**

(4.6)

$$E = \frac{1}{2} \cdot C_{DC-link} \cdot (V_{S,DC} + \Delta V_S)^2 = (P_{DC} + \Delta P) \cdot T_{PWM}$$

(4.7)

$$\frac{1}{2} \cdot C_{DC-link} \cdot (V_{S,DC}^2 + 2 \cdot V_{S,DC} \cdot \Delta V_S + \Delta V_S^2) = P_{DC} \cdot T_{PWM} + \Delta P \cdot T_{PWM}$$

(4.8)

$$\cancel{\frac{1}{2} \cdot C_{DC-link} \cdot V_{S,DC}^2} + C_{DC-link} \cdot V_{S,DC} \cdot \Delta V_S + \underbrace{\frac{1}{2} \cdot C_{DC-link} \cdot \Delta V_S^2}_{negligible} = \cancel{P_{DC} \cdot T_{PWM}} + \Delta P \cdot T_{PWM}$$

Finally the equation to calculate the DC-link capacitor is:

(4.9)

$$\boldsymbol{C_{DC-link} \geq \frac{\Delta P \cdot T_{PWM}}{V_{S,DC} \cdot \Delta V_S}}$$

Based on **Equation (4.1)** and referring to the energy of on single pulse, as marked with E_{pulse} (≈ ΔP • T_{PWM}) in **Figure 7**:

(4.10)

$$\Delta P = V_S \cdot I_{nom} \approx V_S \cdot (I_{OUT,\min} + \frac{1}{2} \Delta I_{OUT})$$

The DC-link capacitor is primarily the energy buffer for the switching process of the PWM motor control. Secondly it is part of the Pi-filter. This means first the DC-link capacitor must be calculated according to **Equation (4.9)**. Based on this, it is recommended that the second capacitor of the Pi-filter C1 be estimated with:

(4.11)

$$\boldsymbol{C_1 = \frac{1}{10} \cdot C_{DC-link} = \frac{1}{10} \cdot C_{10}}$$

Generally the border frequency of the L_1-C_1-filter is determined with

(4.12)

$$f_g = \frac{1}{2 \cdot \Pi \cdot \sqrt{L_1 \cdot C_1}}$$

We recommend setting the border frequency f_g to half the value of the PWM -frequency f_{PWM}.

(4.13)

$$f_g = \frac{1}{2} \cdot f_{PWM} = \frac{1}{2 \cdot \Pi \cdot \sqrt{L_1 \cdot C_1}}$$

(4.14)

$$L_1 = \frac{1}{\Pi^2 \cdot f_{PWM}^2 \cdot C_1}$$

Summary:

First calculate the DC-link capacitor with **Equation (4.9)**.

Second calculate the other capacitor of the Pi-filter with **Equation (4.11)**.

Then calculate the inductor of the Pi-filter with **Equation (4.14)**.

And last but not least, do not forget the important layout rules and how to measure the supply voltage correctly.

4.2.2 Undervoltage toggling

The power supply cable of most modules in a car are several meters long. The longer the supply cable is, the higher its parasitic inductance. In addition, most modules have a Pi-filter at the supply line with a inductor for EMC reasons. The sum of the supply line inductances have a significant influence on the V_s-voltage. When switching the motor ON during a normal motor start or PWM control, with a insufficient DC-link capacitor the supply voltage drops below the undervoltage threshold and the NovalithIC™ is switched to tristate. The supply voltage recovers above the undervoltage threshold and the NovalithIC™ switches on again, again dropping below the undervoltage threshold ...

This effect can result in frequencies higher than 100 kHz, as is shown in **Figure 8**. The device will be damaged by the power dissipation of the switching losses, which is faster than the reaction time of the over temperature shut down, because of the high switching frequency.

The undervoltage toggling will be worse if the OUT is shorted to GND.

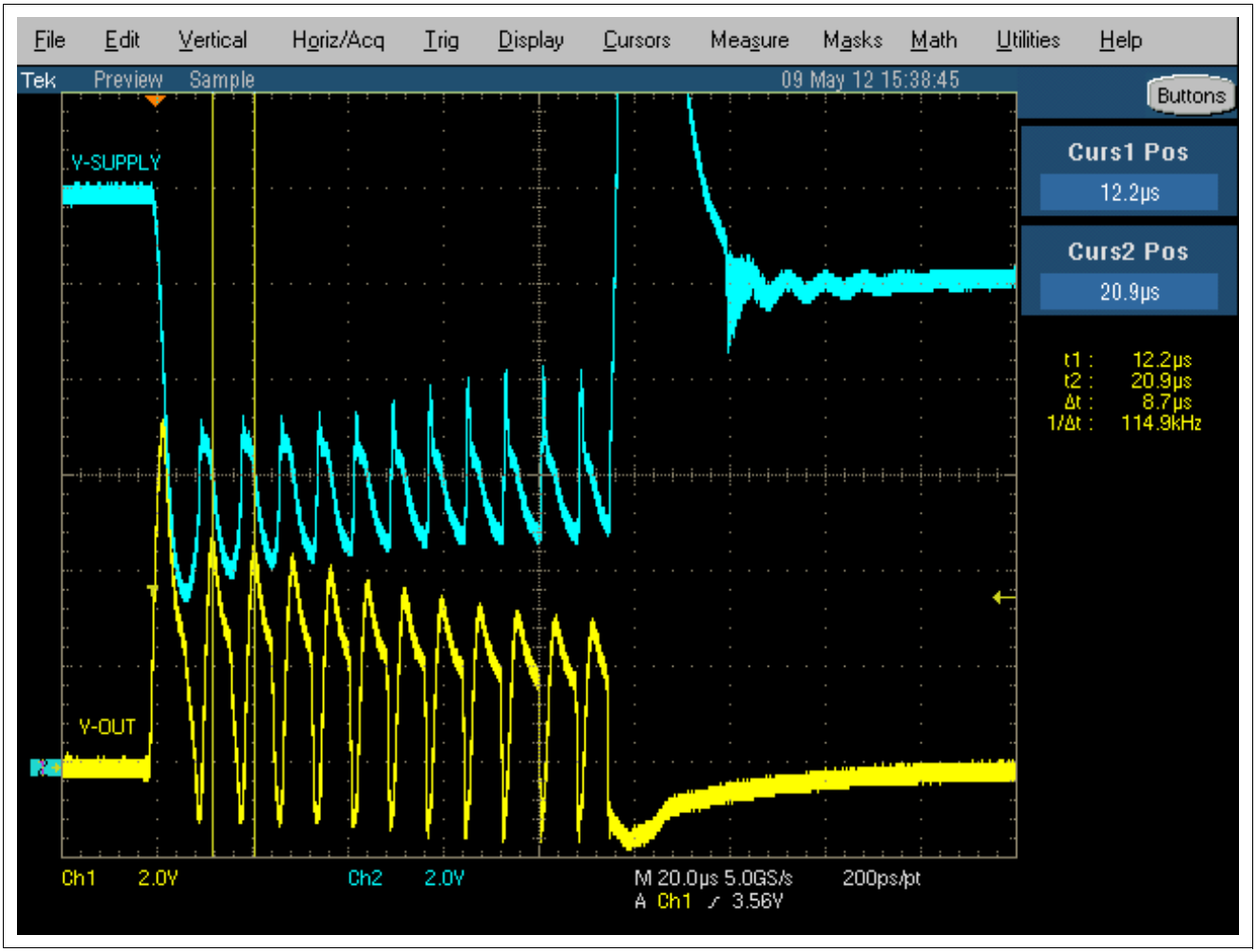

Figure 8 Undervoltage toggling started by short to GND and enabled by an insufficient DC-link capacitor

With a sufficient DC-link capacitor the supply voltage drop is limited so as not to reach the undervoltage threshold, as is shown in **Figure 9**.

Both measurements in **Figure 8** and **Figure 9** are conducted with the Infineon “NovalithIC Demo Board V2.1” with BTN7933. The “ON-time” is limed to 100 µs by the IN-signal, as shown in **Figure 9**. Only the DC-link capacitor is switched between the two measurements.

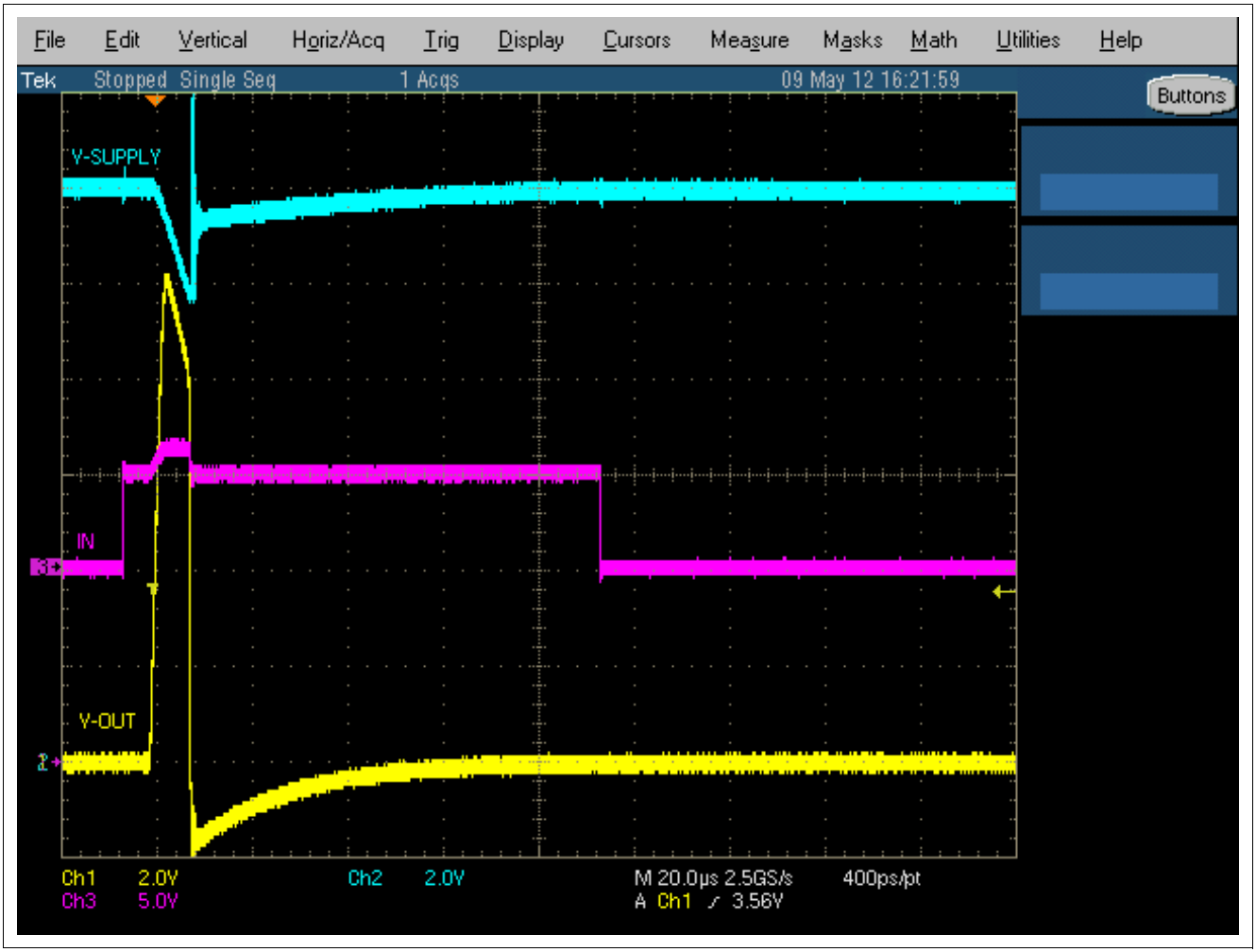

Figure 9 The sufficient DC-link capacitor avoided undervoltage -toggling in case of a short to GND

4.3 Ground references

Depending on the different functionalities, different ground references for each pin of the NovalithIC™ have to be considered, especially in high current applications, in which ground shifts might occur due to parasitic inductances and line resistantaces of the PCB.

Based on the example schematic in **Figure 5**, the different ground reference concepts are illustrated in **Figure 10**.

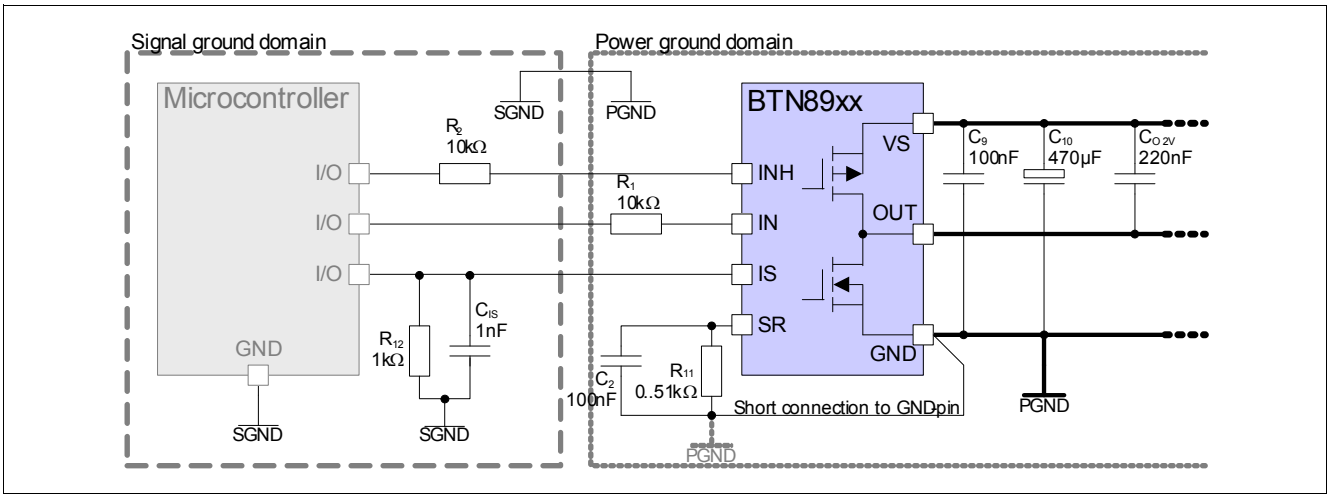

Figure 10 Simplified schematic illustrating the ground references for the signal ground (SGND) and power ground (PGND) of the NovalithIC™

Design rules for the ground reference:

- IS-pin: The reference ground for the current sense and failure flag detection is ideally the Analog-to-Digital Converter's / Microcontroller's ground as the IS-pin is a current source. If this is implemented, the absolute maximum ratings shall be respected, also in the case of a ground shift between the Microcontroller's (signal-) ground and the device's ground (GND-pin). Thus it is recommended to connect R12 and C_IS to the signal ground (SGND) as shown in **Figure 10** thus eliminating the influence of a ground shift.
- SR-pin: For the slew rate functionality the reference ground is the device's ground, the GND-pin. Thus R11 and C2 (in **Figure 5** and **Figure 10**) should be placed close to the device and be connected directly to the device's ground with minimal wiring to prevent any influence of disturbance through ground shifts.
- IN/INH-pins: For the digital input pins IN and INH the internal ground reference is the GND-pin of the NovalithIC™ thus it has to be obtained, that a ground shift between the Microcontroller's (signal-) ground, which is controlling the pins, and the device's ground (GND-pin) isn't influencing the switching behavior and the absolute maximum ratings are respected.

4.4 Driving inductive loads over long wires

Inductive loads have a lowpass filter characteristic, like a motor. Because of this, the wire from the NovalithIC™ OUT to the motor injects electromagnetic disturbances into the OUT-pin. This antenna effect increases as the length of the motor wire increases.

The definition of a long motor wire strongly depends on the application and the environment. To provide a general idea, wire lengths of approximately 20 cm and more are considered as "long wire". The motor wire should therefore be as short as possible.

4.4.1 PWM operation

In case of a long motor wire and PWM operation the electromagnetic emission (EME) increases with the wire length and with the switching speed (inversion of $t_{r(HS)}$, $t_{r(LS)}$, $t_{f(HS)}$ and $t_{f(LS)}$). In this case it is advantageous to reduce the switching speed with the slew rate resistor at the SR-pin (see **Figure 5**, R_{11}). Reducing the switching speed has probably a impact on the PWM-frequency, which may needs to be adapted. In any case the power dissipation and the cooling concept needs to be reviewed. The slew rate resistor at the SR-pin should not exceed the max. slew rate resistor value of the data sheet $R_{SR} \leq 51$ kΩ.

4.4.2 Current sense

A long motor wire can pick up electromagnetic disturbances which could influence the current sense signal at the IS-pin. If a high accuracy of the current measurement is needed, it is recommended to use the IS-pin as status flag diagnosis and perform the current measurement with an external shunt plus current sense amplifier. An schematic example is shown in **Figure 11**.

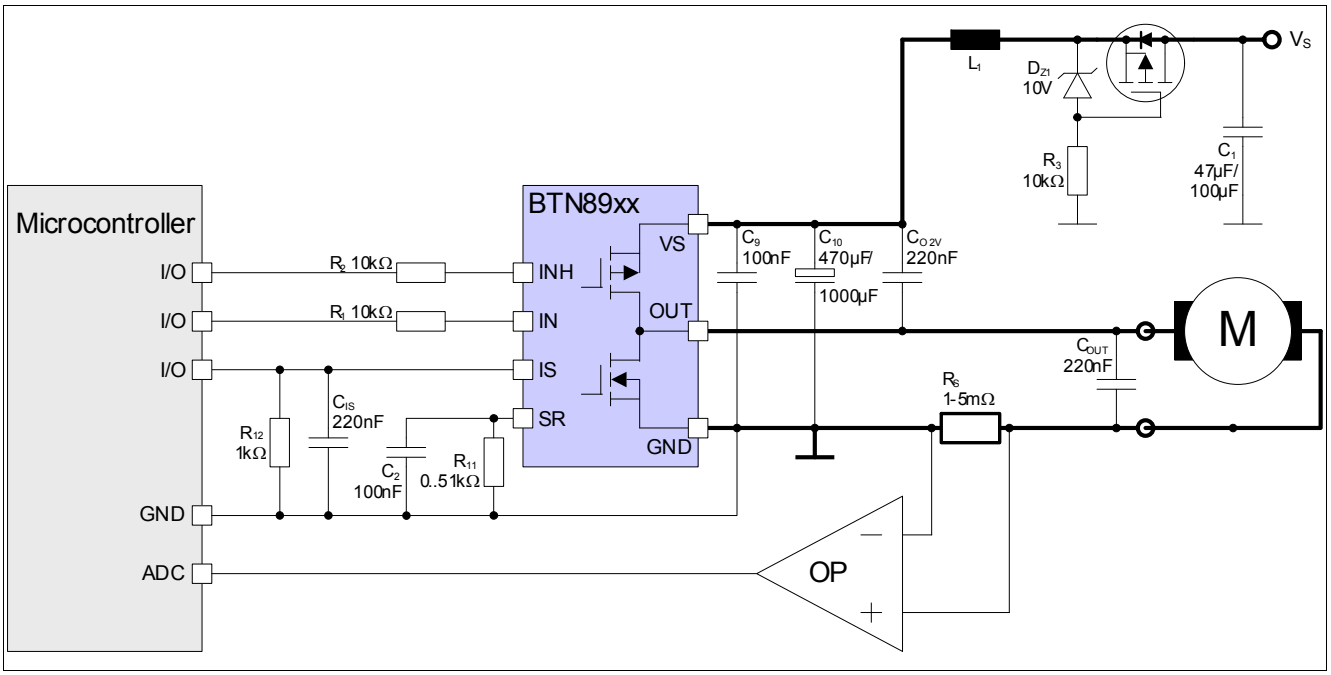

Figure 11 BTN89xx with external current measurement

4.5 Reverse polarity protection

The semiconductor technology of NovalithIC™ used has a parasitic PN -diode from “GND” to the supply voltage pin “V_S”. If the supply voltage is inverted, a huge current will flow through this parasitic PN -diode and will damage the device. With reverse polarity protection, the reverse current is not possible and the semiconductor components of the design are protected.

In the schematic in **Figure 5**, reverse polarity protection is provided with a P-channel MOSFET (IPD90P03P4L-04), a zener-diode (D_1) and a resistor (R_3).

Normal operation V_s > GND:

- P-MOSFET OFF: The application is supplied by the body-diode of the reverse polarity protection transistor (IPD90P03P4L-04), e.g. in case of a power-up. The status “P-MOSFET ON” will quickly be reached.
- P-MOSFET ON: After the power-up in which the body diode was used as a supply path, the zener diode plus the resistor will generate a gate-source voltage in the range of 10 V and the P-MOSFET is in ON-state. Only the $R_{DS,on}$ is in the power supply path.

Reverse polarity condition V_s < GND:

- The gate source voltage of the reverse polarity protection transistor is continuously “LOW” and the transistor is switched OFF. No current can flow in this state. The application will not be damaged.

4.6 Cooling

The NovalithIC™ half-bridge, driving high current generates power dissipation. These are R_{ON} losses and switching losses in case of PWM control, which heat up the device. For details, please see **Chapter 7**. The

package PG-TO263-7-1 provides a low thermal resistance which can be combined with a heat sink on the PCB to avoid exceeding the absolute maximum temperature values of the data sheet.

In **Figure 6** a cooling area (brown top layer, where the NovalithIC™-OUT is connected) has already been drawn. Depending on the power dissipation, other thermal sources on the PCB and the ambient temperature, the cooling needs to be carefully adapted to each application.

In addition the reverse polarity protection transistor T1 (**Figure 5** and **Figure 6**) generates $R_{DS,on}$ power losses and the cooling concept for this transistor must ensure that the device does not exceed the absolute maximum junction temperature.

5 Current Sense Improvement

The NovalithIC™ half-bridge-family has a current sense function with an IS-pin which provides the output current divided by a factor, so called dk_{ILIS}. The precision of the current measurement could be significantly improved by eliminating the IS-offset, dk_{ILIS}-production spread and respecting the temperature dependency of the dk_{ILIS}.

The table below provides an overview of possible combinations of procedures to reduce current measurement errors.

Table 1 Current sense procedure and benefits

Procedures			Load current tolerance
Offset compensation			±28%
Offset compensation	Device dkILIS measurement		±10%
Offset compensation	Device dkILIS measurement	Temperature estimation	±6%
Offset compensation	Device dkILIS measurement	Temperature compensation	±3%

5.1 Characteristic of the dk_{ILIS}

The dk_{ILIS} has characteristic dependencies. The most important ones with respect to the supply voltage V_s and with respect to the temperature, are described in this chapter.

5.1.1 Supply voltage dependency of dk_{ILIS}

The dependency of the dk_{ILIS} of the supply voltage V_s is negligible, as **Figure 12** shows. This means the supply voltage can be ignored when calculating the load current.

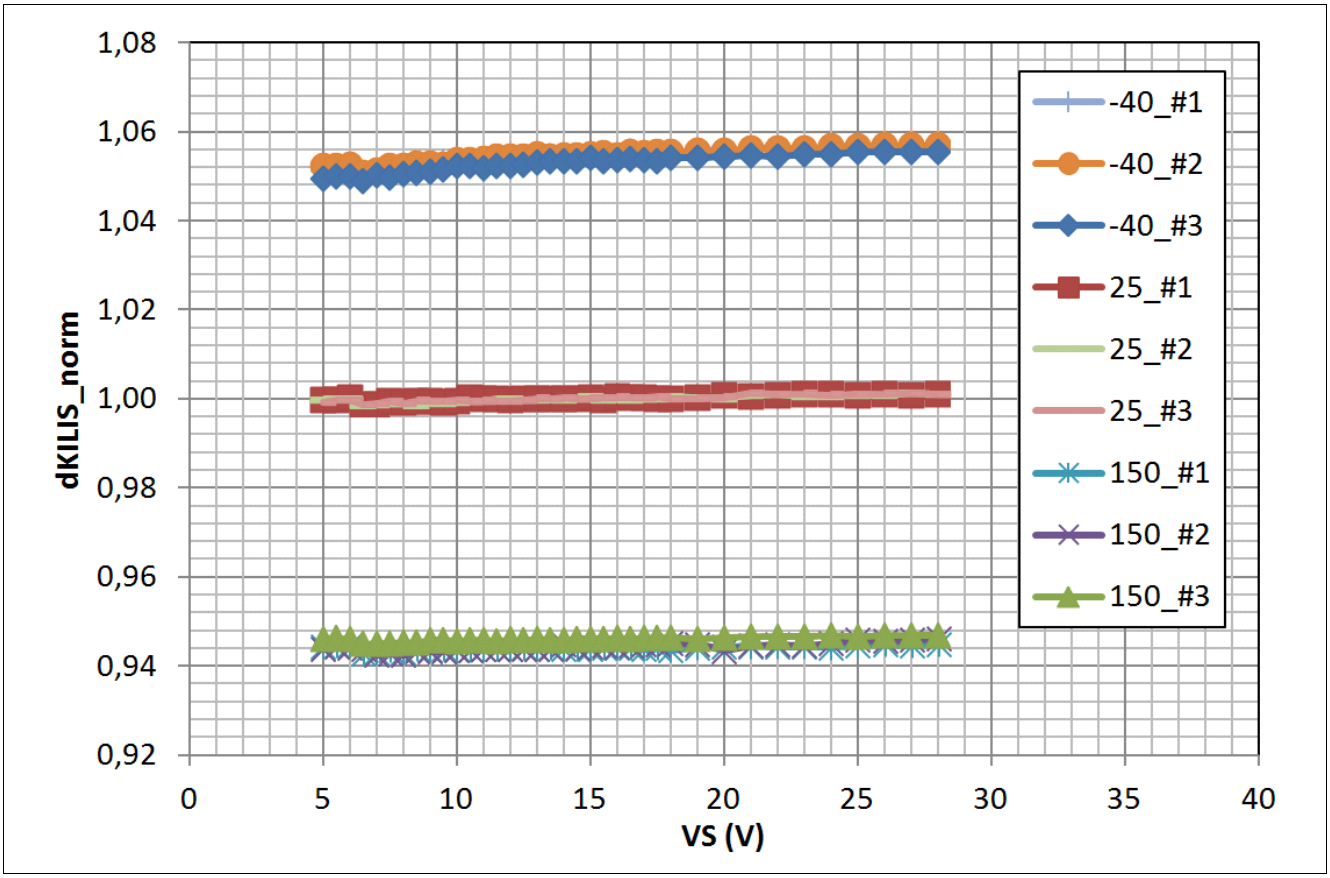

Figure 12 dk_{ILIS} vs. the supply voltage V_s

5.1.2 TC 1000 life time tests

Life time tests of 1000 hours with a dedicated device stress set up and with many devices from different production lots showed the dk_{ILIS} is decreasing over life time up to -3%.

5.1.3 Temperature drift of the dk_{ILIS}

Figure 13 and **Figure 14** show the characteristics of the dk_{ILIS} vs. temperature and production spread with a scaling at 25°C, including a series of lab measurement points for one device.

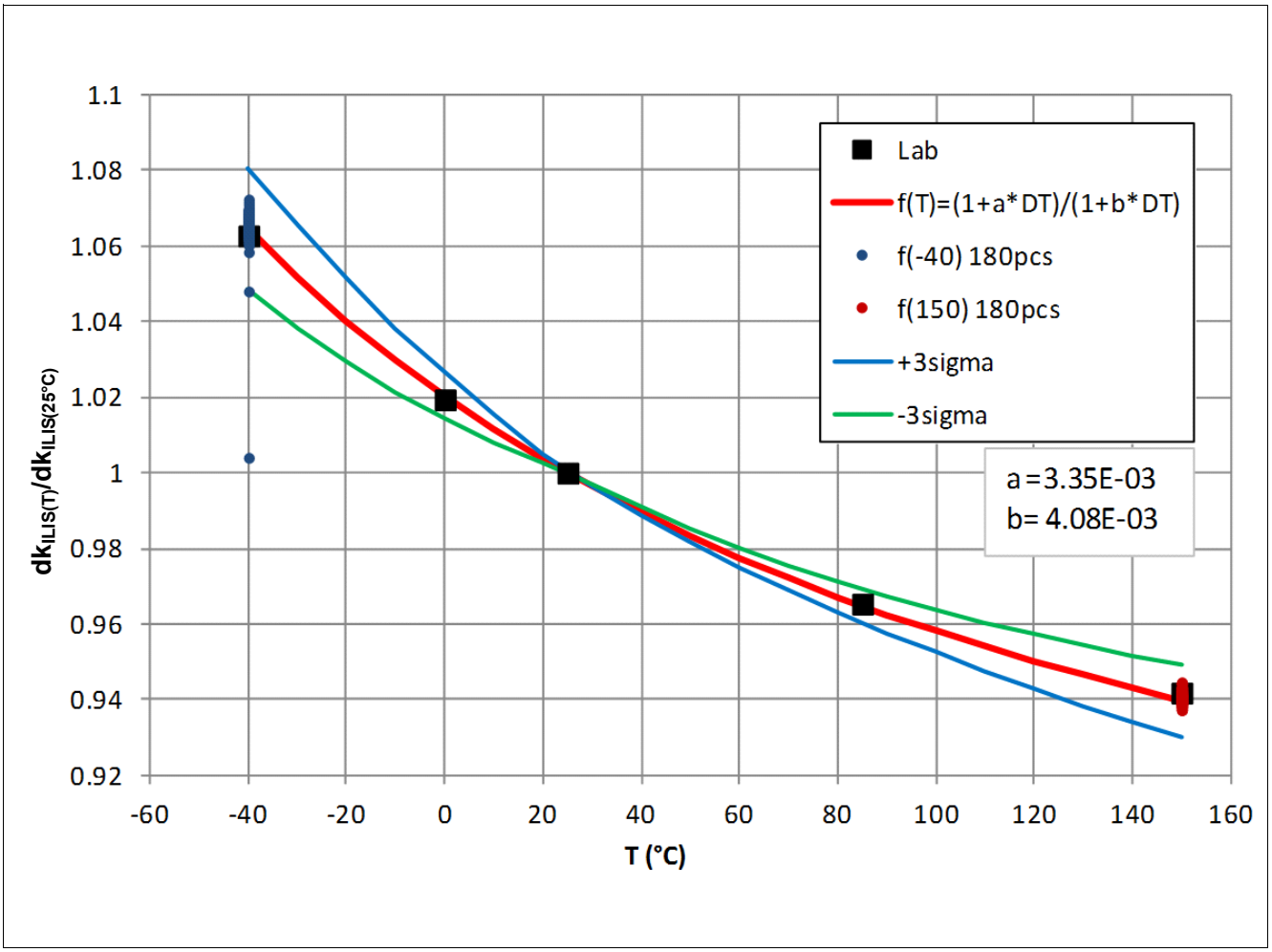

Figure 13 BTN8960 /62 dk_{ILIS} vs. temperature

The function f(T) is dependent on the temperature coefficient of the shunt resistance in the control chip (a), the temperature coefficient of the shunt (b) and DT = T - 25 °C.

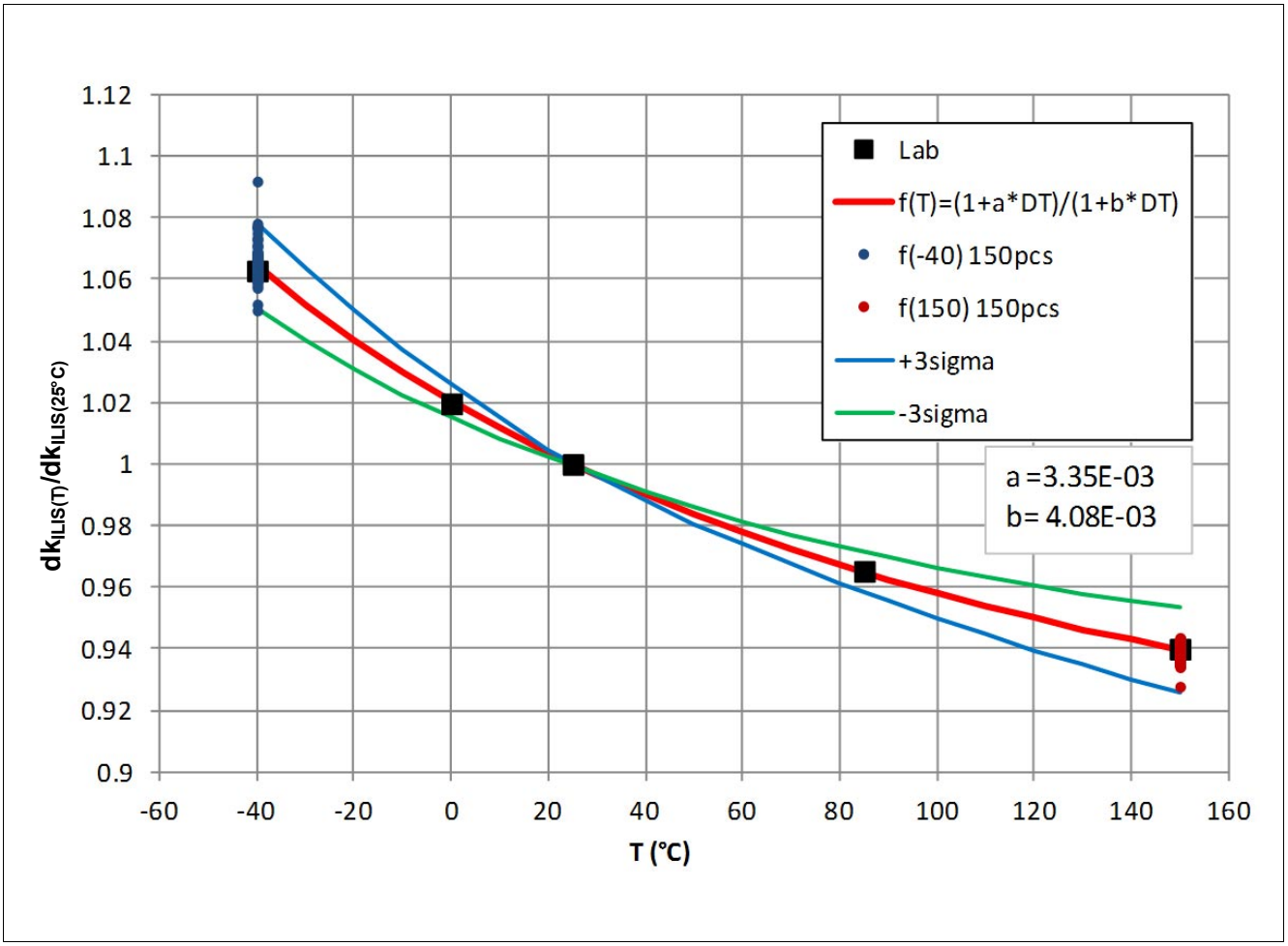

Figure 14 BTN8980 /82 dk_{ILIS} vs. temperature

The function f(T) is dependent on the temperature coefficient of the shunt resistance in the control chip (a), the temperature coefficient of the shunt (b) and DT = T - 25 °C.

5.2 Offset compensation

The BTN89xy series is featured with an artificial offset current at the IS-pin. This is shown in **Figure 15**.

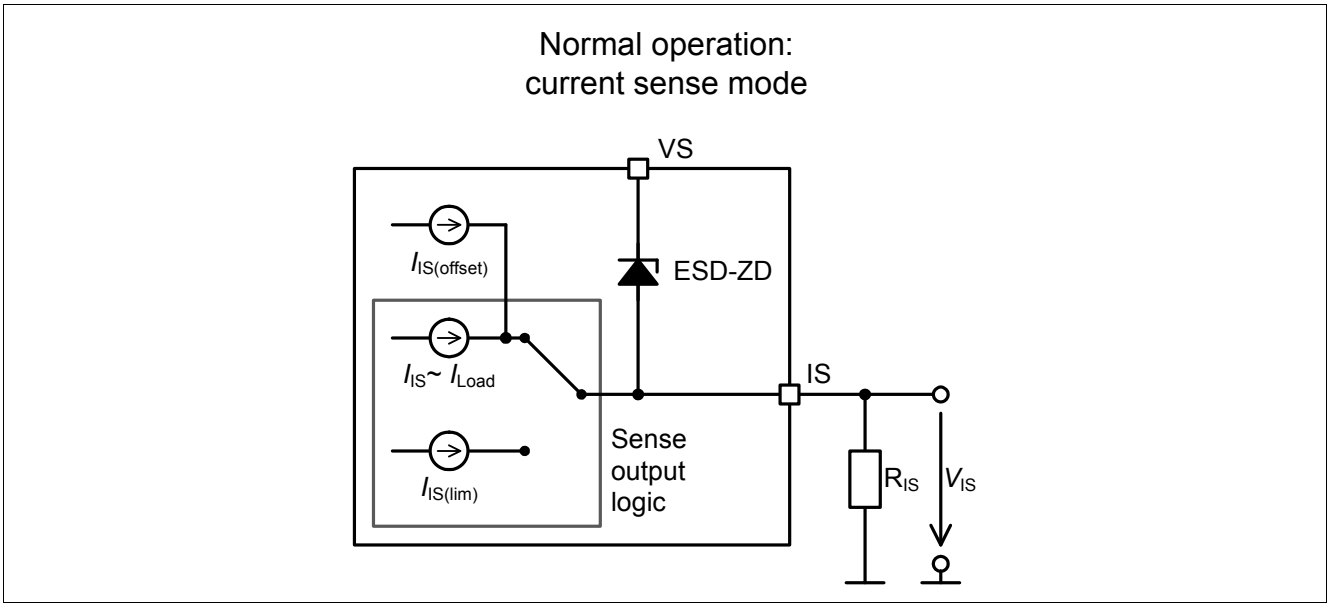

Figure 15 IS-Pin Internal Structure

With this structure, it is possible to always have a measurable offset at IS without a load current. This makes it easy to measure the offset with the microcontroller, store the offset value and process this in the current measurement procedure.

The offset must be compensated to allow a precise current measurement with the IS-pin.

The offset should be compensated before activating the load. When an application such as a fuel pump runs constantly with PWM, you can perform the offset compensation when INH=high and IN=low. In the PWM-phase, the best measurement results are achieved just before the rising edge of the IN-signal.

With this procedure, the specified dk_{ILIS} of ±28% could be reached, even for small load currents. This includes production spread, temperature dependency and aging. Most errors are caused by production spread, which could be compensated by measuring of the dk_{ILIS} of each device (device-specific dk_{ILIS}). Details of this approach are described in the relevant chapter.

5.3 Device specific dk_{ILIS}

With a measurement of the offset current and one IS-value at a certain load current at 25 °C (e.g. 20 A), it is possible to determine the individual $dk_{ILIS\text{-}device}$ and store it permanently to the microcontroller of the application. With this value, the graphs in **Figure 13** and in **Figure 14** are valid. The extreme values are indicated by the blue line (+3sigma):

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS\text{-}min\text{-}H}$ = 0.93 (blue @ 150 °C)

Taking into account the aging of the device (see **Chapter 5.1.2**) the minimum value of **Figure 13** and **Figure 14** (blue line) must be reduced by 3% (multiplying 0.97). This means the extreme values are as follows:

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS\text{-}min\text{-}H\text{-}old} = dk_{ILIS\text{-}min\text{-}H} * 0.97 = 0.9$

This could be assumed as an error of ±10% including temperature drift and aging.

In this case, the typical value should be assumed as follows:

- $dk_{ILIS\text{-}typ}$ = 0.99

The device calibration could be implemented in the module test sequence.

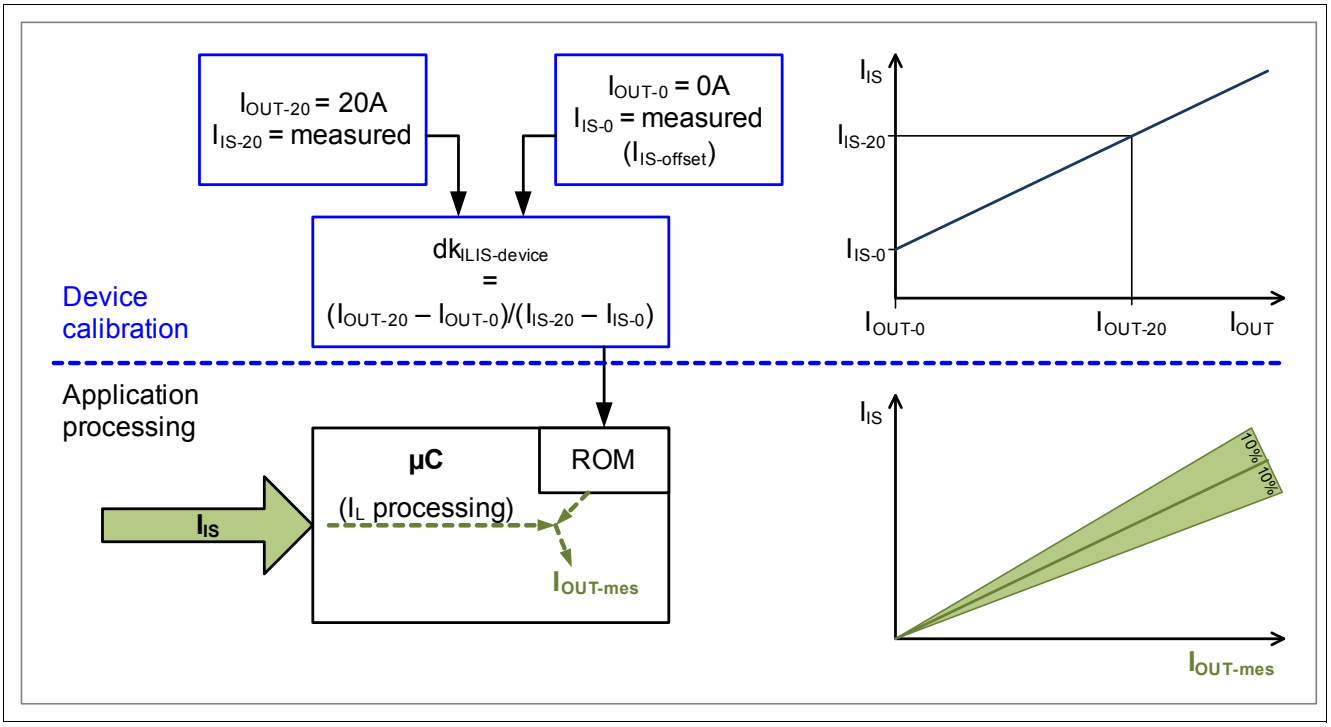

Figure 16 Generating the device fine $dk_{ILIS\text{-}device}$

5.4 Device fine dk_{ILIS} and temperature compensation

On the other hand, the dk_{ILIS} is dependent on the temperature, which is shown in **Figure 13** and **Figure 14**. These figures show a characteristic temperature drift with a low content of production spread. This makes it possible to measure the temperature on the PCB and reduce the temperature dependency by means of a calculation in the microcontroller. This procedure is illustrated in **Figure 17**.