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HITFET™

**BTS3060TF**

Smart Low-Side Power Switch

Single channel, 50 mΩ

**Datasheet**

Rev. 1.0, 2014-07-21

**Automotive Power**

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## 1 Overview

### Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for inductive loads as well as loads with inrush currents

### Basic Features

- Single channel device
- Very low power DMOS leakage current in OFF state
- Electrostatic discharge protection (ESD)
- Green Product (RoHS compliant)
- AEC Qualified



**PG-TO252-3**

### Description

The BTS3060TF is a 50 mΩ single channel Smart Low-Side Power Switch with in a TO252-3 package providing embedded protective functions. The power transistor is built by an N-channel vertical power MOSFET. The device is monolithically integrated. The BTS3060TF is automotive qualified and is optimized for 12V automotive applications.

**Table 1 Product Summary**

|                                                                                  |               |               |
|----------------------------------------------------------------------------------|---------------|---------------|
| Operating voltage range                                                          | $V_{OUT}$     | 3.0 .. 35.0 V |
| Maximum load voltage                                                             | $V_{BAT(LD)}$ | 42 V          |
| Maximum input voltage                                                            | $V_{IN}$      | 5.5 V         |
| Maximum On-State resistance at $T_J = 150^\circ\text{C}$ , $V_{IN} = 5\text{ V}$ | $R_{DS(ON)}$  | 135 mΩ        |
| Nominal load current                                                             | $I_{L(NOM)}$  | 3 A           |
| Minimum current limitation                                                       | $I_{L(LIM)}$  | 10.5 A        |
| Maximum OFF state load current at $T_J = 25^\circ\text{C}$                       | $I_{L(OFF)}$  | 2 μA          |

### Protection Functions

- Latching over temperature protection
- Active clamp over voltage protection
- Current limitation

| Type      | Package | Marking |
|-----------|---------|---------|
| BTS3060TF | TO252-3 | 3060TF  |

**Detailed Description**

The device is able to switch all kind of resistive, inductive and capacitive loads, limited by  $E_{AS}$  and maximum current capabilities.

The BTS3060TF offers ESD protection on the IN Pin which refers to the Source pin (Ground).

The over temperature protection prevents the device from overheating due to overload and/or bad cooling conditions. The temperature information is given by a temperature sensor in the power MOSFET.

The BTS3060TF has a latching thermal shut-down function. The device will turn off until the input is toggled and device reset.

The over voltage protection can be activated during load dump or inductive turn off conditions. The power MOSFET is limiting the drain-source voltage, if it rises above the  $V_{OUT(CLAMP)}$ .

## 2 Block Diagram

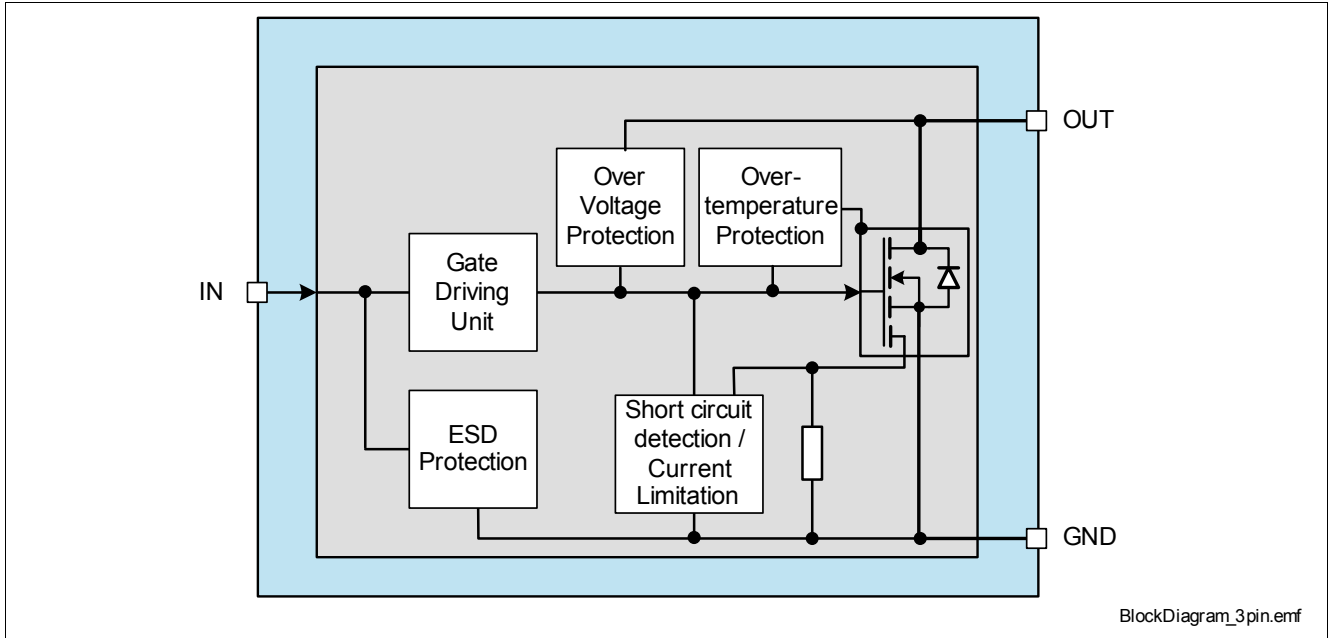


Figure 1 Block Diagram

### 3 Pin Configuration

#### 3.1 Pin Assignment BTS3060TF

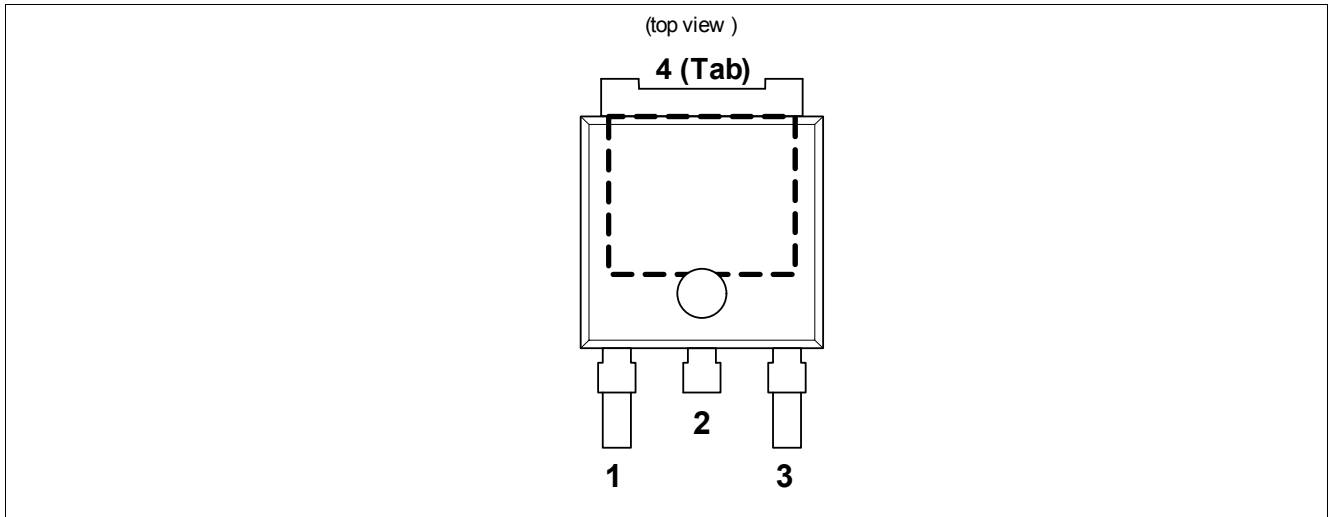


Figure 2 Pin Configuration TO252-3

#### 3.2 Pin Definitions and Functions

| Pin | Symbol | Function                              |
|-----|--------|---------------------------------------|
| 1   | IN     | Input pin                             |
| 2,4 | OUT    | Drain, Load connection for power DMOS |
| 3   | GND    | Ground, Source of power DMOS          |

#### 3.3 Voltage and current definition

Figure 3 shows all external terms used in this data sheet, with associated convention for positive values.

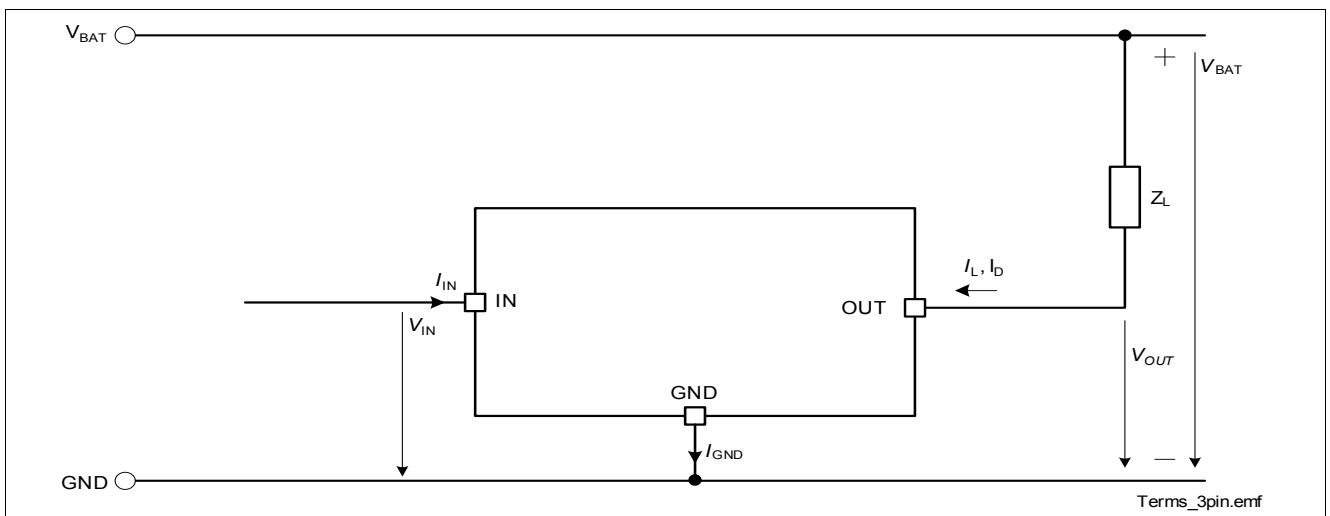


Figure 3 Naming definition of electrical parameters

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings <sup>1)</sup>**

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin  
(unless otherwise specified)

| Pos.                      | Parameter                                                                                            | Symbol         | Limit Values |              | Unit | Note / Test Condition                                                                                                                                                                                                                          |
|---------------------------|------------------------------------------------------------------------------------------------------|----------------|--------------|--------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                           |                                                                                                      |                | Min.         | Max.         |      |                                                                                                                                                                                                                                                |
| <b>Voltages</b>           |                                                                                                      |                |              |              |      |                                                                                                                                                                                                                                                |
| 4.1.1                     | Output voltage                                                                                       | $V_{OUT}$      | –            | 42           | V    | internally clamped                                                                                                                                                                                                                             |
| 4.1.2                     | Battery voltage for short circuit protection                                                         | $V_{BAT(SC)}$  | –            | 35           | V    | $l = 0$ or $5\text{ m}$<br>$R_{SC} = 20\text{ m}\Omega + R_{Cable}$<br>$R_{Cable} = l * 16\text{ m}\Omega/\text{m}$<br>$L_{SC} = 5\text{ }\mu\text{H} + L_{Cable}$<br>$L_{Cable} = l * 1\text{ }\mu\text{H}/\text{m}$<br>$V_{IN} = 5\text{ V}$ |
| 4.1.3                     | Battery voltage for load dump protection<br>( $V_{BAT(LD)} = V_A + V_S$ with $V_A = 13.5\text{ V}$ ) | $V_{BAT(LD)}$  | –            | 42           | V    | <sup>2)</sup><br>$R_i = 2\text{ }\Omega$<br>$R_{Load} = 4.5\text{ }\Omega$<br>$t_d = 400\text{ ms}$<br>suppressed pulse                                                                                                                        |
| <b>Input Pin</b>          |                                                                                                      |                |              |              |      |                                                                                                                                                                                                                                                |
| 4.1.4                     | Input Voltage                                                                                        | $V_{IN}$       | -0.3         | 5.5          | V    | –                                                                                                                                                                                                                                              |
| <b>Power Stage</b>        |                                                                                                      |                |              |              |      |                                                                                                                                                                                                                                                |
| 4.1.5                     | Load current                                                                                         | $ I_L $        | –            | $I_{L(LIM)}$ | A    | –                                                                                                                                                                                                                                              |
| <b>Energies</b>           |                                                                                                      |                |              |              |      |                                                                                                                                                                                                                                                |
| 4.1.6                     | Unclamped single inductive energy single pulse                                                       | $E_{AS}$       | –            | 55           | mJ   | $I_{L(0)} = 3\text{ A}$<br>$V_{BAT} = 13.5\text{ V}$<br>$T_{J(0)} = 150\text{ °C}$                                                                                                                                                             |
| 4.1.7                     | Unclamped repetitive inductive energy pulse with 10k cycles                                          | $E_{AR(10k)}$  | –            | 40           | mJ   | $I_{L(0)} = 3\text{ A}$<br>$V_{BAT} = 13.5\text{ V}$<br>$T_{J(0)} = 85\text{ °C}$                                                                                                                                                              |
| 4.1.8                     | Unclamped repetitive inductive energy pulse with 100k cycles                                         | $E_{AR(100k)}$ | –            | 20           | mJ   | $I_{L(0)} = 3\text{ A}$<br>$V_{BAT} = 13.5\text{ V}$<br>$T_{J(0)} = 85\text{ °C}$                                                                                                                                                              |
| <b>Temperatures</b>       |                                                                                                      |                |              |              |      |                                                                                                                                                                                                                                                |
| 4.1.9                     | Operating temperature                                                                                | $T_j$          | -40          | +150         | °C   | –                                                                                                                                                                                                                                              |
| 4.1.10                    | Storage temperature                                                                                  | $T_{stg}$      | -55          | +150         | °C   | –                                                                                                                                                                                                                                              |
| <b>ESD Susceptibility</b> |                                                                                                      |                |              |              |      |                                                                                                                                                                                                                                                |
| 4.1.11                    | ESD susceptibility (all pins)                                                                        | $V_{ESD}$      | -2           | 2            | kV   | HBM <sup>3)</sup>                                                                                                                                                                                                                              |
| 4.1.12                    | ESD susceptibility OUT-pin to GND                                                                    | $V_{ESD}$      | -4           | 4            | kV   | HBM <sup>3)</sup>                                                                                                                                                                                                                              |
| 4.1.13                    | ESD susceptibility                                                                                   | $V_{ESD}$      | -750         | 750          | V    | CDM <sup>4)</sup>                                                                                                                                                                                                                              |

1) Not subject to production test, specified by design.



- 2)  $V_{BAT(LD)}$  is setup without the DUT connected to the generator per ISO7637-1;  
 $R_i$  is the internal resistance of the load dump test pulse generator;  
 $t_d$  is the pulse duration time for load dump pulse (pulse 5) according ISO 7637-1, -2.
- 3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ , 100 pF)
- 4) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

**Table 3 Functional Range** <sup>1)</sup>

Please refer to **"Electrical Characteristics" on Page 18** for test conditions

| Pos.  | Parameter                                    | Symbol        | Limit Values |      | Unit | Note / Test Condition                                           |
|-------|----------------------------------------------|---------------|--------------|------|------|-----------------------------------------------------------------|
|       |                                              |               | Min.         | Max. |      |                                                                 |
| 4.2.1 | Battery Voltage Range for Nominal Operation  | $V_{BAT}$     | 8.0          | 18.0 | V    | –                                                               |
| 4.2.2 | Extended battery Voltage Range for Operation | $V_{BAT}$     | 3.0          | 35.0 | V    | parameter deviations possible                                   |
| 4.2.3 | Input Voltage for Nominal Operation          | $V_{IN(NOM)}$ | 4.0          | 5.5  | V    | –                                                               |
| 4.2.4 | Extended Input Voltage Range for Operation   | $V_{IN(EXT)}$ | 2.5          | 4.0  | V    | over temperature latch available, parameter deviations possible |
| 4.2.5 | Junction Temperature                         | $T_J$         | -40          | 150  | °C   | –                                                               |

1) Not subject to production test, specified by design

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

### 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards.

For more information, go to [www.jedec.org](http://www.jedec.org).

| Pos.  | Parameter                                        | Symbol           | Limit Values |      |      | Unit | Note / Test Condition |
|-------|--------------------------------------------------|------------------|--------------|------|------|------|-----------------------|
|       |                                                  |                  | Min.         | Typ. | Max. |      |                       |
| 4.3.1 | Junction to Case                                 | $R_{thJC}$       | –            | 2    | 2.7  | K/W  | 1) 2)                 |
| 4.3.2 | Junction to Ambient (2s2p)                       | $R_{thJA(2s2p)}$ | –            | 25   | –    | K/W  | 1) 3)                 |
| 4.3.3 | Junction to Ambient (1s0p+600mm <sup>2</sup> Cu) | $R_{thJA(1s0p)}$ | –            | 40   | –    | K/W  | 1) 4)                 |

- 1) Not subject to production test, specified by design
- 2) Specified  $R_{thJC}$  value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature).  $T_a = 85\text{ °C}$ . Device is loaded with 1W power.
- 3) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 $\mu\text{m}$  Cu, 2 x 35 $\mu\text{m}$  Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.  $T_a = 85\text{ °C}$ , Device is loaded with 1W power.
- 4) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm<sup>2</sup> and 70  $\mu\text{m}$  thickness.  $T_a = 85\text{ °C}$ , Device is loaded with 1W power.

#### 4.3.1 PCB set up

The following PCB set up was implemented to determine the transient thermal impedance

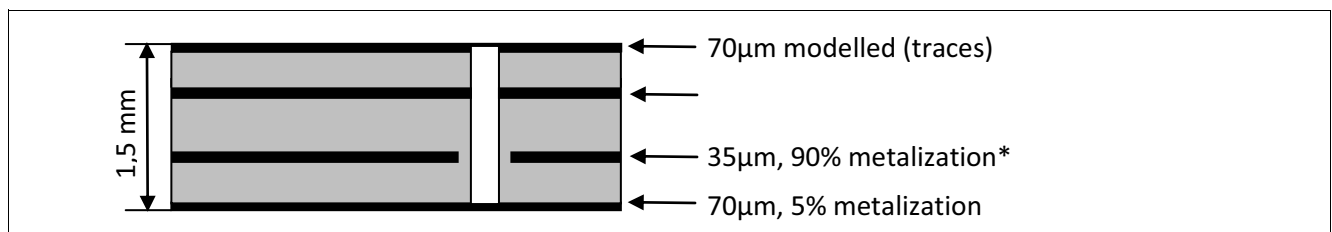


Figure 4 Cross section JEDEC2s2p.

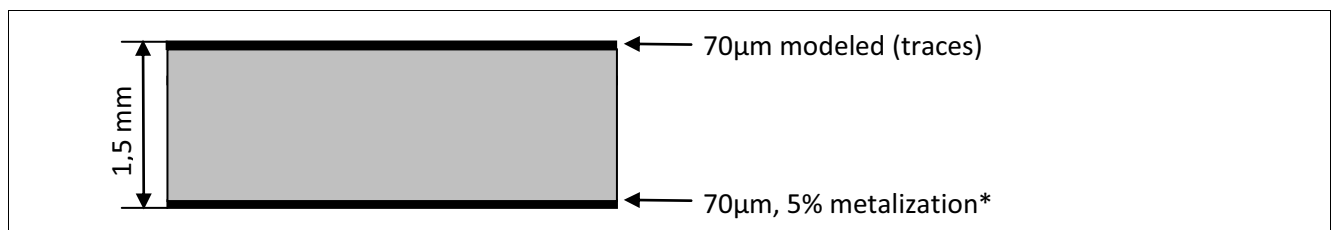


Figure 5 Cross section JEDEC1s0p.

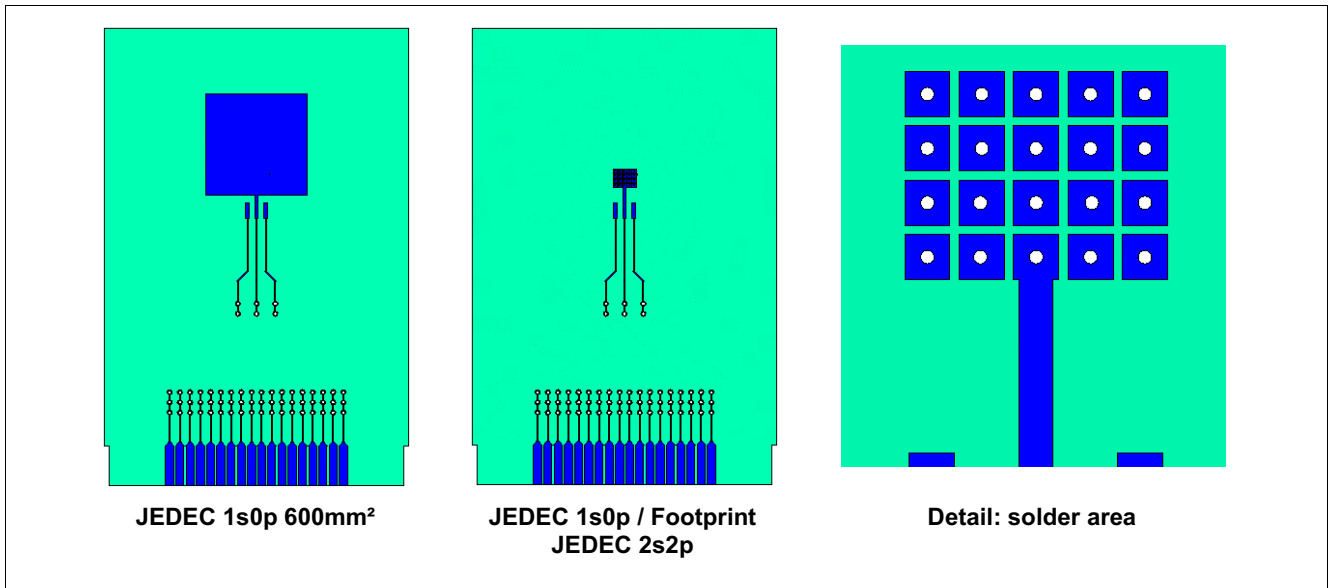


Figure 6 Cross section JEDEC1s0p.

#### 4.3.2 Transient Thermal Impedance

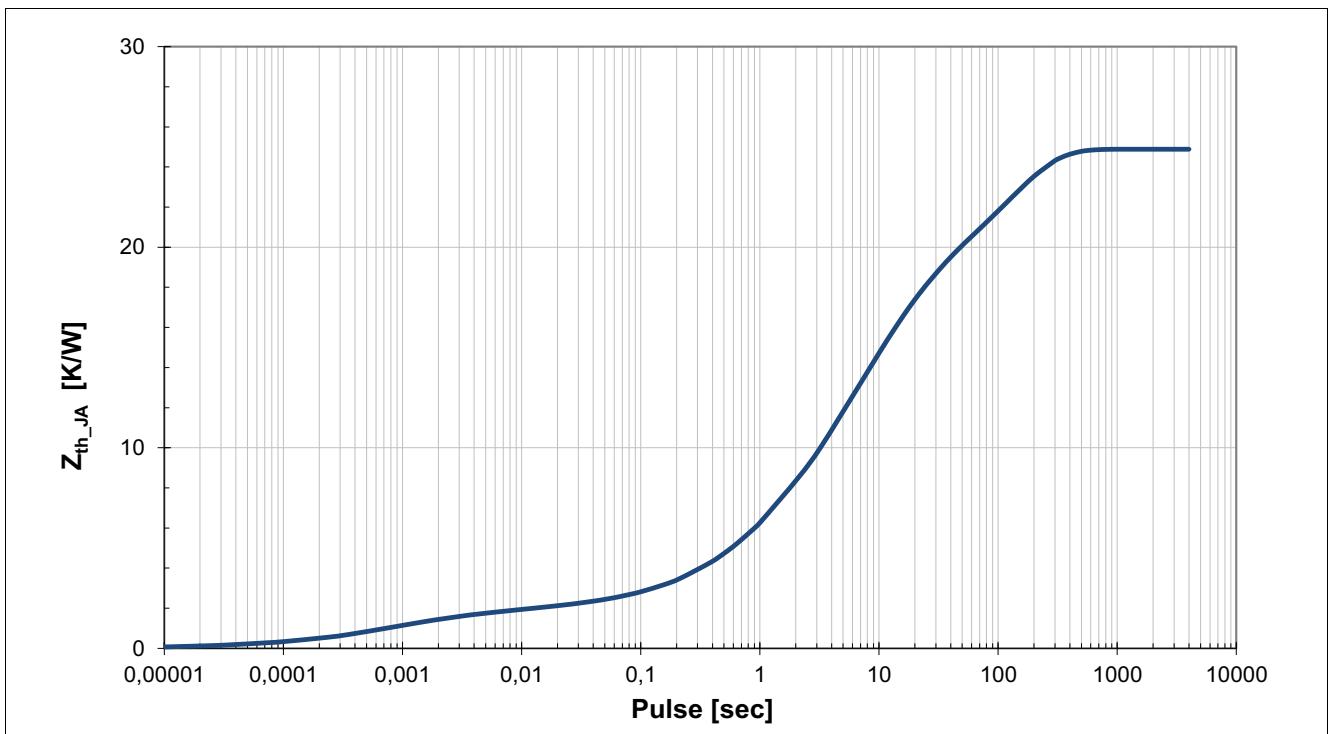


Figure 7 Typical transient thermal impedance  $Z_{thJA} = f(t_p)$ ,  $T_a = 85^\circ\text{C}$   
Value is according to Jecdec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a  $76.2 \times 114.3 \times 1.5 \text{ mm}^3$  board with 2 inner copper layers (2 x  $70 \mu\text{m}$  Cu, 2 x  $35 \mu\text{m}$  Cu). Device is dissipating 1 W power.

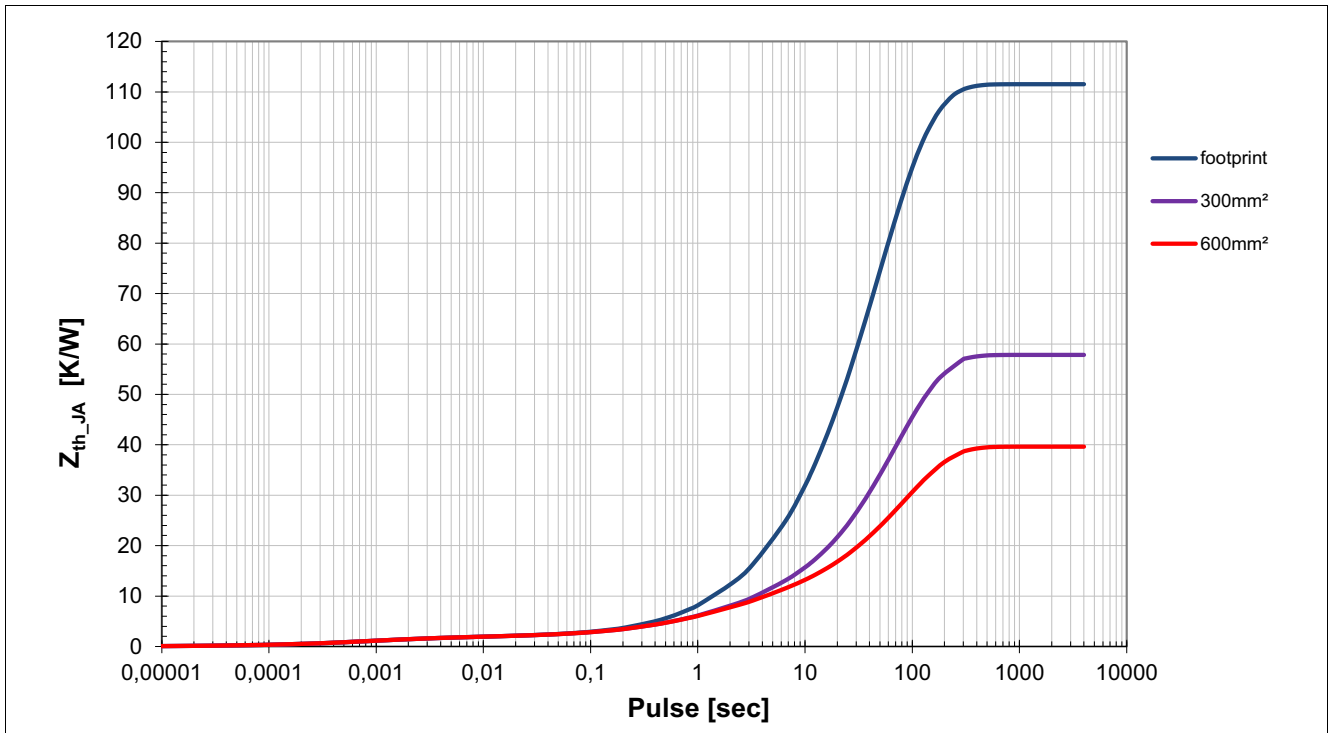
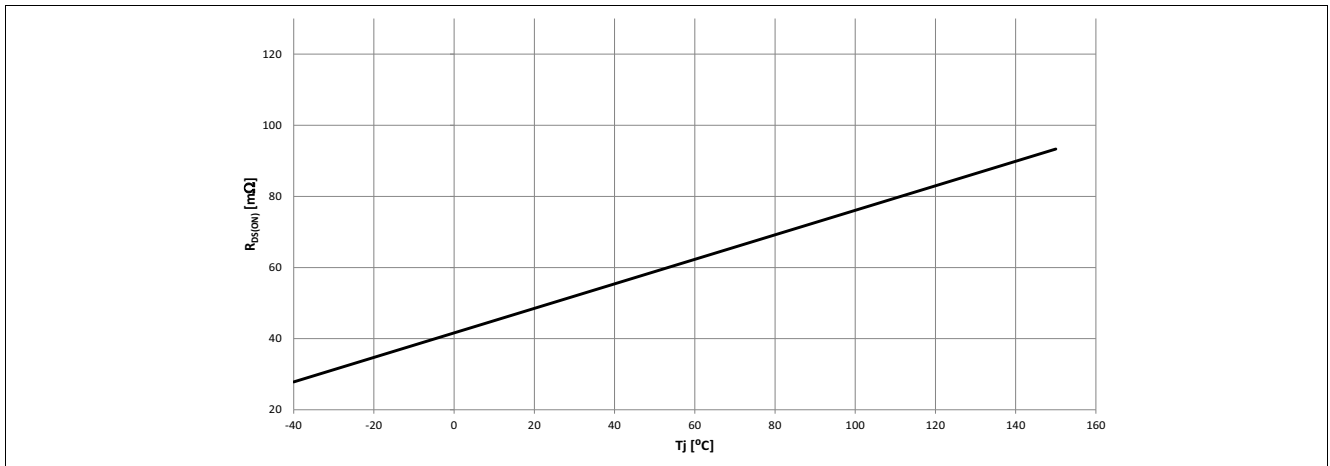


Figure 8 Typical transient thermal impedance  $Z_{thJA} = f(t_p)$ ,  $T_a = 85^\circ\text{C}$ . PCB 1s0p -- cooling areas vs.  $R_{thJA}$ . Device is dissipating 1 W power.

## 5 Power Stage

### 5.1 Output On-state Resistance

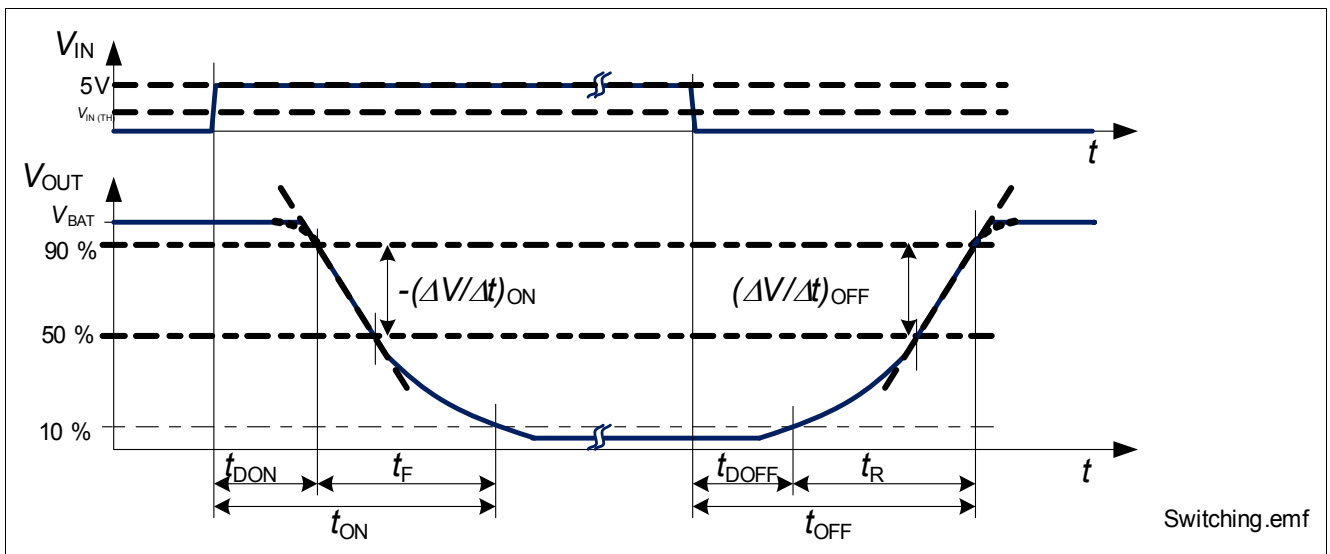
The on-state resistance depends on the junction temperature  $T_j$  and on the applied input voltage. **Figure 9** show this dependencies in terms of temperature and voltage for the typical on-state resistance  $R_{DS(ON)}$ . The behavior in reverse polarity is described in **“Reverse Current capability”** on **Page 14**



**Figure 9** Typical On-State Resistance,  
 $R_{DS(ON)} = f(T_j), V_{IN} = 5\text{ V}$

### 5.2 Resistive Load Output Timing

**Figure 10** shows the typical timing when switching a resistive load .



**Figure 10** Definition of Power Output Timing for Resistive Load

### 5.3 Inductive Load

#### 5.3.1 Output Clamping

When switching off inductive loads with low side switches, the Drain-Source voltage  $V_{OUT}$  rises above battery potential, because the inductance intends to continue driving the current. To prevent unwanted high voltages the

device has a voltage clamping mechanism to keep the voltage at  $V_{OUT(CLAMP)}$ . During this clamping operation mode the device heats up as it dissipates the energy from the inductance. Therefore the maximum allowed load inductance is limited. See [Figure 11](#) and [Figure 12](#) for more details.

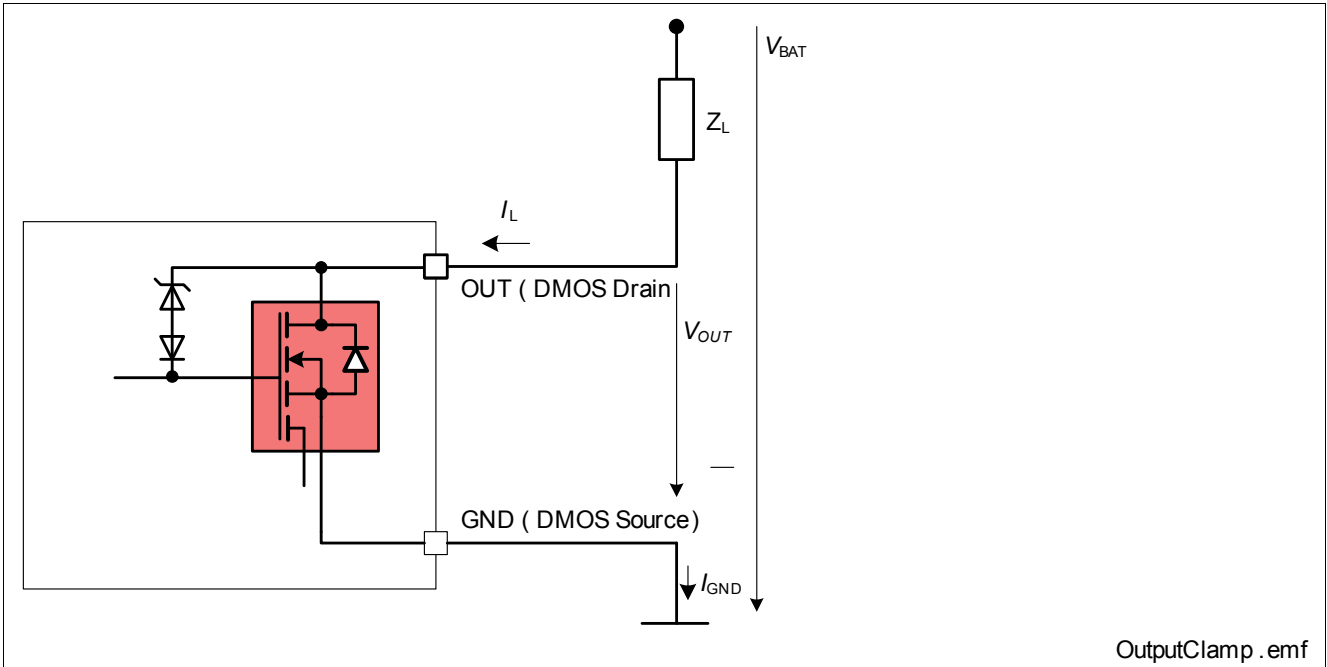


Figure 11 Output Clamp Circuitry

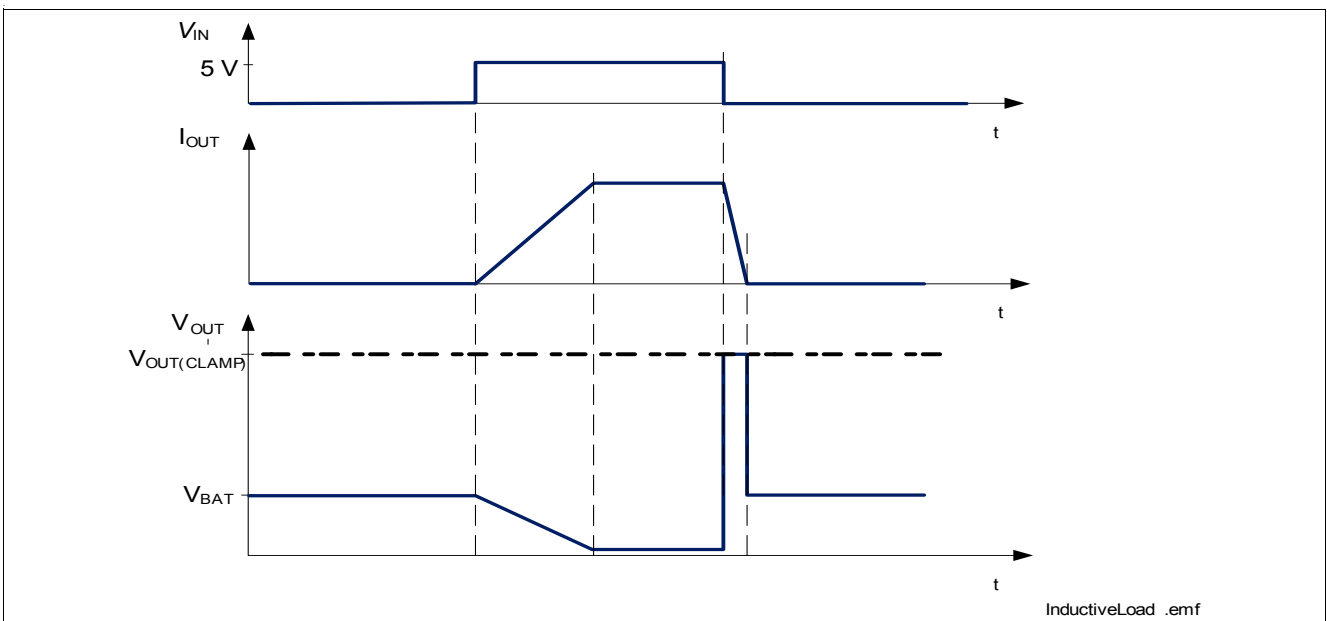


Figure 12 Switching an Inductive Load

### 5.3.2 Maximum Load Inductance

While demagnetization of inductive loads, energy has to be dissipated in the BTS3060TF. This energy can be calculated by the following equation:

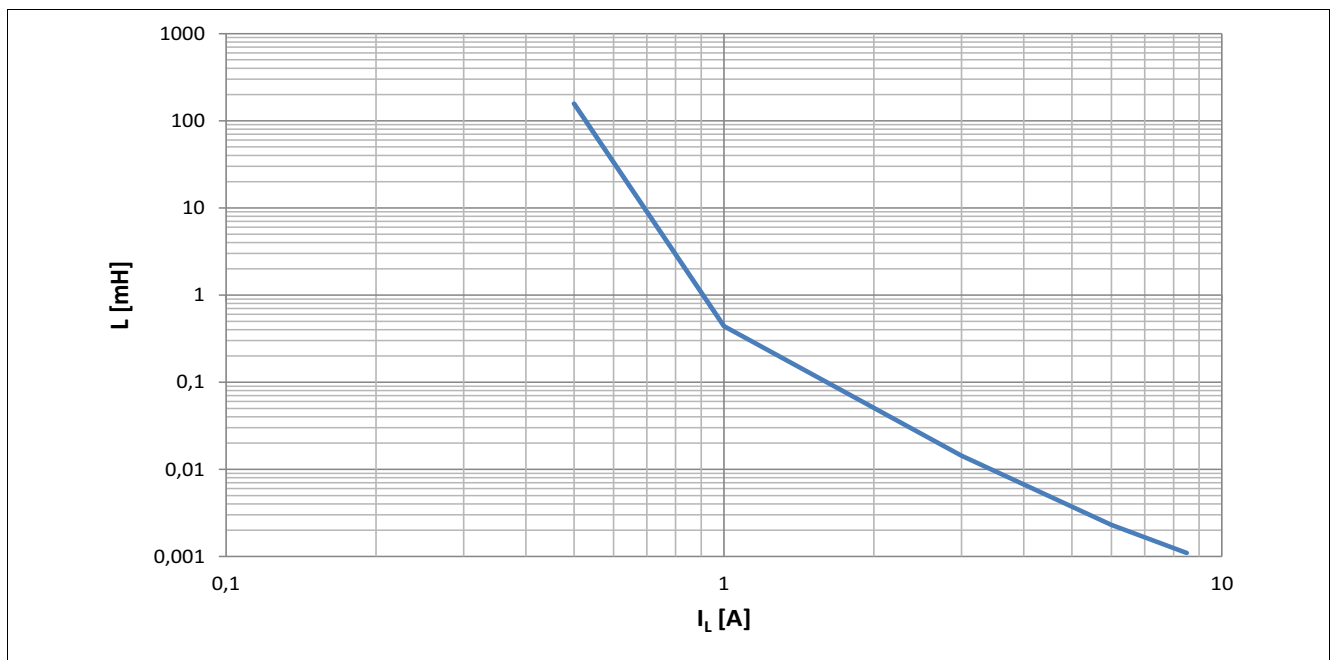
$$E = V_{\text{OUT(CLAMP)}} \cdot \left[ \frac{V_{\text{BAT}} - V_{\text{OUT(CLAMP)}}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_{\text{BAT}} - V_{\text{OUT(CLAMP)}}} \right) + I_L \right] \cdot \frac{L}{R_L}$$

Following equation simplifies under assumption of  $R_L = 0$

$$E = \frac{1}{2} L I_L^2 \cdot \left( 1 - \frac{V_{\text{BAT}}}{V_{\text{BAT}} - V_{\text{OUT(CLAMP)}}} \right)$$

**Figure 13** shows the inductance / current combination the BTS3060TF can handle.

For maximum single avalanche energy please also refer to  $E_{\text{AS}}$  value in **“Energies” on Page 7**



**Figure 13** Maximum load inductance for single pulse  
 $L = f(I_L)$ ,  $T_{j(0)} = T_{j, \text{start}} = 150 \text{ }^\circ\text{C}$ ,  $V_{\text{BAT}} = 13.5 \text{ V}$

## 5.4 Reverse Current capability

A reverse battery situation means the OUT pin is pulled below GND potential to  $-V_{\text{BAT}}$  via the load  $Z_L$ .

In this situation the load is driven by a current through the intrinsic body diode of the BTS3060TF and all protection functions, like current limitation, over temperature shut down or over voltage clamping, are not available.

The device is dissipating a power loss which is defined by the driven current and the voltage drop on the DMOS reverse body diode “ $-V_{\text{OUT}}$ ”.

## 5.5 Characteristics

Please see **“Power Stage” on Page 18** for electrical characteristic table.

## 6 Protection Functions

The device provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operation.

### 6.1 Thermal Protection

The device is protected against over temperature due to overload and / or bad cooling conditions. To ensure this a temperature sensor is located in the power MOSFET.

The device incorporates an absolute ( $T_{J(SD)}$ ) and a dynamic temperature limitation ( $\Delta T_{J(SW)}$ ). Triggering one of them will cause the output to switch off.

The BTS3060TF has a latching thermal protection function. After the device has switched off due to over temperature the device will stay off even if the temperature drops down.

A protective switch off will be reset by setting the input pin voltage to low for a time longer than  $t_{RESET}$ . The next time the voltage on the IN pin rises above the input threshold voltage, the latch will be reset and the device will switch on, if the over temperature protection is no more present or triggered.

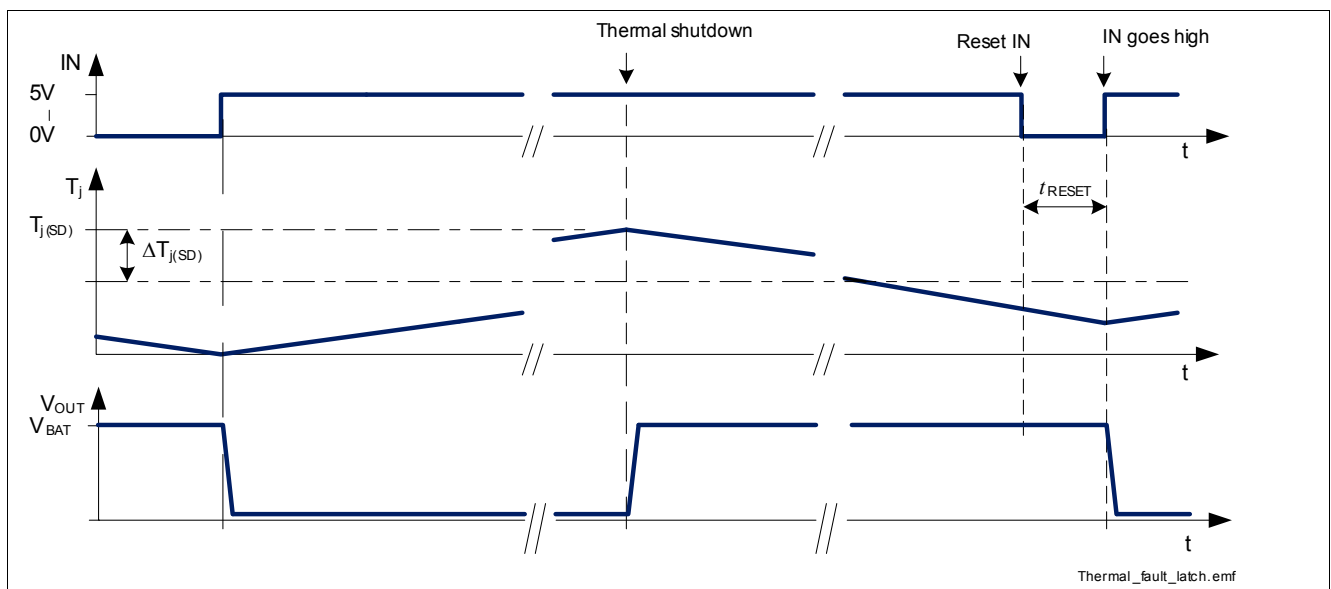


Figure 14 Thermal protective switch OFF scenario

### 6.2 Short Circuit Protection / Current limitation

The condition short circuit is an overload condition to the device. If the load current reaches the limitation value of  $I_{L(LIM)}$  the device limits the current and starts heating up. When the thermal shutdown temperature is reached, the device turns off.

The time from the beginning of current limitation until the over temperature switch off depends strongly on the cooling conditions.

Figure 15 shows this simplified behavior.



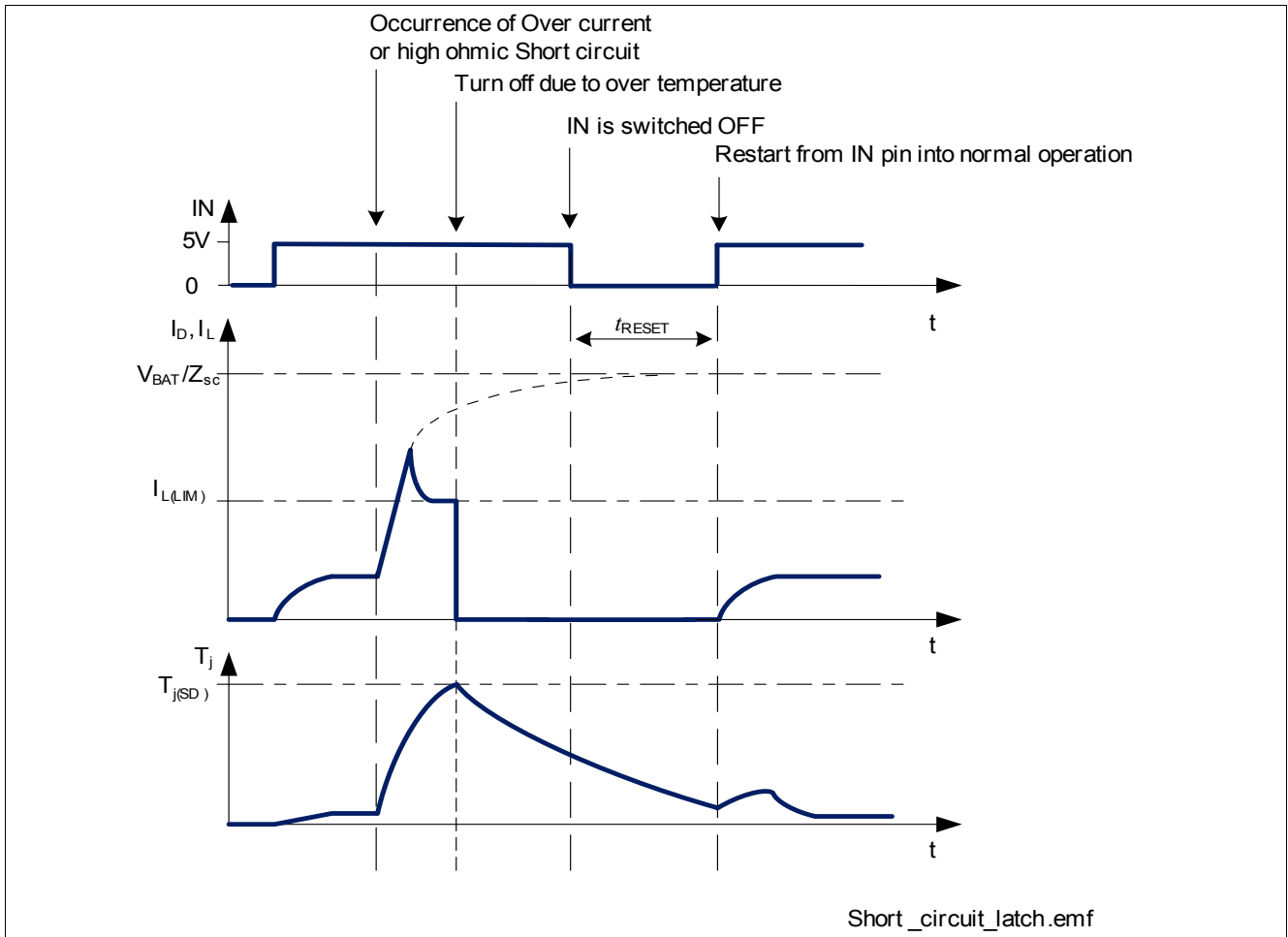


Figure 15 Short circuit protection via current limitation and over temperature switch off

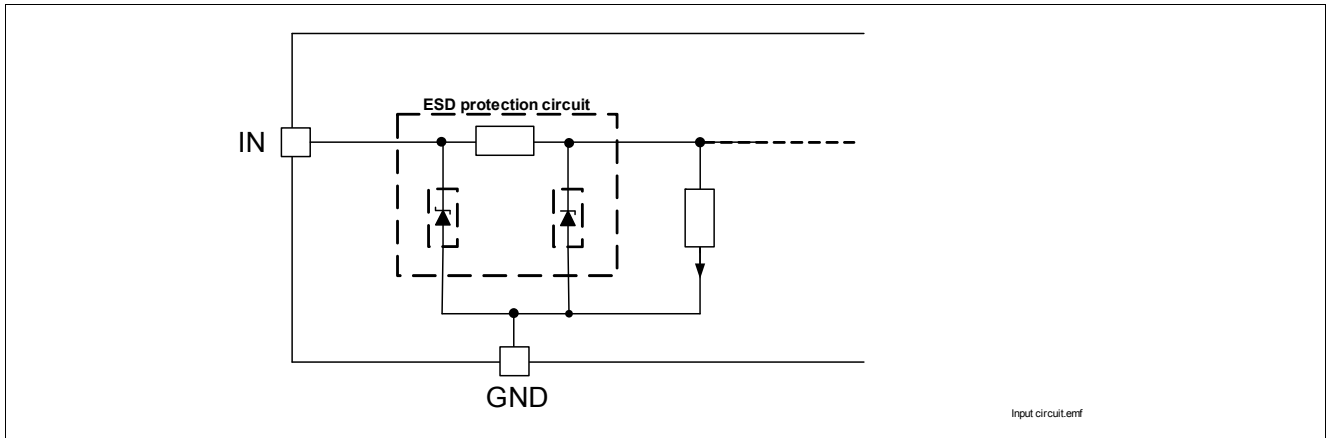
### 6.3 Characteristics

Please see “Protection” on Page 19 for electrical characteristic table.

## 7 Input Stage

### 7.1 Input Circuit

**Figure 16** shows the input circuit of the BTS3060TF. It's ensured that the device switches off in case of open input pin. A ESD Zener structure protects the input circuit against ESD pulses.



**Figure 16** Simplified Input circuitry

### 7.2 Characteristics

Please see [“Input Stage” on Page 20](#) for electrical characteristic table.

## 8 Electrical Characteristics

Note: Characteristics show the deviation of parameter at given input voltage and junction temperature.

Typical values show the typical parameters expected from manufacturing and in typical application condition.

All voltages and currents naming and polarity in accordance to

[Figure 3 “Naming definition of electrical parameters” on Page 6](#)

### 8.1 Power Stage

Please see Chapter [“Power Stage” on Page 12](#) for parameter description and further details.

**Table 4 Electrical Characteristics: Power Stage**

$T_J = -40\text{ °C}$  to  $+150\text{ °C}$ ,  $V_{BAT} = 8\text{ V}$  to  $18\text{ V}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.               | Parameter                                  | Symbol           | Limit Values |      |      | Unit | Note / Test Condition                                                                              |
|--------------------|--------------------------------------------|------------------|--------------|------|------|------|----------------------------------------------------------------------------------------------------|
|                    |                                            |                  | Min.         | Typ. | Max. |      |                                                                                                    |
| <b>Power Stage</b> |                                            |                  |              |      |      |      |                                                                                                    |
| 8.1.1              | On-State resistance at hot temperature     | $R_{DS(ON)_150}$ | –            | 105  | 135  | mΩ   | $T_J = 150\text{ °C}$ ;<br>$V_{IN} = 5\text{ V}$ ;<br>$I_L = 3.0\text{ A}$                         |
| 8.1.2              | On-State resistance at ambient temperature | $R_{DS(ON)_25}$  | –            | 50   | –    | mΩ   | $T_J = 25\text{ °C}$ ;<br>$V_{IN} = 5\text{ V}$ ;<br>$I_L = 3.0\text{ A}$                          |
| 8.1.3              | Nominal load current                       | $I_{L(NOM)}$     | –            | 3    | –    | A    | <sup>1)</sup><br>$T_J < 150\text{ °C}$ ;<br>$T_A = 85\text{ °C}$<br>$V_{IN} = 5\text{ V}$ ;        |
| 8.1.4              | OFF state load current                     | $I_{L(OFF)}$     | –            | –    | 2    | μA   | <sup>2)</sup><br>$V_{BAT} = 13.5\text{ V}$ ;<br>$V_{IN} = 0\text{ V}$ ;<br>$T_J \leq 85\text{ °C}$ |
|                    |                                            |                  | –            | –    | 4    | μA   | $V_{BAT} = 18\text{ V}$ ;<br>$V_{IN} = 0\text{ V}$ ;<br>$T_J = 150\text{ °C}$                      |
| 8.1.5              | Reverse body diode forward voltage drop    | $-V_{OUT}$       | –            | 0.8  | 1.5  | V    | $I_D = -3.0\text{ A}$ ; $V_{IN} = 0\text{ V}$                                                      |

**Table 4 Electrical Characteristics: Power Stage (cont'd)**
 $T_j = -40\text{ °C to }+150\text{ °C}$ ,  $V_{BAT} = 8\text{ V to }18\text{ V}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.                                                                                                                   | Parameter                         | Symbol                      | Limit Values |      |      | Unit                   | Note / Test Condition                                                                            |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------|-----------------------------|--------------|------|------|------------------------|--------------------------------------------------------------------------------------------------|
|                                                                                                                        |                                   |                             | Min.         | Typ. | Max. |                        |                                                                                                  |
| <b>Dynamic characteristics - switching</b>                                                                             |                                   |                             |              |      |      |                        |                                                                                                  |
| $V_{BAT} = 13.5\text{ V}$ , $R_L = 4.7\text{ }\Omega$ ; single pulse                                                   |                                   |                             |              |      |      |                        |                                                                                                  |
| see <a href="#">Figure 10 "Definition of Power Output Timing for Resistive Load"</a> on Page 12 for definition details |                                   |                             |              |      |      |                        |                                                                                                  |
| 8.1.6                                                                                                                  | Turn-on time                      | $t_{ON}$                    | 12           | 38   | 76   | $\mu\text{s}$          | $V_{IN} = 0\text{ V to }5\text{ V}$ ;<br>$V_{OUT} = 10\% V_{BAT}$                                |
| 8.1.7                                                                                                                  | Turn-on delay time                | $t_{DON}$                   | 2            | 8    | 16   | $\mu\text{s}$          | $V_{IN} = 0\text{ V to }5\text{ V}$ ;<br>$V_{OUT} = 90\% V_{BAT}$                                |
| 8.1.8                                                                                                                  | Fall time, Falling output voltage | $t_F$                       | 10           | 30   | 60   | $\mu\text{s}$          | $V_{IN} = 0\text{ V to }5\text{ V}$ ;<br>$V_{OUT} = 90\% V_{BAT}$ to<br>$V_{OUT} = 10\% V_{BAT}$ |
| 8.1.9                                                                                                                  | Turn-off time                     | $t_{OFF}$                   | 20           | 65   | 130  | $\mu\text{s}$          | $V_{IN} = 5\text{ V to }0\text{ V}$ ;<br>$V_{OUT} = 90\% V_{BAT}$                                |
| 8.1.10                                                                                                                 | Turn-off delay time               | $t_{DOFF}$                  | 10           | 35   | 70   | $\mu\text{s}$          | $V_{IN} = 5\text{ V to }0\text{ V}$ ;<br>$V_{OUT} = 10\% V_{BAT}$                                |
| 8.1.11                                                                                                                 | Rise time, Rising output voltage  | $t_R$                       | 10           | 30   | 60   | $\mu\text{s}$          | $V_{IN} = 5\text{ V to }0\text{ V}$ ;<br>$V_{OUT} = 10\% V_{BAT}$ to<br>$V_{OUT} = 90\% V_{BAT}$ |
| 8.1.12                                                                                                                 | Rise time to fall time delta      | $t_R - t_F$                 | –            | 0    | –    | $\mu\text{s}$          | –                                                                                                |
| 8.1.13                                                                                                                 | Rise time/Fall time factor        | $t_R / t_F$                 | –            | 1    | –    | –                      | –                                                                                                |
| 8.1.14                                                                                                                 | Turn-on Slew rate <sup>3)</sup>   | $-(\Delta V/\Delta t)_{ON}$ | –            | 0.85 | –    | $\text{V}/\mu\text{s}$ | $V_{OUT} = 90\% V_{BAT}$ to<br>$V_{OUT} = 50\% V_{BAT}$                                          |
| 8.1.15                                                                                                                 | Turn-off Slew rate <sup>3)</sup>  | $(\Delta V/\Delta t)_{OFF}$ | –            | 0.85 | –    | $\text{V}/\mu\text{s}$ | $V_{OUT} = 50\% V_{BAT}$ to<br>$V_{OUT} = 90\% V_{BAT}$                                          |

1) Not subject to production test, calculated by  $R_{thJA}$  and  $R_{DS(on)}$ .

2) Not subject to production test, specified by design

3) calculated value

## 8.2 Protection

Please see Chapter "[Protection Functions](#)" on Page 15 for parameter description and further details.

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation*

**Table 5 Electrical Characteristics: Protection**

$T_J = -40\text{ °C}$  to  $+150\text{ °C}$ ,  $V_{BAT} = 8\text{ V}$  to  $18\text{ V}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.                          | Parameter                               | Symbol             | Limit Values |      |      | Unit | Note / Test Condition                                                                                                                 |
|-------------------------------|-----------------------------------------|--------------------|--------------|------|------|------|---------------------------------------------------------------------------------------------------------------------------------------|
|                               |                                         |                    | Min.         | Typ. | Max. |      |                                                                                                                                       |
| <b>Thermal Protection</b>     |                                         |                    |              |      |      |      |                                                                                                                                       |
| 8.2.1                         | Thermal shut down junction temperature  | $T_{j(SD)}$        | 150          | 175  | –    | °C   | <sup>1)</sup> ,<br>$V_{IN} > 2.7\text{ V}$                                                                                            |
| 8.2.2                         | Dynamic temperature limitation/shutdown | $\Delta T_{J(SW)}$ | –            | 70   | –    | K    | <sup>1)</sup>                                                                                                                         |
| 8.2.3                         | minimum latch reset time                | $t_{RESET}$        | 50           | –    | –    | µs   | <sup>1)</sup> ;<br>$V_{IN} < 0.8\text{ V}$ ;<br>DMOS is off,<br>no over temperature,<br>pulse times above to<br>assure reset of latch |
| <b>Overvoltage Protection</b> |                                         |                    |              |      |      |      |                                                                                                                                       |
| 8.2.4                         | Drain clamp voltage                     | $V_{OUT(CLAMP)}$   | 42           | 45   | 49   | V    | $V_{IN} = 0\text{ V}$ ; $I_D = 10\text{ mA}$                                                                                          |
| <b>Current limitation</b>     |                                         |                    |              |      |      |      |                                                                                                                                       |
| 8.2.5                         | Current limitation                      | $I_{L(LIM)}$       | 10.5         | 15   | 20   | A    | $V_{IN} = 5\text{ V}$ ;<br>see also <a href="#">Figure 15</a>                                                                         |

1) Not subject to production test, specified by design.

### 8.3 Input Stage

Please see Chapter [“Input Stage” on Page 17](#) for description and further details.

**Table 6 Electrical Characteristics: Input**

$T_J = -40\text{ °C}$  to  $+150\text{ °C}$ ,  $V_{BAT} = 8\text{ V}$  to  $18\text{ V}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.         | Parameter                         | Symbol         | Limit Values |      |      | Unit | Note / Test Condition                                              |
|--------------|-----------------------------------|----------------|--------------|------|------|------|--------------------------------------------------------------------|
|              |                                   |                | Min.         | Typ. | Max. |      |                                                                    |
| <b>Input</b> |                                   |                |              |      |      |      |                                                                    |
| 8.3.1        | Input Current, normal operation   | $I_{IN(NOM)}$  | –            | 310  | 400  | µA   | $2.7 < V_{IN} < 5.5\text{ V}$ ;<br>DC operation normal, no fault   |
| 8.3.1        | Input Current, protection latched | $I_{IN(PROT)}$ | –            | 320  | –    | µA   | $2.7 < V_{IN} < 5.5\text{ V}$ ;<br>latched fault;<br><sup>1)</sup> |
| 8.3.2        | Input Voltage on-threshold        | $V_{IN(TH)}$   | 0.8          | 1.9  | 2.5  | V    | $I_D = 1\text{ mA}$ ;<br>Power DMOS active                         |

1) Not subject to production test, specified by design.

## 9 Characterisation Results

Typical performance characteristics

### 9.1 Power Stage

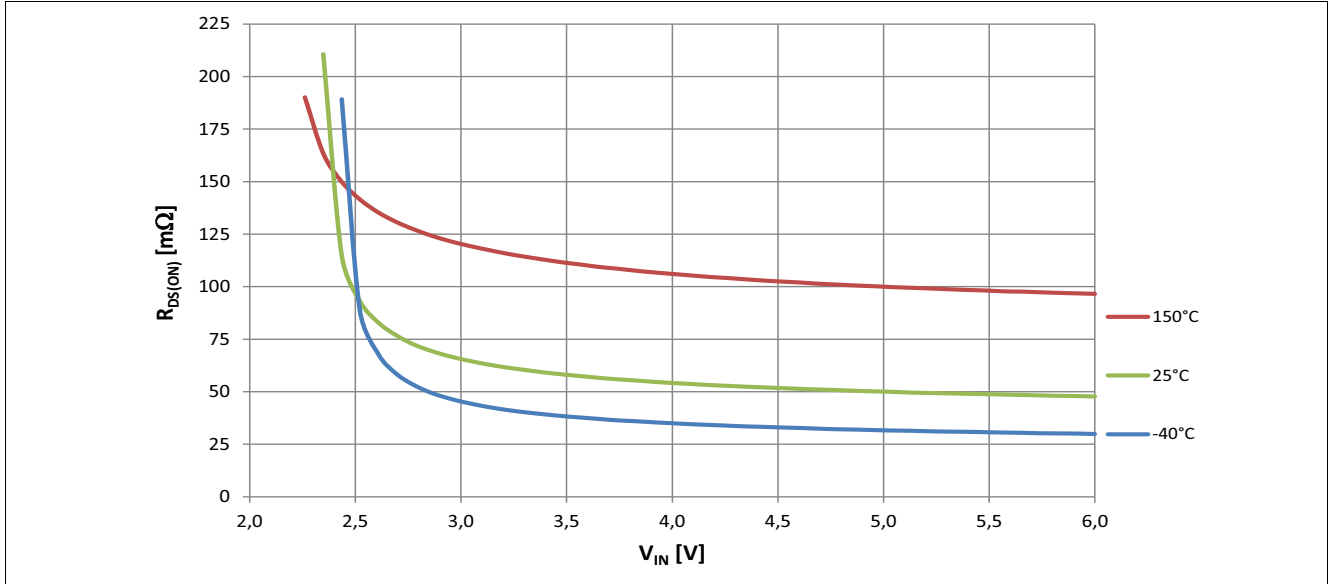


Figure 17 Typical  $R_{DS(ON)}$  vs.  $V_{IN}$  @  $T_J = -40, 85, 150^\circ\text{C}$ ,  $I_L = 3\text{A}$

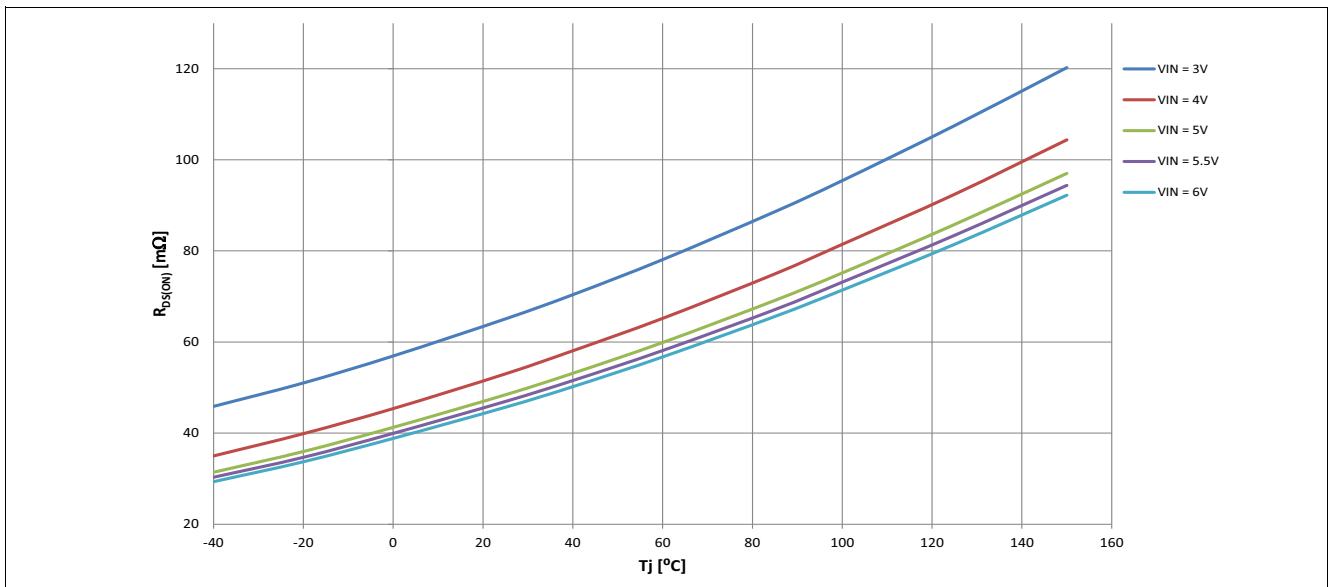


Figure 18 Typical  $R_{DS(ON)}$  vs.  $T_J$  @  $V_{IN} = 3\text{V}, 4\text{V}, 5\text{V}, 5.5\text{V}, 6\text{V}$ ,  $I_L = 3\text{A}$

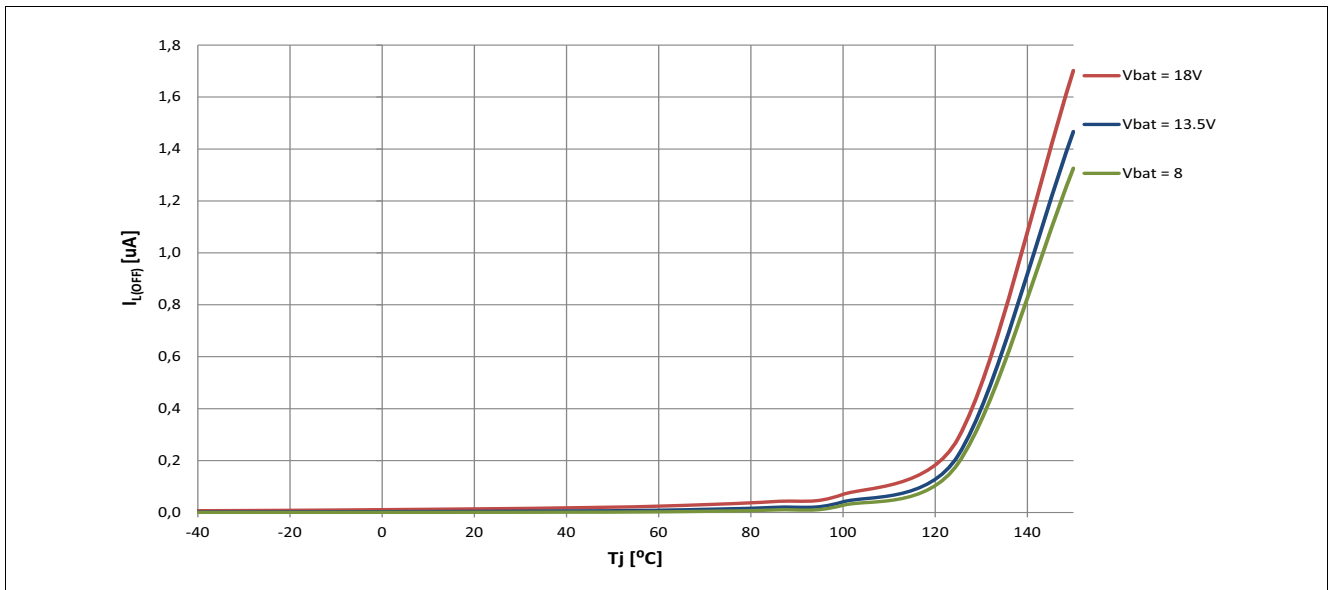


Figure 19 Typical  $I_{L(OFF)}$  vs.  $T_j$  @  $V_{BAT} = 8V, 13.5V, 18V$

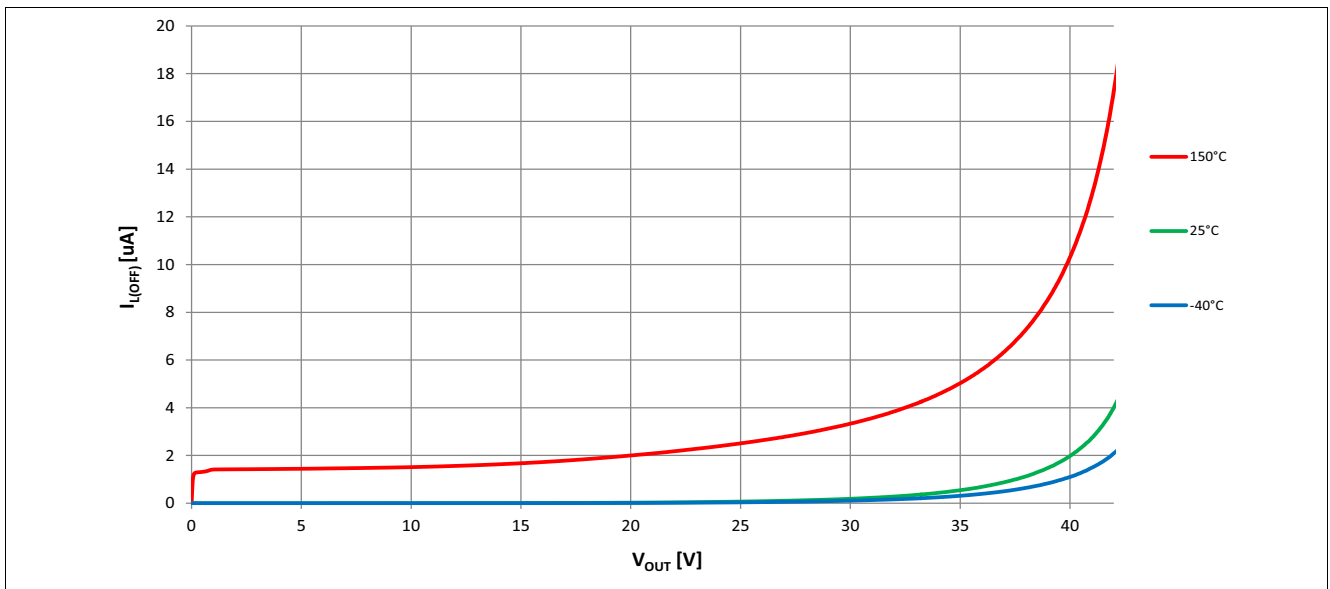


Figure 20 Typical  $I_{L(OFF)}$  vs.  $V_{OUT}$  (0..40V) @  $T_j = -40, 25, 150^\circ C, V_{IN}=0V$

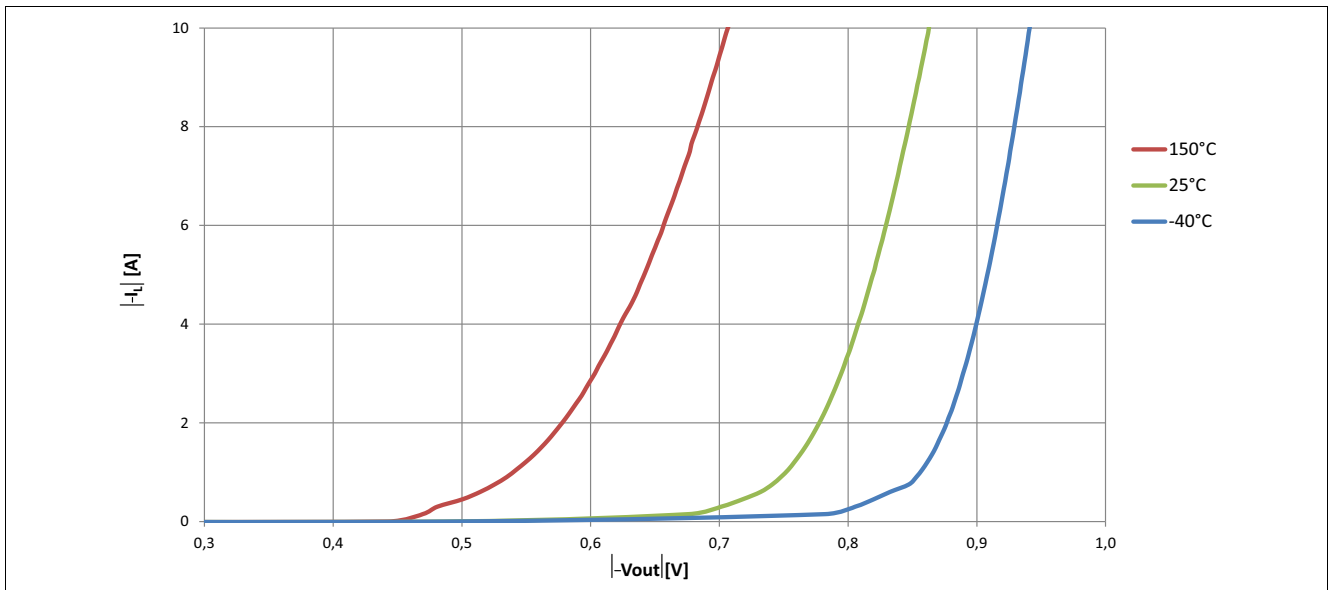


Figure 21 Typical  $-I_L$  vs.  $-V_{OUT}$  @  $T_j = -40, 25, 150^\circ\text{C}$  in absolute values.

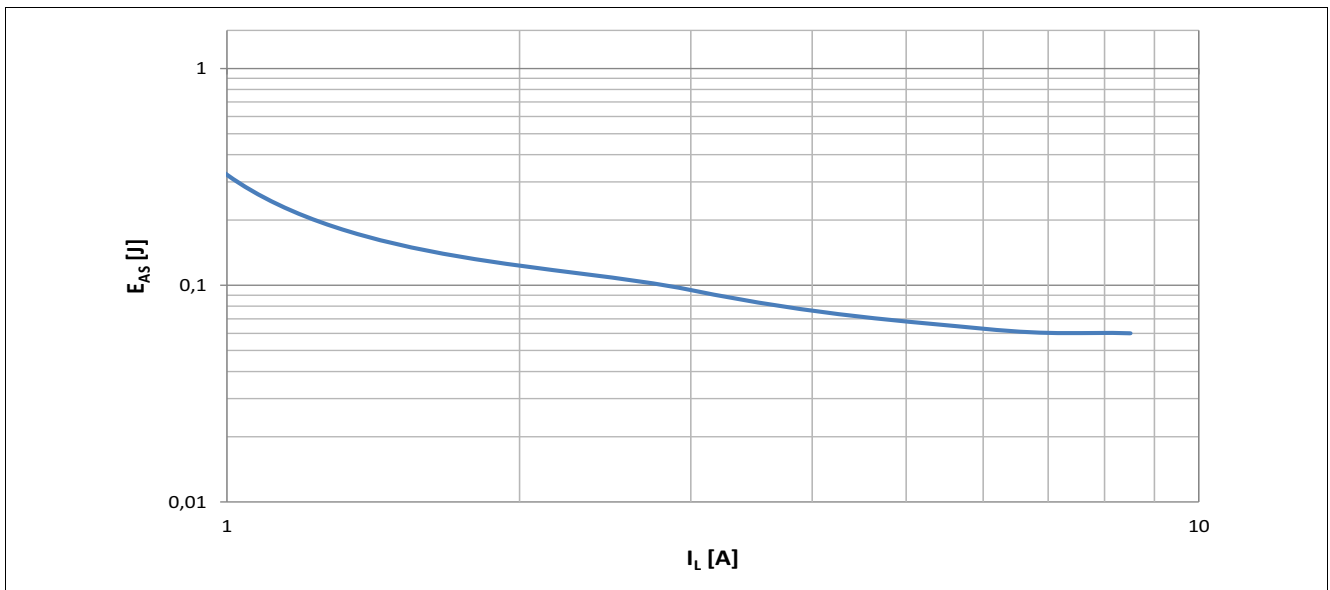


Figure 22 Maximum  $E_{AS}$  vs.  $I_L$  @  $V_{BAT} = 13.5\text{V}$ ,  $T_j = 150^\circ\text{C}$



Dynamic characteristics:

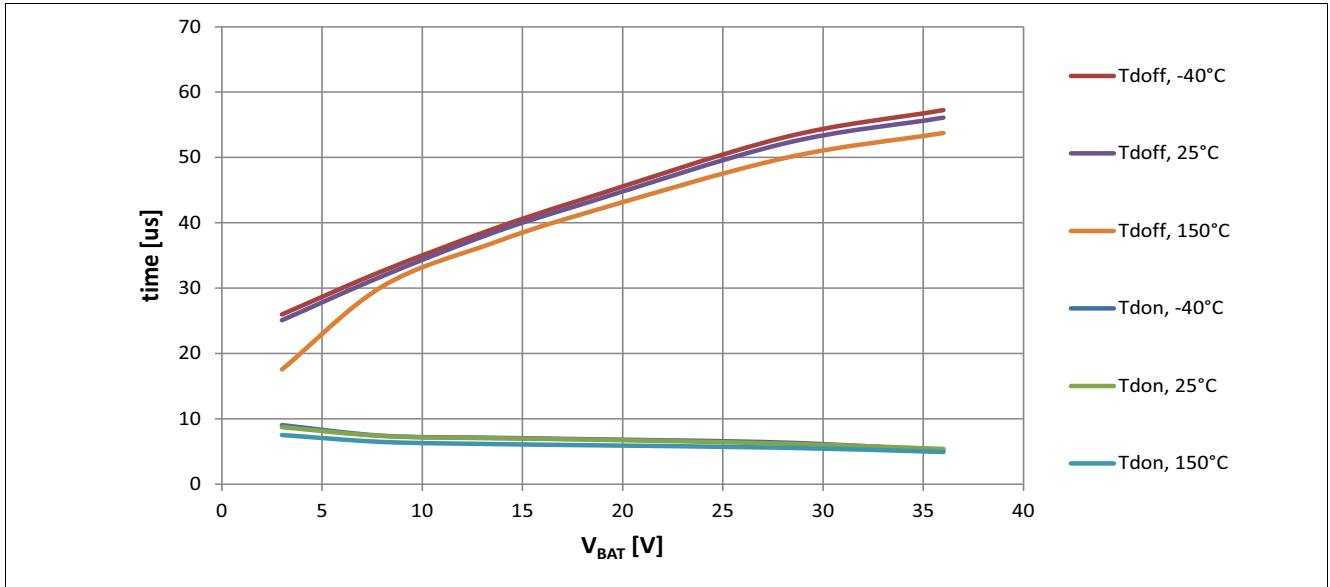


Figure 23 Typical delay on time, delay off time vs.  $V_{BAT}$  @  $V_{IN}=5V$ ,  $I_L=3A$ ,  $T_j=-40, 25, 150^\circ C$

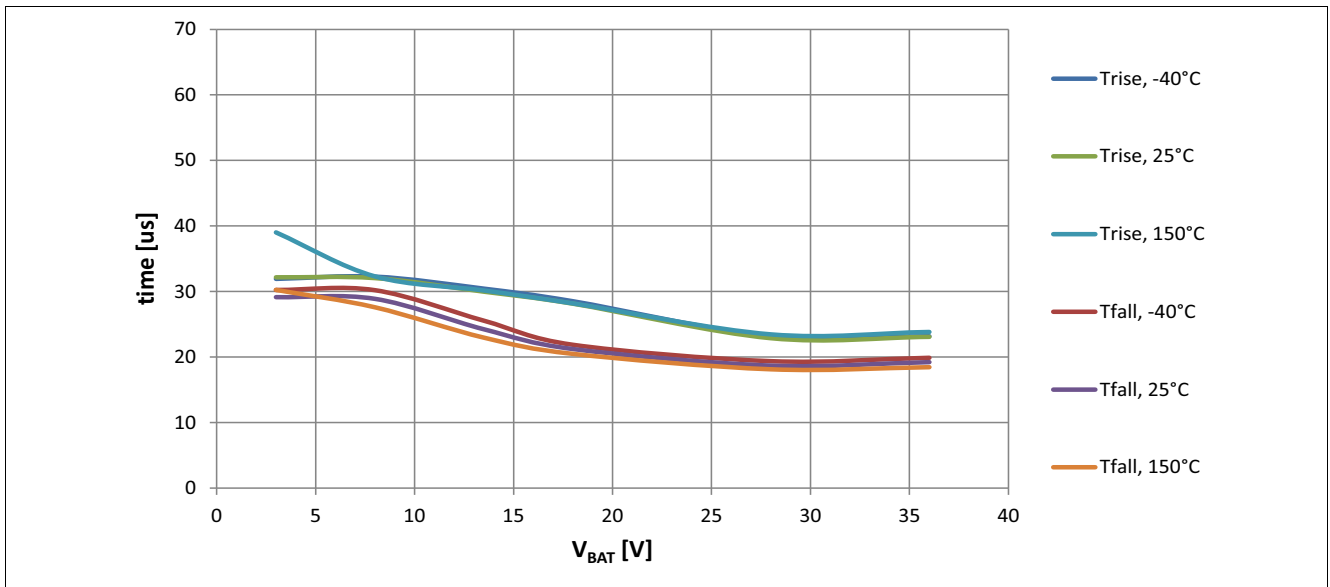


Figure 24 Typical rise time, fall time vs.  $V_{BAT}$  @  $V_{IN}=5V$ ,  $I_L=3A$ ,  $T_j=-40, 25, 150^\circ C$

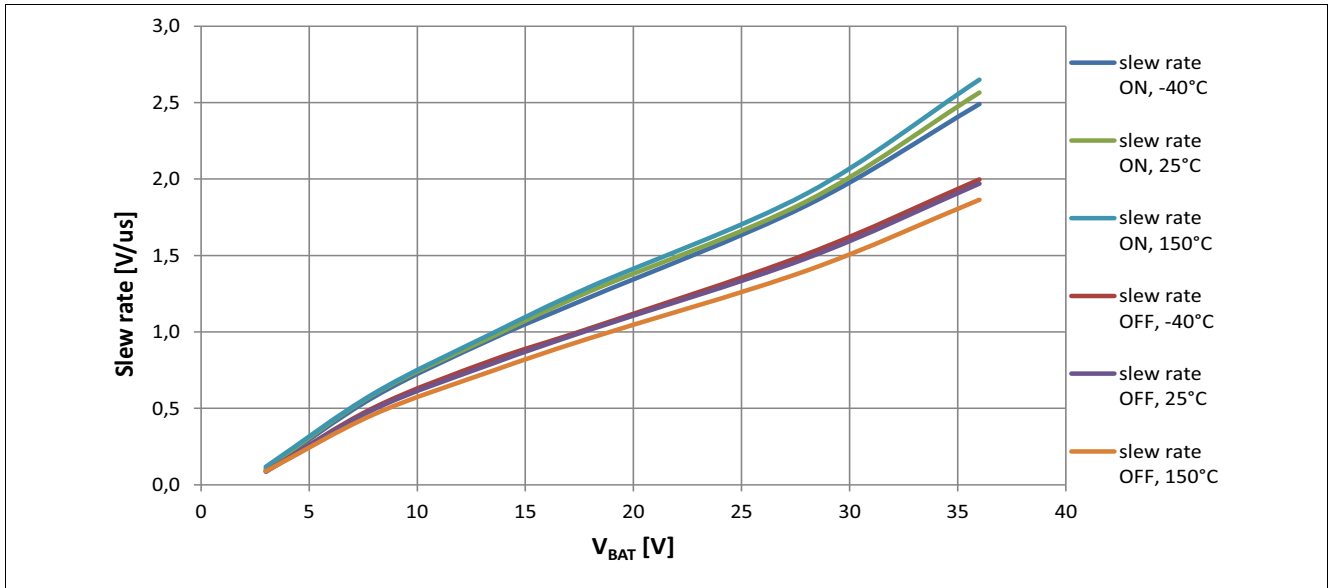


Figure 25 Typical slew rate vs.  $V_{BAT}$  @  $V_{IN}=5V$ ,  $I_L=3A$ ,  $T_j=-40, 25, 150^\circ C$

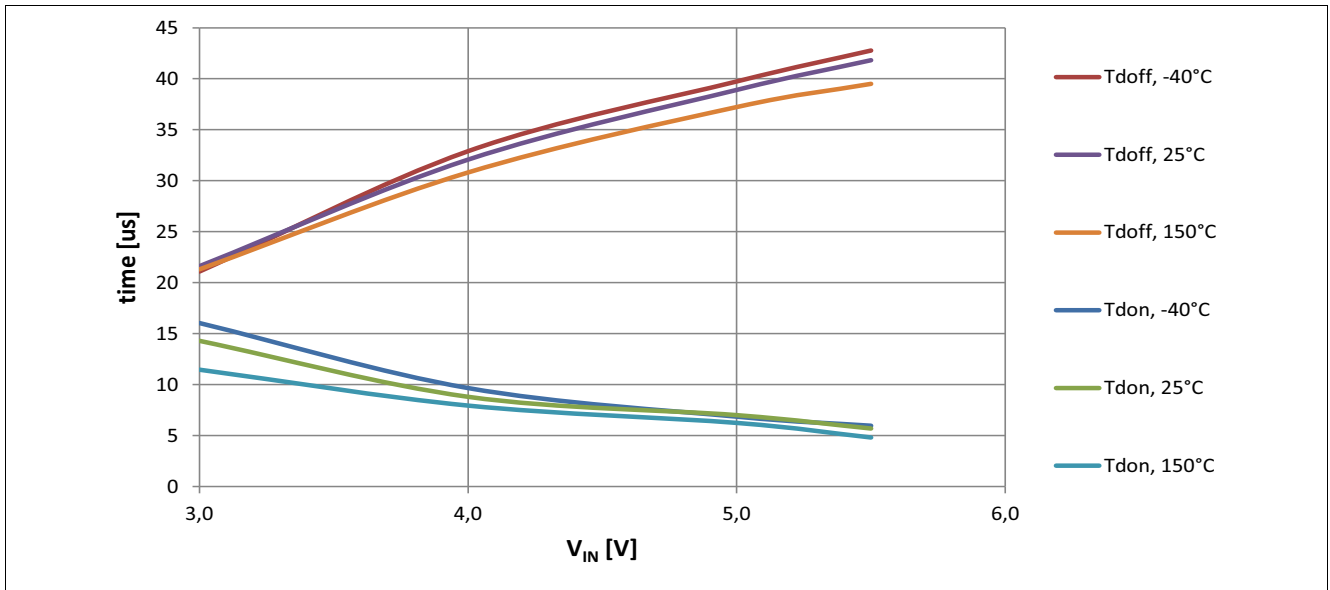


Figure 26 Typical delay on time, delay off time vs.  $V_{IN}$  @  $V_{BAT}=13.5$ ,  $R_L=4.5 \text{ Ohm}$ ,  $T_j=-40, 25, 150^\circ C$