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BTS3160D

10mOhm Smart Low Side Power Switch

Automotive Power

Never stop thinking

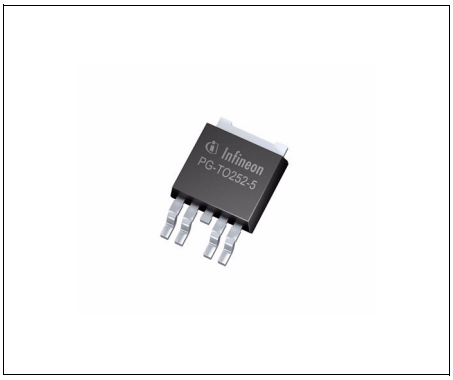
Table of Contents

1 Overview

The BTS3160D is a one channel low-side power switch in PG-TO-252-5-13 package providing embedded protective functions.

The power transistor is realized by a N-channel vertical power MOSFET.

The device is controlled by a chip in Smart Power Technology.



PG-TO-252-5-13

Features

- Logic level input compatible to 3.3 V or 5V micro controllers
- Supply by V_{bb} line, down to 6 V
- Very low over all leakage current
- Providing digital fault information
- Electrostatic discharge protection (ESD)
- Green Product (RoHS compliant)
- AEC Qualified

Table 1 Basic Electrical Data

Drain voltage	V_D	40 V
Supply voltage	V_S	6.0 … 45 V
On-State resistance at 25°C	$R_{DS(ON,max)}$	10 mΩ
Nominal load current	I_{Dnom}	7.8 A
Maximum inrush current	I_{DSC}	70 A
Leakage current MOSFET at V_{bb} = 13.5 V, T_J = 85 °C	I_{DSS}	2 µA
Supply current in off mode at V_{bb} = 13.5 V, T_J = 85 °C	I_{SSS}	4 µA
Clamping Energy	E_{AS}	0.3 J

Type	Package
BTS3160D	PG-TO-252-5-13

Digital Diagnostic

- Over temperature shutdown
- Over load shutdown
- Short circuit shutdown

Protection Functions

- Electrostatic discharge (ESD)
- Under voltage lock out
- Over temperature (shutdown with latch)
- Over voltage (active clamped)

Application

- Micro controller compatible low side power switch with digital feedback for 12V loads
- All types of resistive, inductive and capacitive loads
- Suitable for loads with high inrush current, such as lamps
- Also suitable for LEDs because of low leakage current
- Replaces electromechanical relays, fuses and discrete circuits

Description

The BTS3160D is a latching one channel low-side power switch in PG-TO-252-5-13 package providing embedded protective functions. The power transistor is build by a N-channel vertical power MOSFET. The device is controlled by a control chip in Smart Power Technology.

The device is able to switch all kind of resistive, inductive and capacitive loads. For lamp loads the lamp-inrush-current, eight- to ten-times the nominal current, has to be considered. The maximal inrush current has to be below the minimum short circuit shutdown current.

The ESD protection of the V_S and IN/Fault pin is in relation to GND.

The BTS3160D is supplied by the V_S Pin. This Pin can be connected to battery line. The supply voltage is monitored by the under voltage lock out circuit. The Gate driving unit allows to operate the device in the low ohmic range even with 3.3 V input signal. For PWM application the device offers smooth turn-on and off due to the embedded edge shaping function, in order to reduce EMC noise.

The over voltage protection is for protection during load-dump or inductive turn off conditions. The power MOSFET is limiting the drain-source voltage, if it gets too high. This function is available even without supply.

The over temperature protection is in order to save the device from overheating due to overload and bad cooling conditions. In order to reduce the device stress the edge shaping is disabled during thermal shutdown. After thermal shutdown the device stays off until the latch is reset by a IN-Low signal. For high dynamic overload conditions such as short circuit the device will turn off if a certain load current is reached. The short circuit shutdown is a latch function. The device will stay off until the latch is reset by IN-Low signal. In order to reduce the device stress the edge shaping is disabled during short circuit turn off.

2 Block Diagram

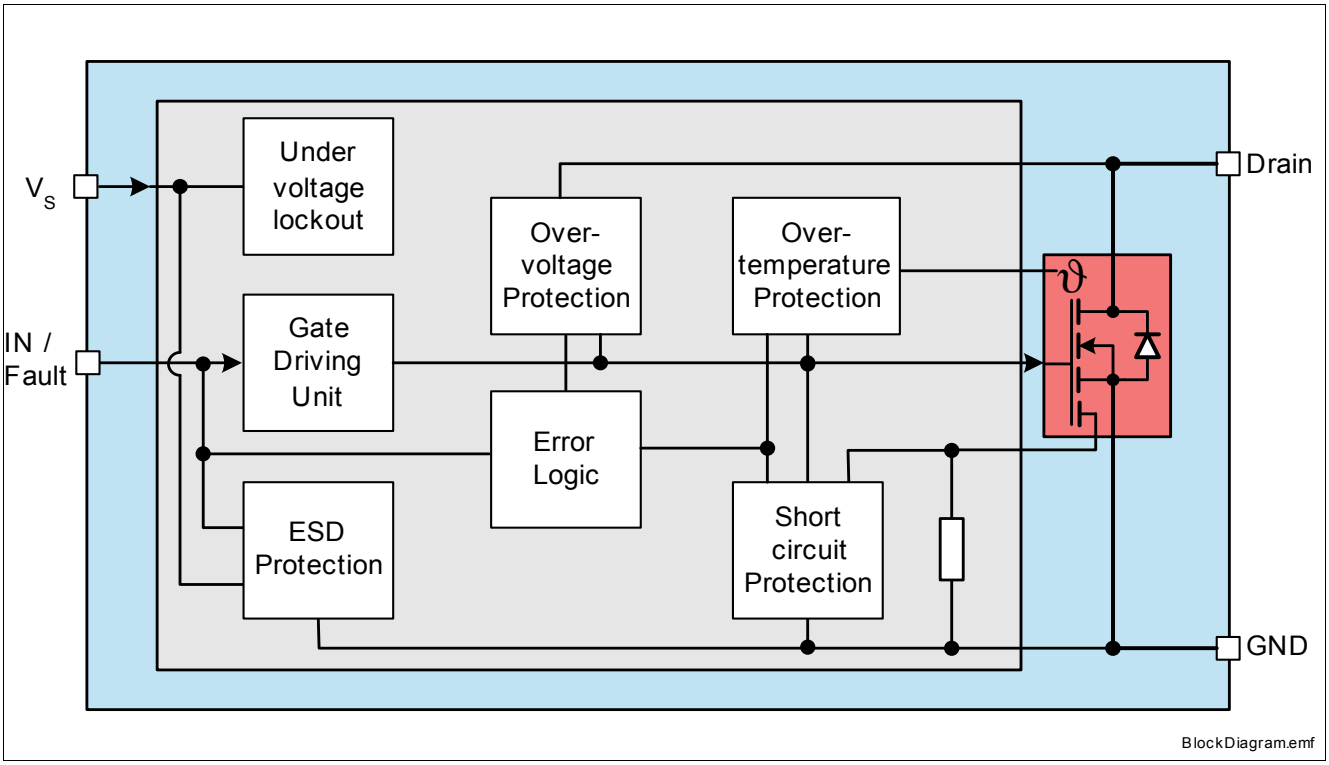


Figure 1 Block Diagram for the BTS3160D

2.1 Voltage and current naming definition

Following figure shows all the terms used in this datasheet, with associated convention for positive values.

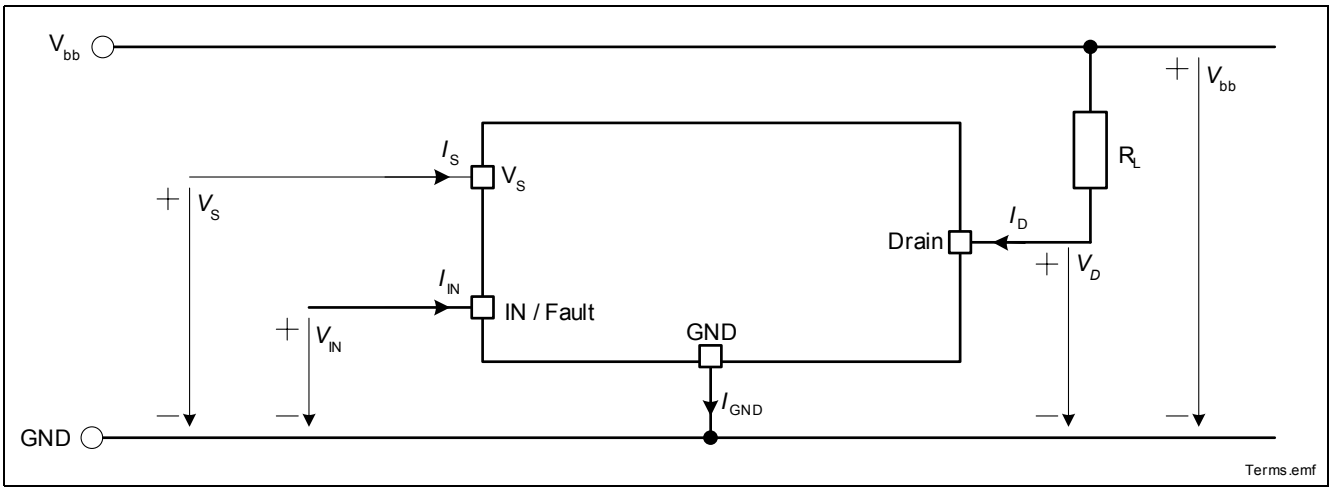


Figure 2 Terms

3 Pin Configuration

3.1 Pin Assignment BTS3160D

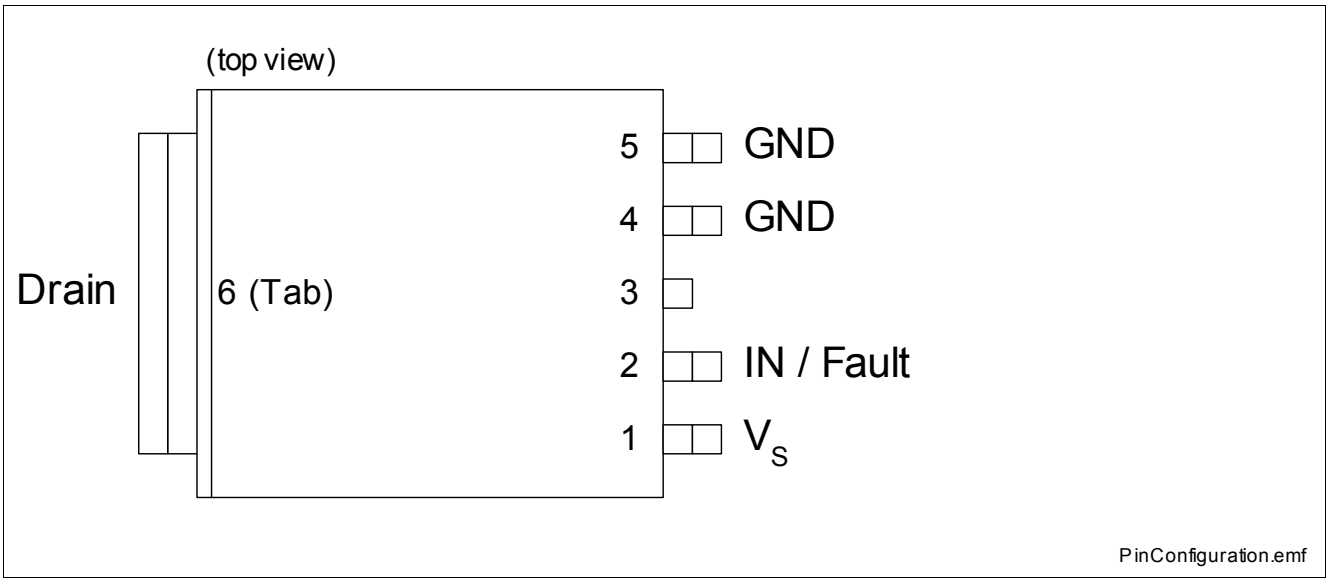


Figure 3 Pin Configuration PG-TO-252-5-13

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	V_S	**Supply Voltage;** Connected to Battery Voltage with Reverse polarity protection
2	IN	**Control Input and Status Feedback;** Digital input 3.3 V or 5 V logic.
3, Tab	Drain	**Drain output;** Protected low side power output channel
4,5	GND	**Ground;** Signal ground, Pin 4 and 5 must be externally shorted[1)]

1) Not shorting pin 4 and 5 will considerably increase the on-state resistance and reduce the peak current capability.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; V_S = 6 V to 30 V.

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-0.3	30	V	–
4.1.2	Supply voltage during active clamping	$V_{S(pulse)}$	-0.3	45	V	2)
4.1.3	Drain voltage	V_D	-0.3	40	V	3)
4.1.4	Drain voltage for short circuit protection	$V_{D(SC)}$	0	30	V	–
4.1.5	Logic input voltage	V_{IN}	-0.3	5.3	V	–
Energies						
4.1.6	Unclamped single pulse inductive energy	E_{AS}	0	0.3	J	I_D = 20 A; V_{bb} = 30 V $T_{J(Start)}$ = 150°C
4.1.7	Load dump protection $V_{LoadDump} = V_A + V_S$	V_{LD}	0	45	V	T_J = 25°C
Temperatures						
4.1.8	Junction Temperature	T_j	-40	150	°C	–
4.1.9	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.10	ESD Resistivity on all pins	V_{ESD}	-4	4	kV	HBM[4)]

1) Not subject to production test, specified by design.
2) Not for DC operation, only for short pulse (i.e. loaddump) for a total of 100 h in full device life.
3) Active clamped.
4) ESD susceptibility, HBM according to EIA/JESD 22-A114B

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.2.1	Supply Voltage	V_S	6	13.5	30	V	–
4.2.2	Supply current in off mode	$I_{S(OFF)}$	–	1.5	–	µA	V_{IN} = 0.0 V; V_S = 13.5 V; T_J = 25 °C
			–	–	4		V_{IN} = 0.0 V; V_S = 13.5 V; T_J = 85 °C[1)]
			–	–	10		V_{IN} = 0.0 V; V_S = 13.5 V; T_J = 150 °C
4.2.3	Supply current in on	I_S	–	1.6	3	mA	V_{IN} = 5.0 V; V_S = 30 V

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	R_{thJC}	–	0.9	1.1	K/W	1)
4.3.2	Junction to Ambient	R_{thJA}	–	80		K/W	1) @min. footprint
			–	45		K/W	1) @ 6 cm² cooling area, see **Figure 4**

1) Not subject to production test, specified by design

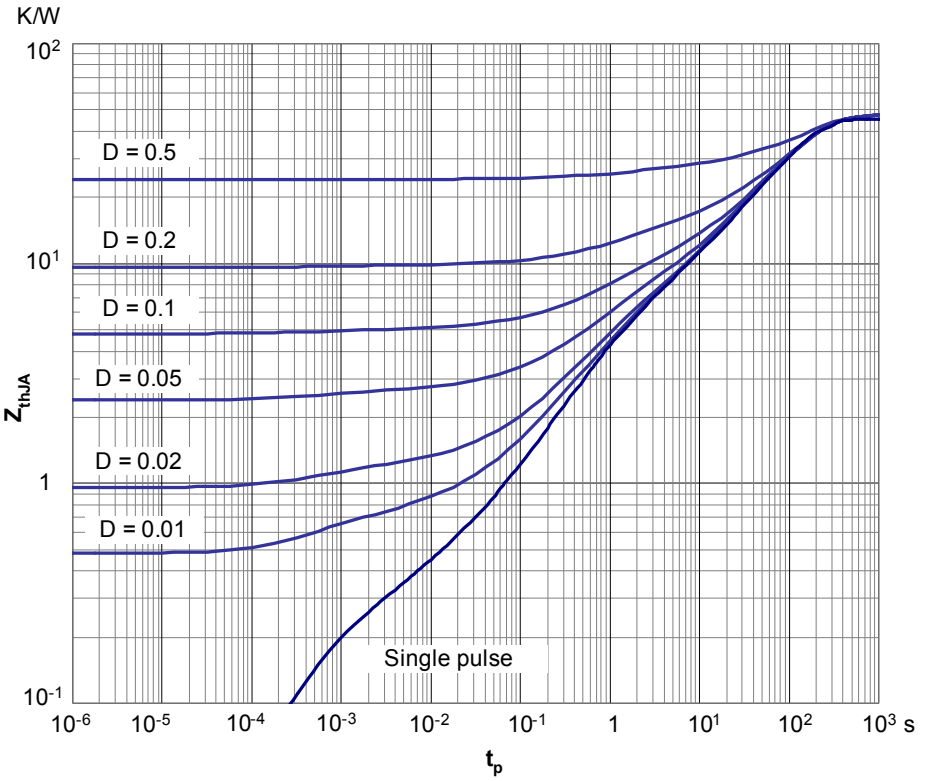


Figure 4 Typical transient thermal impedance
$Z_{thJA} = f(t_p)$, D = tp/T, T_a = 25 °C
Device on 50 mm × 50 mm × 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB mounted vertical without blown air.

5 Supply and Input Stage

5.1 Supply Circuit

The Supply pin V_S is protected against ESD pulses as shown in **Figure 5**. Due to an internal voltage regulator the device can be supplied from battery line.

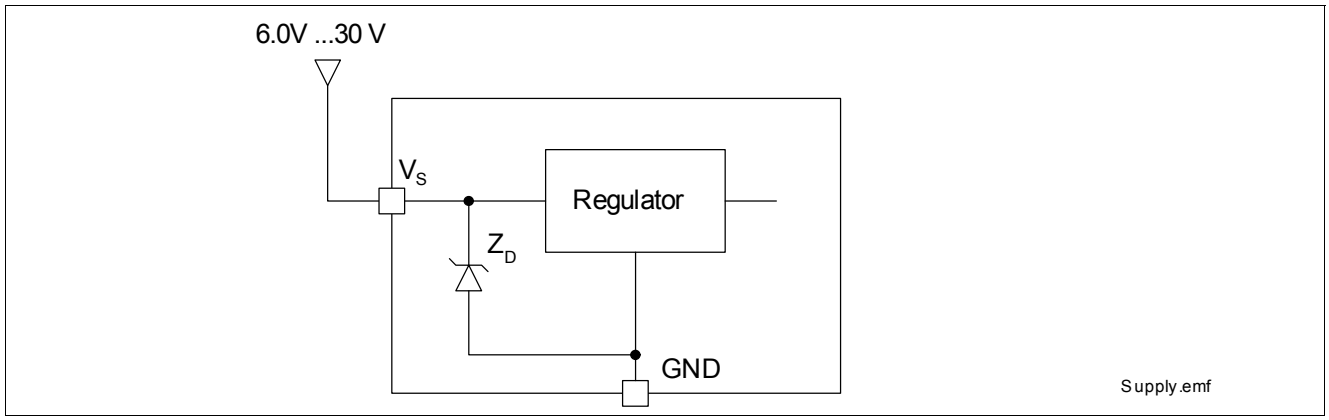


Figure 5 Supply Circuit

5.1.1 Under Voltage Lock Out / Power On Reset

In order to ensure a stable device behavior under all allowed conditions the Supply voltage V_S is monitored by the under voltage lock out circuit. All device functions and protection are given for supply voltages above under voltage lockout V_{SUVON} but parameter deviations are possible below $V_{S(min)}$. There is no failure feedback for $V_S < V_{SUVON}$.

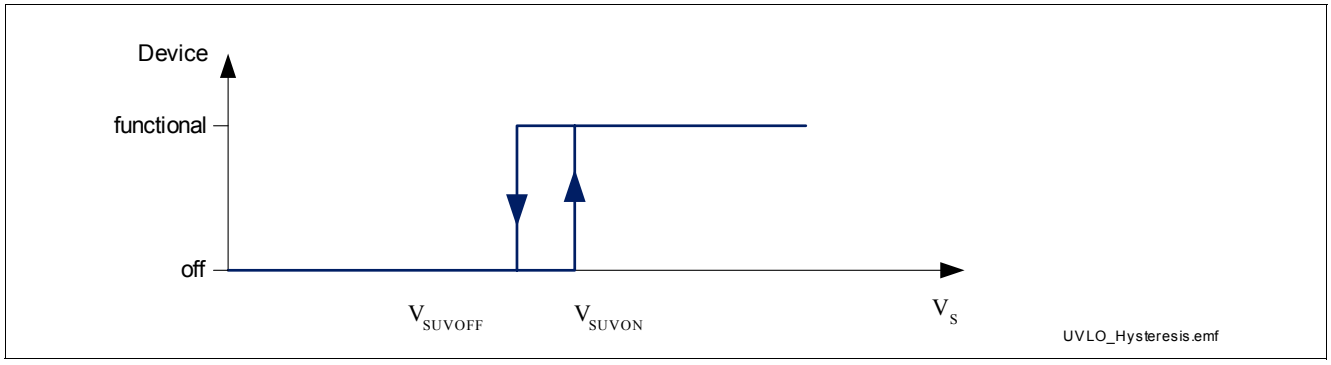


Figure 6 Under Voltage Lock Out

5.2 Input Circuit

Figure 7 shows the input circuit of the BTS3160D. It's ensured that the device switches off in case of open input pin. A zener structure protects the input circuit against ESD pulses. As the BTS3160D has a supply pin, the operation of the power MOS can be maintained regardless of the voltage on the IN pin, therefore a digital status feedback down to logic low is realized. For readout of the fault information, please refer to **"Readout of Fault Information" on Page 12**

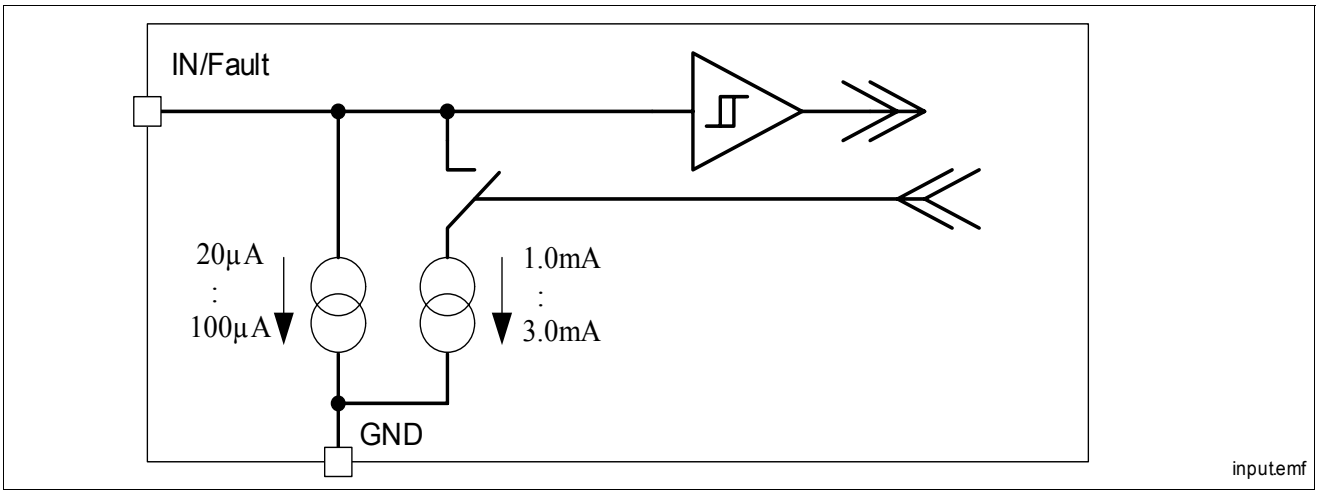


Figure 7 Input Circuit

5.2.1 Readout of Fault Information

The BTS3160D provides digital status information via an increased current on the IN / Fault pin.
The voltage on this pin is pulled down to logic low if a proper resistor is used. An example for the required circuitry is shown in Figure 8.
The increased current $I_{IN(fault)}$ is an order of magnitude above the normal operation current $I_{IN(nom)}$ therefore the voltage at the IN/Fault pin will decrease. The voltage at the pin is determined by the current and the serial resistor.

We recommend 3k3 for a 3.3V µC and 5k6 for a 5V µC to achieve a logic low signal.

For detailed calculation please refer to **"Dimensioning of serial Resistor at IN pin" on Page 26**

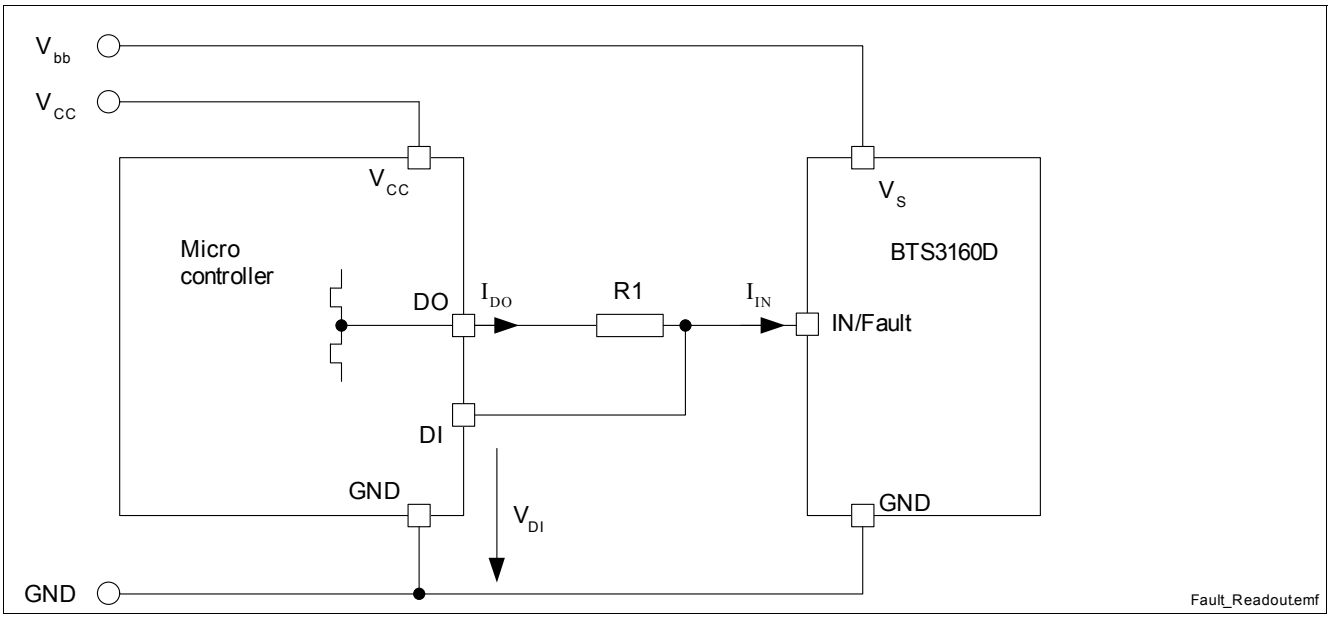


Figure 8 Readout of Fault Information

5.3 Electrical Characteristics Supply and Input Stages

V_S = 6 V to 30 V, T_j = -40 °C to +150 °C

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Under Voltage Lockout							
5.3.1	UV-switch-on voltage	V_{SUVON}	–	–	5.5	V	V_S = 5.5 V
5.3.2	UV-switch-off voltage	V_{SUVOFF}	4.0	–	–	V	V_S = 4.0 V
5.3.3	UV-switch-off hysteresis	V_{SUVHY}	–	0.2	–	V	V_{SUVON} - V_{SUVOFF}
Digital Input / Fault Feedback							
5.3.4	Low level voltage	V_{INL}	–	–	0.8	V	V_S = 6 V; no fault condition
5.3.5	High level voltage	V_{INH}	2.0	–	–	V	V_S = 6 V; no fault condition
5.3.6	Input pull down current	I_{IN}	20	50	100	µA	V_{IN} = 5.3 V; no fault condition
		$I_{IN-Fault}$	1	2	3	mA	V_{IN} = 5.3 V; all fault conditions
5.3.7	Input Fault ON threshold	I_{Fault_ONth}			600	uA	1)

1) not subject to production test

6 Power Stage

The power stage is built by a N-channel vertical power MOSFET (DMOS)

6.1 Output On-state Resistance

The on-state resistance depends on the supply voltage as well as on the junction temperature T_J. **Figure 9** shows the dependency over temperature for the typical on-state resistance $R_{DS(on)}$,while **Figure 10** shows the dependency over Vs.

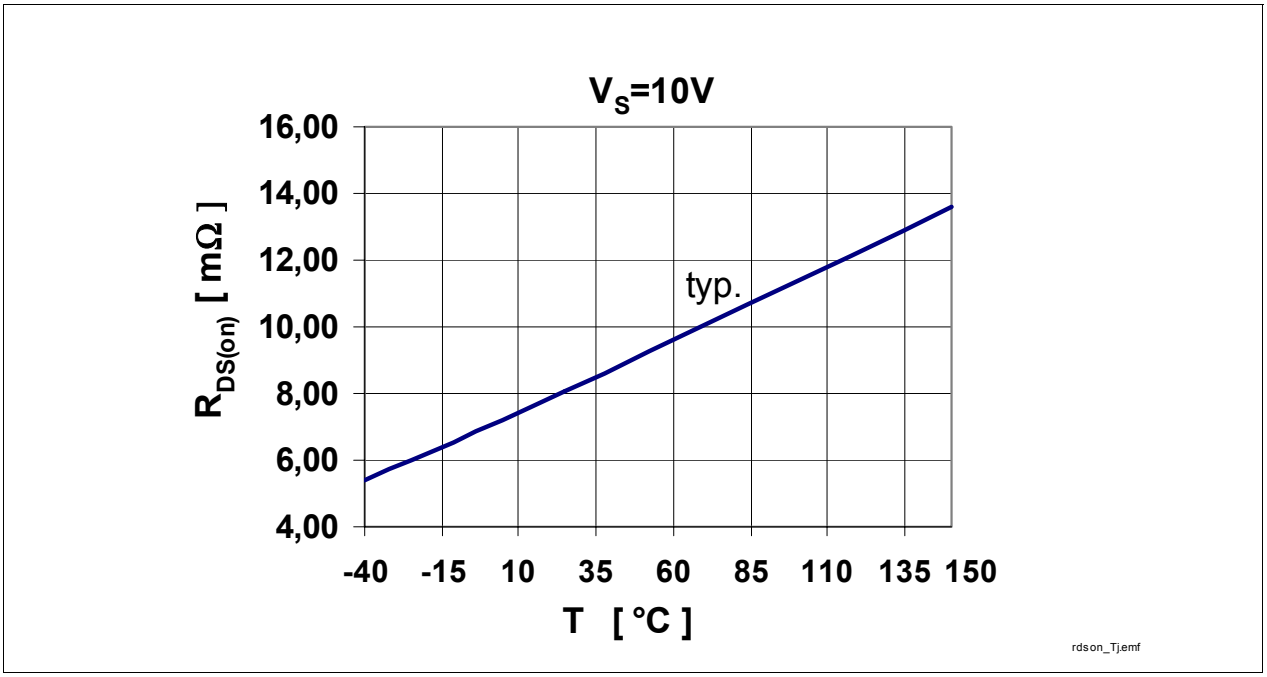


Figure 9 Typical On-State Resistance

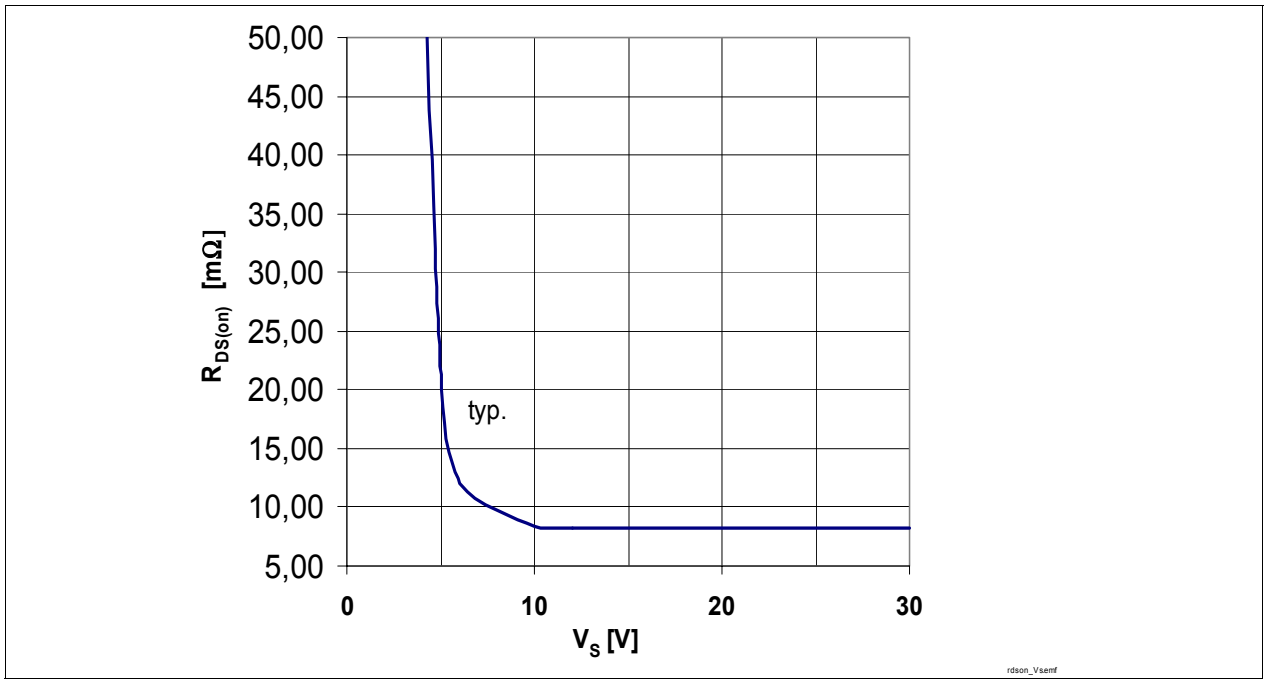


Figure 10 Typical On-State Resistance R_{DSon} = f(V_S)

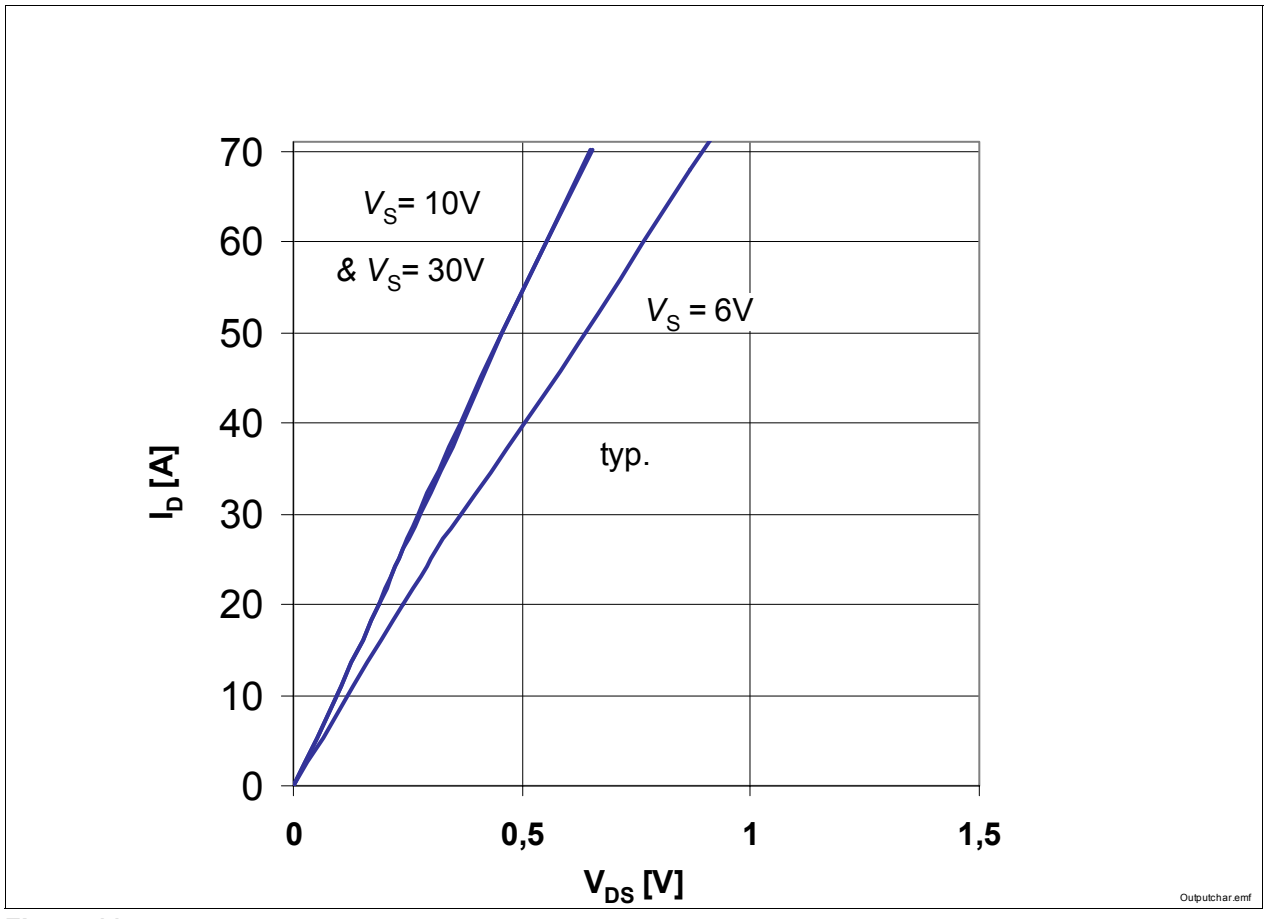


Figure 11 Typical Output Characteristics, T_{Jstart} = 25 °C, Parameter V_S

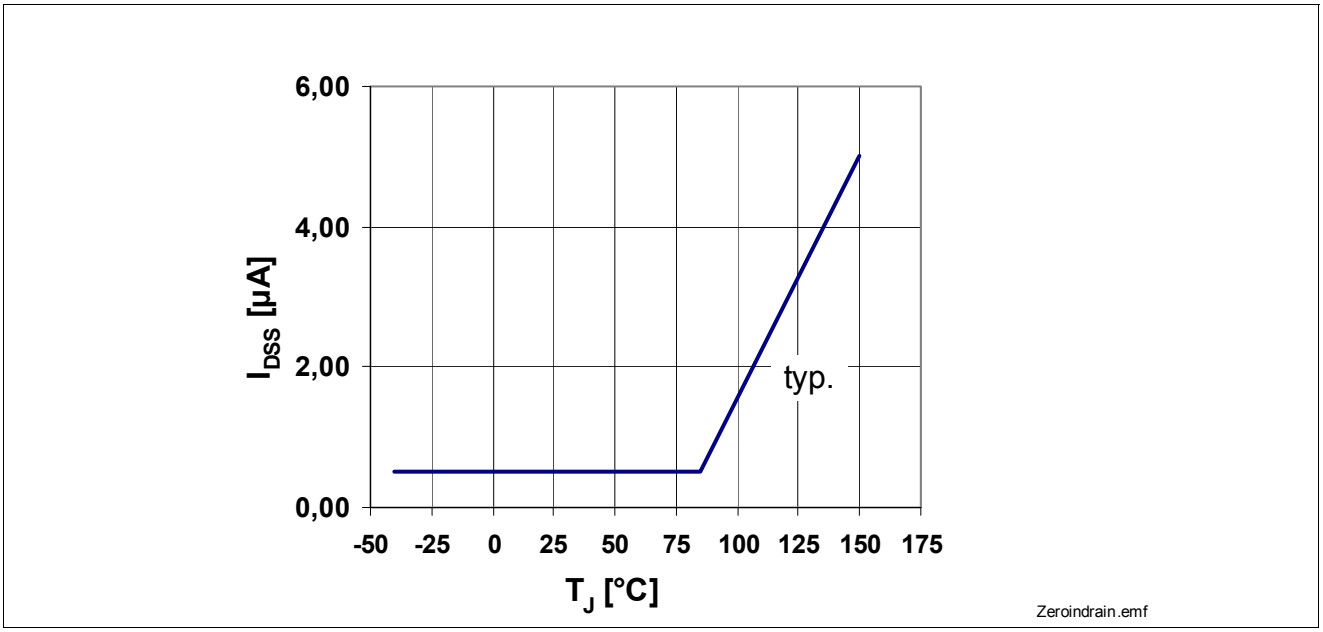


Figure 12 Typical Zero Input Voltage Drain Current, I_{DSS} = f(T_J)

6.2 Output Timing and Slopes

A high signal on the input pin causes the power MOSFET to switch on with a dedicated slope which is optimized for low EMC emission. **Figure 13** shows the timing definition.

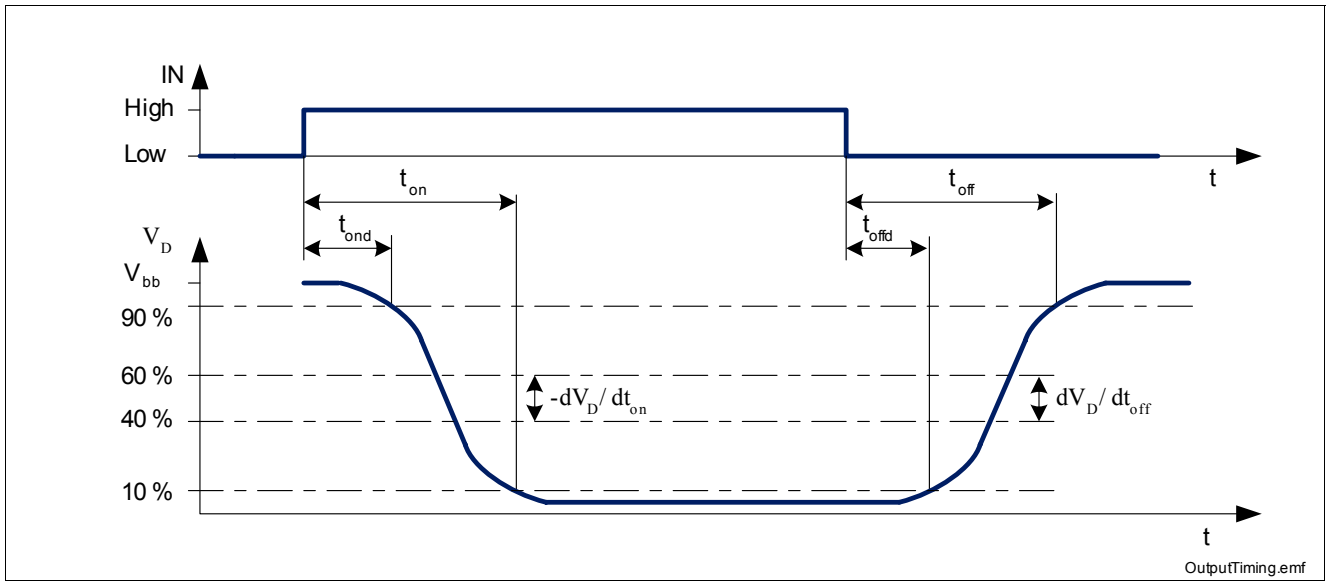


Figure 13 Switching a resistive Load

In order to minimize the emission during switching the BTS3160D limits the slopes during turn on- and off to slow slew rate settings.The definition is shown in **Figure 14**. For best performance of the edge shaping the supply pin V_S should be connected to battery voltage. For supply voltages other than nominal battery the edge shaping can differ from the values in the electrical characteristics table below.

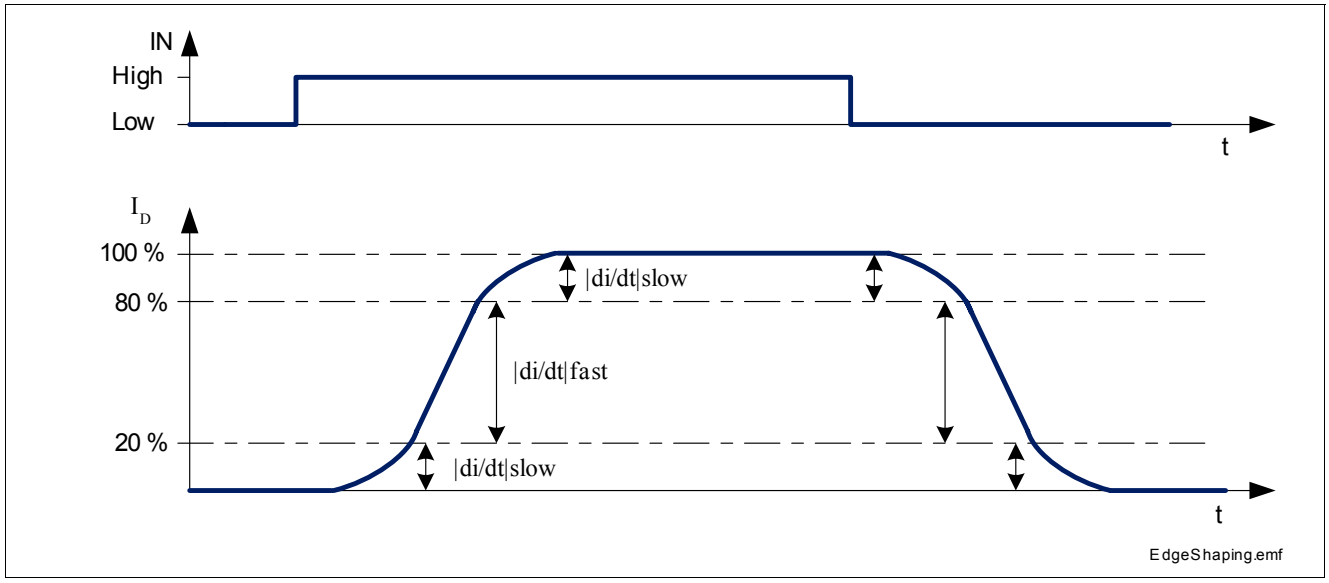


Figure 14 Typical Slopes for resistive Loads

6.3 Inductive Output Clamp

When switching off inductive loads with low-side switches, the Drain Source voltage V_D rises above battery potential, because the inductance intends to continue driving the current.

The BTS3160D is equipped with a voltage clamp mechanism that keeps the Drain-Source voltage V_D at a certain level. See **Figure 15** for more details.

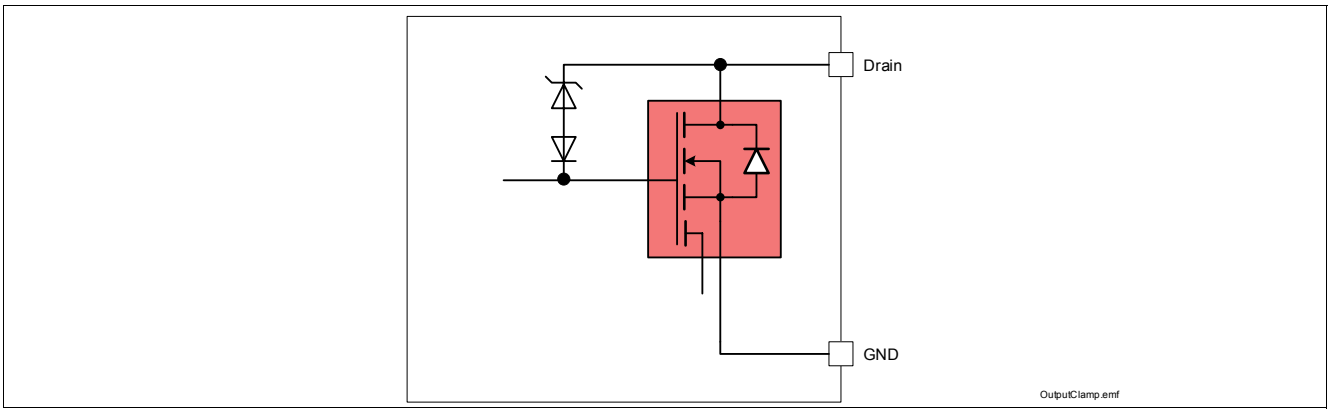


Figure 15 Output Clamp

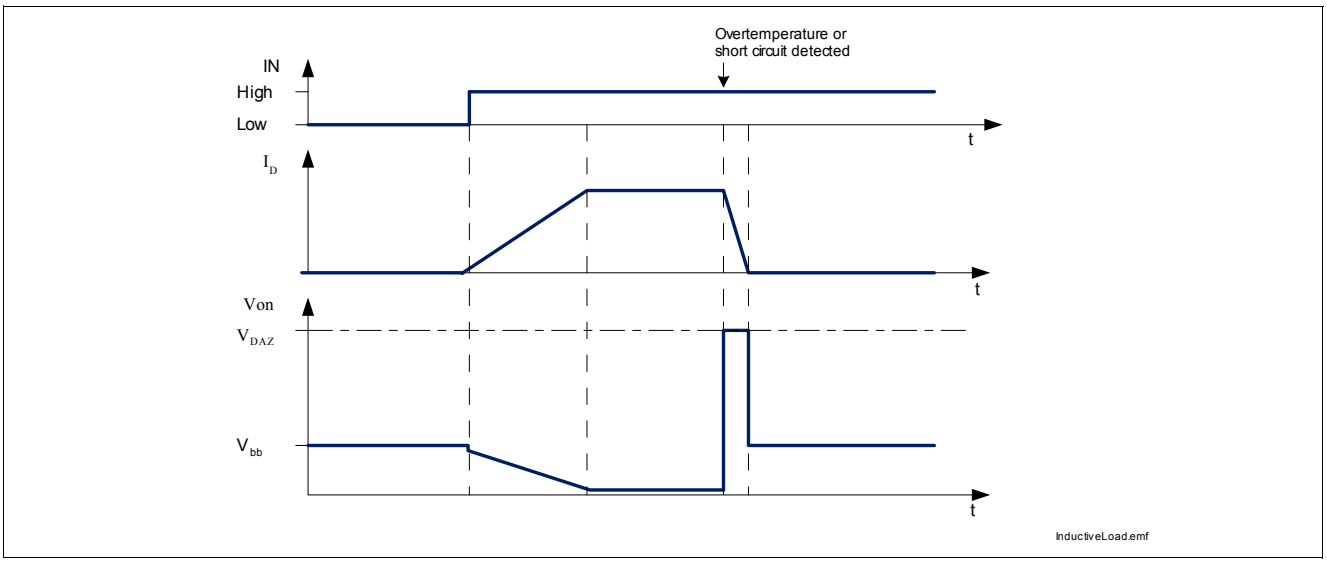


Figure 16 Switching an inductance

While demagnetization of inductive loads, energy has to be dissipated in the BTS3160D. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \cdot \left[\frac{V_{bb} - V_{DS(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_{bb} - V_{DS(CL)}}\right) + I_L \right] \cdot \frac{L}{R_L}$$

Following equation simplifies under assumption of R_L = 0

$$E = \frac{1}{2} L I_L^2 \cdot \left(1 - \frac{V_{bb}}{V_{bb} - V_{DS(CL)}}\right)$$

Figure 17 shows the inductance / current combination the BTS3160D can handle.

For maximum single avalanche energy please also refer to E_{AS} value in **"Energies" on Page 8**

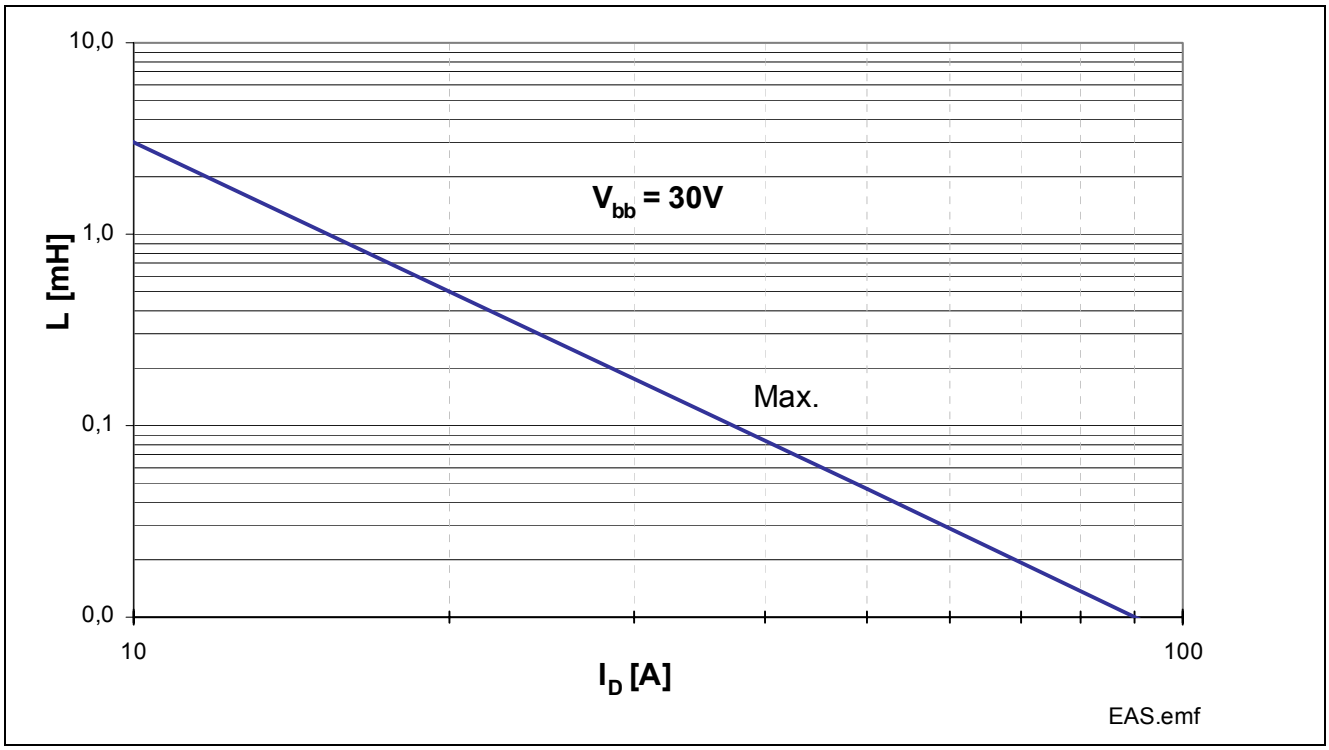


Figure 17 Maximum load inductance for single pulse
$L = f(I_L)$, $T_{j,start}$= 150 °C

6.4 Electrical Characteristics Power Stage

V_S = 6 V to 30 V, T_j = -40 °C to +150 °C

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Power Supply							
6.4.1	On-state resistance	$R_{DS(on)}$	–	8	10	mΩ	I_D = 20 A; V_{IN} = high; V_S = 10 V; T_J = 25 °C
			–	14	18	mΩ	I_D = 20 A; V_{IN} = high; V_S = 10 V; T_J = 150 °C
6.4.2	Nominal load current	I_{Dnom}	7.8	9.7	–	A	[1] V_{on} = 0.5 V; T_A = 85 °C SMD[2]; V_{IN} = 5.0 V; $V_S \geq$ 10 V; $T_J <$ 150 °C
6.4.3	ISO load current	I_{DISO}	33	41	–	A	[1] V_{on} = 0.5 V; T_C = 85 °C; V_{IN} = 5.0 V; $V_S \geq$ 10 V; $T_J <$ 150 °C
6.4.4	Off state drain current	I_{DSS}	–	6	12	µA	V_{bb} = 32 V; V_{IN} = 0.0 V
6.4.5			–	1	2	µA	[1] V_{bb} = 13.5 V; V_{IN} = 0.0 V; T_J = 85 °C
Dynamic Characteristics							
6.4.6	Turn-on delay	t_{ond}	20	75	110	µs	R_L = 2.2 Ω; V_{bb} = V_S = 13.5 V
6.4.7	Turn-on time	t_{on}	80	150	250	µs	R_L = 2.2 Ω; V_{bb} = V_S = 13.5 V
6.4.8	Turn-off delay	t_{offd}	20	75	110	µs	R_L = 2.2 Ω; V_{bb} = V_S = 13.5 V
6.4.9	Turn-off time	t_{off}	80	150	250	µs	R_L = 2.2 Ω; V_{bb} = V_S = 13.5 V
6.4.10	Slew rate on	$-dV_D/dt_{on}$	0.1	0.3	0.7	V/µs	R_L = 2.2 Ω; V_{bb} = V_S = 13.5 V
6.4.11	Slew rate off	dV_D/dt_{off}	0.1	0.3	0.7	V/µs	R_L = 2.2 Ω; V_{bb} = V_S = 13.5 V
6.4.12	Slew rate during edge shaping	$\|dI/dt\|_{slow}$	–	0.04	0.07	A/µs	[1] R_L = 2.2 Ω V_{bb} = V_S = 13.5 V; ohmic load

V_S = 6 V to 30 V, T_j = -40 °C to +150 °C

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.4.13	Slew rate between edge shaping	$\|dI/dt\|_{fast}$	–	–	0.3	A/µs	1) R_L = 2.2 Ω V_{bb} = V_S = 13.5 V; ohmic load
6.4.14	Fault signal delay	t_{dfault}	–	4	10	µs	1)
Inverse Diode							
6.4.15	Inverse Diode forward voltage	V_D	-0.3	-1.0	-1.5	V	I_D = -12 A; V_S = 0 V; V_{IN} = 0.0 V

1) Not subject to production test.

2) Device on 50 mm × 50 mm × 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB mounted vertical without blown air.

7 Protection Functions

The device provides embedded protection functions against over temperature, over load and short circuit.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operation.

7.1 Thermal Protection

The device is protected against over temperature resulting due to overload and / or bad cooling conditions.

The BTS3160D has a thermal latch function. The thermal latch is reset by IN-Low signal. See **Figure 18** for the latch behavior.

The diagram naming refers to **Figure 8**

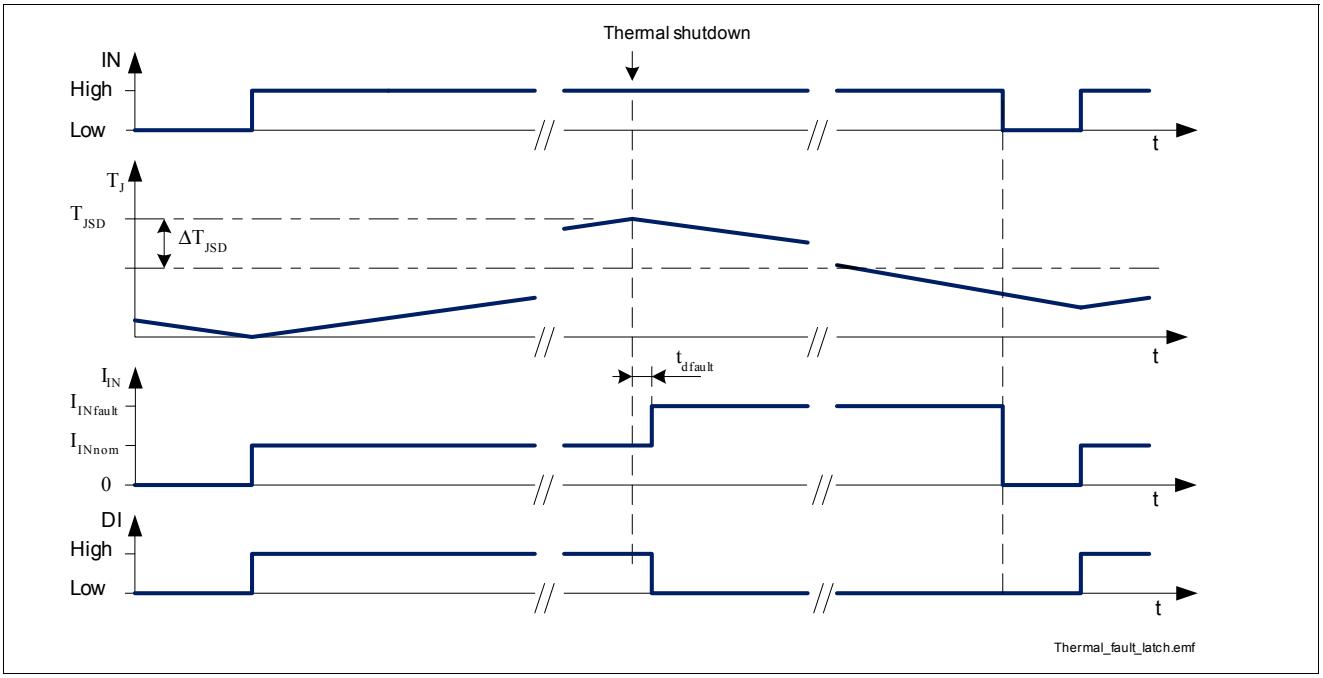


Figure 18 Status Feedback via Input Current at Over temperature

7.2 Over Voltage Protection

The BTS3160D is equipped with a voltage clamp mechanism that keeps the Drain-Source voltage V_D at a certain level. This stage is also used for inductive clamping.

See **"Inductive Output Clamp" on Page 18** for details.

7.3 Short Circuit Protection

The condition short circuit is an overload condition of the device. Dependent on the short circuit resistance the current increase is more or less steep. In condition of high ohmic short the device heats up and the turn off is due to over temperature. In condition low ohmic short the device turns off on a threshold current level before the over temperature condition is detected. In order to allow short current spikes, the turn off occurs with the delay time t_{dSC}. **Figure 19** shows the behavior mentioned above. In this example the short circuit always occurs after the device has switched on under normal load condition - Short circuit type 2. The definitions of voltages and currents are in respect to **Figure 8**. The behavior of V_{DI} also depends on R_{IN}.

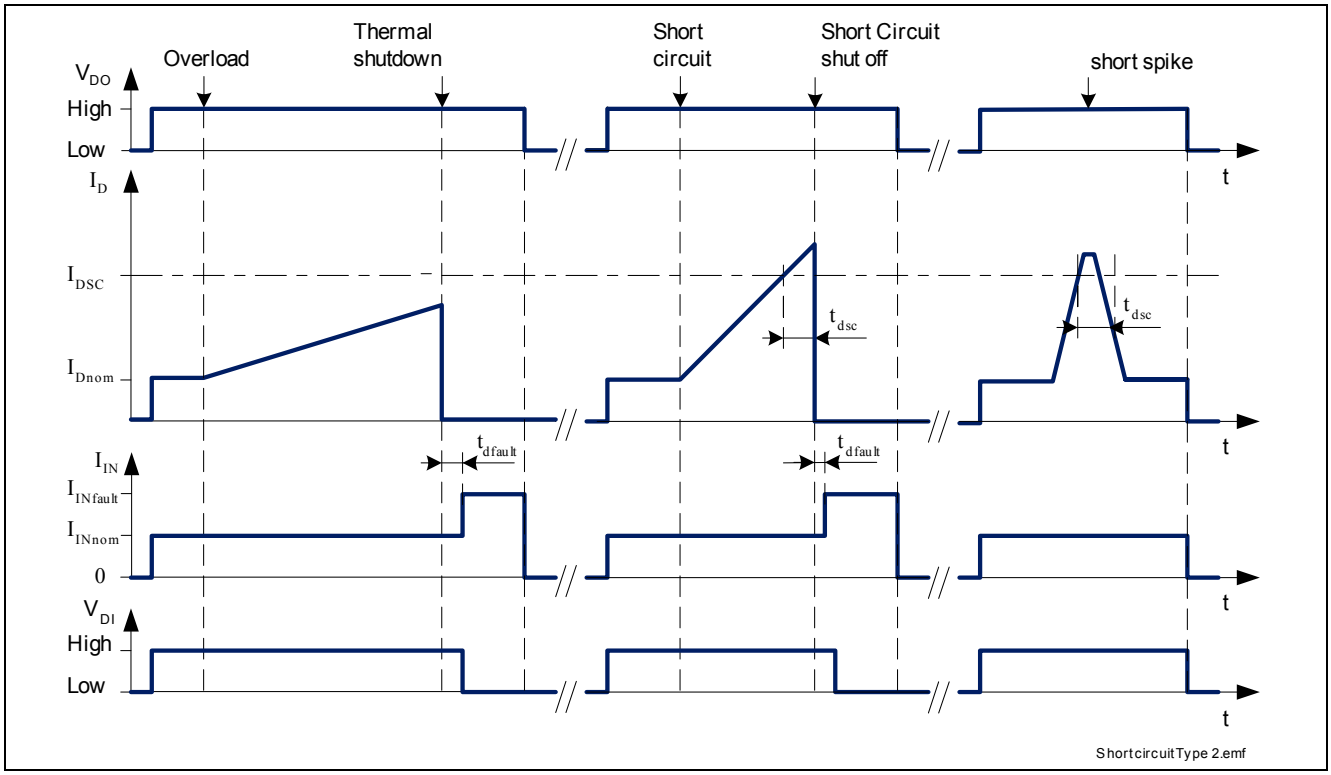


Figure 19 Short Circuit during On State, Typical Behavior for Ohmic Loads

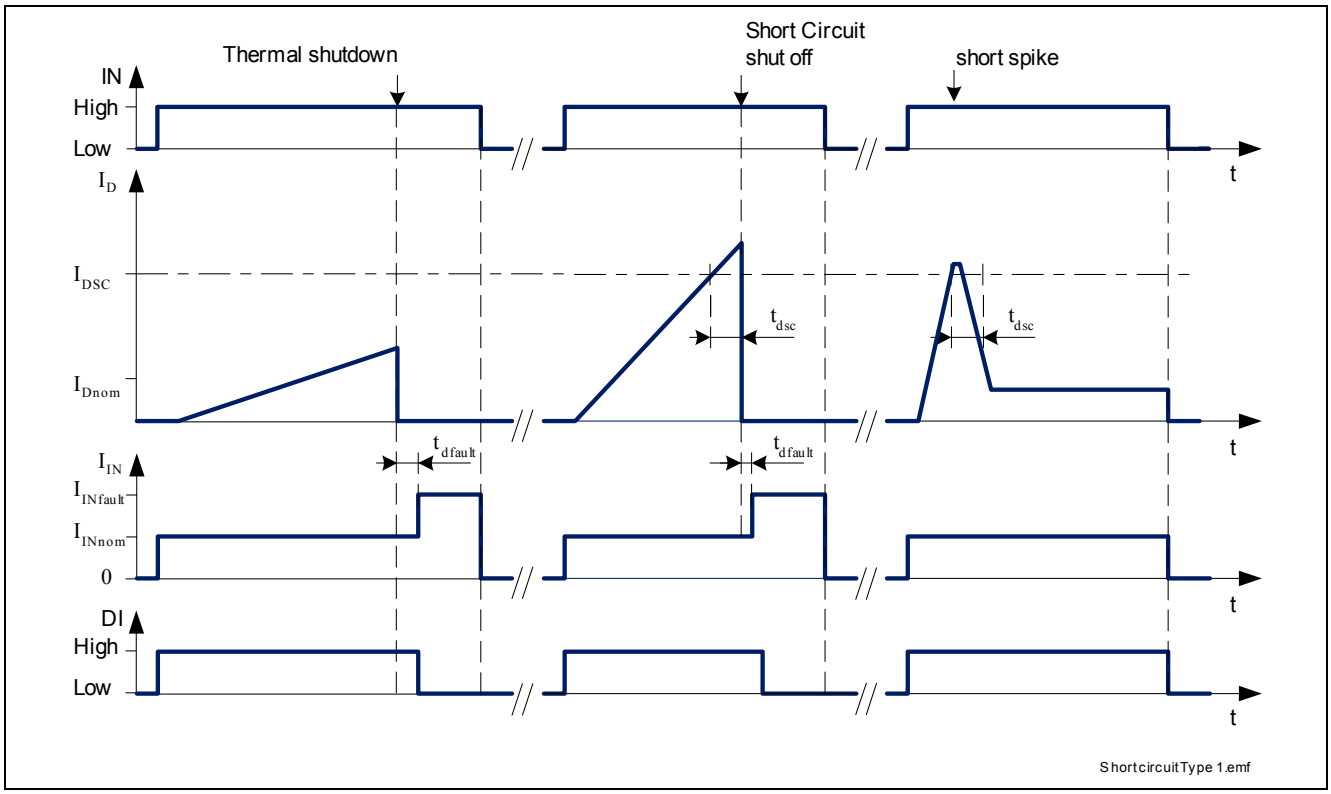


Figure 20 Turn On into Existing Short Circuit, Typical Behavior for Ohmic Loads

The case when the device switches on into an existing short circuit - Short circuit type 1- is shown in **Figure 20**.

The test setup for short circuit characterization is shown in **Figure 21**. The BTS3160D is a low side switch. Therefore it can be assumed that the micro controller and device GND connection have a low impedance. The V_s voltage needs to be stabilized to ensure the protection features. In application this is often already covered from the module standard circuits.

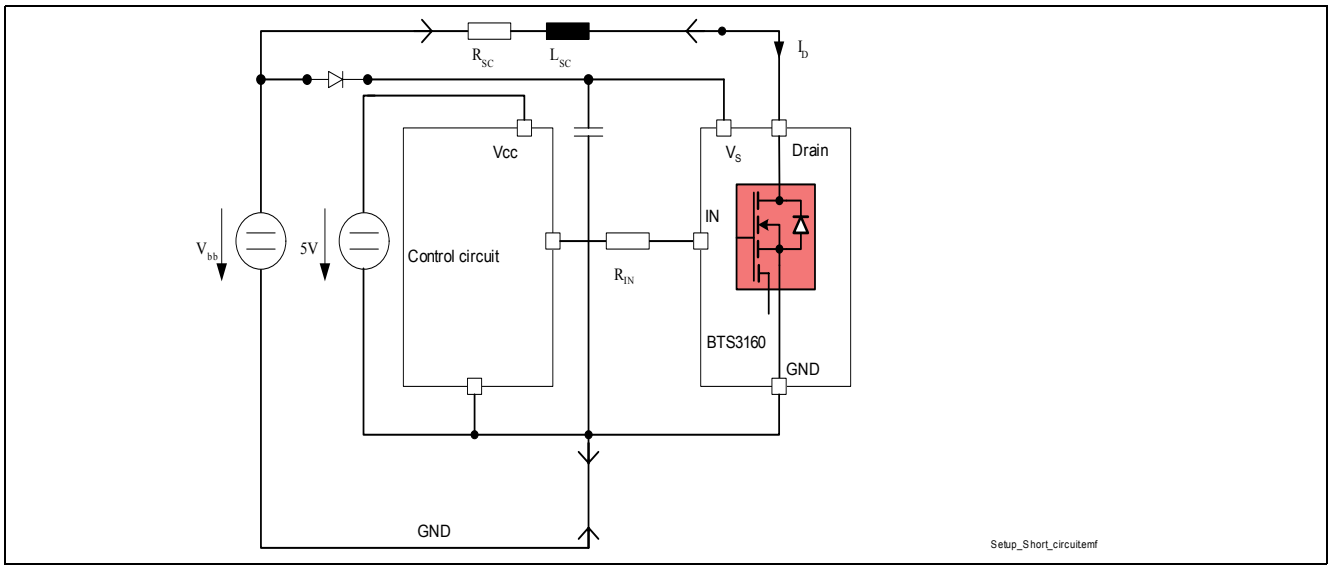


Figure 21 Test Setup for Short Circuit Characterization Test

7.4 Electrical Characteristics Protection

V_S = 6 V to 30 V, T_j = -40 °C to +150 °C

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Thermal Protection							
7.4.1	Thermal shut down junction temperature	T_{JSD}	150	175[1)]	–	°C	V_S = 6.0 V
7.4.2	Thermal hysteresis	ΔT_{JSD}	–	10	–	K	[1)] V_S = 6.0 V
Over Voltage Protection							
7.4.3	Drain source clamp voltage	V_{DAZ}	40	44	–	V	I_D = 10 mA; V_S = 0.0 V; V_{IN} = 0.0 V
			–	45	49	V	I_D = 8 A; V_S = 0.0 V; V_{IN} = 0.0 V
Short Circuit Protection, 6.0 V ≤ V_S ≤ 30 V							
7.4.4	Short circuit shutdown current for max. t_{dSC}	I_{DSC}	70	100	130	A	
7.4.5	Short circuit shutdown delay	t_{dSC}	1	4	8	µs	[1)] $I_D > I_{D(SC)}$, ohmic load

1) Not subject to production test, specified by design.