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BTS50015-1TAD

Smart High-Side Power Switch

1 Overview

Features

- One channel device
- Low Stand-by current
- 3.3 V to V_S level capable input pin
- Electrostatic discharge protection (ESD)
- Optimized Electromagnetic Compatibility (EMC)
- Logic ground independent from load ground
- Very low leakage current at OUT pin
- Compatible to cranking pulse requirement (test pulse 4 of ISO 7637 and cold start pulse in LV124)
- Embedded diagnostic functions
- Embedded protection functions
- Green Product (RoHS compliant)
- AEC Qualified

Applications

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for applications with high current loads, such as heating system, main switch for power distribution, start-stop power supply switch
- PWM applications with low frequencies

Description

The BTS50015-1TAD is a 1.5 mΩ single channel Smart High-Side Power Switch, embedded in a PG-TO-263-7-10 package, providing protective functions and diagnosis. It contains Infineon® ReverSave™ functionality. The power transistor is built by a N-channel power MOSFET with charge pump. It is specially designed to drive high current loads up to 80 A, for applications like switched battery couplings, power distribution switches, heaters, glow plugs, in the harsh automotive environment.

Overview

Table 1 Product Summary

Parameter	Symbol	Values
Operating voltage range	$V_{S(OP)}$	8 V … 18 V
Extended supply voltage including dynamic undervoltage capability	$V_{S(DYN)}$	3.2 V … 28 V
Maximum ON-state resistance (T_J = 150°C)	$R_{DS(ON)}$	3 mΩ
Minimum nominal load current (T_A = 85°C)	$I_{L(NOM)}$	33 A
Typical current sense differential ratio	dk_{ILIS}	51500
Minimum short circuit current threshold	$I_{CL(0)}$	135 A
Maximum stand-by current for the whole device with load (T_A = T_J = 85°C)	$I_{VS\ (OFF)}$	18 µA
Maximum reverse battery voltage (T_A = 25°C for 2 min)	$-V_{S(REV)}$	16 V

Embedded Diagnostic Functions

- Proportional load current sense
- Short circuit / Overtemperature detection
- Latched status signal after short circuit or overtemperature detection

Embedded Protection Functions

- Infineon® ReverSave™: Reverse battery protection by self turn ON of power MOSFET
- Infineon® Inversave: Inverse operation robustness capability
- Secure load turn-OFF while device loss of GND connection
- Overtemperature protection with latch
- Short circuit protection with latch
- Overvoltage protection with external components
- Enhanced short circuit operation
- Infineon® SMART CLAMPING

Type	Package	Marking
BTS50015-1TAD	PG-TO-263-7-10	S50015D

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2 Block Diagram

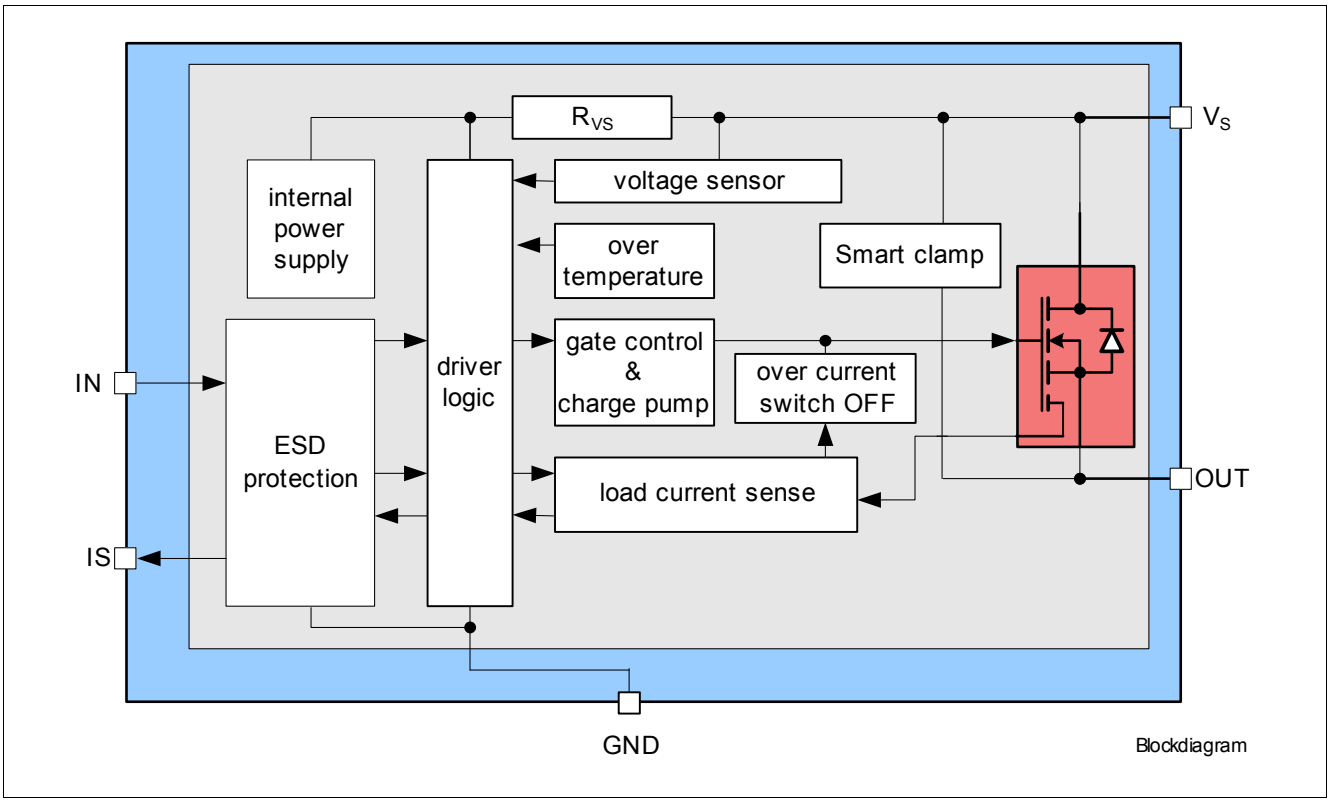

Figure 1 Block Diagram for the BTS50015-1TAD

3 Pin Configuration

3.1 Pin Assignment

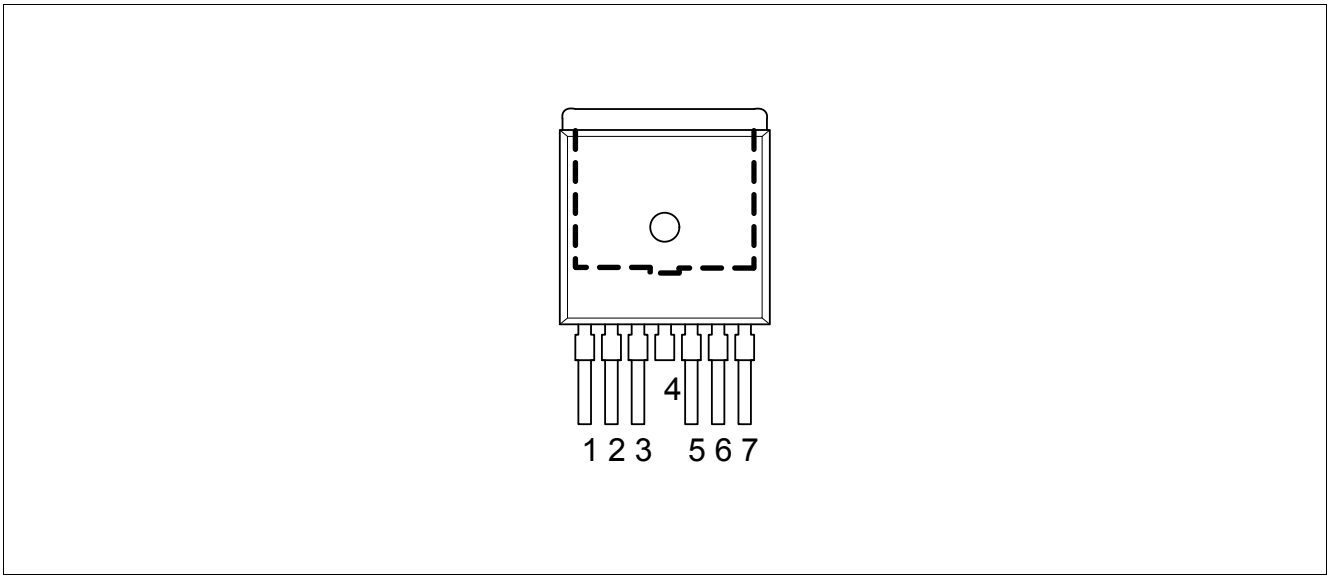

Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**GrouND;** Signal Ground
2	IN	**INput;** Digital signal to switch ON channel (“high” active)
3	IS	**Sense;** Analog/Digital signal for diagnosis, if not used: left open
4, Cooling tab	VS	**Supply Voltage;** Battery voltage
5, 6, 7	OUT	**OUTput;** Protected high side power output channel[1)]

1) All output pins are internally connected and they also have to be connected together on the PCB. Not shorting all outputs on PCB will considerably increase the ON-state resistance and decrease the current sense / overcurrent tripping accuracy. PCB traces have to be designed to withstand the maximum current.

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this Data Sheet, with associated convention for positive values.

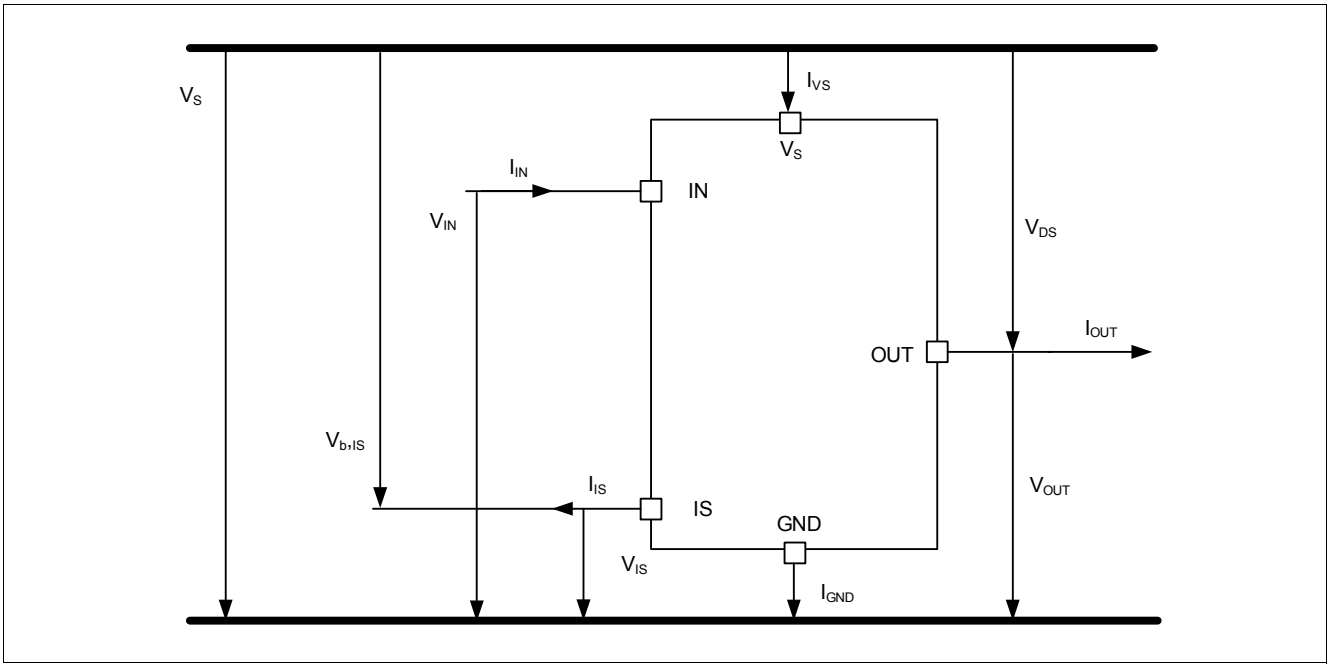

Figure 3 Voltage and Current Definition

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1)]

T_J = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply Voltage	V_S	-0.3	–	28	V	–	P_4.1.1
Reverse Polarity Voltage	$-V_{S(REV)}$	0	–	16	V	[2)] $t < 2$ min T_A = 25°C $R_L \geq 0.5\ \Omega$	P_4.1.2
Load Dump Voltage	$V_{BAT(LD)}$	–	–	45	V	[3)] R_I = 2 Ω R_L = 2.2 Ω R_{IS} = 1 kΩ R_{IN} = 4.7 kΩ	P_4.1.5
Short Circuit Capability							
Supply Voltage for Short Circuit Protection	$V_{S(SC)}$	5	–	20	V	[4)] R_{ECU} = 20 mΩ L_{ECU} = 1 µH R_{cable} = 6 mΩ/m L_{cable} = 1 µH/m l = 0 to 5 m R, C as shown in **Figure 31** See **Chapter 5.3**	P_4.1.3
Short Circuit is Permanent: IN Pin Toggles Short Circuit (SC type 1)	n_{RSC1}	–	–	1 million (Grade A)	–	[5)]	P_4.1.4
GND Pin							
Current through GND pin	I_{GND}	-15 –[6)]	– –	10[7)] 15	mA	– $t \leq 2$ min	P_4.1.6
Input Pin							
Voltage at IN pin	V_{IN}	-0.3	–	V_S	V	–	P_4.1.7
Current through IN pin	I_{IN}	-5 -5	– –	5 50[6)]	mA	– $t \leq 2$ min	P_4.1.8
Maximum Retry Cycle Rate in Fault Condition	f_{fault}	–	–	1	Hz	–	P_4.1.9

Table 2 Absolute Maximum Ratings[1)] (cont'd)

T_J = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Sense Pin							
Voltage at IS pin	V_{IS}	-0.3	–	V_S	V	–	P_4.1.10
Current through IS Pin	I_{IS}	-15 –[6)]	– –	10[7)] 15	mA	– $t \leq 2$ min	P_4.1.11
Power Stage							
Maximum Energy Dissipation by Switching Off Inductive Load Single Pulse over Lifetime	E_{AS}	–	–	3000	mJ	V_S = 13.5 V $I_L = I_{L(NOM)}$ = 33A $T_{J(0)} \leq$ 150°C See **Figure 5**	P_4.1.12
Maximum Energy Dissipation Repetitive Pulse	E_{AR}	–	–	550	mJ	[8)] V_S = 13.5 V $I_L = I_{L(NOM)}$ = 33A $T_{J(0)} \leq$ 105°C See **Figure 5**	P_4.1.13
Maximum Energy Dissipation Repetitive Pulse	E_{AR}	–	–	200	mJ	[8)] V_S = 13.5 V I_L = 80A $T_{J(0)} \leq$ 105°C See **Figure 5**	P_4.1.14
Average Power Dissipation	P_{TOT}	–	–	200	W	T_C = -40°C to 150°C	P_4.1.15
Voltage at OUT Pin	V_{OUT}	-64	–	–	V	–	P_4.1.21
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	P_4.1.16
Dynamic Temperature Increase while Switching	ΔT_J	–	–	60	K	See **Chapter 5.3**	P_4.1.17
Storage Temperature	T_{STG}	-55	–	150	°C	–	P_4.1.18
ESD Susceptibility							
ESD Susceptibility (all Pins)	$V_{ESD(HBM)}$	-2	–	2	kV	HBM[9)]	P_4.1.19
ESD Susceptibility OUT Pin vs. GND / V_S	$V_{ESD(HBM)}$	-4	–	4	kV	HBM[9)]	P_4.1.20

1) Not subject to production test, specified by design.
2) The device is mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection.
3) $V_{S(LD)}$ is setup without DUT connected to the generator per ISO 7637-1.
4) In accordance to AEC Q100-012, Figure-1 Test Circuit.
5) In accordance to AEC Q100-012, Chapter 3 conditions. Short circuit conditions deviating from AEC Q100-012 may influence the specified short circuit cycle number in the Data Sheet.
6) The total reverse current (sum of I_{GND}, I_{IS} and $-I_{IN}$) is limited by $-V_{S(REV)\_max}$ and R_{VS}.
7) $T_C \leq$ 125°C
8) Setup with repetitive EAR and superimposed TC conditions (like AEC-Q100-PTC, $\leq 10^6$ pulses with E $\leq E_{AR}$, $\leq 10^3$ passive temperature cycles), parameter drift within datasheet limits possible
9) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the Data Sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

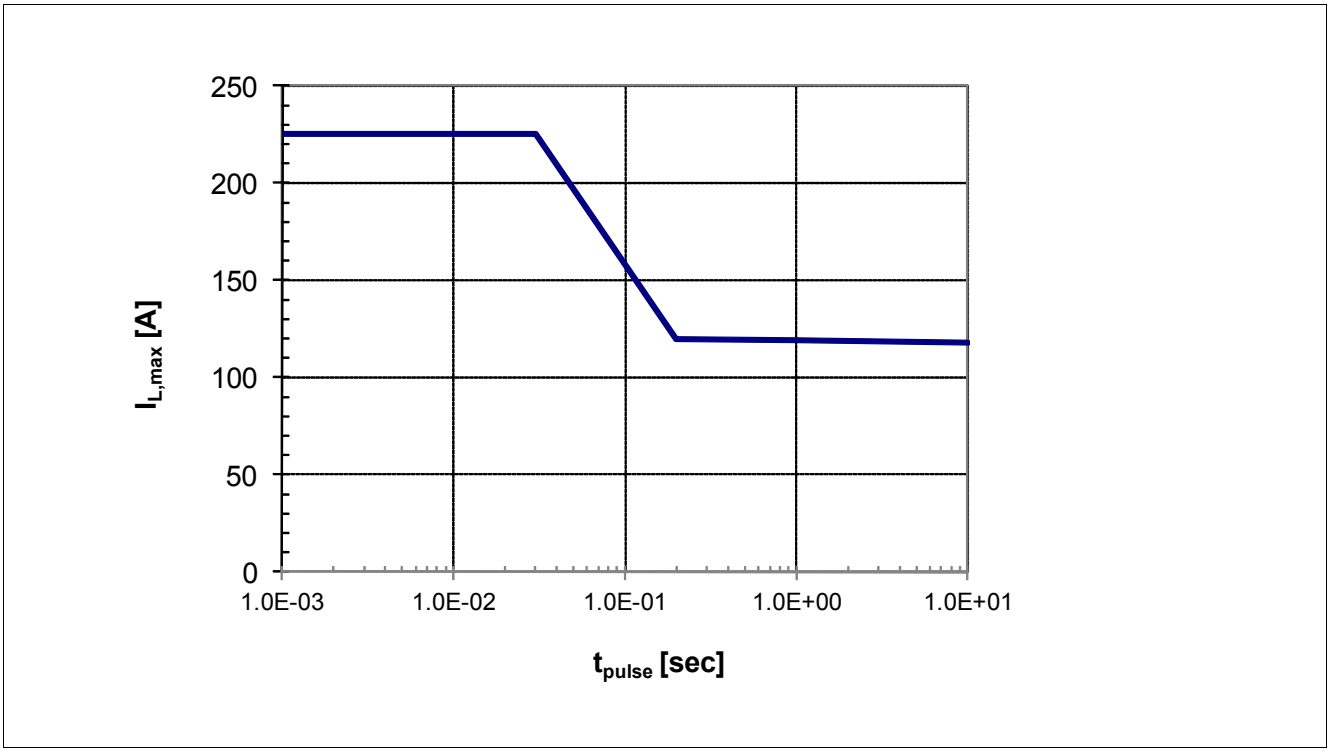

Figure 4 Maximum Single Pulse Current vs. Pulse Time, $T_J \leq 150°C$, $T_{PIN} = 85°C$

Note: Above diagram shows the maximum single pulse current that can be maintained by the internal power stage bond wires for a given pulse time t_{pulse}. The maximum reachable current may be smaller depending on the device current limitation level. The maximum reachable pulse time may be shorter due to thermal protection of the device. T_{PIN} is the temperature of pins 5, 6 and 7.

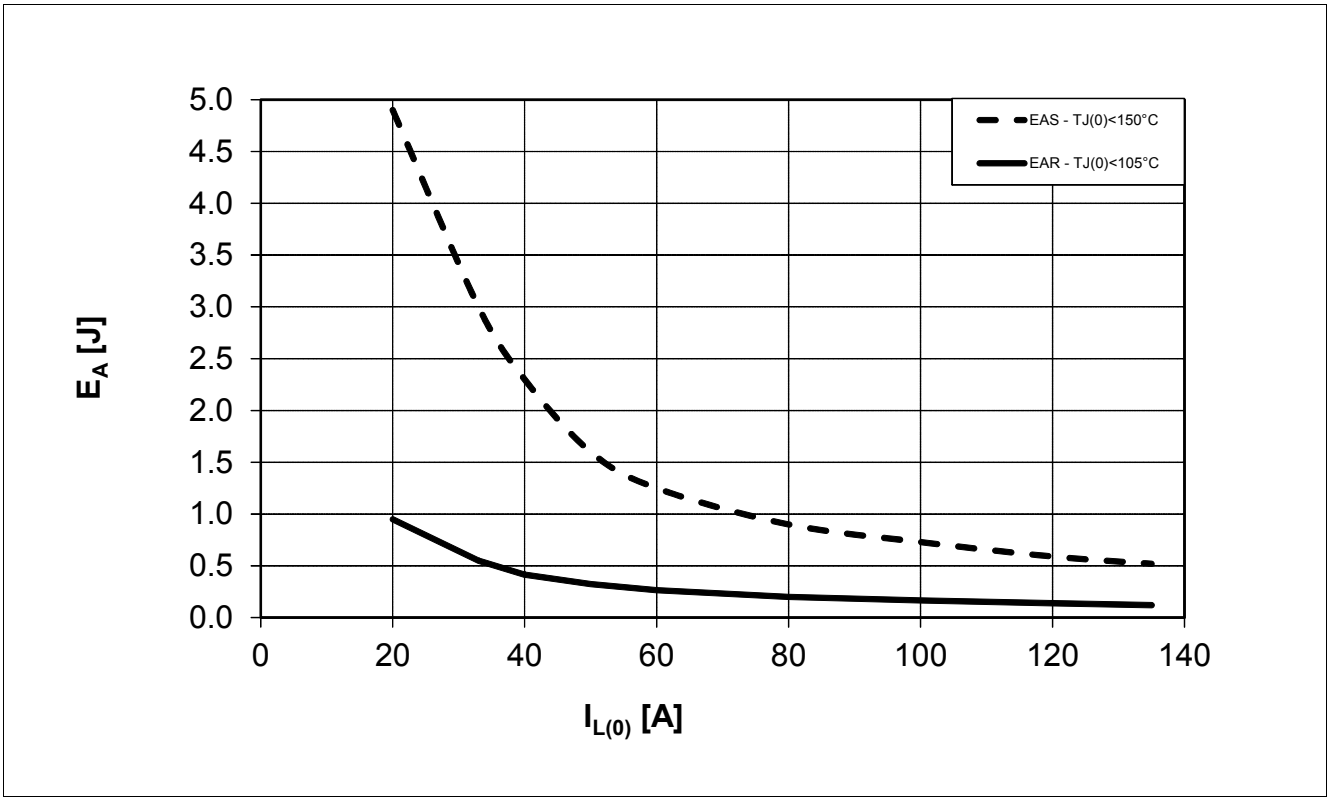

Figure 5 Maximum Energy Dissipation for Inductive Switch OFF, E_A vs. I_L at V_S = 13.5 V

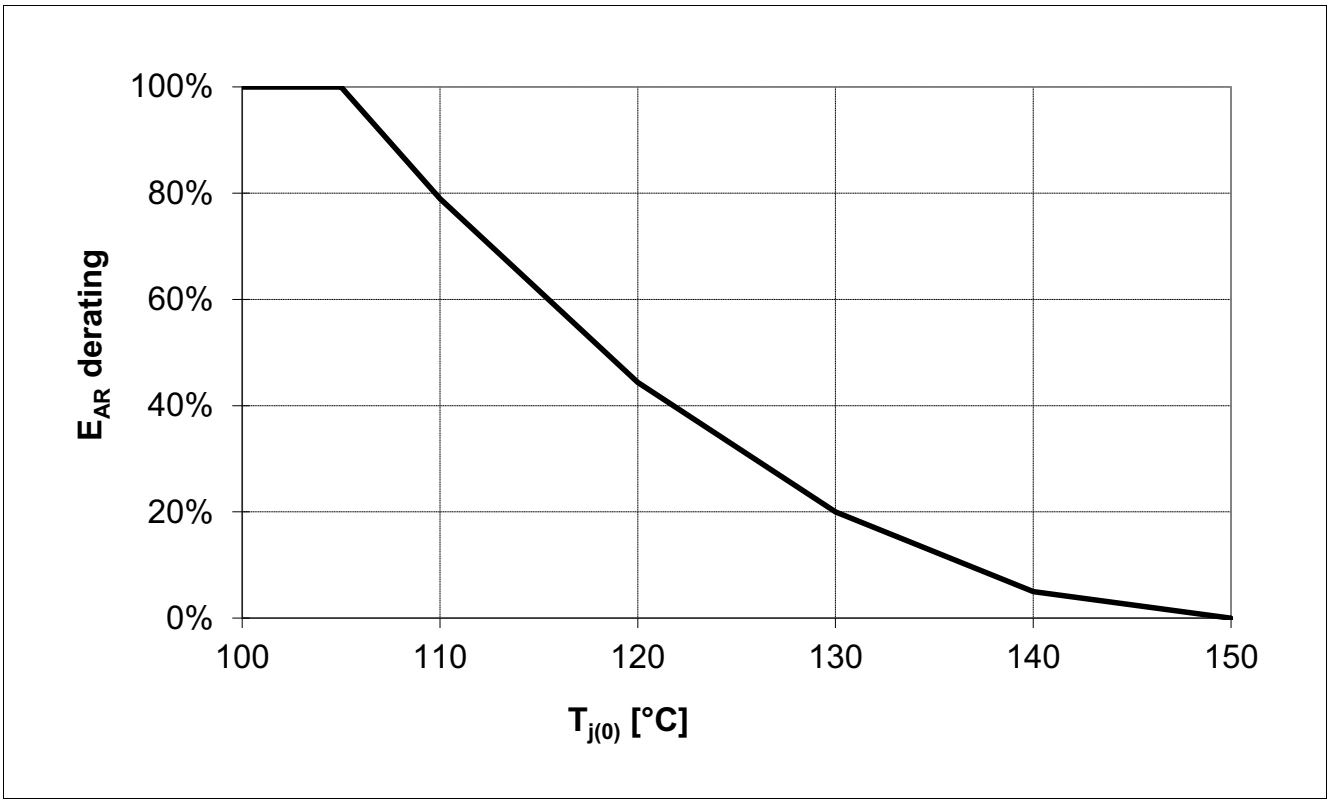

Figure 6 Maximum Energy Dissipation Repetitive Pulse temperature derating

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Nominal Operation	$V_{S(NOM)}$	8	–	18	V	–	P_4.2.1
Supply Voltage Range for Extended Operation	$V_{S(EXT)}$	5.3	–	28	V	1) $V_{IN} \geq 2.2$ V $I_L \leq I_{L(NOM)}$ $T_J \leq 25$°C Parameter deviations possible	P_4.2.2
	$V_{S(EXT)}$	5.5	–	28	V	1) $V_{IN} \geq 2.2$ V $I_L \leq I_{L(NOM)}$ $T_J = 150$°C Parameter deviations possible	
Supply Voltage Range for Extended Operation Dynamic Undervoltage Capability	$V_{S(EXT,DYN)}$	3.2 2)	–	–	V	1) acc. to ISO 7637	P_4.2.3
Supply Undervoltage Shutdown	$V_{S(UV)}$	–	–	4.5	V	1) $V_{IN} \geq 2.2$ V $R_L = 270\ \Omega$ V_S decreasing See **Figure 20**	P_4.2.4
Slewrate at OUT	$\lvert dV_{DS}/dt \rvert$	–	–	10	V/µs	1) $\lvert V_{DS} \rvert < 3$V See **Chapter 5.1.4**	P_4.2.7
Slewrate at OUT	$\lvert dV_{DS}/dt \rvert$	–	–	0.2	V/µs	1) $V_{S(EXT)} < V_S < 8$ V $0 < V_{DS} < 1$ V $t < t_{ON(DELAY)}$ See **Chapter 5.1.4**	P_4.2.8

1) Not subject to production test. Specified by design

2) $T_A = 25$°C; $R_L = 0.5\ \Omega$; pulse duration 6 ms; cranking capability is depending on load and must be verified under application conditions

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	–	0.5	K/W	1)	P_4.3.1
Junction to Ambient	$R_{thJA(2s2p)}$	–	20	–	K/W	1)2)	P_4.3.2
Junction to Ambient	R_{thJA}	–	70	–	K/W	1)3)	P_4.3.3

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. T_A = 25°C. Device is dissipating 2 W power.

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board; the Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with only one top copper layer 1 × 70 µm. T_A = 25°C. Device is dissipating 2 W power.

Figure 7 is showing the typical thermal impedance of BTS50015-1TAD mounted according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 1s0p and 2s2p boards.

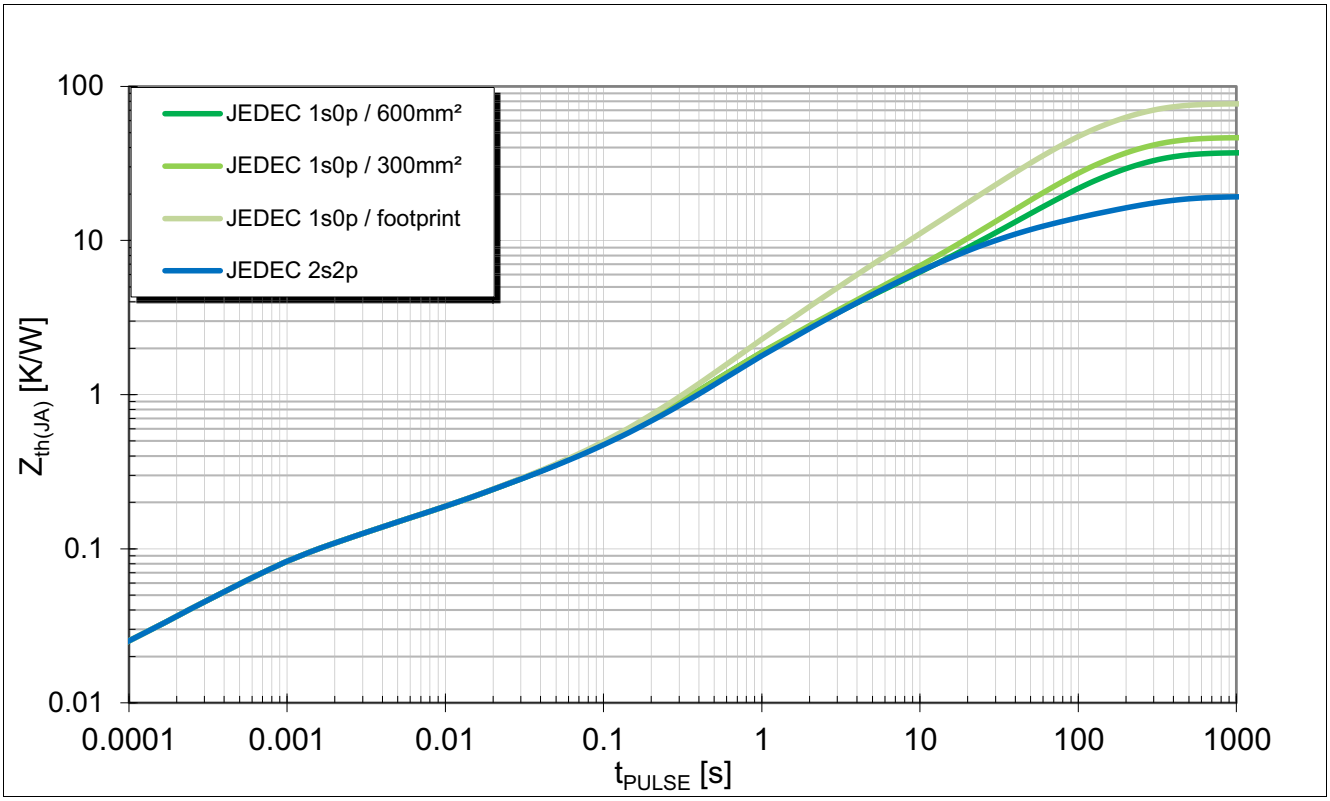

Figure 7 Typical Transient Thermal Impedance $Z_{th(JA)}$ = f(time) for Different PCB Conditions

5 Functional Description

5.1 Power Stage

The power stage is built by a N-channel power MOSFET (DMOS) with charge pump.

5.1.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J. **Page 42** shows the dependencies in terms of temperature and supply voltage, for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 5.3.5**.

A HIGH signal (see **Chapter 5.2**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.1.2 Switching Resistive Loads

Figure 8 shows the typical timing when switching a resistive load. The power stage has a defined switching behavior. Defined slew rates results in lowest EMC emission at minimum switching losses.

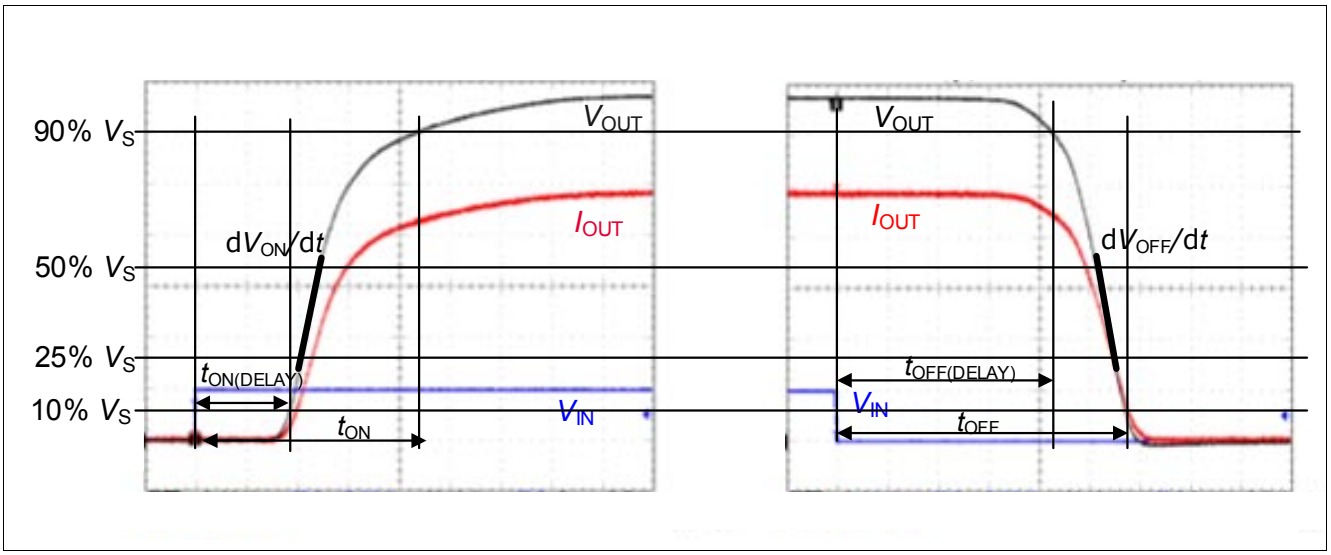

Figure 8 Switching a Resistive Load: Timing

5.1.3 Switching Inductive Loads

5.1.3.1 Output Clamping

When switching OFF inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, there is a Infineon® SMART CLAMPING mechanism implemented that keeps negative output voltage to a certain level (V_S - $V_{DS(CL)}$). Please refer to **Figure 9** and **Figure 10** for details. Nevertheless, the maximum allowed load inductance remains limited.

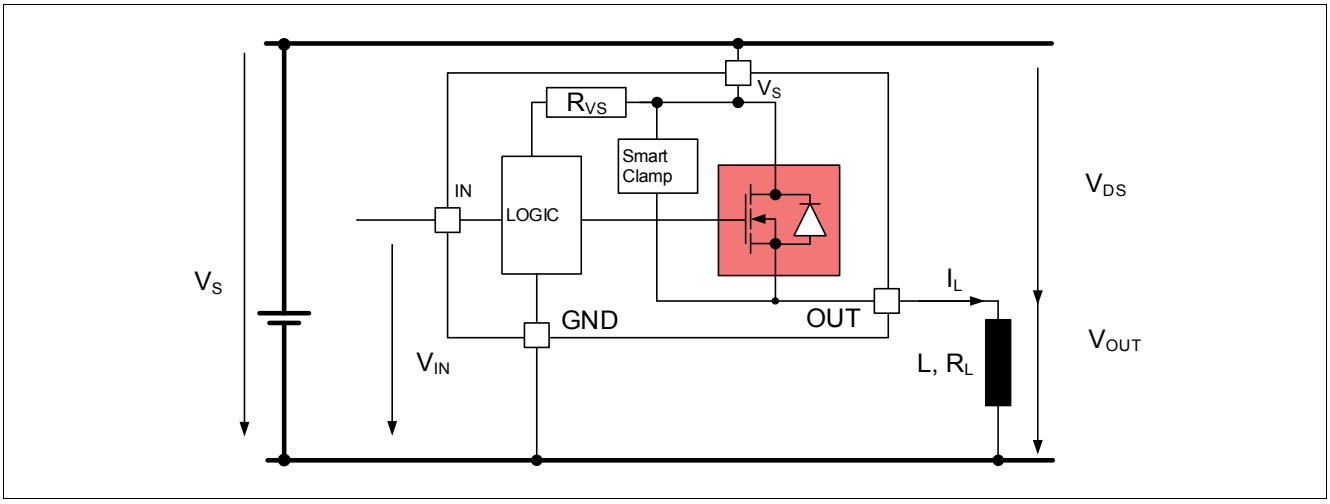

Figure 9 Output Clamp

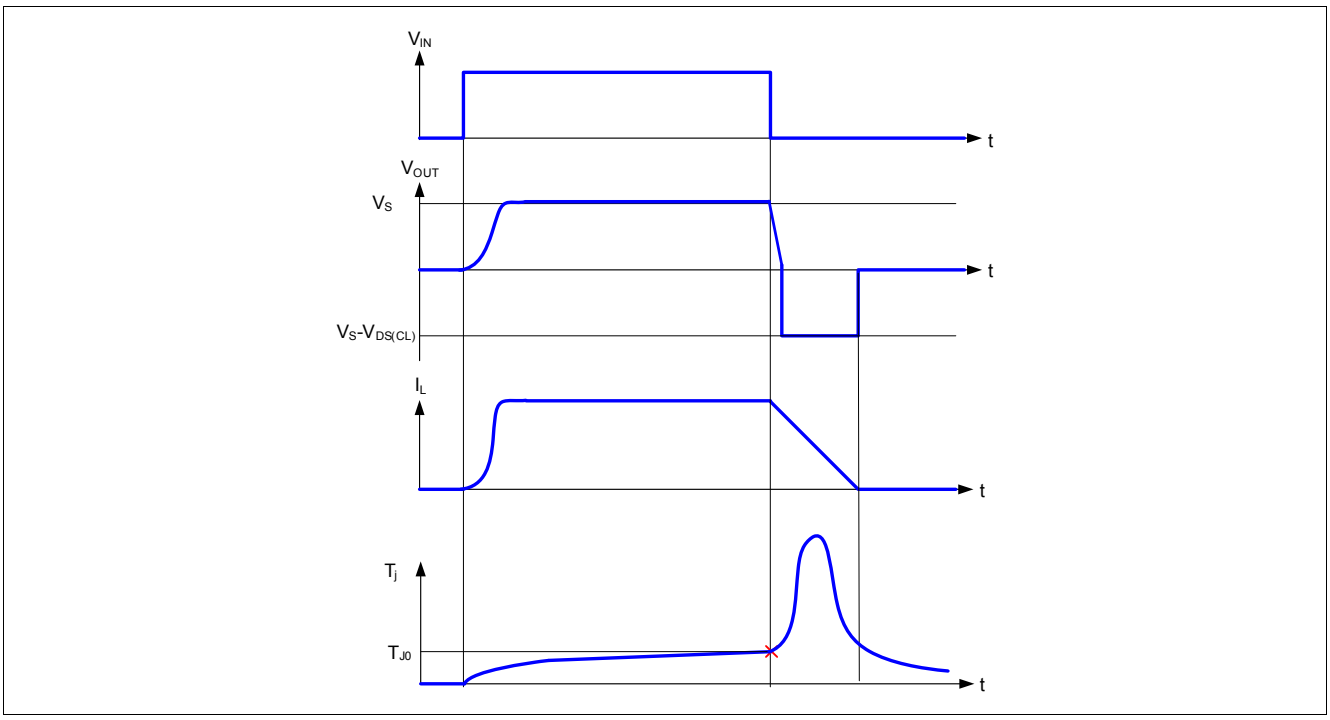

Figure 10 Switching an Inductance

The BTS50015-1TAD provides Infineon® SMART CLAMPING functionality. To increase the energy capability, the clamp voltage $V_{DS(CL)}$ increases with junction temperature T_J and with load current I_L. Refer to **Page 44**.

5.1.3.2 Maximum Load Inductance

During demagnetization of inductive loads, energy must be dissipated in the BTS50015-1TAD. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{DS(CL)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(CL)}}\right) + I_L \right] \quad (5.1)$$

Following equation simplifies under the assumption of R_L = 0 Ω.

$$E = \frac{1}{2} \times L \times I_L^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(CL)}}\right) \quad (5.2)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 5** for the maximum allowed energy dissipation as function of the load current.

5.1.4 Switching Active Loads

When switching generative or electronic loads such as motors or secondary ECUs which have the ability to feed back voltage disturbances to the OUT pins, special attention is required about the resulting absolute and dynamic voltage V_{DS} between VS pin and OUT pins.

To maintain device functionality it is required to limit the maximum positive or negative slew rate of $V_{DS} = V_S - V_{OUT}$ below $|dV_{DS}/dt|$ (parameter P_4.2.7) .

In case the device operates at low battery voltage ($V_S < V_{S(NOM), Min}$) where the load feeds back a positive output voltage reaching almost VS potential ($0 < V_{DS} < 1$ V), it has to be ensured that for each activation (turn-on event), where the device is commanded on by applying $V_{IN(H)}$ at IN pin, a maximum positive or negative slew rate of V_{DS} below $|dV_{DS}/dt|$ (parameter P_4.2.8) will not be exceeded until $t_{ON(DELAY)}$ has expired.

Also in the case of low V_S and low V_{DS} during the rising edge of IN, the device might not turn on. **Figure 11** shows the worst case boundary condition. In such condition, if the device does not turn on, it will be latched.

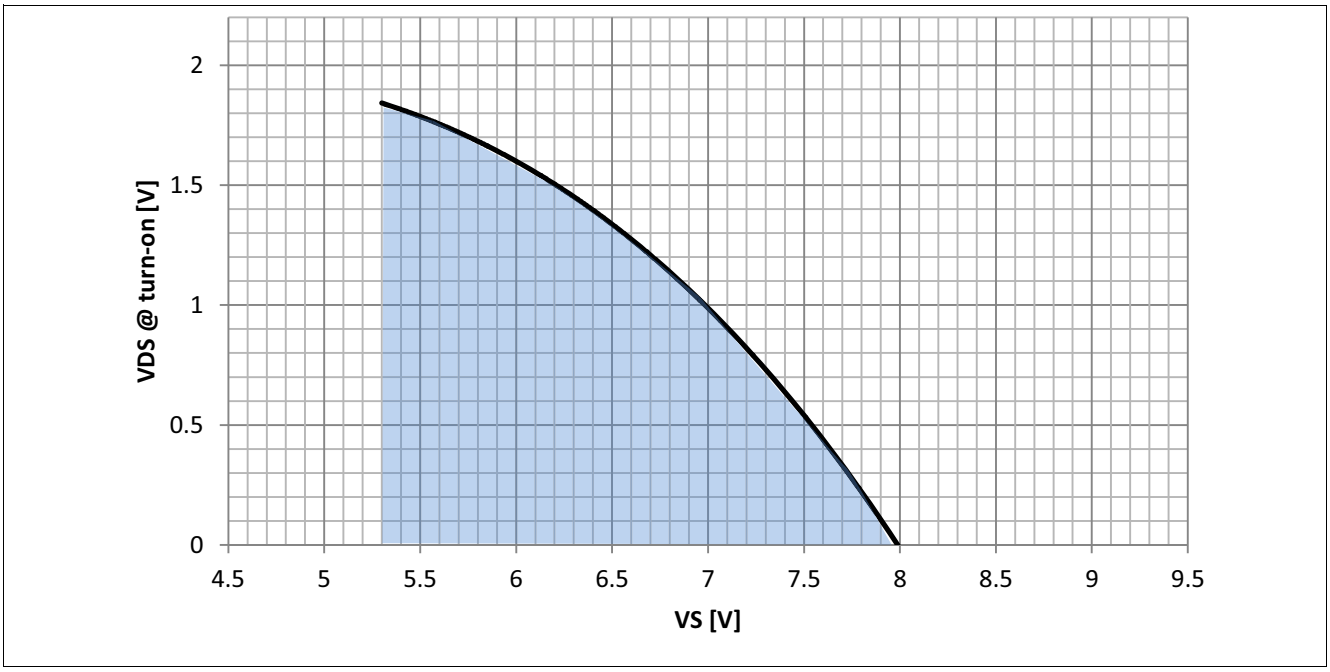

Figure 11 Boundary conditions for switching active loads at low V_S with low initial V_{DS} voltage. (Not subject to production test, specified by design)

For loads that generate steady or dynamic voltage at the OUT pins which is higher than voltage at VS pin please consider **Chapter 5.1.5**.

5.1.5 Inverse Current Capability

In case of inverse current, meaning a voltage $V_{OUT(INV)}$ at the output higher than the supply voltage V_S, a current $I_{L(INV)}$ will flow from output to V_S pin via the body diode of the power transistor (please refer to **Figure 12**). In case the IN pin is HIGH, the power DMOS is already activated and will continue to remain in ON state during the inverse event. In case, the input goes from “L” to “H”, the DMOS will be activated even during an inverse event. Under inverse condition, the device is not overtemperature / overload protected. During inverse mode at ON the sense pin will provide a leakage current of less or equal to I_{IS0}. Due to the limited speed of INV comparator, the inverse duration needs to be limited.

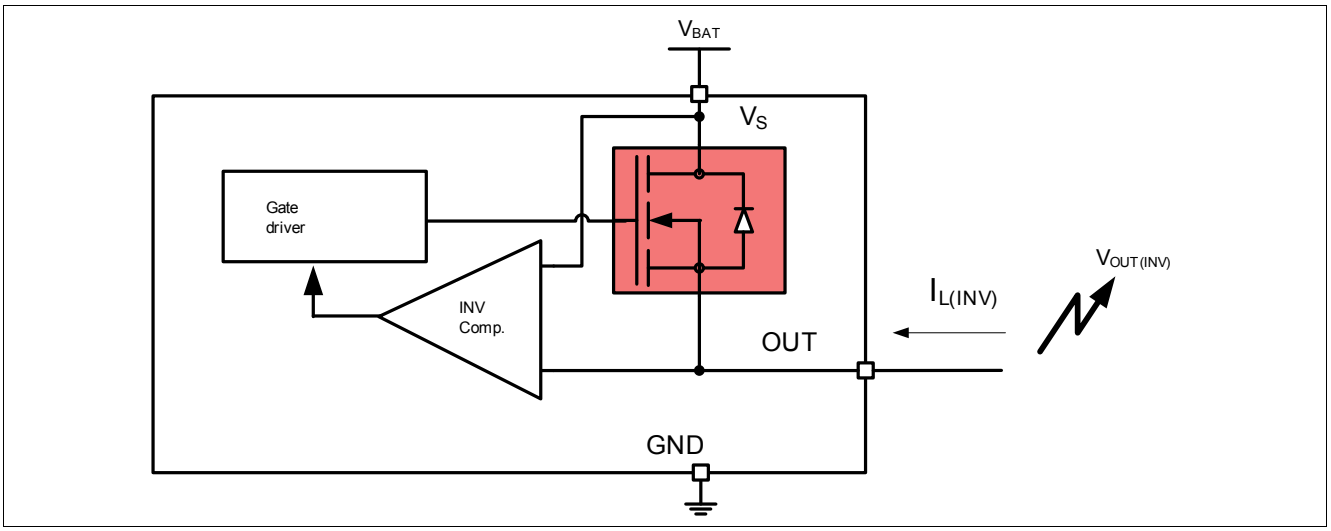

Figure 12 Inverse Current Circuitry

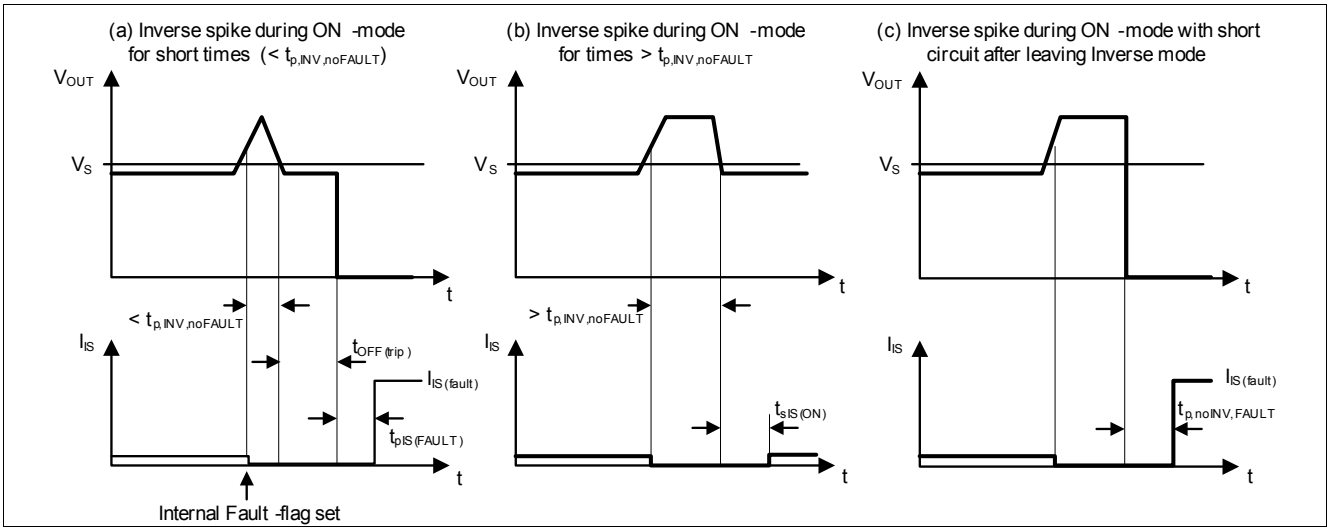

Figure 13 Inverse Behavior - Timing Diagram

5.1.6 PWM Switching

The switching losses during this operation should be properly considered (see following equation):

P_{TOTAL} = (switching_ON_energy + switching_OFF_energy + $I_L^2 \times R_{DS(ON)} \times t_{DC}$) / period

PWM switching application slightly above $t_{IN(RESETDELAY)}$ parameter (see **Figure 26**) with calculated power dissipation $P_{TOTAL} > P_{TOT}$ parameter limit causes an effective increase in $T_{J(TRIP)}$ parameter.

In the event of a fault condition it has to be ensured, that the PWM frequency will not exceed a maximum retry frequency of f_{FAULT} (parameter P_4.1.9). With this measure the short circuit robustness n_{RSC1} (parameter P_4.1.4) can be utilized. Operation at nominal PWM frequency can only be restored, once the fault condition is overcome.

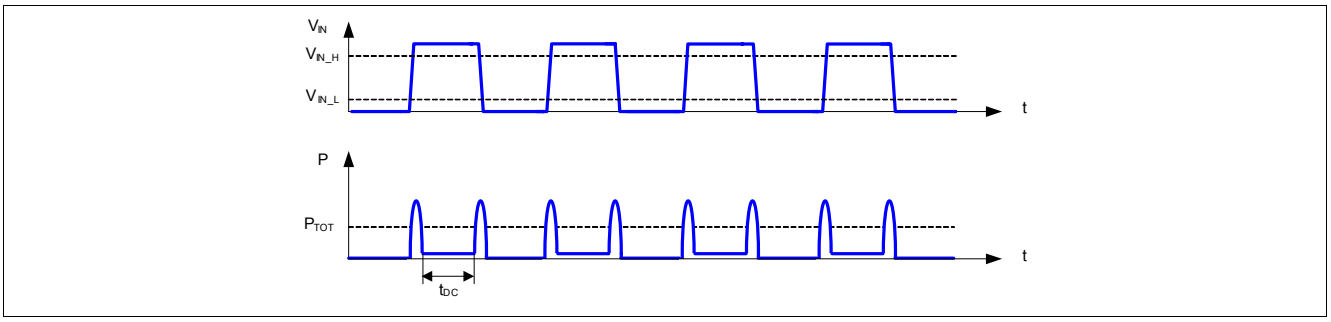

Figure 14 Switching in PWM

5.1.7 Advanced switch-off behavior

In order to reduce device stress when switching OFF critical loads and/or critical load conditions, the device provides an advanced switch off functionality which results in a typically ten times faster switch off behavior. This fast switch off functionality is triggered by one the following conditions:

- The device is commanded off by applying $V_{IN(L)}$ at the IN pin. During the switch OFF operation the OUT pins' voltage in respect to GND pin drops to typically -3 V or below (typically $V_{OUT} - V_{GND} \leq$ -3 V).
- The device is commanded on or is already in on-state. The device then detects a short circuit condition ($I_L \geq I_{CL(0)}$) and initiates a protective switch off. Please refer to **Chapter 5.3.6.1** and **Chapter 5.3.6.2** for details.

5.2 Input Pins

5.2.1 Input Circuitry

The input circuitry is compatible with 3.3 V and 5 V microcontrollers or can be directly driven by V_S. The concept of the input pin is to react to voltage threshold. With the Schmitt trigger, the output is either ON or OFF. **Figure 15** shows the electrical equivalent input circuitry.

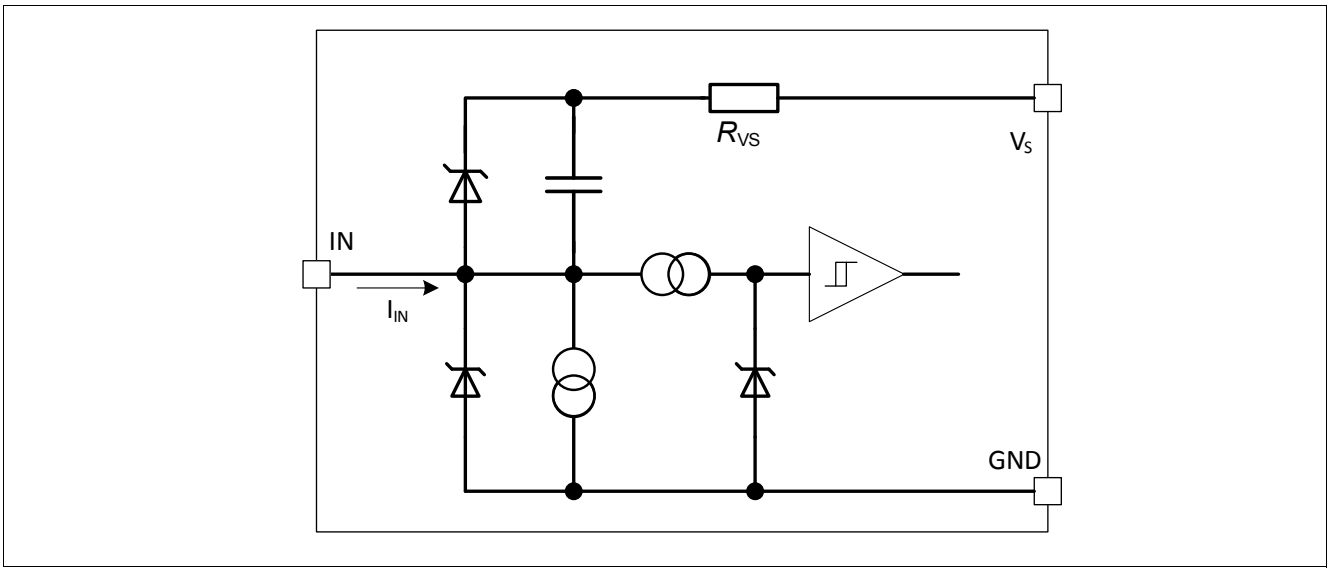

Figure 15 Input Pin Circuitry

5.2.2 Input Pin Voltage

The IN uses a comparator with hysteresis. The switching ON / OFF takes place in a defined region, set by the threshold $V_{IN(L)\ Max}$ and $V_{IN(H)\ Min.}$ The exact value where ON and OFF take place depends on the process, as well as the temperature. To avoid cross talk and parasitic turn ON and OFF, an hysteresis is implemented. This ensures immunity to noise.

5.3 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent the destruction of the IC from fault conditions described in the Data Sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed neither for continuous nor for repetitive operation.

Figure 16 describes the typical functionality of the diagnosis and protection block.

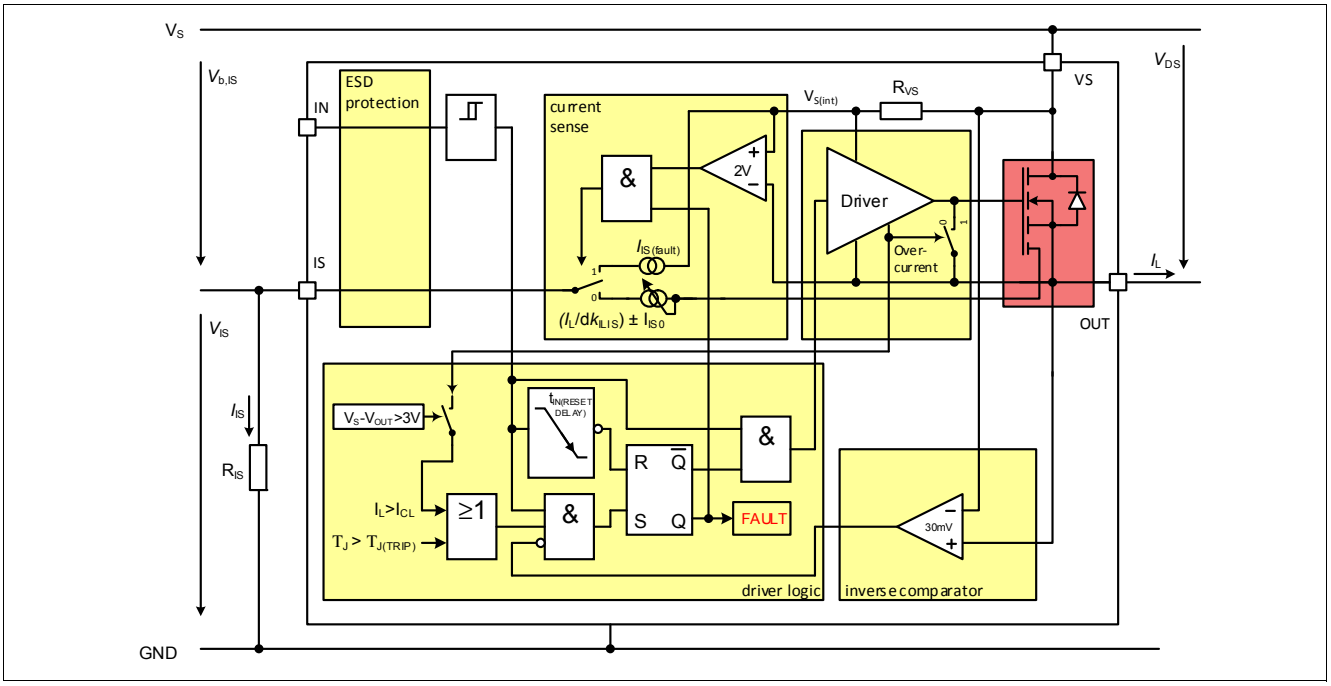

Figure 16 Diagram of Diagnosis & Protection Block

5.3.1 Loss of Ground Protection

In case of loss of module or device ground, where the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied at IN pin. It is recommended to use input resistors between the microcontroller and the BTS50015-1TAD to ensure switching OFF of channel. In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS. **Figure 17** sketches the situation.

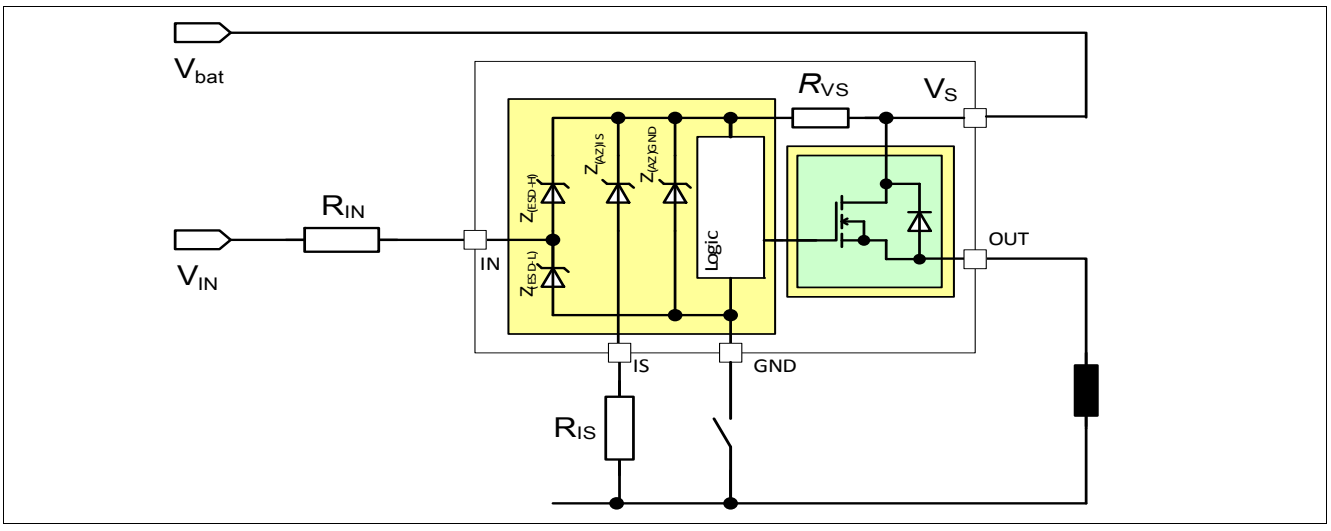

Figure 17 Loss of Ground Protection with External Components

5.3.2 Protection during Loss of Load or Loss of V_S Condition

In case of loss of load with charged primary inductances the supply voltage transient has to be limited. It is recommended to use a Zener diode, a varistor or V_S clamping power switches with connected loads in parallel. The voltage must be limited according to the minimum value of the parameter 6.1.33 indicated in **Table 6**.

In case of loss of V_S connection with charged inductive loads, a current path with sufficient load current capability has to be provided, to demagnetize the charged inductances. It is recommended to protect the device using a Zener diode together with a diode ($V_{Z1} + V_{D1} < 16$ V), with path (A) or path (B) as shown in **Figure 18**.

For a proper restart of the device after loss of V_S, the input voltage must be delayed compared to the supply voltage ramp up. This can be realized by a capacitor between IN and GND (see **Figure 31**).

For higher clamp voltages, currents through all pins have to be limited according to the maximum ratings. Please see **Figure 18** and **Figure 19** for details.

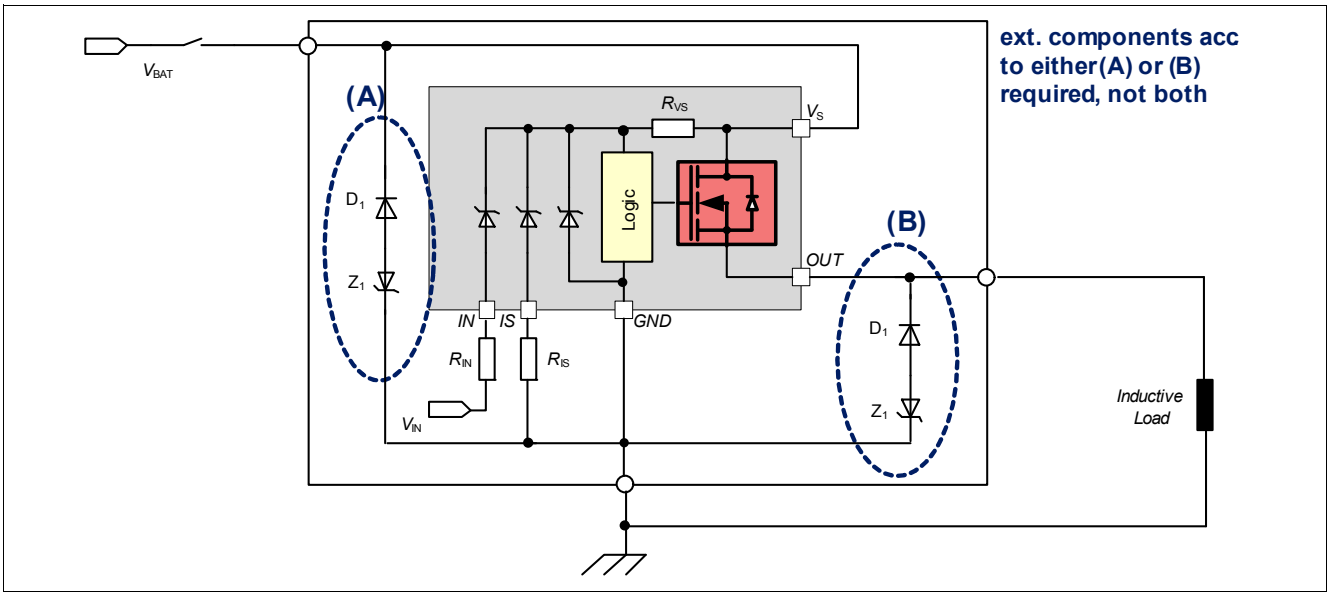

Figure 18 Loss of V_S

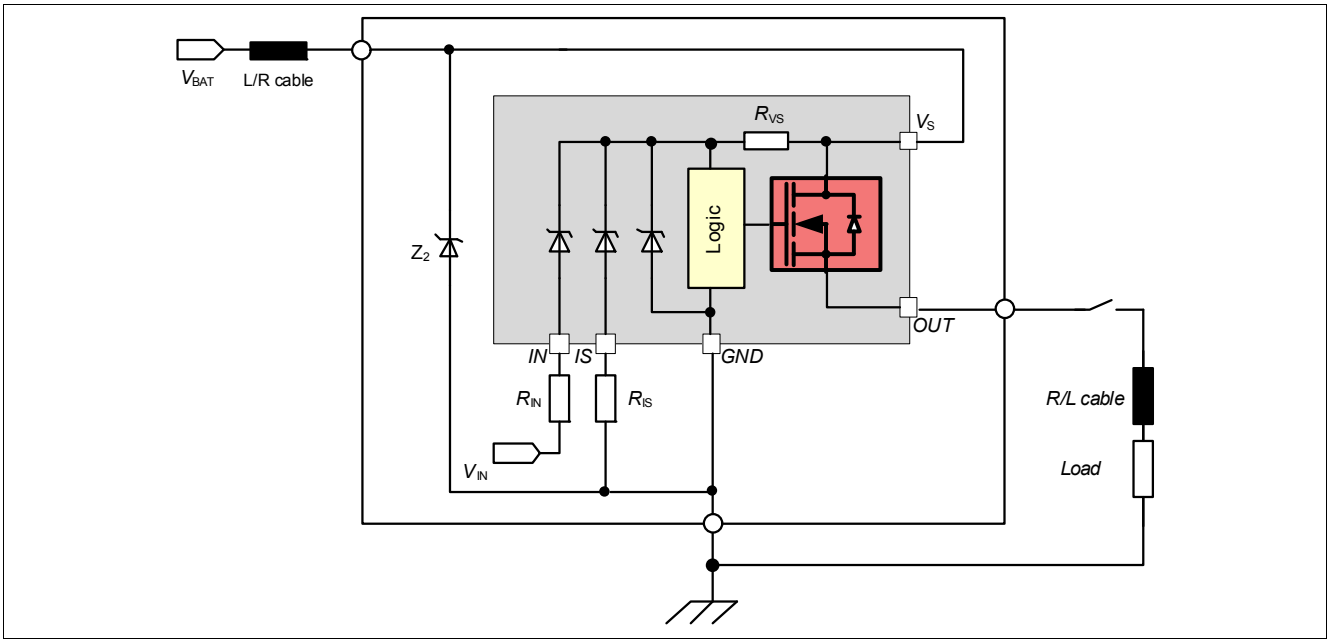

Figure 19 Loss of Load

5.3.3 Undervoltage Behavior

If the device is already ON and the power supply decreases but remains above the $V_{S(UV)}$, no effect is observed and the device keeps on working normally (case 1, **Figure 20**)

If the power supply falls below the $V_{S(UV)}$ but remains above the $V_{S(EXT,DYN)}$, the device turns off, but it turns automatically on again when the power supply goes above Min. $V_{S(EXT)}$ (case 2, **Figure 20**).

In case the power supply becomes lower than $V_{S(EXT,DYN)}$, the device turns off and can be switched on again only after a reset signal at the IN pin, provided that the power supply is higher than Min. $V_{S(EXT)}$ (case 3, **Figure 20**).

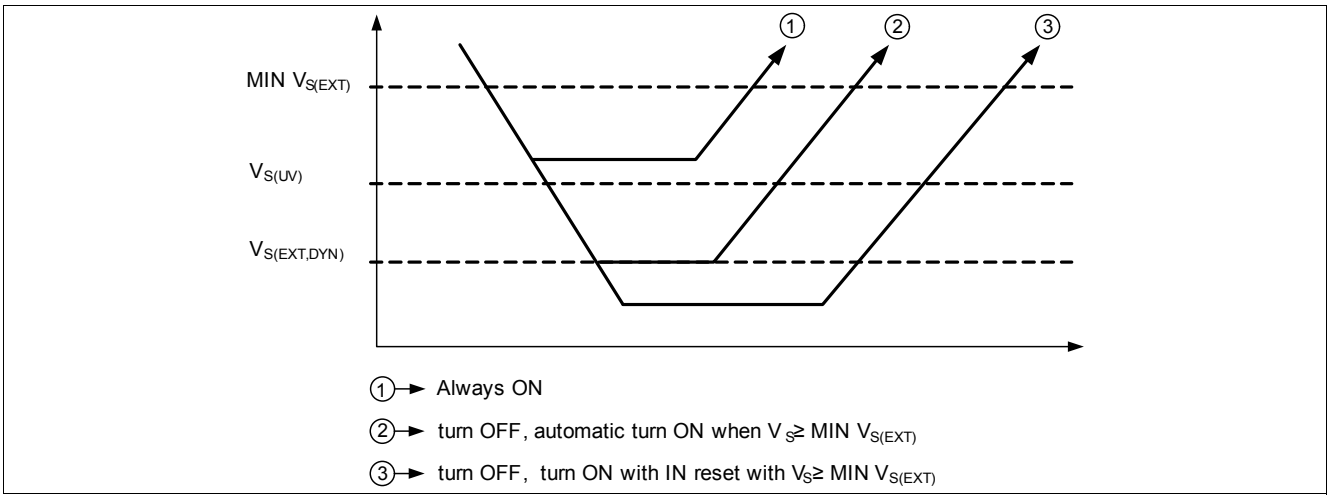

Figure 20 Undervoltage Behavior

5.3.4 Overvoltage Protection

In case $V_{S(SC)\_max} < V_S < V_{DS(CL)}$, the device will switch ON/OFF normally as in the nominal voltage range.

Parameters may deviate from the specified limits and lifetime is reduced. This specially impacts the short circuit robustness, as well as the maximum energy E_{AS} and E_{AR} the device can handle.

The BTS50015-1TAD provides Infineon® SMART CLAMPING functionality, which suppresses excessive transient overvoltage by actively clamping the overvoltage across the power stage and the load. This is achieved by controlling the clamp voltage $V_{DS(CL)}$ depending on the junction temperature T_J and the load current I_L (see **Figure 21** for details).

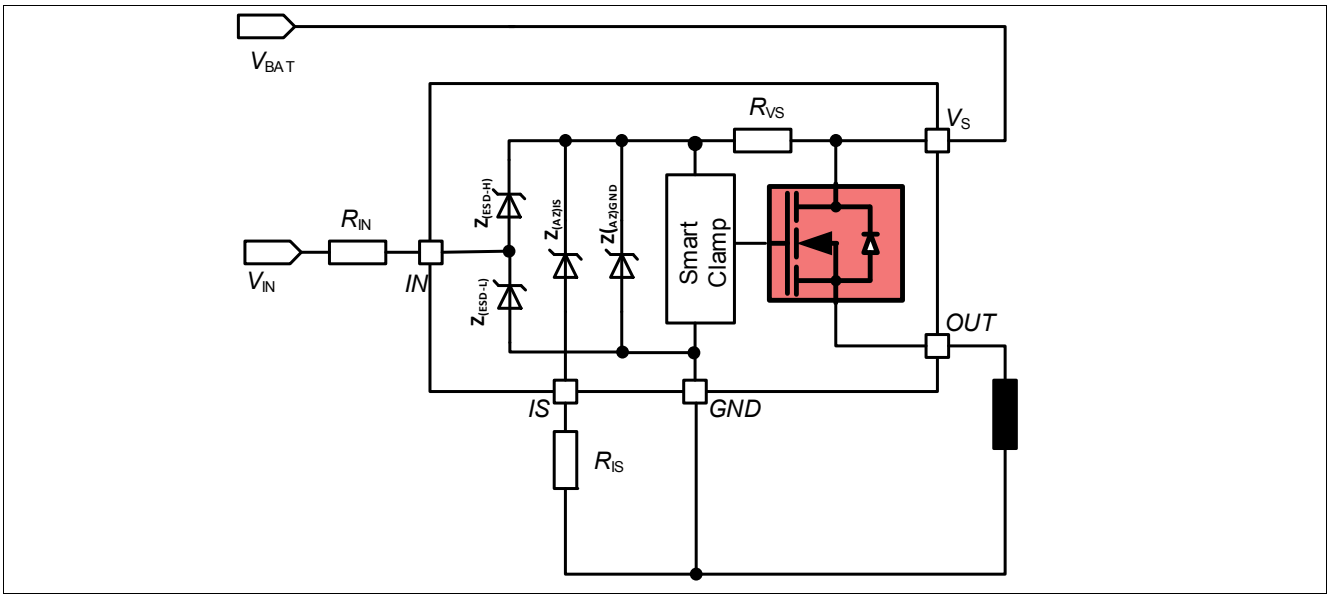

Figure 21 Overvoltage Protection with External Components

5.3.5 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode of the power DMOS causes power dissipation. To limit the risk of overtemperature, the device provides Infineon® ReverSave™ functionality. The power in this intrinsic body diode is limited by turning the DMOS ON. The DMOS resistance is then equal to $R_{DS(REV)}$.

Additionally, the current into the logic has to be limited. The device includes a R_{VS} resistor which limits the current in the diodes. To avoid overcurrent in the R_{VS} resistor, it is nevertheless recommended to use a R_{IN} resistor. Please refer to maximum current described in **Chapter 4.1**.

Figure 22 shows a typical application.

R_{IS} is used to limit the current in the sense transistor, which behaves as a diode.

The recommended typical value for R_{IN} is 4.7 kΩ and for R_{IS} 1 kΩ.