Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

BTS50015-1TMA

Smart High-Side Power Switch

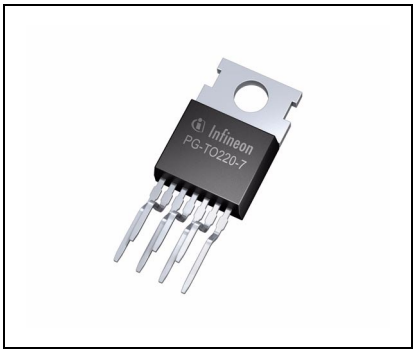
Data Sheet

Rev. 1.3, 2014-07-21

Automotive Power

Table of Contents

1 Overview



PG-TO220-7-232

Application

- All types of resistive and capacitive loads
- Suitable for inductive loads in conjunction with an effective, peripheral free wheeling circuit
- Replaces electromechanical relays and fuses
- Most suitable for applications with high current loads, such as heating system, main switch for power distribution, start-stop power supply switch
- PWM application with low frequencies

Features

- One channel device
- Low Stand-by current
- Wide input voltage range (can be driven by logic levels 3.3V and 5V as well as directly by V_S)
- Electrostatic discharge protection (ESD)
- Optimized Electromagnetic Compatibility (EMC)
- Logic ground independent from load ground
- Very low leakage current on OUT pin
- Compatible to cranking pulse requirement (test pulse 4 of ISO7637 and cold start pulse in LV124)
- Embedded diagnostic functions
- Embedded protection functions
- Green Product (RoHS compliant)
- AEC Qualified

Description

The BTS50015-1TMA is a 1.5 mΩ single channel Smart High-Side Power Switch, embedded in a PG-TO-220-7-232 package, providing protective functions and diagnosis. It contains Infineon® Reversave. The power transistor is built by a N-channel power MOSFET with charge pump. It is specially designed to drive high current loads up to 80A, for applications like switched battery couplings, power distribution switches, heaters, glow plugs, in the harsh automotive environment.

Type	Package	Marking
BTS50015-1TMA	PG-TO-220-7-232	S50015A

Table 1 Product Summary

Parameter	Symbol	Values
Operating voltage range	$V_{S(OP)}$	8 V … 18 V
Extended supply voltage contain dynamic undervoltage capability	$V_{S\ (DYN)}$	3.2 V … 28 V
Maximum on-state resistance at T_j = 150 °C	$R_{DS(ON)}$	3 mΩ
Minimum nominal load current	$I_{L\ (nom)}$	33 A
Typical current sense differential ratio	dk_{ILIS}	51500
Minimum short circuit current threshold	$I_{L\ (OVL)}$	135 A
Maximum stand-by current for the whole device with load at T_A=T_J= 85°C	$I_{S\ (OFF)}$	18 µA
Maximum reverse battery voltage at T_A = 25°C for 2 min	$-V_{S(REV)}$	16 V

Embedded Diagnostic Functions

- Proportional load current sense
- Short circuit / Overtemperature detection
- Latched status signal after short circuit or overtemperature detection

Embedded Protection Functions

- Infineon® Reversave: Reverse battery protection by self turn ON of power MOSFET
- Infineon® Inversave: Inverse operation robustness capability
- Secure load turn-OFF while device loss of GND connection
- Overtemperature protection with latch
- Short circuit protection with latch
- Overvoltage protection with external components
- Enhanced short circuit operation

2 Block Diagram

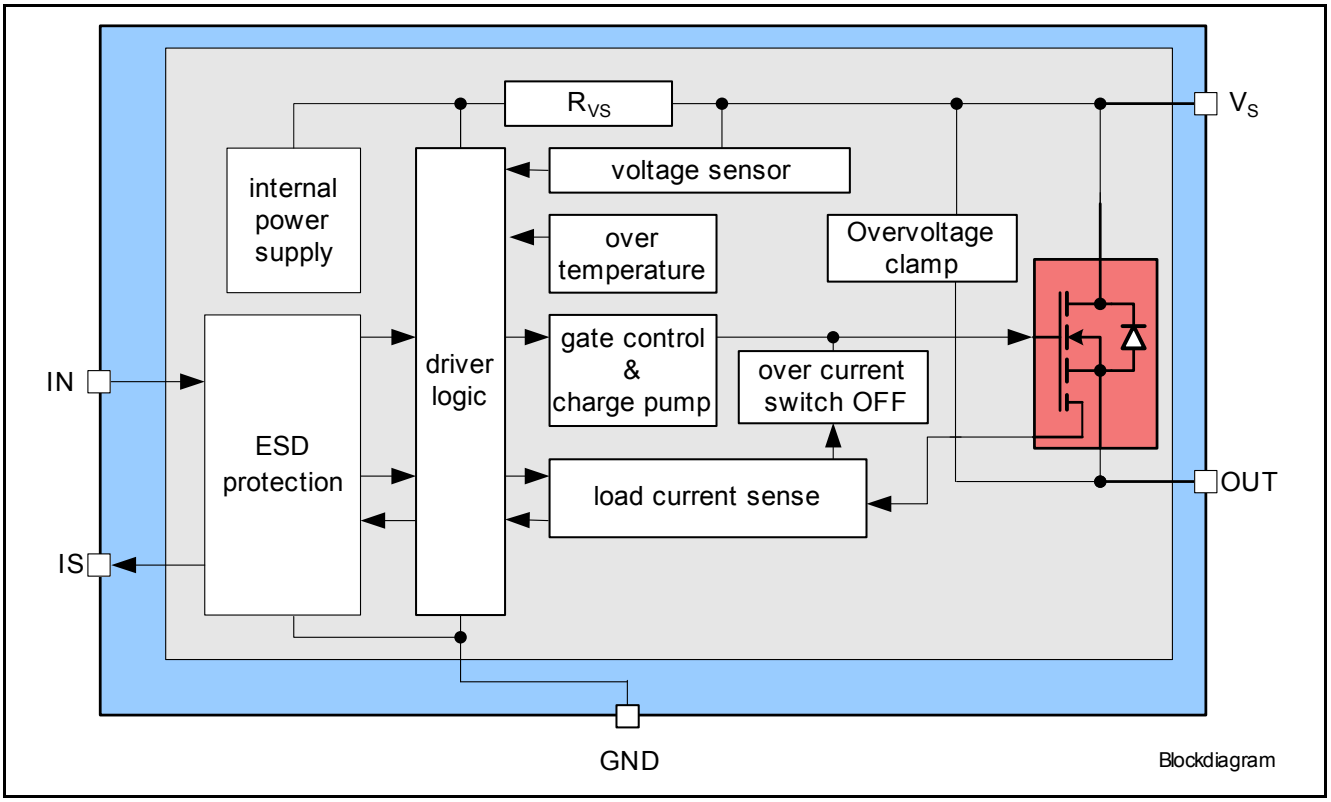


Figure 1 Block Diagram for the BTS50015-1TMA

3 Pin Configuration

3.1 Pin Assignment

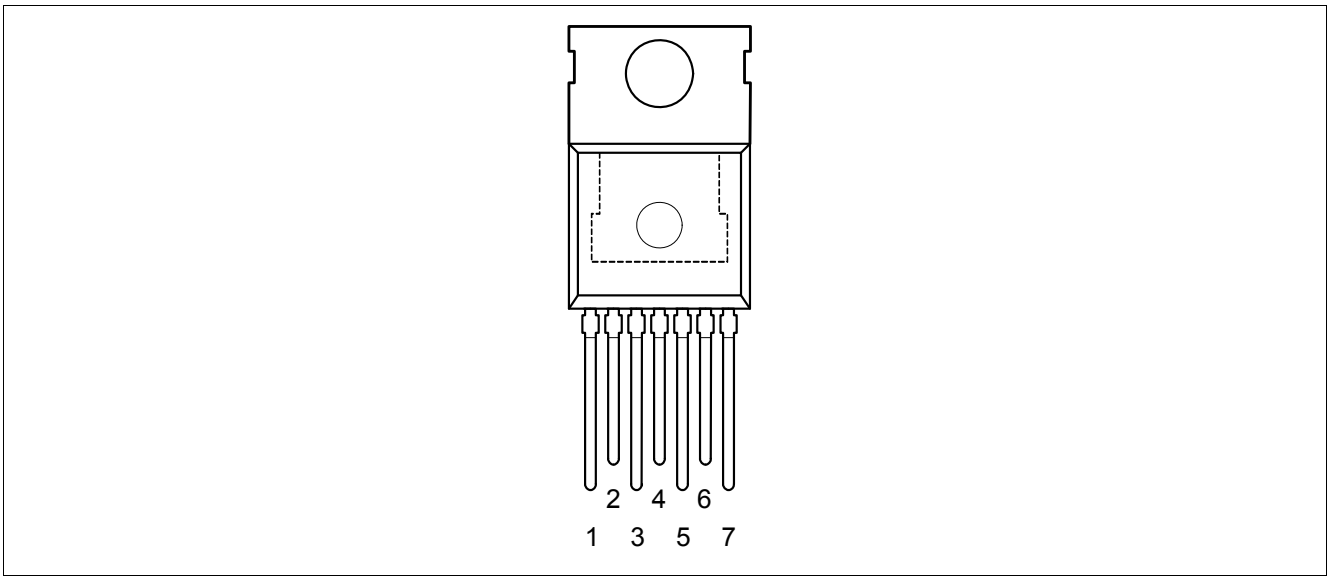


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**GrouND;** Ground connection
2	IN	**INput;** Input signal for channel activation. HIGH active
3	IS	**Sense;** Provides signal for diagnosis
4, Cooling tab	VS	[1] **Supply Voltage;** Battery voltage
5, 6, 7	OUT	[2] **OUTput;** Protected high side power output

1) When cooling tab is not connected to VS and the whole current is only flowing via pin 4, additional 0.8mΩ resistance must be added to $R_{DS(ON)}$

2) All output pins are internally connected and they also have to be connected together on the PCB. Not shorting all outputs on PCB will considerably increase the ON-state resistance and decrease the current sense / overcurrent tripping accuracy. PCB traces have to be designed to withstand the maximum current.

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this datasheet, with associated convention for positive values.

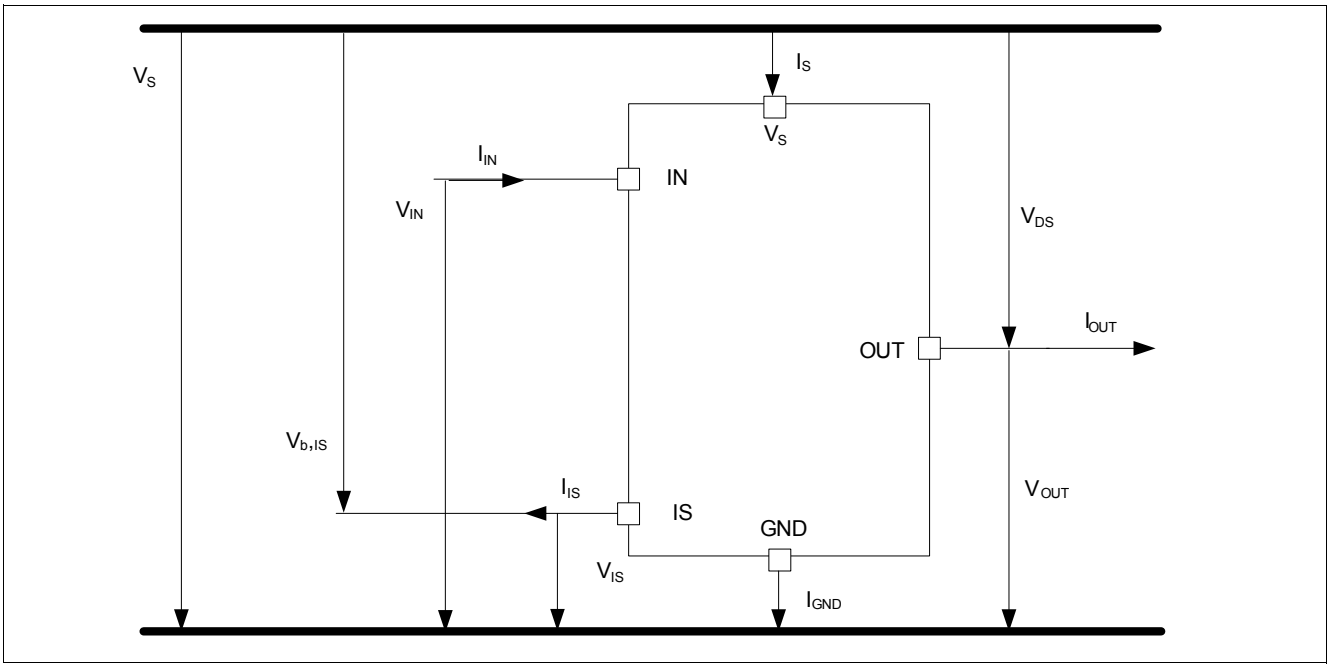


Figure 3 Voltage and Current Definition

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_j = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply Voltage	V_S	-0.3	–	28	V	–	4.1.1
Reverse polarity voltage	$-V_{S(REV)}$	0	–	16	V	[2)] t < 2 min T_A = 25°C $R_L \geq 0.5\Omega$	4.1.2
Supply voltage for load dump protection	$V_{S(LD)}$	–	–	45	V	[3)] R_I = 2Ω R_L = 2.2Ω R_{IS} = 1kΩ R_{IN} = 4.7kΩ	4.1.5
Short circuit capability							
Supply voltage for short circuit protection	$V_{S(SC)}$	5	–	20	V	[4)] R_{ECU} = 20mΩ L_{ECU} = 1µH R_{cable} = 6mΩ/m L_{cable} = 1µH/m l = 0 to 5m *R*, *C* as shown in **Figure 51** See **Chapter 5.3**	4.1.3
Short circuit is permanent: IN pin toggles short circuit (SC type 1)	n_{RSC1}	–	–	100k (Grade D)	–	[5)]	4.1.4
GND pin							
Current through ground pin	I_{GND}	-15 –[6)]	– –	[7)] 10 15	mA	– $t \leq$ 2 min	4.1.6
Input Pin							
Voltage at IN pin	V_{IN}	-0.3	–	V_S	V	–	4.1.7
Current through IN pin	I_{IN}	-5 -5	– –	5 [6)] 50	mA	– $t \leq$ 2 min	4.1.8
Maximum retry cycle rate in fault condition	f_{fault}	–	–	1	Hz	–	4.1.9
Sense Pin							
Voltage at IS pin	V_{IS}	-0.3	–	V_S	V	–	4.1.10
Current through IS pin	I_{IS}	-15 –[6)]	– –	[7)] 10 15	mA	– $t \leq$ 2 min	4.1.11

Table 2 Absolute Maximum Ratings (cont'd)[1)]

T_j = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power Stage							
Average power dissipation	P_{TOT}	–	–	200	W	T_C = -40°C to 150°C	4.1.15
Voltage at OUT Pin	V_{OUT}	-64	–	–	V	–	4.1.21
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	4.1.16
Dynamic temperature increase while switching	ΔT_J	–	–	60	K	See **Chapter 5.3**	4.1.17
Storage Temperature	T_{STG}	-55	–	150	°C	–	4.1.18
ESD Susceptibility							
ESD susceptibility (all pins)	V_{ESD}	-2	–	2	kV	HBM[8)]	4.1.19
ESD susceptibility OUT Pin vs. GND / V_S	V_{ESD}	-4	–	4	kV	HBM[8)]	4.1.20

1) Not subject to production test, specified by design.
2) The device is mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection.
3) $V_{S(LD)}$ is setup without DUT connected to the generator per ISO 7637-1.
4) In accordance to AEC Q100-012
5) In accordance to AEC Q100-012. Test aborted after 100,000 cycles. Short circuit conditions deviating from AEC Q100-012 may influence the specified short circuit cycle number in the datasheet.
6) The total reverse current (sum of I_{GND}, I_{IS} and $-I_{IN}$) is limited by $-V_{S(REV)\_max}$ and R_{VS}.
7) $T_C \leq 125$°C
8) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

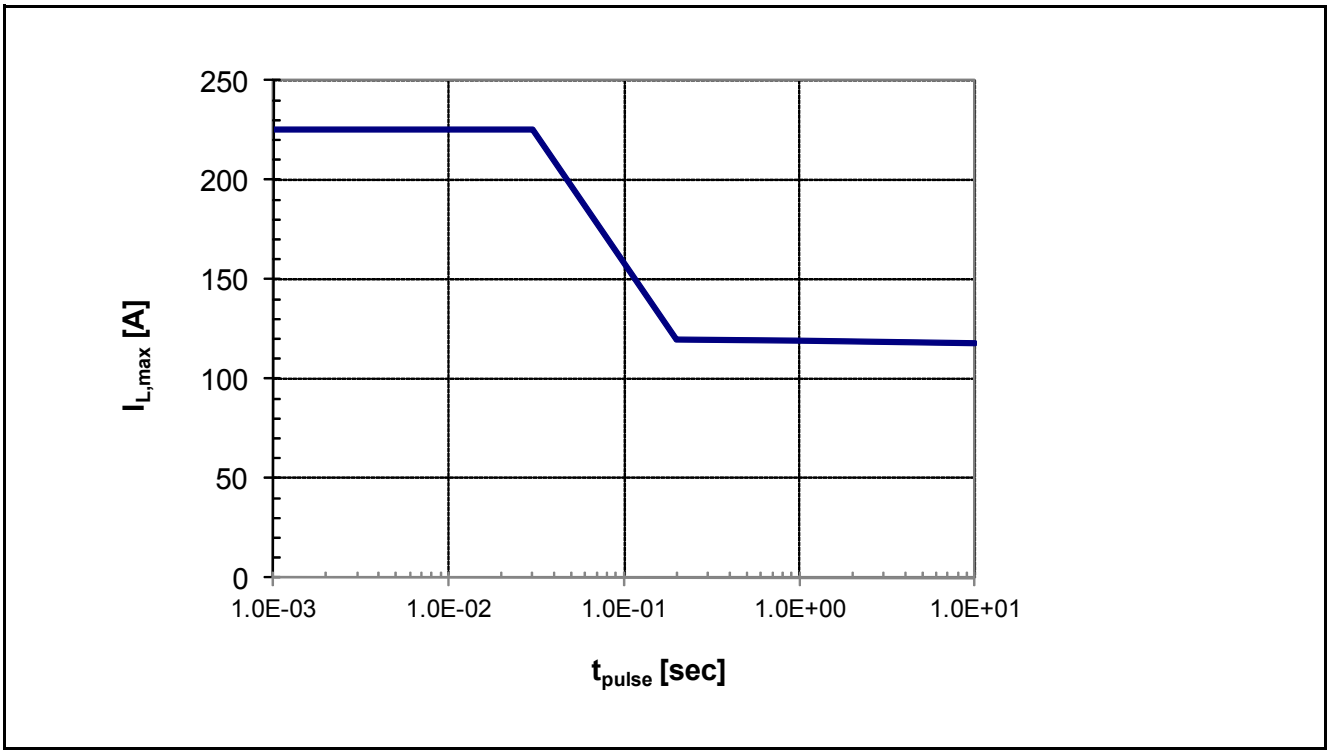


Figure 4 Maximum Single Pulse Current vs. Pulse Time, $T_J \leq 150°C$, $T_{amb} = 85°C$

Above diagram shows the maximum single pulse current that can be driven for a given pulse time t_{pulse}. The maximum reachable current may be smaller depending on the current limitation level. Pulse time may be limited due to thermal protection of the device.

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	$V_{S(OP)}$	8	–	18	V	–	4.2.1
Extended operating voltage	$V_{S(OP\_EXT)}$	5.3	–	28	V	1) $V_{IN} \geq$ 2.2V $I_L \leq I_{L(NOM)}$ $T_J \leq$ 25°C Parameter deviations possible	4.2.2
		5.5	–	28	V	1) $V_{IN} \geq$ 2.2V $I_L \leq I_{L(NOM)}$ T_J = 150°C Parameter deviations possible	
Extended operating voltage contain short dynamic undervoltage capability	$V_{S(DYN)}$	3.2 2)	–	28	V	1) acc. to ISO7637	4.2.3
Undervoltage turn OFF voltage	$V_{S(UV\_OFF)}$	–	–	4.5	V	1) $V_{IN} \geq$ 2.2V R_L = 270Ω V_S decreasing See **Figure 19**	4.2.4
Undervoltage shutdown hysteresis	$V_{S(UV)\_HYS}$	–	500 1)	–	mV	R_L = 270Ω See **Figure 19**	4.2.6
Slewrate at OUT	$\lvert dV_{DS}/dt \rvert$	–	–	10 1)	V/µs	$\lvert V_{DS} \rvert$ < 3V See **Chapter 5.1.4**	4.2.7
Drain to source voltage in OFF condition	V_{DS_OFF}	–	–	28	V	1) VIN ≤ 0.8V	4.2.8

1) Not subject to production test. Specified by design

2) T_A = 25°C; R_L = 0.5Ω; pulse duration 6ms; cranking capability is depending on load and must be verified under application conditions

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	–	0.5	K/W	1)	4.3.1
Junction to Ambient	R_{thJA}	–	110	–	K/W	1)2)	4.3.2

1) Not subject to production test, specified by design.

2)Specified R_{thJA} value is according to JEDEC JESD51 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with pin tracks only.T_A = 25°C. Device is dissipating 1W power.

Figure 5 is showing the typical thermal impedance (junction to ambient and junction to case) of BTS50015-1TMA mounted according to JEDEC on FR4 1s0p board at natural convection

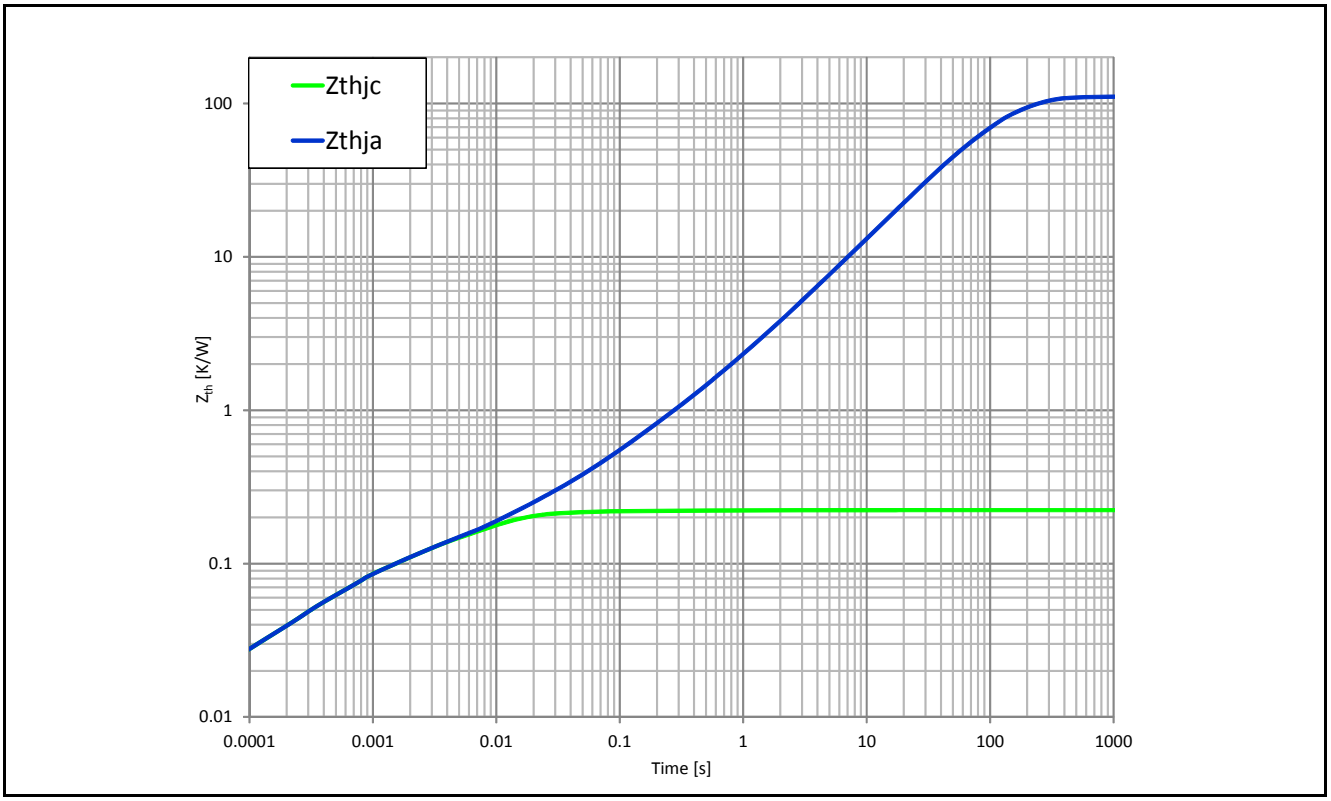


Figure 5 Typical Transient Thermal Impedance $Z_{th(JA)}$=f(time) and $Z_{th(JC)}$=f(time)

5 Functional Description

5.1 Power Stage

The power stage is built by a N-channel power MOSFET (DMOS) with charge pump.

5.1.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J. **Figure 31** shows the dependencies in terms of temperature and supply voltage, for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 5.3.5**.

A HIGH signal (see **Chapter 5.2**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.1.2 Switching a Resistive Load

Figure 6 shows the typical timing when switching a resistive load. The power stage has a defined switching behavior. Defined slew rates results in lowest EMC emission at minimum switching losses.

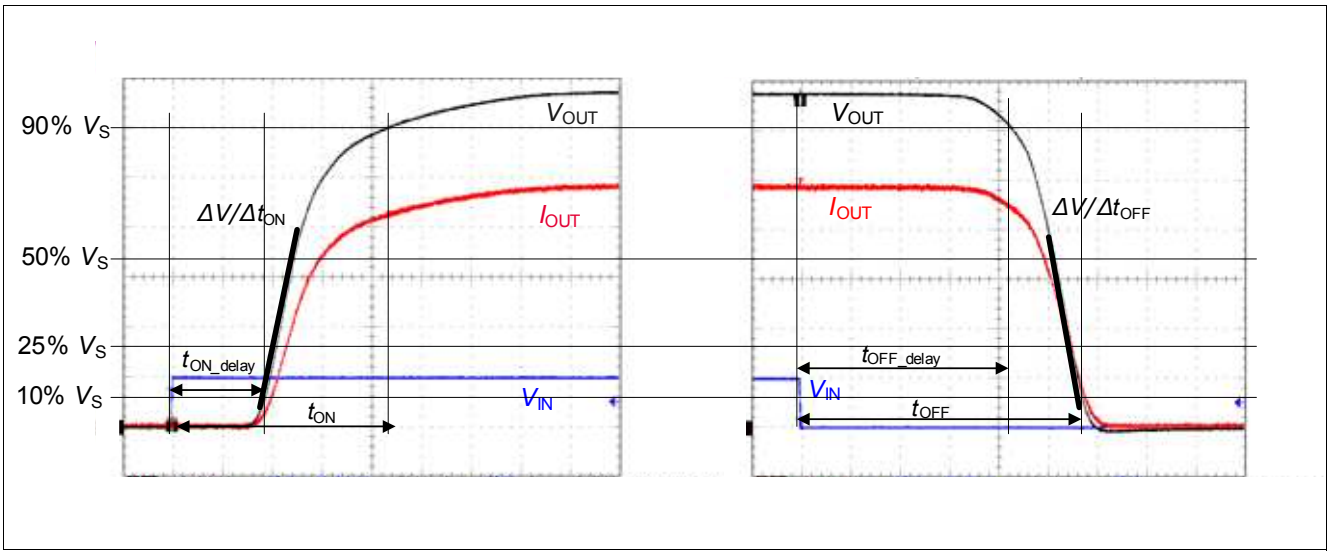


Figure 6 Switching a Resistive Load:Timing

The connection to the load as well as the load itself (if not purely resistive) bring an inductive component. For that reason the drain to source voltage of the BTS50015-1TMA during switch off can differ compared to the pure resistive load condition (see **Figure 7**). It must be assured that under these conditions the drain to source voltage does not exceed the $V_{DS(CL)min}$.

If $V_{DS(CL)min}$ is exceeded, a free wheeling path should be implemented following the recommendation provided in the next chapter.

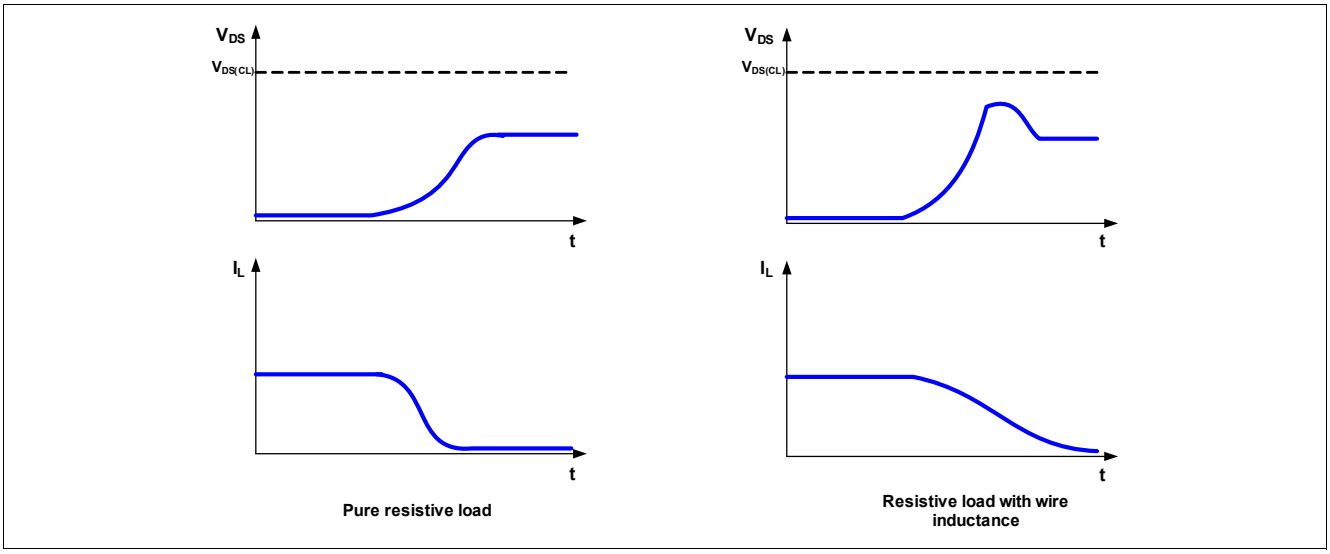


Figure 7 Effect of the wire inductance

5.1.3 Switching an Inductive Load

When switching OFF inductive loads with high side switches, the voltage V_{OUT} is driven below ground potential, due to the fact that the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, the device implements an overvoltage protection, which clamps the voltage between V_S and V_{OUT} at $V_{DS(CL)}$ (see **Figure 8**).

Nevertheless it is not recommended to operate the device repetitively under this condition. Therefore, when driving inductive loads, a free wheeling diode must be always placed.

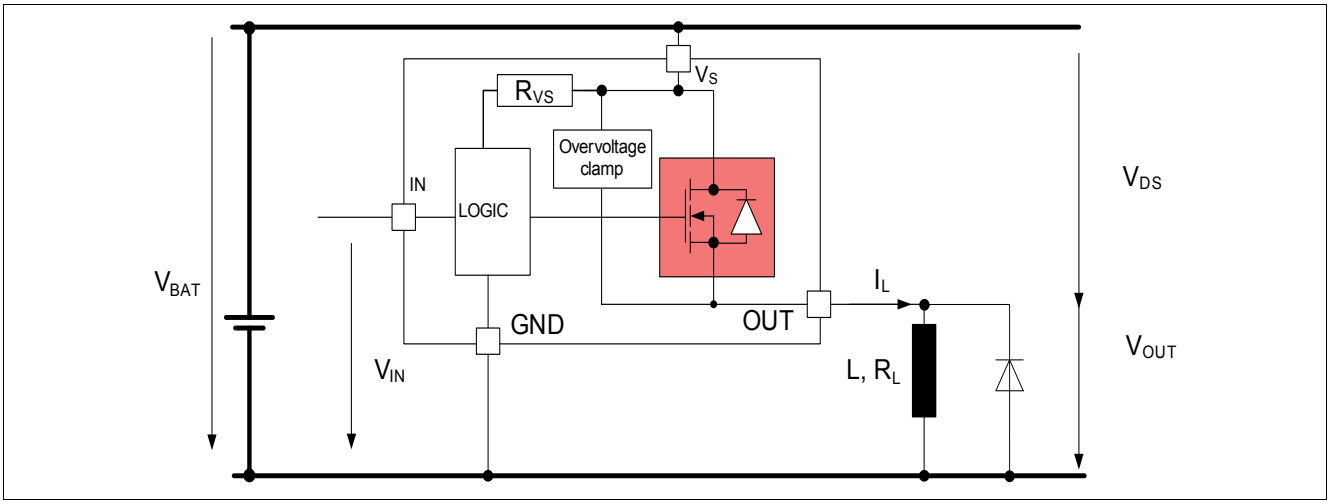


Figure 8 Overvoltage Clamp

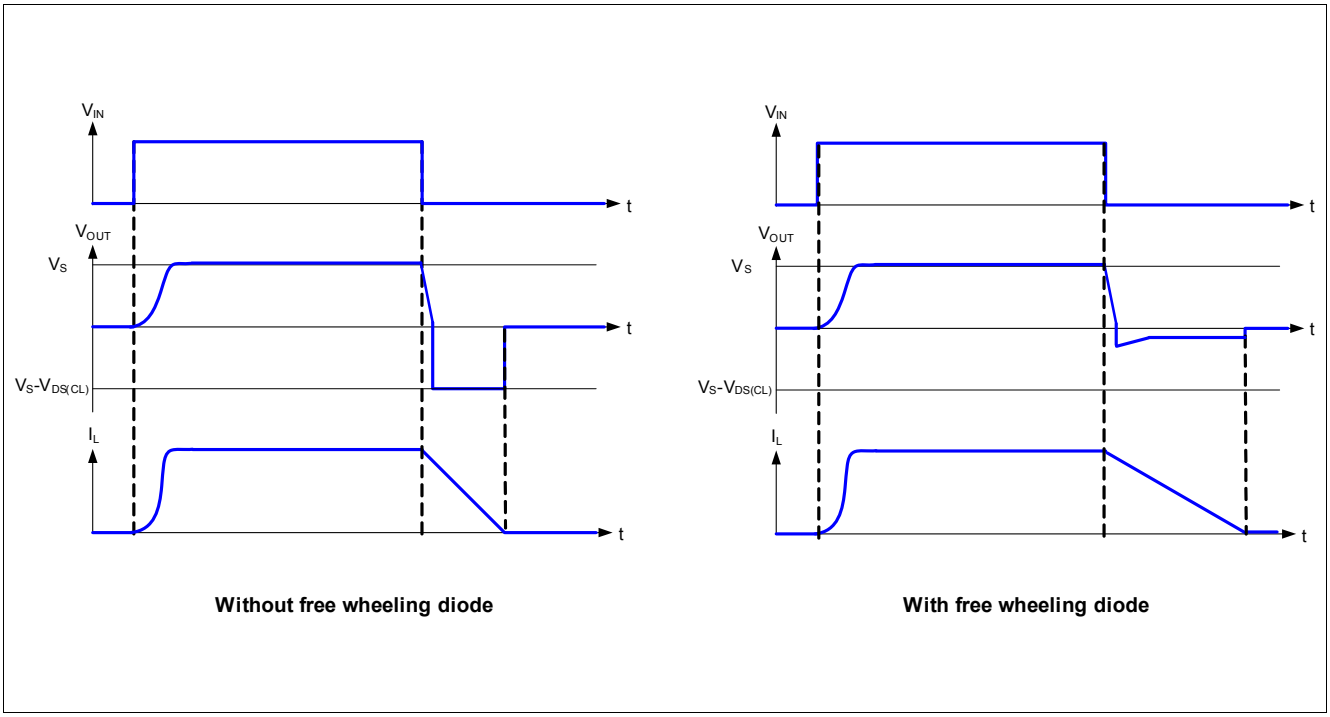


Figure 9 Switching an Inductance with or without free wheeling diode

It is important to verify the effectiveness of the freewheeling solution (see **Figure 9**), which means the selection of the proper diode and of an appropriate free wheeling path. With regard to the choice of the free wheeling diode, low threshold and fast response are key parameter to achieve an effective result.

Moreover the diode should be placed in order to have the shortest wire connection with the load (see **Figure 10**).

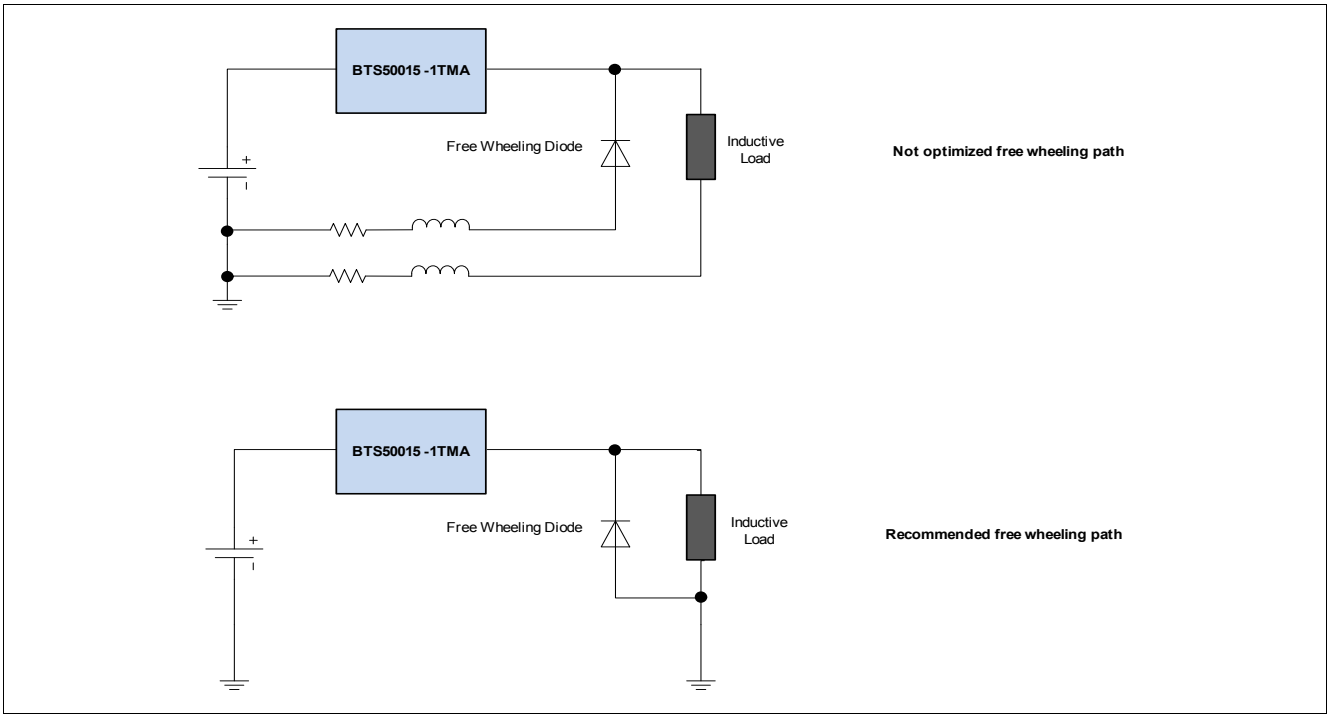


Figure 10 Optimization of the free wheeling path

5.1.4 Inverse Current Capability

In case of inverse current, meaning a voltage $V_{OUT(INV)}$ at the output higher than the supply voltage V_S, a current $I_{L(INV)}$ will flow from output to V_S pin via the body diode of the power transistor (please refer to **Figure 11**). In case the IN pin is HIGH, the power DMOS is already activated and keeps ON. In case, the input goes from “L” to “H”, the DMOS will be activated. Under inverse condition, the device is not overtemperature / overload protected. The IS pin is high impedance. Due to the limited speed of INV comparator, the output voltage slope needs to be limited.

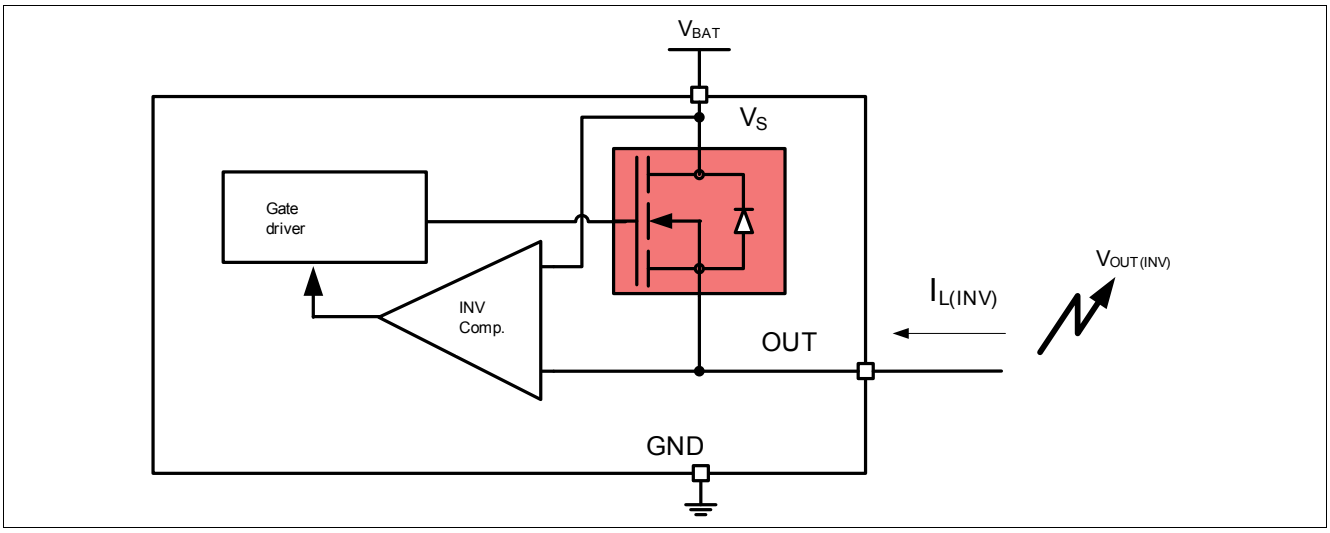


Figure 11 Inverse Current Circuitry

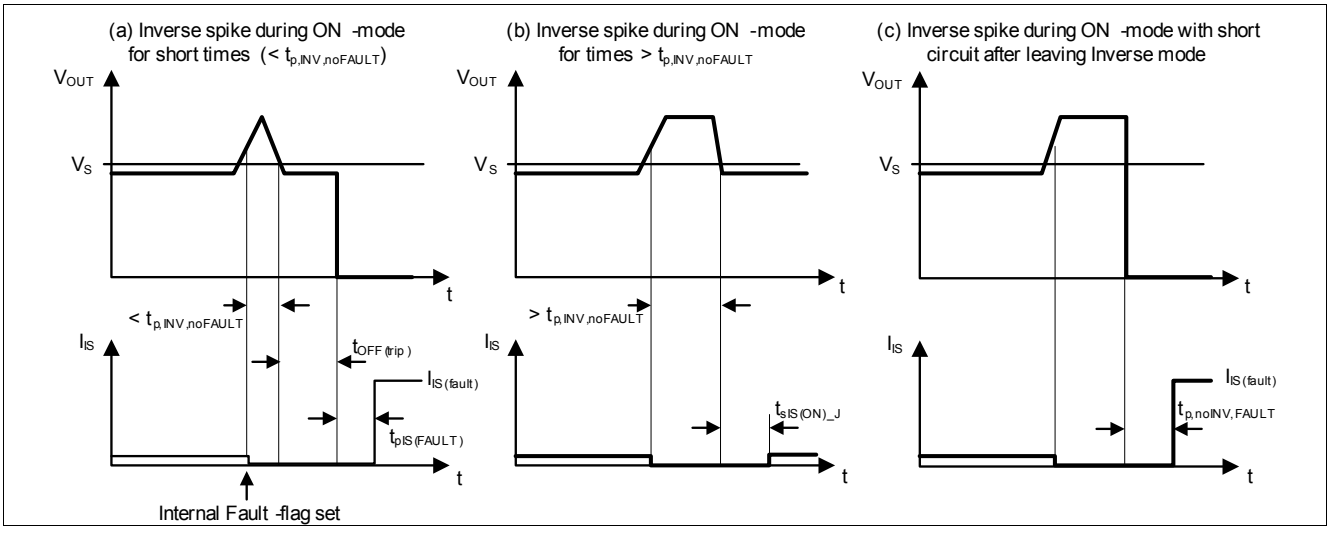


Figure 12 Inverse Behavior - Timing Diagram

5.1.5 PWM Switching

For PWM switching application, a $t_{IN(RESETDELAY)}$ parameter should be respected by defining the maximum PWM frequency (see **Figure 22**). The average power over time must be below the specified value (see paramater 4.1.15) and is defined as (see **Figure 13**):

P_{TOT} = (switching_ON_energy + switching_OFF_energy + I_L^2 * $R_{DS(ON)}$ * t_{DC}) / period

For system with PWM switching, the maximum retry cycle (f_{fault}) under fault condition should not be exceeded.

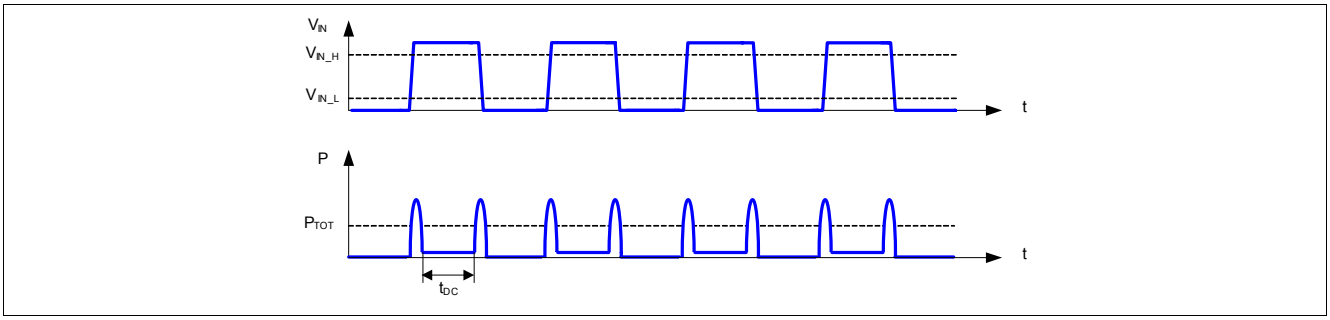


Figure 13 Switching in PWM

5.2 Input Pins

5.2.1 Input Circuitry

The input circuitry is compatible with 3.3V and 5V microcontrollers or can be directly driven by V_S. The concept of the input pin is to react to voltage threshold. With the Schmitt trigger, the output is either ON or OFF. **Figure 14** shows the electrical equivalent input circuitry.

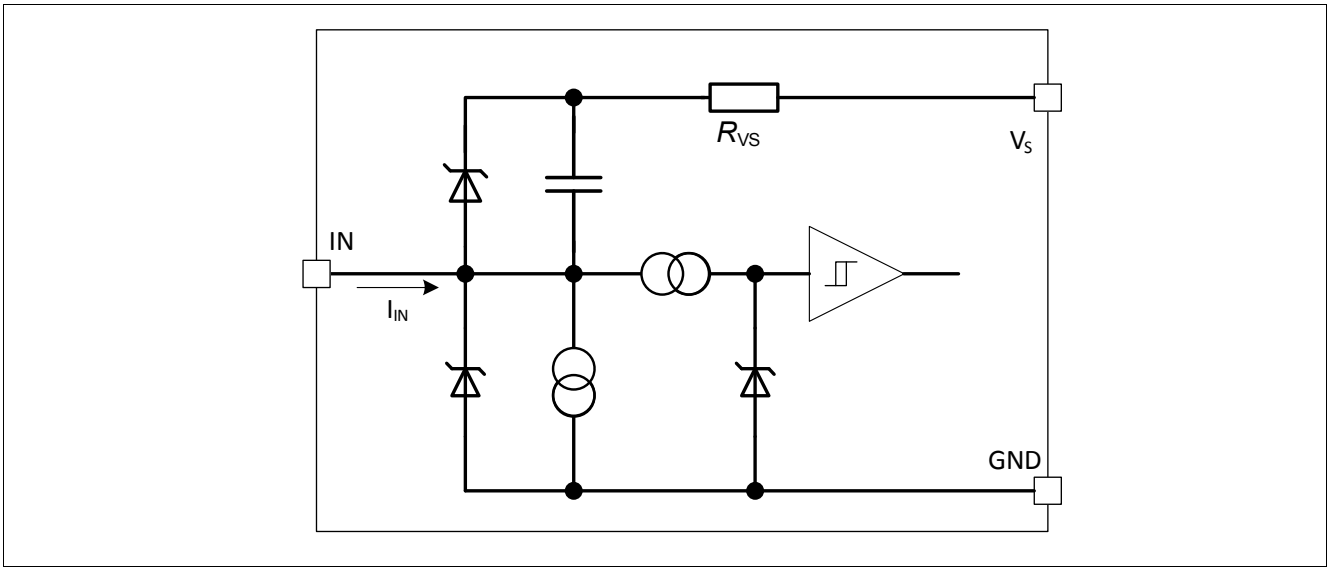


Figure 14 Input Pin Circuitry

5.2.2 Input Pin Voltage

The IN uses a comparator with hysteresis. The switching ON / OFF takes place in a defined region, set by the threshold $V_{IN(L)}$ Max and $V_{IN(H)}$ Min. The exact value where ON and OFF take place depends on the process, as well as the temperature. To avoid cross talk and parasitic turn ON and OFF, an hysteresis is implemented. This ensures immunity to noise.

5.3 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent the destruction of the IC from fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed neither for continuous nor for repetitive operation.

Figure 15 describes the typical functionality of the diagnosis and protection block.

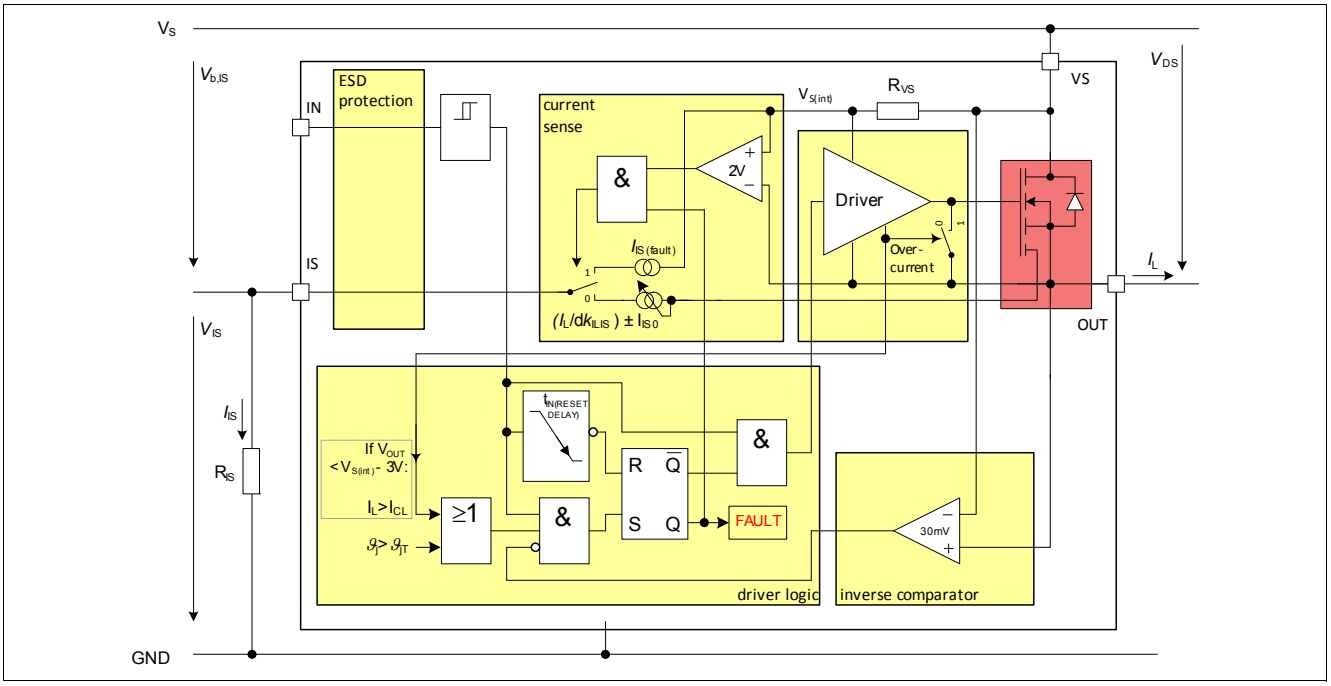


Figure 15 Diagram of Diagnosis & Protection Block

5.3.1 Loss of Ground Protection

In case of loss of module or device ground, where the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pin. It is recommended to use input resistors between the microcontroller and the BTS50015-1TMA to ensure switching OFF of channel. In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS. **Figure 16** sketches the situation.

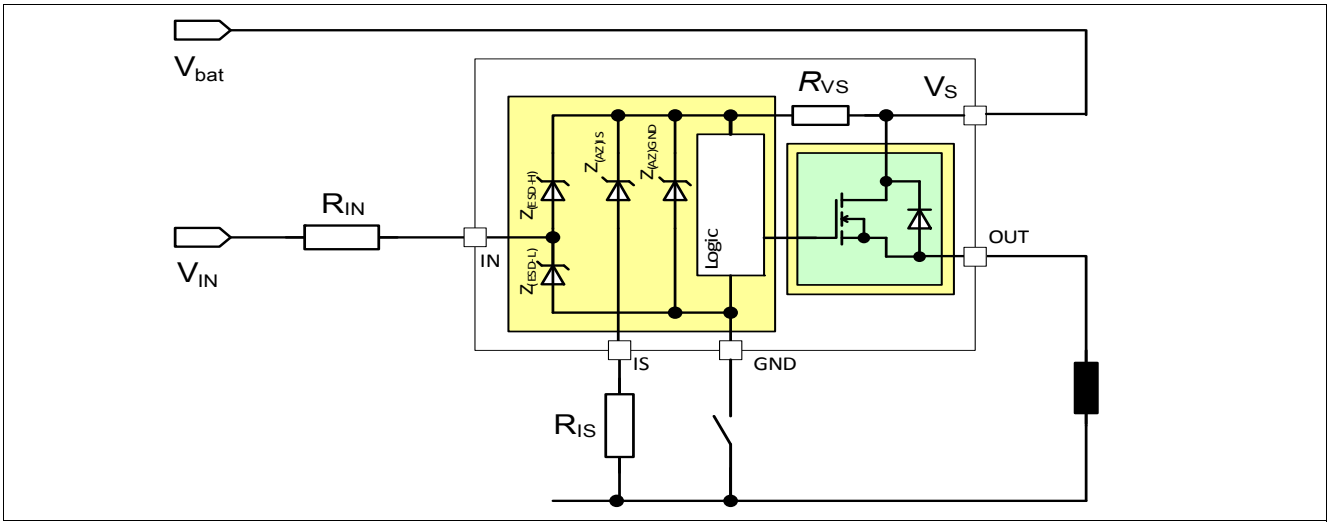


Figure 16 Loss of Ground Protection with External Components

5.3.2 Protection during Loss of Load or Loss of V_S Condition

In case of loss of load with charged primary inductances the maximum supply voltage has to be limited. It is recommended to use a Z-diode, a varistor or V_S clamping power switches with connected loads in parallel. The voltage must be limited according to the minimum value of the parameter 6.1.33 indicated in **Table 6**.

In case of loss of V_S connection, the inductance of the wire and/or of the load should be taken into account and should be demagnetized by providing a proper current path. It is recommended to protect the device using a zener diode together with a(V_{Z1} + V_{D1} < 16V), as shown in **Figure 17**.

For a proper restart of the device after loss of V_S, the input voltage must be applied delayed to the supply voltage. This can be realized by an capacitor between IN and GND (see **Figure 51**).

For higher clamp voltages, currents through all pins have to be limited according to the maximum ratings. Please see **Figure 17** and **Figure 18** for details.

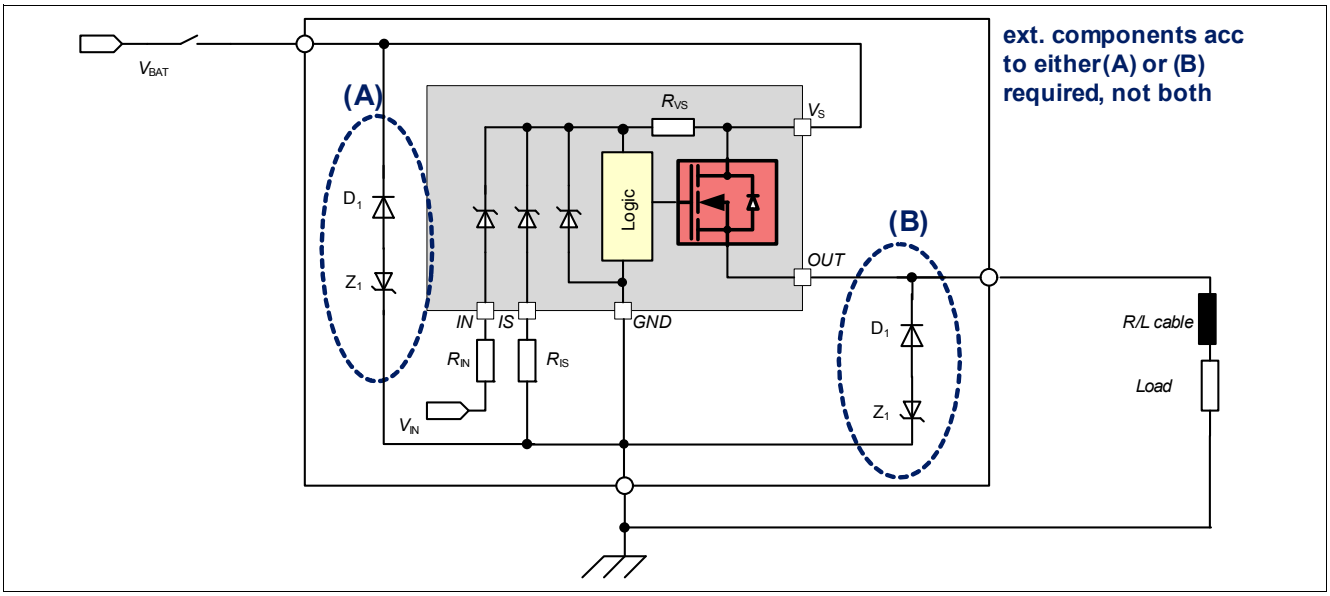


Figure 17 Loss of V_S

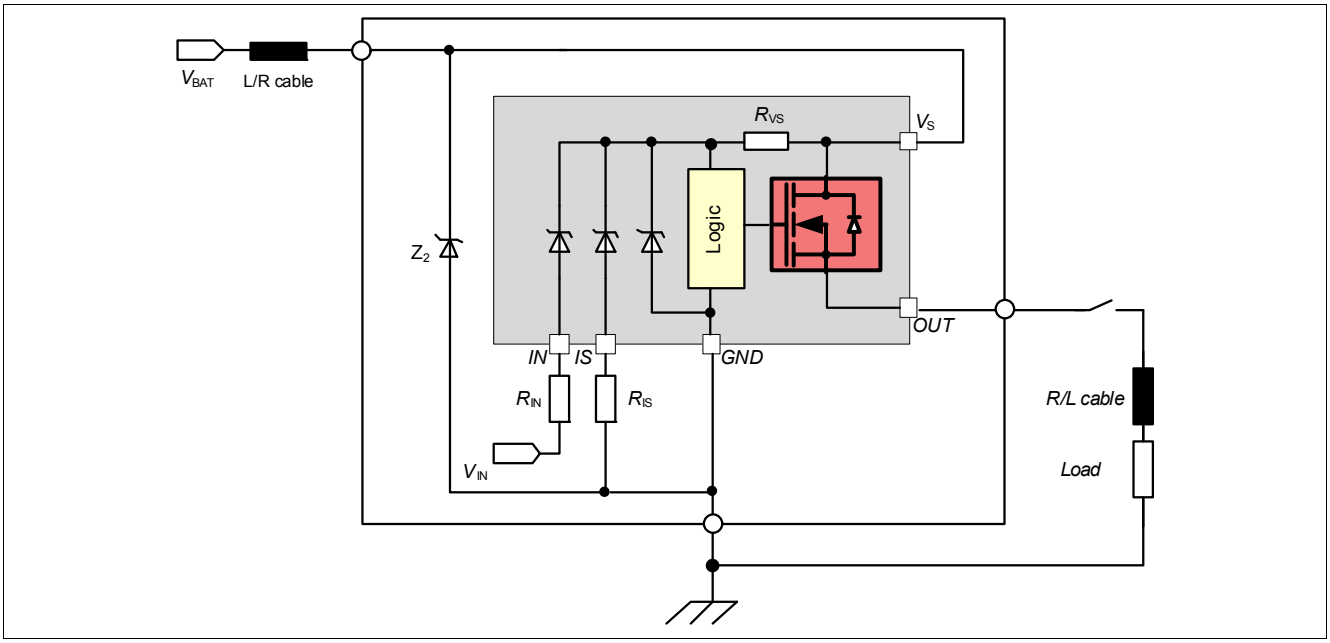


Figure 18 Loss of Load

5.3.3 Undervoltage Behavior

If the supply voltage is in the area below $V_{S(UV\_OFF)}$, the device is OFF (turns OFF). As soon as the supply voltage is above $V_{S(OP\_EXT)\_min}$, the device will switch ON again. **Figure 19** sketches the undervoltage behavior.

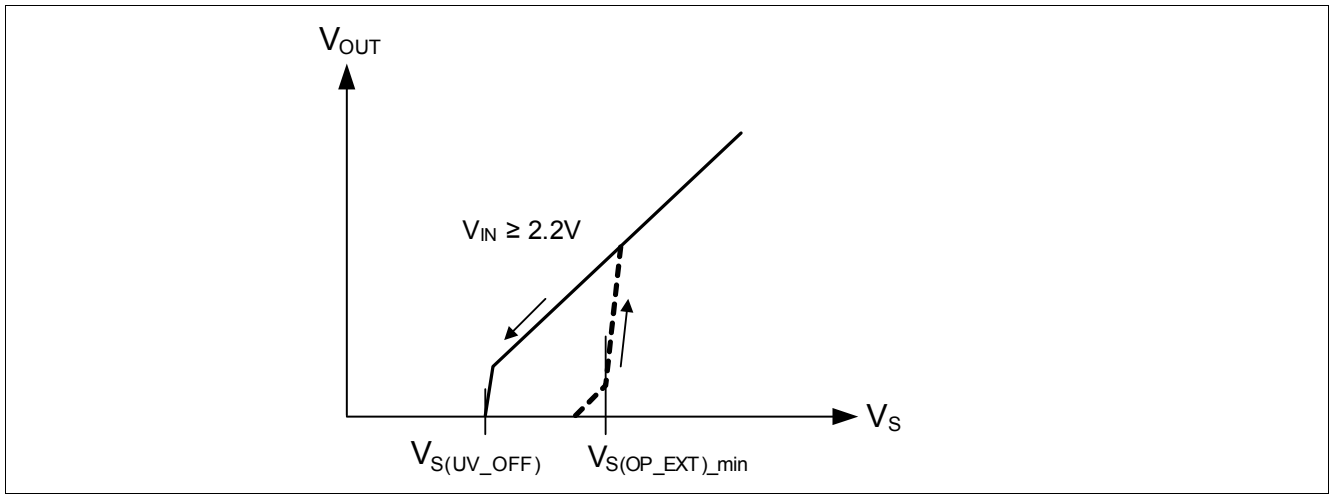


Figure 19 Undervoltage Behavior

5.3.4 Overvoltage Protection

In case $V_{S(SC)\_max} < V_S < V_{DS(CL)}$, the device will switch ON/OFF as in nominal voltage range. Parameters may deviate from the specified limits and the lifetime is reduced.

The BTS50015-1TMA provides an overvoltage clamp functionality, which suppresses non nominal overvoltage transients by actively clamping the voltage across the power stage (see **Table 6**, parameters 6.1.11). The clamping voltage $V_{DS(CL)}$is depending on the junction temperature T_j and load current I_L (see **Figure 20** for details).

A repetitive operation under clamping condition must be avoided.

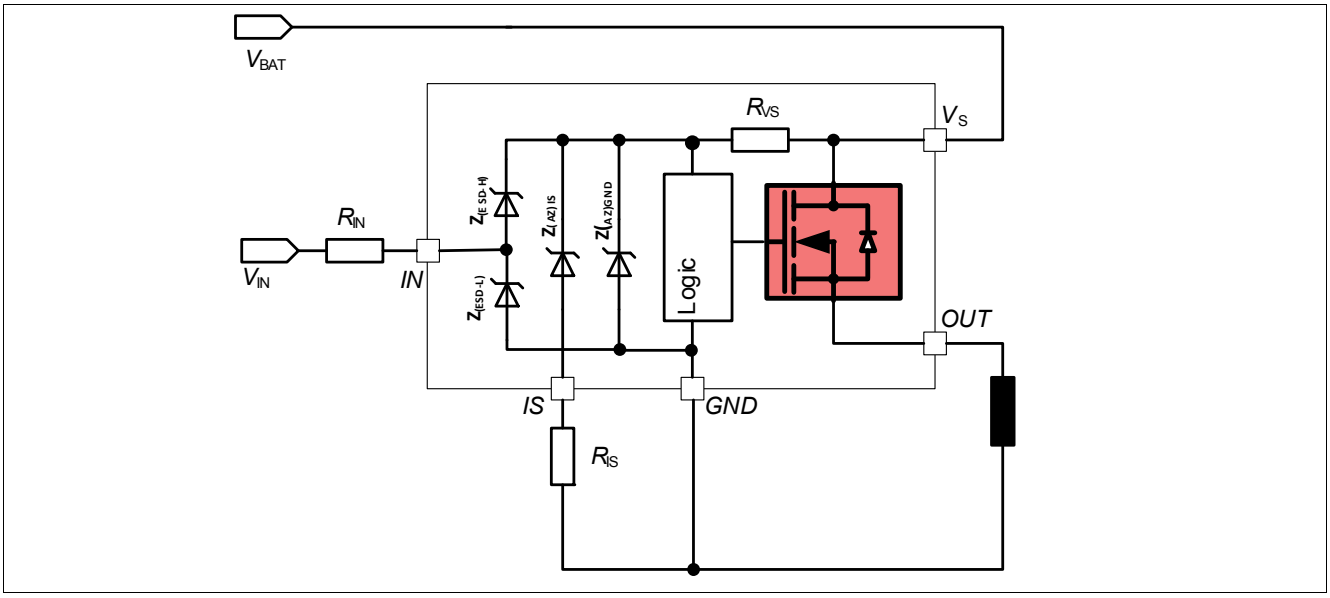


Figure 20 Overvoltage Protection with External Components

5.3.5 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode of the power DMOS causes power dissipation. To limit the risk of overtemperature, the device provides Infineon® Reversave function. The power in this intrinsic body diode is limited by turning the DMOS ON. The DMOS resistance is then equal to $R_{DS(ON)\_REV}$.

Additonally, the current into the logic has to be limited. The device includes a R_{VS} resistor which limits the current in the diodes. To avoid overcurrent in the R_{VS} resistor, it is nevertheless recommended to use a R_{IN} resistor. Please refer to maximum current described in **Chapter 4.1**. **Figure 21** shows a typical application. R_{IS} is used to limit the current in the sense transistor which behaves as a diode.

The recommended typical values for R_{IN} is 4.7kΩ and for R_{SENSE} 1kΩ.

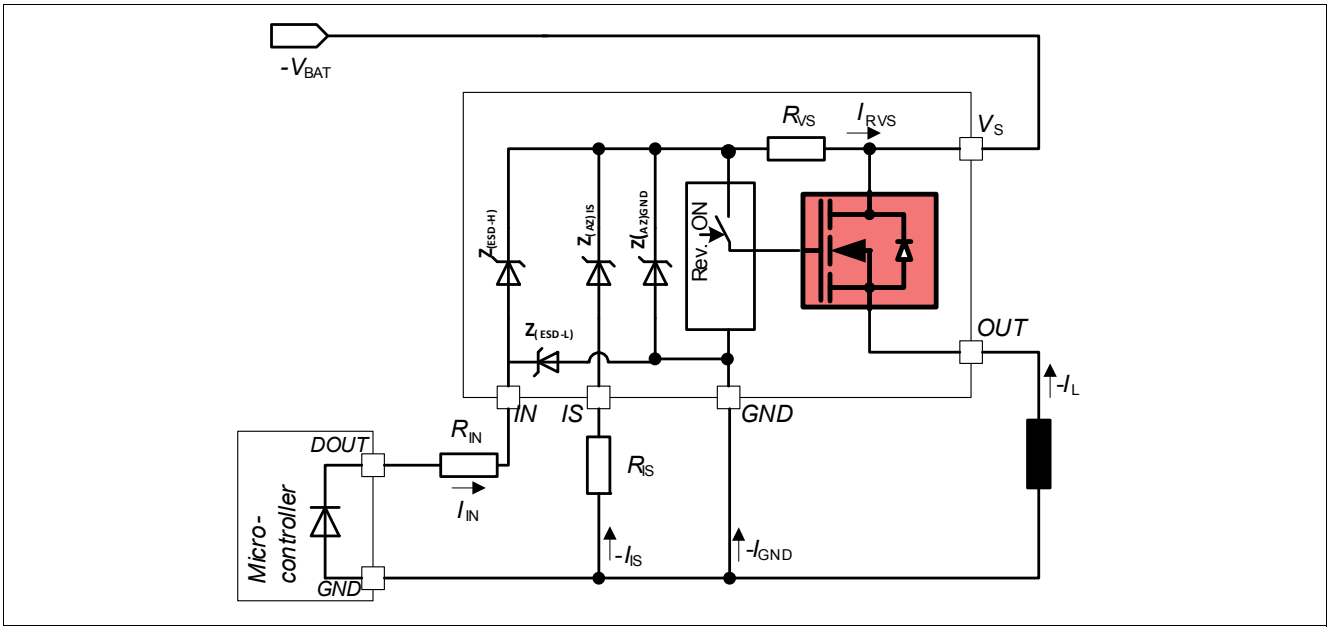


Figure 21 Reverse Polarity Protection with External Components

5.3.6 Overload Protection

In case of overload, high inrush current or short circuit to ground, the BTS50015-1TMA offers several protection mechanisms. Any protective switch OFF latches the output. To restart the device, it is necessary to set IN=LOW for $t > t_{IN(RESETDELAY)}$. This behavior is known as latch behavior. **Figure 22** gives a sketch of the situation.

5.3.6.1 Activation of the Switch into Short Circuit (Short circuit Type 1)

When the switch is activated into short circuit, the current will raise until reaching the $I_{L(TRIP)}$ value. After $t_{OFF(TRIP)}$, the device will turn OFF and latches until the IN pin is set to low for $t > t_{IN(RESETDELAY)}$. An undervoltage shutdown will not reset the latched fault overcurrent. For overload (short circuit or overtemperature), the maximum retry cycle (f_{fault}) under fault condition must be considered.

5.3.6.2 Short Circuit Appearance when the Device is already ON (Short circuit Type 2)

When the device is in ON state and a short circuit to ground appears at the output (SC2) with a overcurrent higher than $I_{L(TRIP)}$ for a time longer than $t_{OFF(TRIP)}$, the device automatically turns OFF and latches until the IN pin is set to low for $t > t_{IN(RESETDELAY)}$.

5.3.7 Temperature Limitation in the Power DMOS

The BTS50015-1TMA incorporates an absolute ($T_{J(TRIP)}$) temperature sensor. Activation of the sensor will cause an overheated channel to switch OFF to prevent destruction. The device restarts when the IN pin is toggled and the temperature has decreased below $T_{J(TRIP)} - \Delta T_{J(TRIP)}$.

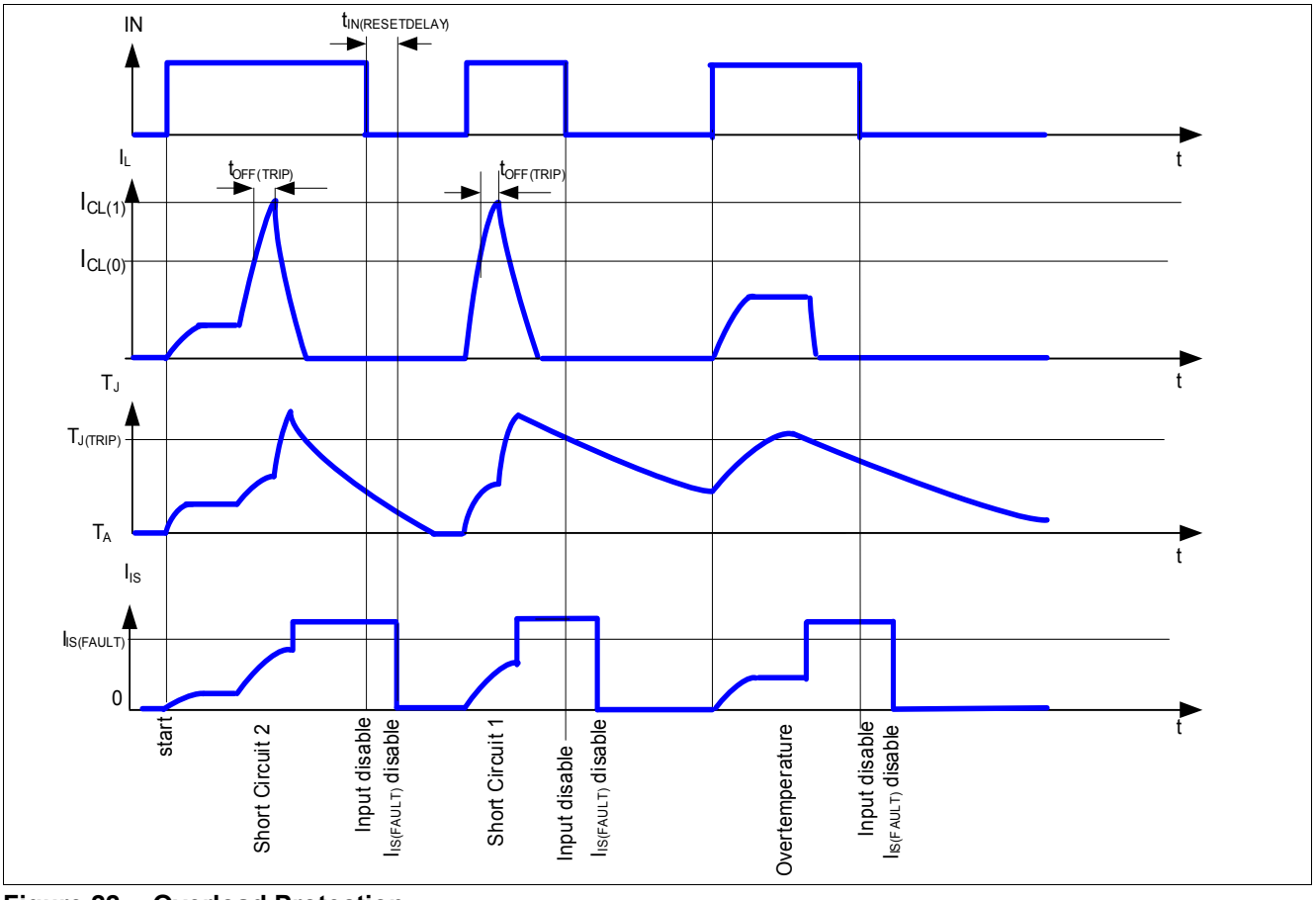


Figure 22 Overload Protection

The current sense exact signal timing can be found in the **Chapter 5.4**. It is represented here only for device's behavior understanding.

In order to allow the device to detect overtemperature conditions and react effectively, it is recommended to limit the power dissipation below P_{TOT} (parameter 4.1.15).

5.4 Diagnostic Functions

For diagnosis purposes, the BTS50015-1TMA provides a combination of digital and analog signal at pin IS.

5.4.1 IS Pin

The BTS50015-1TMA provides an enhanced current sense signal called I_{IS} at pin IS. As long as no “hard” failure mode occurs (short circuit to GND / overcurrent / overtemperature) and the condition $V_{IS} \leq V_{OUT}$ - 5V is fulfilled, a proportional signal to the load current (ratio k_{ILIS} = I_L / I_S) is provided. The complete IS pin and diagnostic mechanism is described in **Figure 23**. The accuracy of the sense current depends on temperature and load current. In case of failure, a fixed $I_{IS(FAULT)}$ is provided. In order to enable the fault current reporting, the condition V_S - V_{OUT} > 2V must be fulfilled. In order to get the fault current in the specified range, the condition V_S - $V_{IS} \geq$ 5V must be fulfilled.

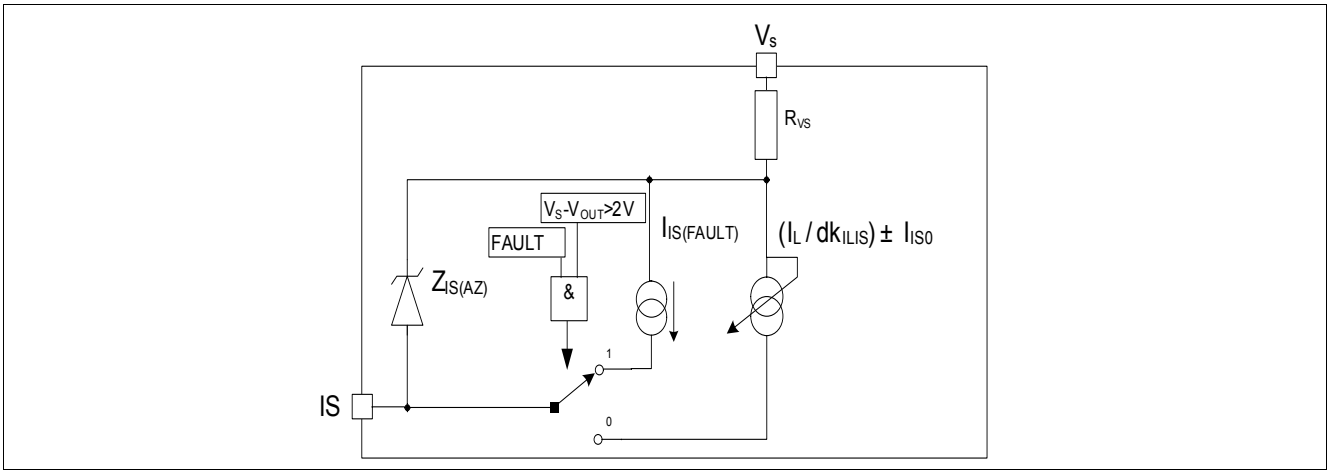


Figure 23 Diagnostic Block Diagram

5.4.2 SENSE Signal in Different Operation Mode

Table 5 Sense Signal, Function of Operation Mode[1)]

Operation mode	Input Level	Output Level V_{OUT}	Diagnostic Output (IS)[2)]
Normal operation	LOW (OFF)	~ GND	$I_{IS(OFF)}$
Short circuit to GND		GND	Z
Overtemperature		Z	Z
Short circuit to VS		V_S	Z
Open Load		Z	Z
Inverse current		> V_S	Z
Normal operation	HIGH (ON)	~ V_S	I_{IS} = (I_L / dk_{ILIS}) ± I_{IS0}
Overcurrent condition		< V_S	I_{IS} = (I_L / dk_{ILIS}) ± I_{IS0}...$I_{IS(FAULT)}$
Short circuit to GND		~ GND	$I_{IS(FAULT)}$
Overtemperature $T_{J(TRIP)}$ event		Z	$I_{IS(FAULT)}$
Short circuit to VS		V_S	I_{IS} = 0 ... I_L / dk_{ILIS} ± I_{IS0}
Open Load		~ V_S	I_{IS0}
Inverse current		> V_S	Z

1) Z = High Impedance

2) See **Chapter 5.4.3** for Current Sense Range and Improved Current Sense Accuracy

5.4.3 SENSE Signal in the Nominal Current Range

Figure 24 and **Figure 25** show the current sense as function of the load current in the power DMOS. Usually, a pull-down resistor R_{IS} is connected to the current sense pin IS. A typical value is 1kΩ. The dotted curve represents the typical sense current, assuming a typical dk_{ILIS} factor value. The range between the two solid curves shows the sense accuracy the device is able to provide, at a defined current.

$$I_{IS} = \frac{I_L}{dk_{ILIS}} \pm I_{IS0} \qquad with (I_{IS} \geq 0) \tag{1}$$

Where the definition of dk_{ILIS} is:

$$dk_{ILIS} = \frac{I_{L4} - I_{L1}}{I_{IS4} - I_{IS1}} \tag{2}$$

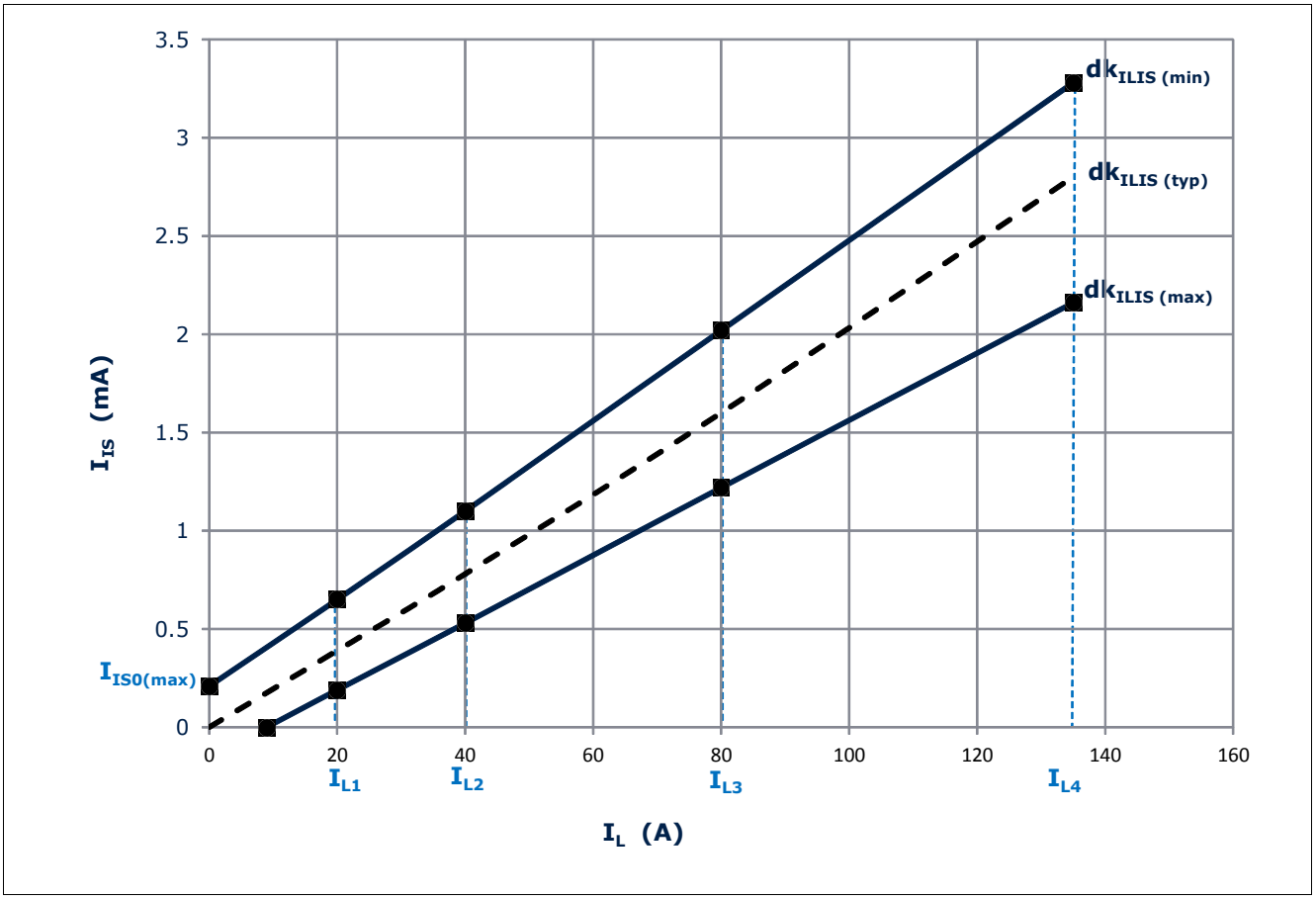


Figure 24 Current Sense for Nominal and Overload Condition

5.4.3.1 SENSE Signal Variation and calibration

In some application, an enhanced accuracy is required around the device nominal current range $I_{L(NOM)}$. To achieve this accuracy requirement, a calibration on the application is possible. After two points calibration, the BTS50015-1TMA will have a limited I_{IS} value spread at different load currents and temperature conditions. The I_{IS}