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# PROFET™ + 12V

# BTS5120-2EKA

Smart High-Side Power Switch

Dual Channel, 120mΩ

## Data Sheet

Rev. 2.1, 2011-09-01

## Automotive Power

## Table of Contents

|          |  |           |
|----------|--|-----------|
| <b>1</b> | <b>Overview</b>  | <b>4</b>  |
| <b>2</b> | <b>Block Diagram</b>   | <b>6</b>  |
| <b>3</b> | <b>Pin Configuration</b>   | <b>7</b>  |
| 3.1      | Pin Assignment   | 7         |
| 3.2      | Pin Definitions and Functions  | 7         |
| 3.3      | Voltage and Current Definition                                       | 8         |
| <b>4</b> | <b>General Product Characteristics</b>                               | <b>9</b>  |
| 4.1      | Absolute Maximum Ratings   | 9         |
| 4.2      | Functional Range   | 11        |
| 4.3      | Thermal Resistance   | 12        |
| 4.3.1    | PCB set up   | 12        |
| 4.3.2    | Thermal Impedance  | 13        |
| <b>5</b> | <b>Power Stage</b>   | <b>15</b> |
| 5.1      | Output ON-state Resistance   | 15        |
| 5.2      | Turn ON/OFF Characteristics with Resistive Load                      | 15        |
| 5.3      | Inductive Load   | 16        |
| 5.3.1    | Output Clamping  | 16        |
| 5.3.2    | Maximum Load Inductance  | 17        |
| 5.4      | Inverse Current Capability   | 17        |
| 5.5      | Electrical Characteristics Power Stage                               | 19        |
| <b>6</b> | <b>Protection Functions</b>  | <b>21</b> |
| 6.1      | Loss of Ground Protection  | 21        |
| 6.2      | Undervoltage Protection  | 21        |
| 6.3      | Overvoltage Protection   | 22        |
| 6.4      | Reverse Polarity Protection  | 23        |
| 6.5      | Overload Protection  | 23        |
| 6.5.1    | Current Limitation   | 23        |
| 6.5.2    | Temperature Limitation in the Power DMOS                             | 24        |
| 6.5.3    | Short Circuit Appearance with Channel in Parallel                    | 25        |
| 6.6      | Electrical Characteristics for the Protection Functions              | 26        |
| <b>7</b> | <b>Diagnostic Functions</b>  | <b>27</b> |
| 7.1      | IS Pin   | 27        |
| 7.2      | SENSE Signal in Different Operating Modes                            | 28        |
| 7.3      | SENSE Signal in the Nominal Current Range                            | 29        |
| 7.3.1    | SENSE Signal Variation as a Function of Temperature and Load Current | 29        |
| 7.3.2    | SENSE Signal Timing  | 30        |
| 7.3.3    | SENSE Signal in Open Load  | 31        |
| 7.3.3.1  | Open Load in ON Diagnostic   | 31        |
| 7.3.3.2  | Open Load in OFF Diagnostic  | 31        |
| 7.3.3.3  | Open Load Diagnostic Timing  | 32        |
| 7.3.4    | SENSE Signal with OUT in Short Circuit to $V_S$                      | 33        |
| 7.3.5    | SENSE Signal in Case of Overload                                     | 33        |
| 7.3.6    | SENSE Signal in Case of Inverse Current                              | 33        |
| 7.4      | Electrical Characteristics Diagnostic Function                       | 34        |
| <b>8</b> | <b>Input Pins</b>  | <b>37</b> |
| 8.1      | Input Circuitry  | 37        |

Table of Contents

|           |  |           |
|-----------|--|-----------|
| 8.2       | DEN / DSEL Pin                                     | 37        |
| 8.3       | Input Pin Voltage                                  | 37        |
| 8.4       | Electrical Characteristics                         | 38        |
| <b>9</b>  | <b>Characterization Results</b>                    | <b>39</b> |
| 9.1       | General Product Characteristics                    | 39        |
| 9.1.1     | Minimum Functional Supply Voltage                  | 39        |
| 9.1.2     | Undervoltage Shutdown                              | 39        |
| 9.1.3     | Current Consumption One Channel active             | 40        |
| 9.1.4     | Current Consumption Two Channels active            | 40        |
| 9.1.5     | Standby Current for Whole Device with Load         | 40        |
| 9.2       | Power Stage  | 41        |
| 9.2.1     | Output Voltage Drop Limitation at Low Load Current | 41        |
| 9.2.2     | Drain to Source Clamp Voltage                      | 41        |
| 9.2.3     | Slew Rate at Turn ON                               | 42        |
| 9.2.4     | Slew Rate at Turn OFF                              | 42        |
| 9.2.5     | Turn ON  | 42        |
| 9.2.6     | Turn OFF   | 43        |
| 9.2.7     | Turn ON / OFF matching                             | 43        |
| 9.2.8     | Switch ON Energy                                   | 44        |
| 9.2.9     | Switch OFF Energy                                  | 44        |
| 9.3       | Protection Functions                               | 45        |
| 9.3.1     | Overload Condition in the Low Voltage Area         | 45        |
| 9.3.2     | Overload Condition in the High Voltage Area        | 45        |
| 9.4       | Diagnostic Mechanism                               | 46        |
| 9.4.1     | Current Sense at no Load                           | 46        |
| 9.4.2     | Open Load Detection Threshold in ON State          | 46        |
| 9.4.3     | Sense Signal Maximum Voltage                       | 47        |
| 9.4.4     | Sense Signal maximum Current                       | 47        |
| 9.5       | Input Pins   | 48        |
| 9.5.1     | Input Voltage Threshold ON to OFF                  | 48        |
| 9.5.2     | Input Voltage Threshold OFF to ON                  | 48        |
| 9.5.3     | Input Voltage Hysteresis                           | 49        |
| 9.5.4     | Input Current High Level                           | 49        |
| <b>10</b> | <b>Application Information</b>                     | <b>50</b> |
| 10.1      | Further Application Information                    | 51        |
| <b>11</b> | <b>Package Outlines</b>                            | <b>52</b> |
| <b>12</b> | <b>Revision History</b>                            | <b>53</b> |



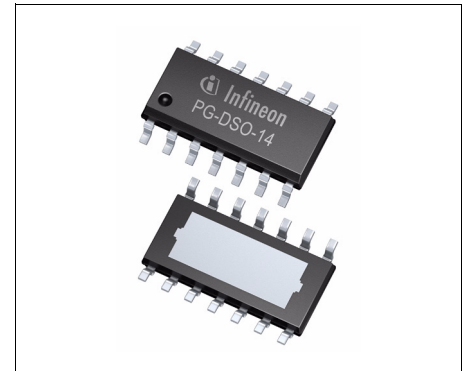
## 1 Overview

### Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps

### Basic Features

- Two channel device
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Logic ground independent from load ground
- Very low power DMOS leakage current in OFF state
- Green product (RoHS compliant)
- AEC qualified



PG-DSO-14-40 EP

### Description

The BTS5120-2EKA is a 120 mΩ dual channel Smart High-Side Power Switch, embedded in a PG-DSO-14-40 EP, Exposed Pad package, providing protective functions and diagnosis. The power transistor is built by an N-channel vertical power MOSFET with charge pump. The device is integrated in Smart6 technology. It is specially designed to drive lamps up to 1 \* 10W, as well as LEDs in the harsh automotive environment.

Table 1 Product Summary

| Parameter  | Symbol        | Value        |
|--|---------------|--------------|
| Operating voltage range  | $V_{S(OP)}$   | 5 V ... 28 V |
| Maximum supply voltage   | $V_{S(LD)}$   | 41 V         |
| Maximum ON state resistance at $T_J = 150\text{ °C}$ per channel | $R_{DS(ON)}$  | 240 mΩ       |
| Nominal load current (one channel active)                        | $I_{L(NOM)1}$ | 2.5 A        |
| Nominal load current (both channels active)                      | $I_{L(NOM)2}$ | 2 A          |
| Typical current sense ratio                                      | $k_{ILIS}$    | 550          |
| Minimum current limitation                                       | $I_{L5(SC)}$  | 9 A          |
| Maximum standby current with load at $T_J = 25\text{ °C}$        | $I_{S(OFF)}$  | 500 nA       |

| Type         | Package         | Marking      |
|--------------|-----------------|--------------|
| BTS5120-2EKA | PG-DSO-14-40 EP | BTS5120-2EKA |

**Diagnostic Functions**

- Proportional load current sense for both channels multiplexed
- Open load in ON and OFF
- Short circuit to battery and ground
- Overtemperature
- Stable diagnostic signal during short circuit
- Enhanced  $k_{ILIS}$  dependency with temperature and load current

**Protection Functions**

- Stable behavior during undervoltage
- Reverse polarity protection with external components
- Secure load turn-off during logic ground disconnect with external components
- Overtemperature protection with restart
- Overvoltage protection with external components
- Voltage dependent current limitation
- Enhanced short circuit operation

## 2 Block Diagram

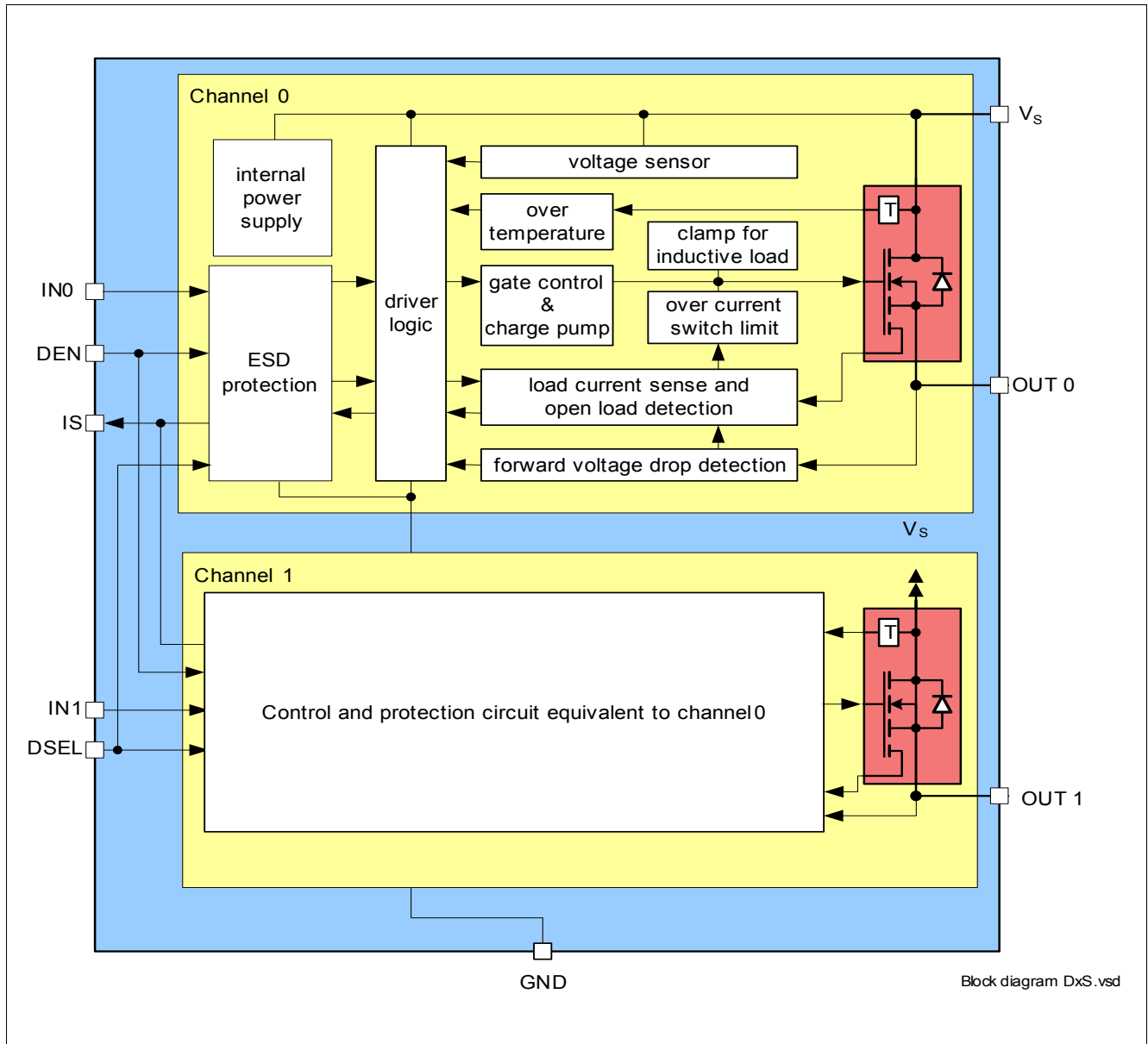


Figure 1 Block Diagram for the BTS5120-2EKA

### 3 Pin Configuration

#### 3.1 Pin Assignment

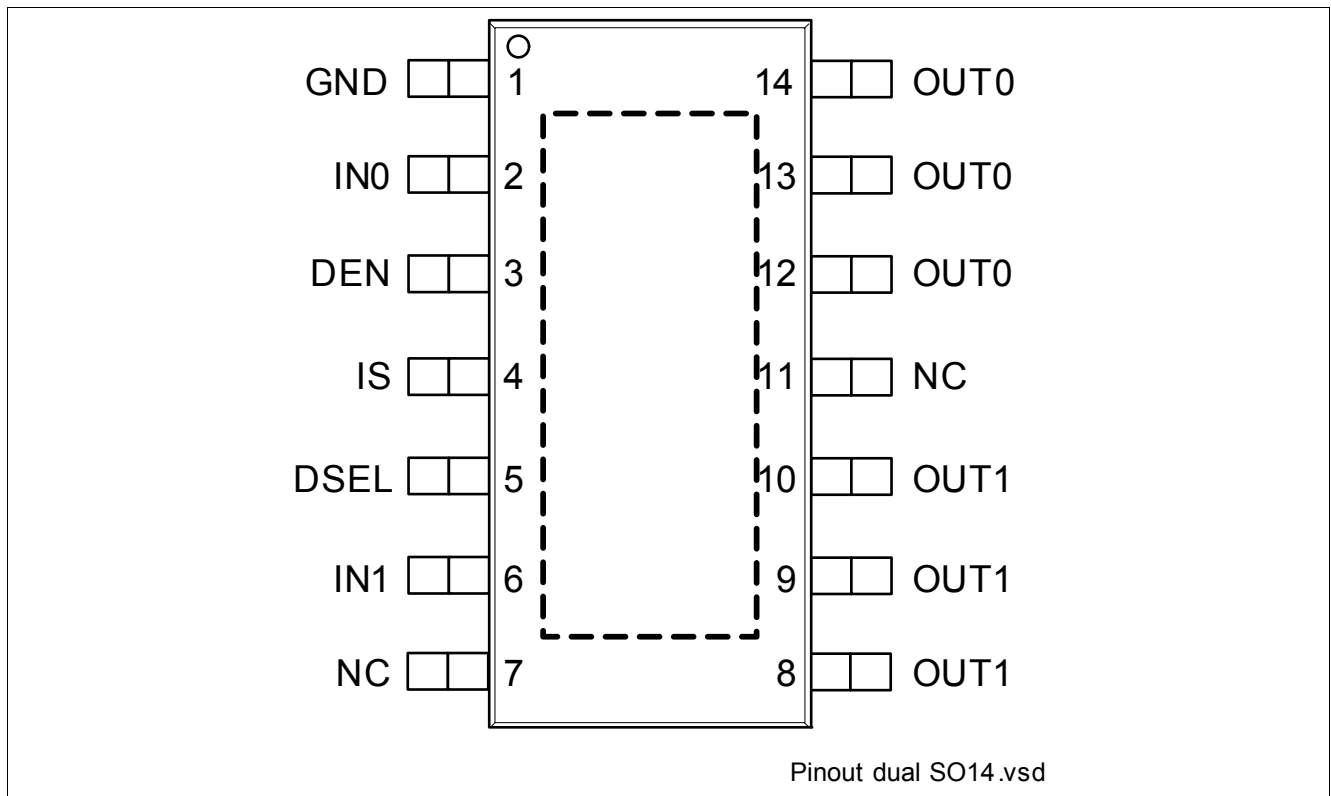


Figure 2 Pin Configuration

#### 3.2 Pin Definitions and Functions

| Pin         | Symbol | Function  |
|-------------|--------|---|
| 1           | GND    | <b>GrouND</b> ; Ground connection   |
| 2           | IN0    | <b>INput channel 0</b> ; Input signal for channel 0 activation                          |
| 3           | DEN    | <b>Diagnostic ENable</b> ; Digital signal to enable/disable the diagnosis of the device |
| 4           | IS     | <b>Sense</b> ; Sense current of the selected channel                                    |
| 5           | DSEL   | <b>Diagnostic SElection</b> ; Digital signal to select the channel to be diagnosed      |
| 6           | IN1    | <b>INput channel 1</b> ; Input signal for channel 1 activation                          |
| 7, 11       | NC     | <b>Not Connected</b> ; No internal connection to the chip                               |
| 8, 9, 10    | OUT1   | <b>OUTput 1</b> ; Protected high side power output channel 1 <sup>1)</sup>              |
| 12, 13, 14  | OUT0   | <b>OUTput 0</b> ; Protected high side power output channel 0 <sup>1)</sup>              |
| Cooling Tab | $V_S$  | <b>Voltage Supply</b> ; Battery voltage   |

1) All output pins of a given channel must be connected together on the PCB. All pins of an output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.



### 3.3 Voltage and Current Definition

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

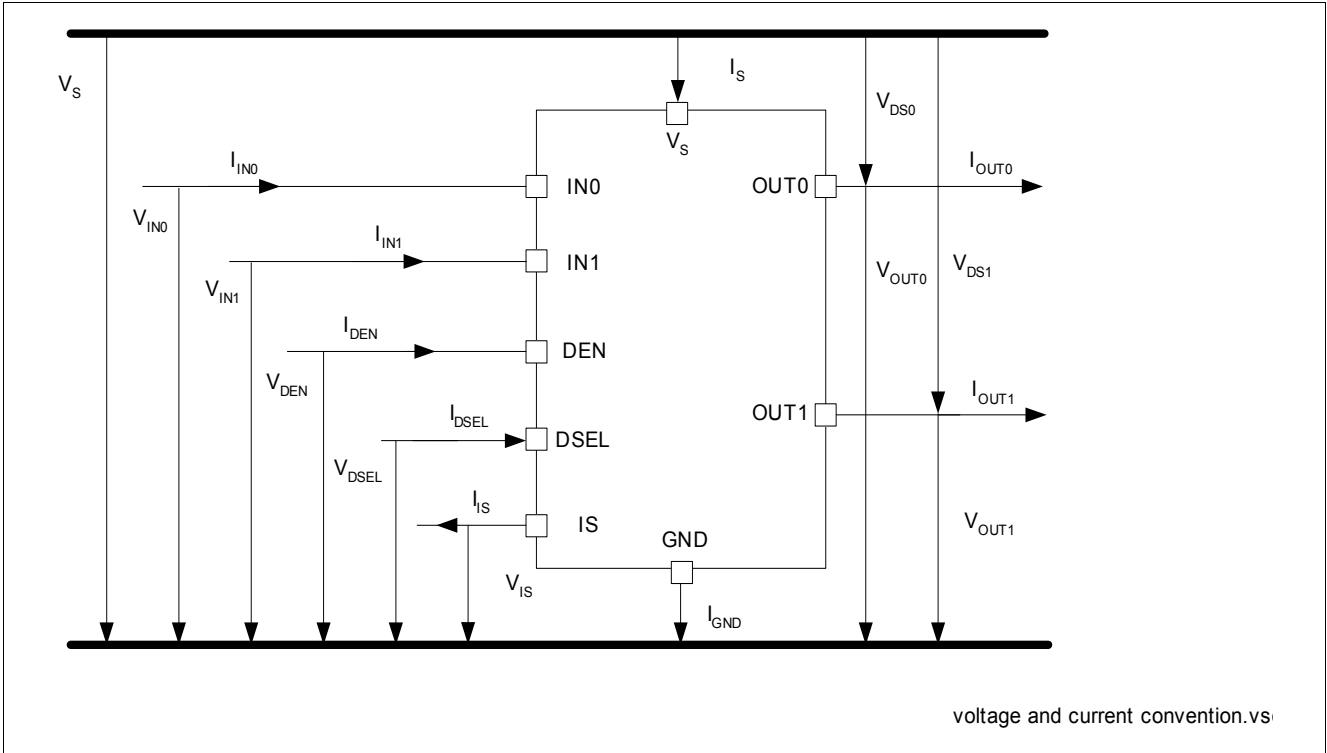


Figure 3 Voltage and Current Definition

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings <sup>1)</sup>**
 $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ; (unless otherwise specified)

| Parameter                                   | Symbol               | Values    |      |                     | Unit     | Note / Test Condition  | Number   |
|---|----------------------|-----------|------|---------------------|----------|--|----------|
|   |                      | Min.      | Typ. | Max.                |          |  |          |
| <b>Supply Voltages</b>                      |                      |           |      |                     |          |  |          |
| Supply voltage                              | $V_S$                | -0.3      | –    | 28                  | V        | –  | P_4.1.1  |
| Reverse polarity voltage                    | $-V_{S(\text{REV})}$ | 0         | –    | 16                  | V        | $t < 2$ min<br>$T_A = 25^\circ\text{C}$<br>$R_L \geq 12\ \Omega$<br>$R_{\text{GND}} = 150\ \Omega$   | P_4.1.2  |
| Supply voltage for short circuit protection | $V_{\text{BAT(SC)}}$ | 0         | –    | 24                  | V        | <sup>2)</sup> $R_{\text{ECU}} = 20\ \text{m}\Omega$<br>$R_{\text{Cable}} = 16\ \text{m}\Omega/\text{m}$<br>$L_{\text{Cable}} = 1\ \mu\text{H}/\text{m}$ ,<br>$l = 0$ or $5$ m<br>See <a href="#">Chapter 6</a> and <a href="#">Figure 53</a> | P_4.1.3  |
| Supply voltage for Load dump protection     | $V_{S(\text{LD})}$   | –         | –    | 41                  | V        | <sup>3)</sup> $R_I = 2\ \Omega$<br>$R_L = 12\ \Omega$  | P_4.1.12 |
| <b>Short Circuit Capability</b>             |                      |           |      |                     |          |  |          |
| Permanent short circuit IN pin toggles      | $n_{\text{RSC1}}$    | –         | –    | 100                 | k cycles | <sup>4)</sup> $t_{\text{ON}} = 300\text{ms}$   | P_4.1.4  |
| <b>Input Pins</b>                           |                      |           |      |                     |          |  |          |
| Voltage at INPUT pins                       | $V_{\text{IN}}$      | -0.3<br>– | –    | 6<br>7              | V        | –<br>$t < 2$ min   | P_4.1.13 |
| Current through INPUT pins                  | $I_{\text{IN}}$      | -2        | –    | 2                   | mA       | –  | P_4.1.14 |
| Voltage at DEN pin                          | $V_{\text{DEN}}$     | -0.3<br>– | –    | 6<br>7              | V        | –<br>$t < 2$ min   | P_4.1.15 |
| Current through DEN pin                     | $I_{\text{DEN}}$     | -2        | –    | 2                   | mA       | –  | P_4.1.16 |
| Voltage at DSEL pin                         | $V_{\text{DSEL}}$    | -0.3<br>– | –    | 6<br>7              | V        | –<br>$t < 2$ min   | P_4.1.17 |
| Current through DSEL pin                    | $I_{\text{DSEL}}$    | -2        | –    | 2                   | mA       | –  | P_4.1.18 |
| <b>Sense Pin</b>                            |                      |           |      |                     |          |  |          |
| Voltage at IS pin                           | $V_{\text{IS}}$      | -0.3      | –    | $V_S$               | V        | –  | P_4.1.19 |
| Current through IS pin                      | $I_{\text{IS}}$      | -25       | –    | 50                  | mA       | –  | P_4.1.20 |
| <b>Power Stage</b>                          |                      |           |      |                     |          |  |          |
| Load current                                | $ I_L $              | –         | –    | $I_{L(\text{LIM})}$ | A        | –  | P_4.1.21 |
| Power dissipation (DC)                      | $P_{\text{TOT}}$     | –         | –    | 1.8                 | W        | $T_A = 85^\circ\text{C}$<br>$T_J < 150^\circ\text{C}$  | P_4.1.22 |

**Table 2 Absolute Maximum Ratings (cont'd)<sup>1)</sup>**
 $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; (unless otherwise specified)

| Parameter   | Symbol    | Values      |      |          | Unit               | Note / Test Condition  | Number   |
|---|-----------|-------------|------|----------|--------------------|--|----------|
|   |           | Min.        | Typ. | Max.     |                    |  |          |
| Maximum energy dissipation<br>Single pulse (one channel)  | $E_{AS}$  | –           | –    | 15       | mJ                 | $I_{L(0)} = 2\text{ A}$<br>$T_{J(0)} = 150^{\circ}\text{C}$<br>$V_S = 13.5\text{ V}$ | P_4.1.23 |
| Voltage at power transistor                               | $V_{DS}$  | –           | –    | 41       | V                  | –  | P_4.1.26 |
| <b>Currents</b>   |           |             |      |          |                    |  |          |
| Current through ground pin                                | $I_{GND}$ | -10<br>-150 | –    | 10<br>20 | mA                 | –<br>$t < 2\text{ min}$  | P_4.1.27 |
| <b>Temperatures</b>                                       |           |             |      |          |                    |  |          |
| Junction temperature                                      | $T_J$     | -40         | –    | 150      | $^{\circ}\text{C}$ | –  | P_4.1.28 |
| Storage temperature                                       | $T_{STG}$ | -55         | –    | 150      | $^{\circ}\text{C}$ | –  | P_4.1.30 |
| <b>ESD Susceptibility</b>                                 |           |             |      |          |                    |  |          |
| ESD susceptibility (all pins)                             | $V_{ESD}$ | -2          | –    | 2        | kV                 | <sup>5)</sup> HBM  | P_4.1.31 |
| ESD susceptibility OUT Pin<br>vs. GND and $V_S$ connected | $V_{ESD}$ | -4          | –    | 4        | kV                 | <sup>5)</sup> HBM  | P_4.1.32 |
| ESD susceptibility  | $V_{ESD}$ | -500        | –    | 500      | V                  | <sup>6)</sup> CDM  | P_4.1.33 |
| ESD susceptibility pin<br>(corner pins)                   | $V_{ESD}$ | -750        | –    | 750      | V                  | <sup>6)</sup> CDM  | P_4.1.34 |

1) Not subject to production test. Specified by design.

2) Hardware set-up in accordance to AEC Q100-012 and AEC Q101-006.

3)  $V_{S(LD)}$  is setup without the DUT connected to the generator per ISO 7637-1.

4) EOL tests according to AECQ100-012. Threshold limit for short circuit failures: 100 ppm. Please refer to the legal disclaimer for short-circuit capability on Page 54 of this document.

5) ESD susceptibility HBM according to EIA/JESD 22-A 114B.

6) "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

**Notes**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

## 4.2 Functional Range

**Table 3 Functional Range  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; (unless otherwise specified)**

| Parameter   | Symbol                 | Values |      |      | Unit          | Note / Test Condition   | Number   |
|---|------------------------|--------|------|------|---------------|---|----------|
|   |                        | Min.   | Typ. | Max. |               |   |          |
| Nominal operating voltage                             | $V_{\text{NOM}}$       | 8      | 13.5 | 18   | V             | –   | P_4.2.1  |
| Extended operating voltage                            | $V_{\text{S(OP)}}$     | 5      | –    | 28   | V             | <sup>2)</sup> $V_{\text{IN}} = 4.5\text{ V}$<br>$R_{\text{L}} = 12\ \Omega$<br>$V_{\text{DS}} < 0.5\text{ V}$<br>See <a href="#">Figure 15</a>  | P_4.2.2  |
| Minimum functional supply voltage                     | $V_{\text{S(OP)_MIN}}$ | 3.8    | 4.3  | 5    | V             | <sup>1)</sup> $V_{\text{IN}} = 4.5\text{ V}$<br>$R_{\text{L}} = 12\ \Omega$<br>From $I_{\text{OUT}} = 0\text{ A}$ to<br>$V_{\text{DS}} < 0.5\text{ V}$ ;<br>See <a href="#">Figure 15</a><br>See <a href="#">Figure 29</a>                                | P_4.2.3  |
| Undervoltage shutdown                                 | $V_{\text{S(UV)}}$     | 3      | 3.5  | 4.1  | V             | <sup>1)</sup> $V_{\text{IN}} = 4.5\text{ V}$<br>$V_{\text{DEN}} = 0\text{ V}$<br>$R_{\text{L}} = 12\ \Omega$<br>From $V_{\text{DS}} < 1\text{ V}$ ;<br>to $I_{\text{OUT}} = 0\text{ A}$<br>See <a href="#">Figure 15</a><br>See <a href="#">Figure 30</a> | P_4.2.4  |
| Undervoltage shutdown hysteresis                      | $V_{\text{S(UV)_HYS}}$ | –      | 850  | –    | mV            | <sup>2)</sup> –   | P_4.2.13 |
| Operating current<br>One channel active               | $I_{\text{GND}_1}$     | –      | 3.5  | 6    | mA            | $V_{\text{IN}} = 5.5\text{ V}$<br>$V_{\text{DEN}} = 5.5\text{ V}$<br>Device in $R_{\text{DS(ON)}}$<br>$V_{\text{S}} = 18\text{ V}$<br>See <a href="#">Figure 31</a>   | P_4.2.5  |
| Operating current<br>All channels active              | $I_{\text{GND}_2}$     | –      | 5    | 8    | mA            | $V_{\text{IN}} = 5.5\text{ V}$<br>$V_{\text{DEN}} = 5.5\text{ V}$<br>Device in $R_{\text{DS(ON)}}$<br>$V_{\text{S}} = 18\text{ V}$<br>See <a href="#">Figure 32</a>   | P_4.2.6  |
| Standby current for whole device with load (ambiente) | $I_{\text{S(OFF)}}$    | –      | 0.1  | 0.5  | $\mu\text{A}$ | <sup>1)</sup> $V_{\text{S}} = 18\text{ V}$<br>$V_{\text{OUT}} = 0\text{ V}$<br>$V_{\text{IN}}$ floating<br>$V_{\text{DEN}}$ floating<br>$T_J \leq 85^{\circ}\text{C}$<br>See <a href="#">Figure 33</a>  | P_4.2.7  |

**Table 3 Functional Range (cont'd)  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; (unless otherwise specified)**

| Parameter   | Symbol            | Values |      |      | Unit          | Note / Test Condition  | Number   |
|---|-------------------|--------|------|------|---------------|--|----------|
|   |                   | Min.   | Typ. | Max. |               |  |          |
| Maximum standby current for whole device with load            | $I_{S(OFF\_150)}$ | –      | 2    | 20   | $\mu\text{A}$ | $V_S = 18\text{ V}$<br>$V_{OUT} = 0\text{ V}$<br>$V_{IN}$ floating<br>$V_{DEN}$ floating<br>$T_J = 150^{\circ}\text{C}$<br>See <a href="#">Figure 33</a> | P_4.2.10 |
| Standby current for whole device with load, diagnostic active | $I_{S(OFF\_DEN)}$ | –      | 0.6  | –    | mA            | <sup>2)</sup> $V_S = 18\text{ V}$<br>$V_{OUT} = 0\text{ V}$<br>$V_{IN}$ floating<br>$V_{DEN} = 5.5\text{ V}$   | P_4.2.8  |

1) Test at  $T_J = -40^{\circ}\text{C}$  only

2) Not subject to production test. Specified by design.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

### 4.3 Thermal Resistance

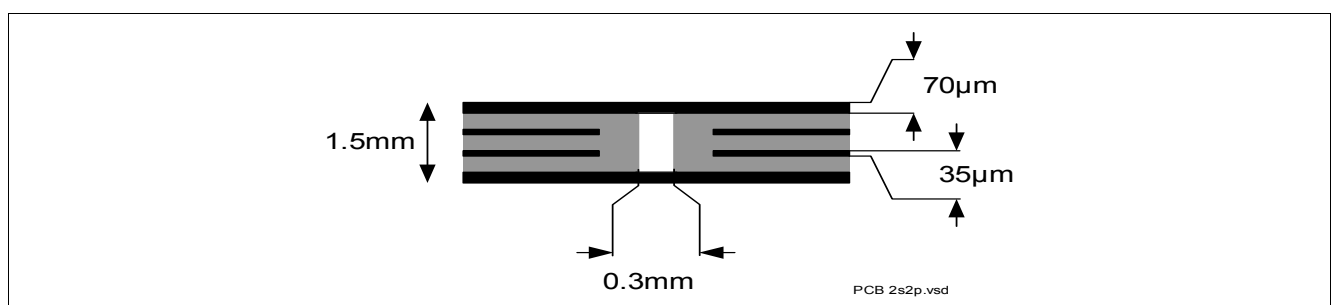
**Table 4 Thermal Resistance**

| Parameter                                   | Symbol     | Values |      |      | Unit | Note / Test Condition | Number  |
|---|------------|--------|------|------|------|-----------------------|---------|
|   |            | Min.   | Typ. | Max. |      |                       |         |
| Junction to soldering point                 | $R_{thJS}$ | –      | 5    | –    | K/W  | 1)                    | P_4.3.1 |
| Junction to ambient<br>Both channels active | $R_{thJA}$ | –      | 37   | –    | K/W  | 1) 2)                 | P_4.3.2 |

1) Not subject to production test. Specified by design.

2) Specified  $R_{thja}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 $\mu\text{m}$  Cu, 2 x 35 $\mu\text{m}$  Cu). Where applicable, a thermal via array under the exposed pad contacts the first inner copper layer. Please refer to [Figure 4](#) and [Figure 5](#).

#### 4.3.1 PCB set up


**Figure 4 2s2p PCB Cross Section**

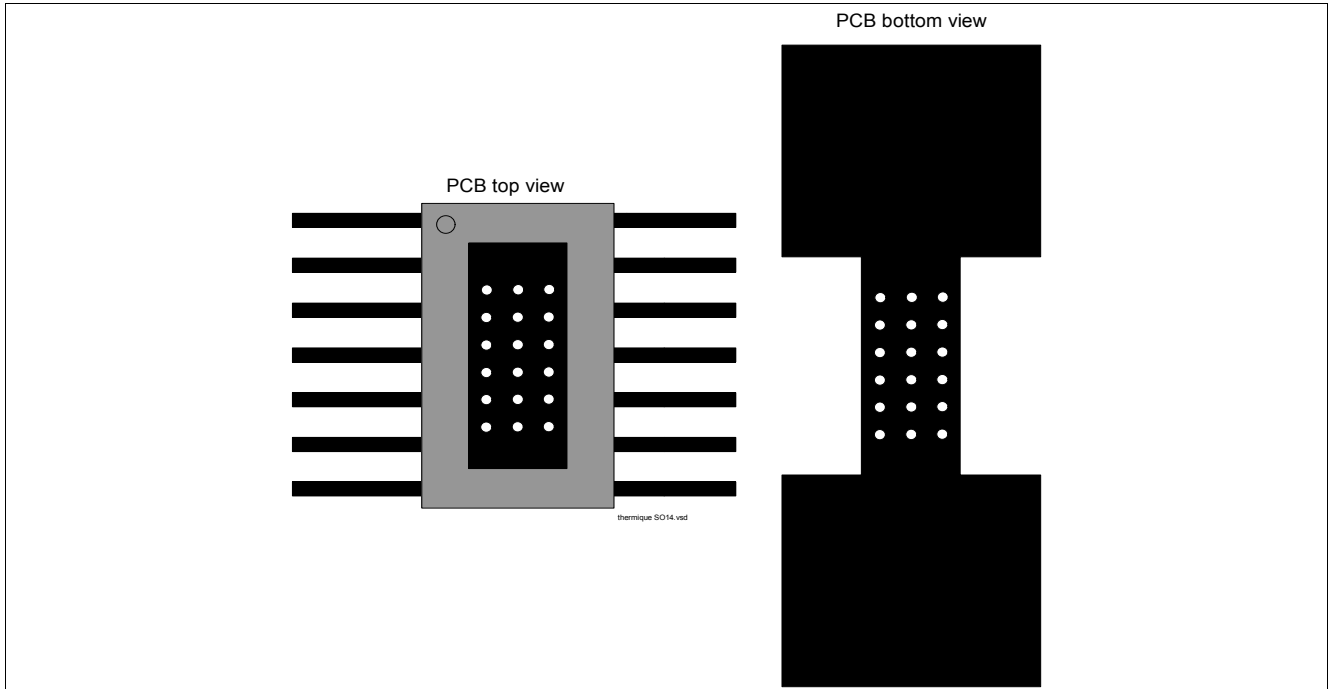


Figure 5 PC Board Top and Bottom View for Thermal Simulation with 600 mm<sup>2</sup> Cooling Area

### 4.3.2 Thermal Impedance

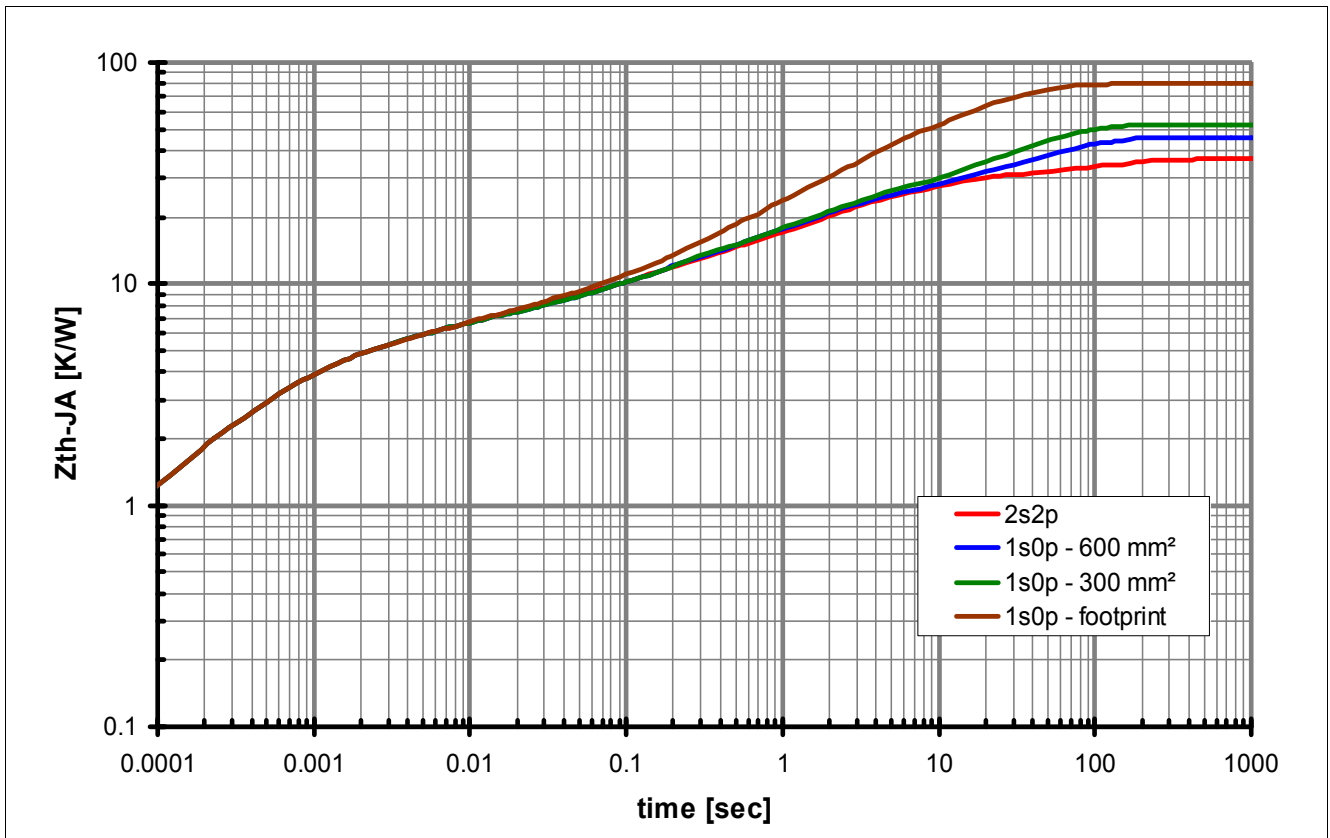


Figure 6 Typical Thermal Impedance. PCB set up according to Figure 5

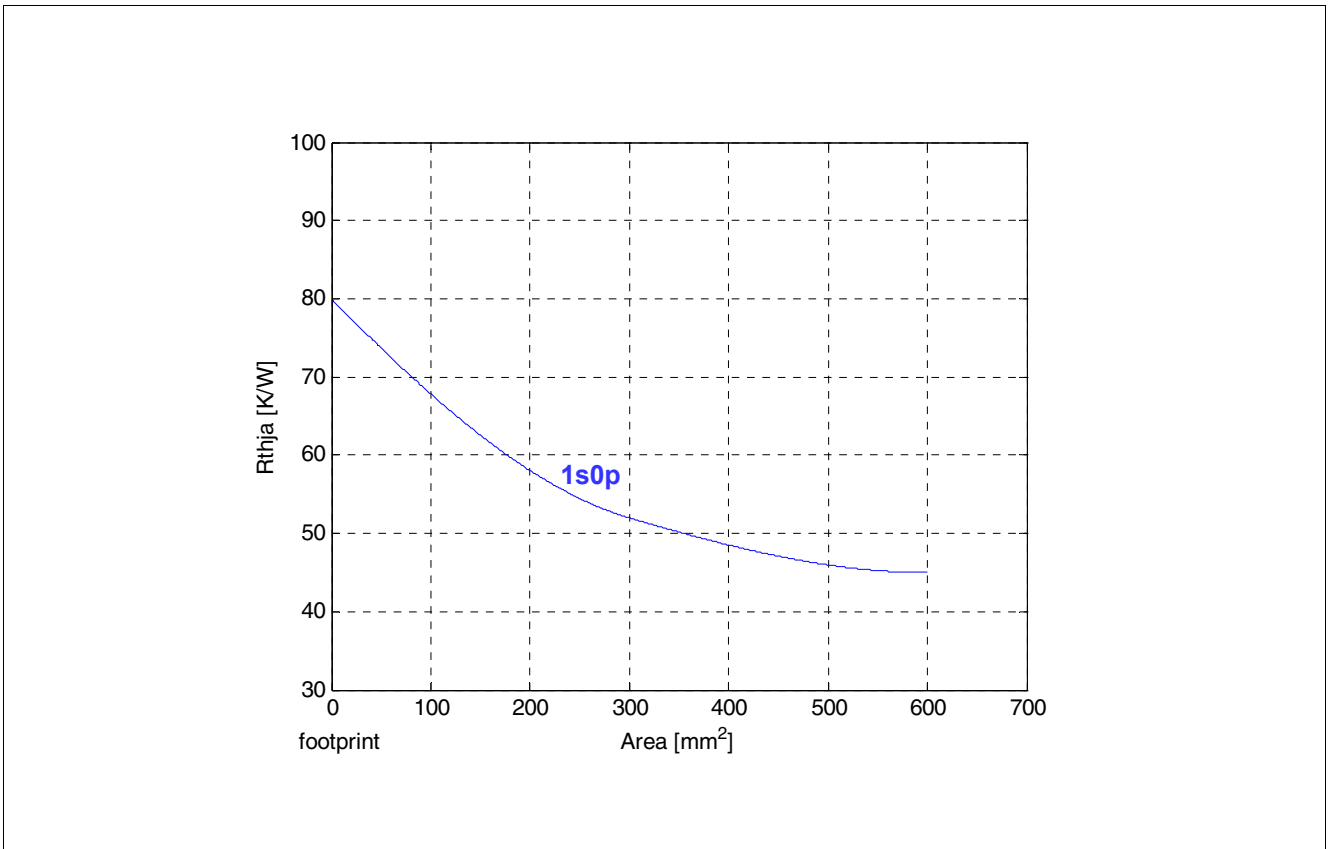


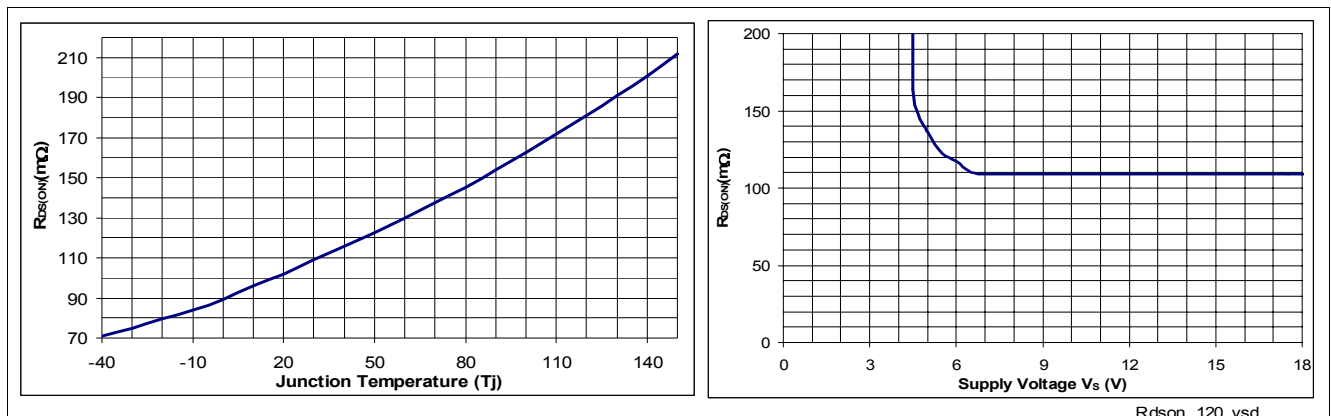
Figure 7 Typical Thermal Resistance. PCB set up 1s0p

## 5 Power Stage

The power stages are built using an N-channel vertical power MOSFET (DMOS) with charge pump.

### 5.1 Output ON-state Resistance

The ON-state resistance  $R_{DS(ON)}$  depends on the supply voltage as well as the junction temperature  $T_J$ . **Figure 8** shows the dependencies in terms of temperature and supply voltage for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 6.4**.

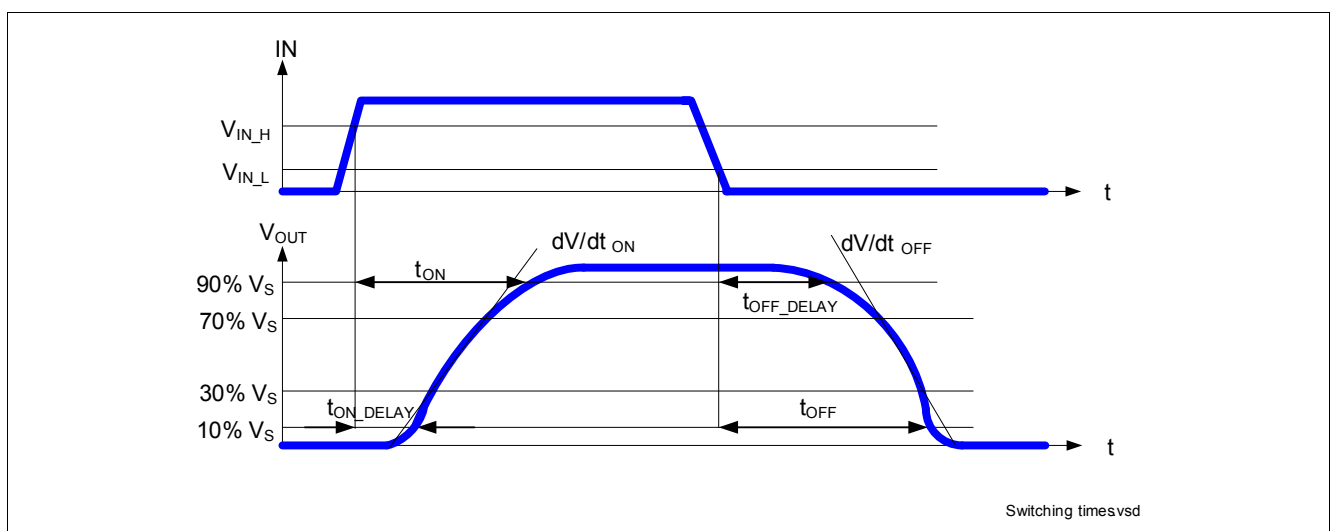


**Figure 8** Typical ON-state Resistance

A high signal at the input pin (see **Chapter 8**) causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

### 5.2 Turn ON/OFF Characteristics with Resistive Load

**Figure 9** shows the typical timing when switching a resistive load.



**Figure 9** Switching a Resistive Load Timing



### 5.3 Inductive Load

#### 5.3.1 Output Clamping

When switching OFF inductive loads with high side switches, the voltage  $V_{OUT}$  drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltages, there is a voltage clamp mechanism  $Z_{DS(AZ)}$  implemented that limits negative output voltage to a certain level ( $V_S - V_{DS(AZ)}$ ). Please refer to **Figure 10** and **Figure 11** for details. Nevertheless, the maximum allowed load inductance is limited.

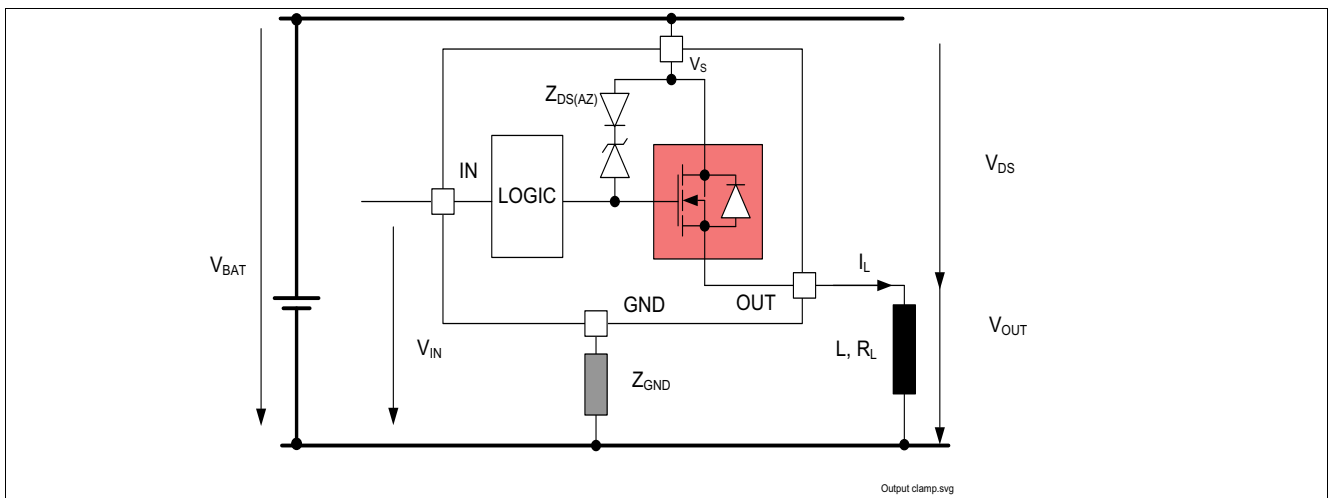


Figure 10 Output Clamp (OUT0 and OUT1)

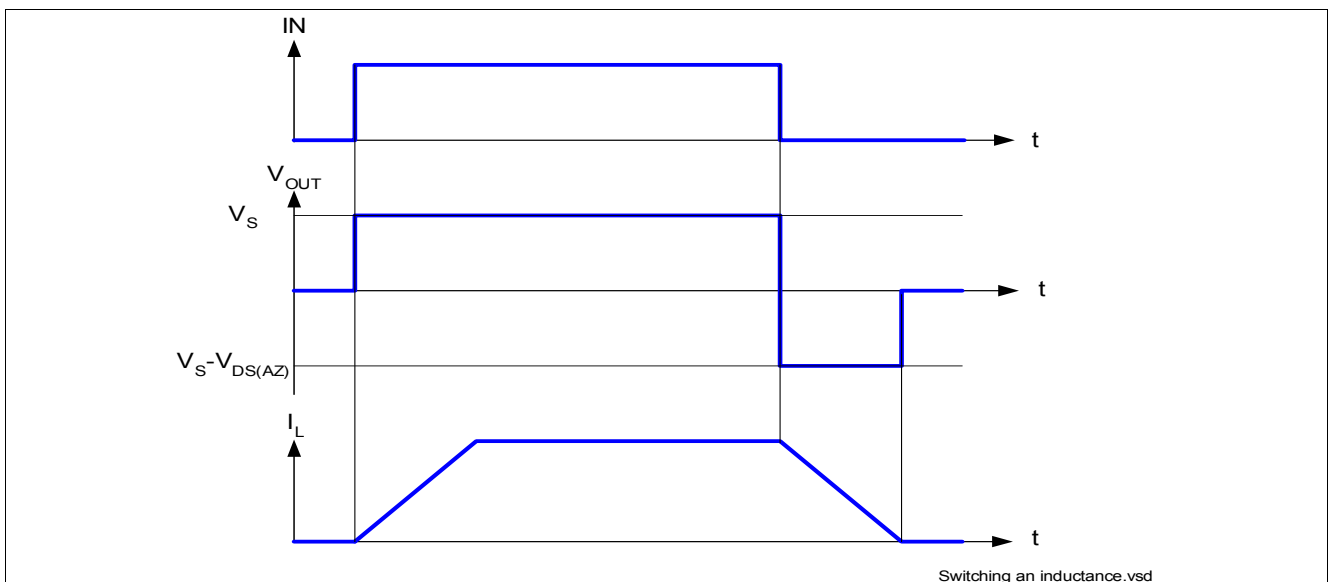


Figure 11 Switching an Inductive Load Timing

### 5.3.2 Maximum Load Inductance

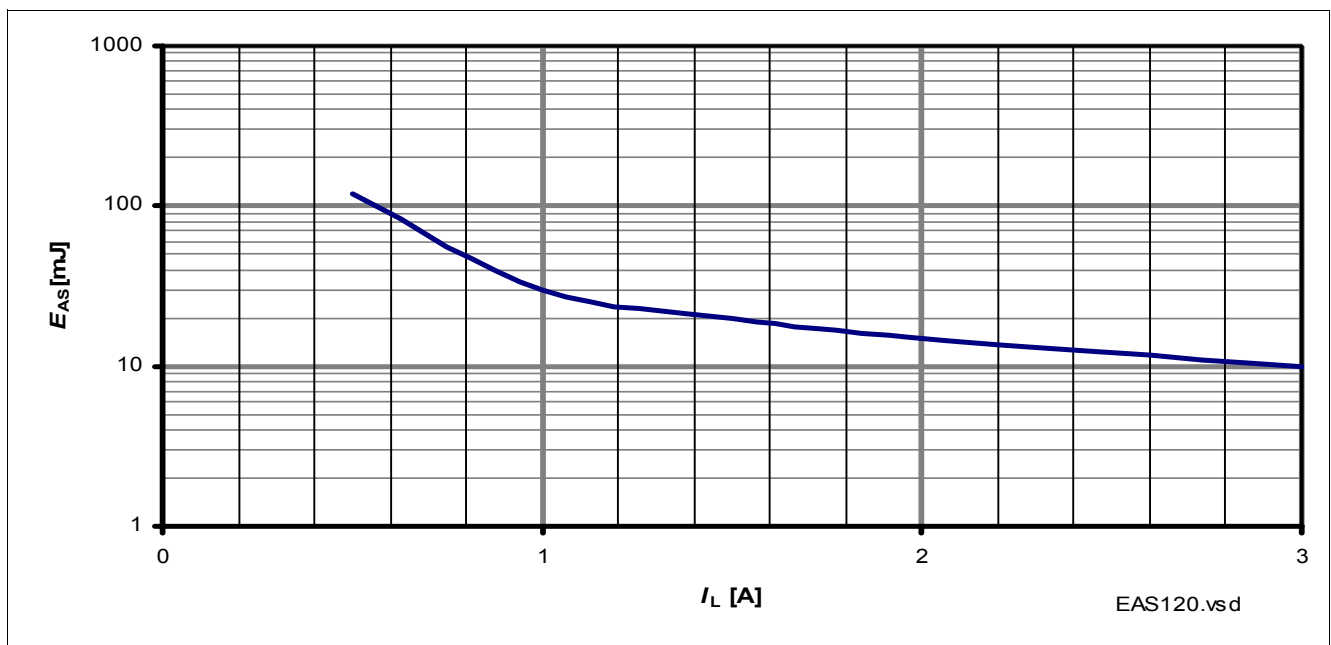
During demagnetization of inductive loads, energy has to be dissipated in the BTS5120-2EKA. This energy can be calculated with following equation:

$$E = V_{DS(AZ)} \times \frac{L}{R_L} \times \left[ \frac{V_S - V_{DS(AZ)}}{R_L} \times \ln \left( 1 - \frac{R_L \times I_L}{V_S - V_{DS(AZ)}} \right) + I_L \right] \quad (1)$$

Following equation simplifies under the assumption of  $R_L = 0 \Omega$ .

$$E = \frac{1}{2} \times L \times I^2 \times \left( 1 - \frac{V_S}{V_S - V_{DS(AZ)}} \right) \quad (2)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See [Figure 12](#) for the maximum allowed energy dissipation as a function of the load current.



**Figure 12** Maximum Energy Dissipation Single Pulse,  $T_{J(0)} = 150 \text{ }^\circ\text{C}$ ;  $V_S = 13.5\text{V}$

### 5.4 Inverse Current Capability

In case of inverse current, meaning a voltage  $V_{INV}$  at the OUTput higher than the supply voltage  $V_S$ , a current  $I_{INV}$  will flow from output to  $V_S$  pin via the body diode of the power transistor (please refer to [Figure 13](#)). The output stage follows the state of the IN pin, except if the IN pin goes from OFF to ON during inverse. In that particular case, the output stage is kept OFF until the inverse current disappears. Nevertheless, the current  $I_{INV}$  should not be higher than  $I_{L(INV)}$ . Otherwise, the second channel can be corrupted and erratic behavior can be observed. If the affected channel is OFF, the diagnostic will detect an open load at OFF. If the affected channel is ON, the diagnostic will detect open load at ON (the overtemperature signal is inhibited). At the appearance of  $V_{INV}$ , a parasitic diagnostic can be observed at the unaffected channel. After, the diagnosis is valid and reflects the output state. At  $V_{INV}$  vanishing, the diagnosis is valid and reflects the output state. During inverse current, no protection function are available.

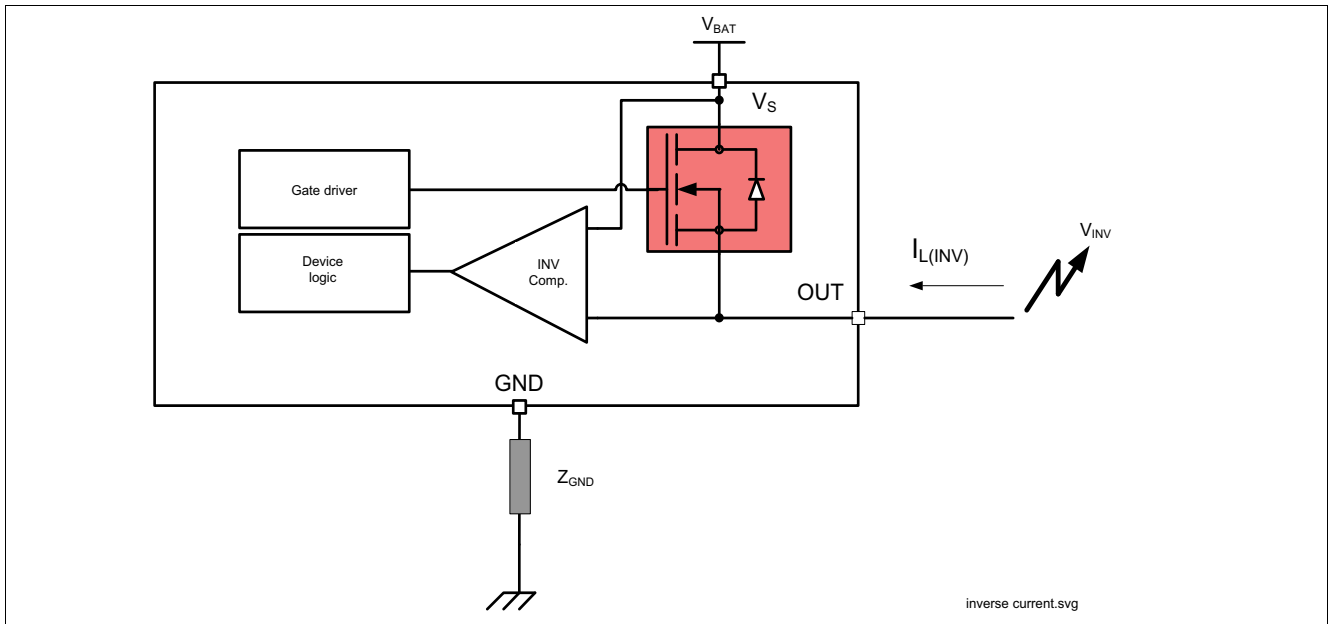


Figure 13 Inverse Current Circuitry

## 5.5 Electrical Characteristics Power Stage

**Table 5 Electrical Characteristics: Power Stage**
 $V_S = 8\text{ V to }18\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$  (unless otherwise specified).

 Typical values are given at  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$ 

| Parameter   | Symbol           | Values |      |      | Unit             | Note / Test Condition   | Number   |
|---|------------------|--------|------|------|------------------|---|----------|
|   |                  | Min.   | Typ. | Max. |                  |   |          |
| ON-state resistance per channel                                       | $R_{DS(ON)_150}$ | 180    | 220  | 240  | m $\Omega$       | $I_L = I_{L4} = 2\text{ A}$<br>$V_{IN} = 4.5\text{ V}$<br>$T_J = 150^\circ\text{C}$<br>See <a href="#">Figure 8</a> | P_5.5.1  |
| ON-state resistance per channel                                       | $R_{DS(ON)_25}$  | –      | 120  | –    | m $\Omega$       | <sup>1)</sup> $T_J = 25^\circ\text{C}$  | P_5.5.21 |
| Nominal load current<br>One channel active                            | $I_{L(NOM)1}$    | –      | 2.5  | –    | A                | <sup>1)</sup> $T_A = 85^\circ\text{C}$<br>$T_J < 150^\circ\text{C}$   | P_5.5.2  |
| Nominal load current<br>All channel active                            | $I_{L(NOM)2}$    | –      | 2    | –    | A                |   | P_5.5.3  |
| Output voltage drop limitation<br>at small load currents              | $V_{DS(NL)}$     | –      | 10   | 25   | mV               | $I_L = I_{L0} = 30\text{ mA}$<br>See <a href="#">Figure 34</a>  | P_5.5.4  |
| Drain to source clamping<br>voltage<br>$V_{DS(AZ)} = [V_S - V_{OUT}]$ | $V_{DS(AZ)}$     | 41     | 47   | 53   | V                | $I_{DS} = 20\text{ mA}$<br>See <a href="#">Figure 11</a><br>See <a href="#">Figure 35</a>                           | P_5.5.5  |
| Output leakage current per<br>channel; $T_J \leq 85^\circ\text{C}$    | $I_{L(OFF)}$     | –      | 0.1  | 0.5  | $\mu\text{A}$    | <sup>2)</sup> $V_{IN}$ floating<br>$V_{OUT} = 0\text{ V}$<br>$T_J \leq 85^\circ\text{C}$                            | P_5.5.6  |
| Output leakage current per<br>channel; $T_J = 150^\circ\text{C}$      | $I_{L(OFF)_150}$ | –      | 1    | 10   | $\mu\text{A}$    | $V_{IN}$ floating<br>$V_{OUT} = 0\text{ V}$<br>$T_J = 150^\circ\text{C}$  | P_5.5.8  |
| Inverse current capability  | $I_{L(INV)}$     | –      | 2    | –    | A                | <sup>1)</sup> $V_S < V_{OUTx}$  | P_5.5.9  |
| Slew rate<br>30% to 70% $V_S$   | $dV/dt_{ON}$     | 0.1    | 0.25 | 0.5  | V/ $\mu\text{s}$ | $R_L = 12\ \Omega$<br>$V_S = 13.5\text{ V}$   | P_5.5.11 |
| Slew rate<br>70% to 30% $V_S$   | $-dV/dt_{OFF}$   | 0.1    | 0.25 | 0.5  | V/ $\mu\text{s}$ | See <a href="#">Figure 9</a><br>See <a href="#">Figure 36</a>   | P_5.5.12 |
| Slew rate matching<br>$dV/dt_{ON} - dV/dt_{OFF}$                      | $\Delta dV/dt$   | -0.15  | 0    | 0.15 | V/ $\mu\text{s}$ | See <a href="#">Figure 37</a><br>See <a href="#">Figure 38</a>  | P_5.5.13 |
| Turn-ON time to $V_{OUT} = 90\%$<br>$V_S$                             | $t_{ON}$         | 30     | 100  | 230  | $\mu\text{s}$    | See <a href="#">Figure 39</a><br>See <a href="#">Figure 40</a>  | P_5.5.14 |
| Turn-OFF time to $V_{OUT} = 10\%$<br>$V_S$                            | $t_{OFF}$        | 30     | 100  | 230  | $\mu\text{s}$    |   | P_5.5.15 |
| Turn-ON / OFF matching<br>$t_{OFF} - t_{ON}$                          | $\Delta t_{SW}$  | -50    | 0    | 50   | $\mu\text{s}$    |   | P_5.5.16 |
| Turn-ON time to $V_{OUT} = 10\%$<br>$V_S$                             | $t_{ON\_delay}$  | 10     | 35   | 100  | $\mu\text{s}$    |   | P_5.5.17 |
| Turn-OFF time to $V_{OUT} = 90\%$<br>$V_S$                            | $t_{OFF\_delay}$ | 10     | 35   | 100  | $\mu\text{s}$    |   | P_5.5.18 |

**Table 5 Electrical Characteristics: Power Stage (cont'd)**

$V_S = 8\text{ V to }18\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$  (unless otherwise specified).  
 Typical values are given at  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$

| Parameter         | Symbol    | Values |      |      | Unit | Note / Test Condition  | Number   |
|-------------------|-----------|--------|------|------|------|--|----------|
|                   |           | Min.   | Typ. | Max. |      |  |          |
| Switch ON energy  | $E_{ON}$  | –      | 0.4  | –    | mJ   | <sup>1)</sup> $R_L = 12\ \Omega$<br>$V_{OUT} = 90\% V_S$<br>$V_S = 18\text{ V}$<br>See <a href="#">Figure 41</a> | P_5.5.19 |
| Switch OFF energy | $E_{OFF}$ | –      | 0.4  | –    | mJ   | <sup>1)</sup> $R_L = 12\ \Omega$<br>$V_{OUT} = 10\% V_S$<br>$V_S = 18\text{ V}$<br>See <a href="#">Figure 42</a> | P_5.5.20 |

- 1) Not subject to production test, specified by design.
- 2) Test at  $T_J = -40^\circ\text{C}$  only

## 6 Protection Functions

The device provides integrated protection functions. These functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

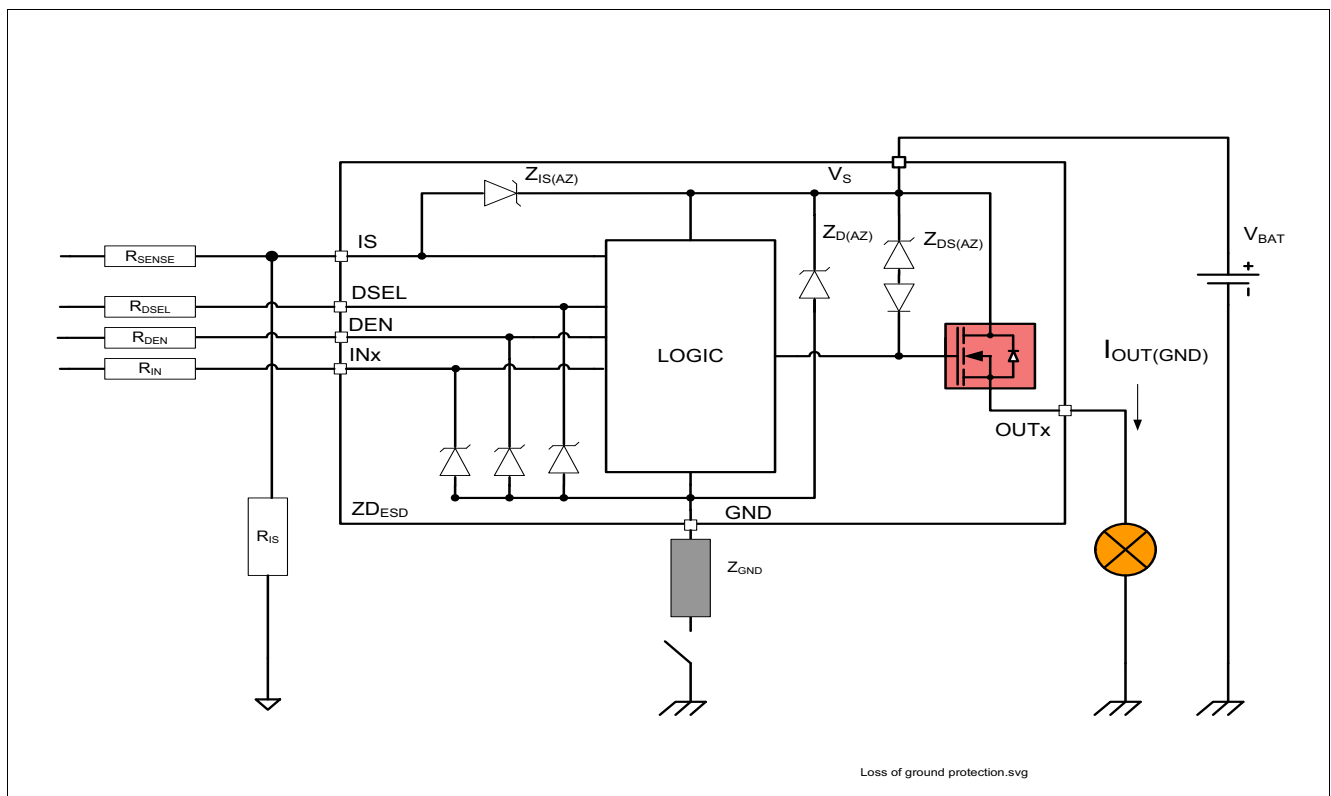
### 6.1 Loss of Ground Protection

In case of loss of the module ground and the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pins.

In case of loss of device ground, it's recommended to use input resistors between the microcontroller and the BTS5120-2EKA to ensure switching OFF of channels.

In case of loss of module or device ground, a current ( $I_{OUT(GND)}$ ) can flow out of the DMOS. **Figure 14** sketches the situation.

$Z_{GND}$  can be either resistor or diode.



**Figure 14** Loss of Ground Protection with External Components

### 6.2 Undervoltage Protection

Between  $V_{S(UV)}$  and  $V_{S(OP)}$ , the undervoltage mechanism is triggered.  $V_{S(OP)}$  represents the minimum voltage where the switching ON and OFF can take place.  $V_{S(UV)}$  represents the minimum voltage the switch can hold ON. If the supply voltage is below the undervoltage mechanism  $V_{S(UV)}$ , the device is OFF (turns OFF). As soon as the supply voltage is above the undervoltage mechanism  $V_{S(OP)}$ , then the device can be switched ON. When the switch is ON, protection functions are operational. Nevertheless, the diagnosis is not guaranteed until  $V_S$  is in the  $V_{NOM}$  range. **Figure 15** sketches the undervoltage mechanism.

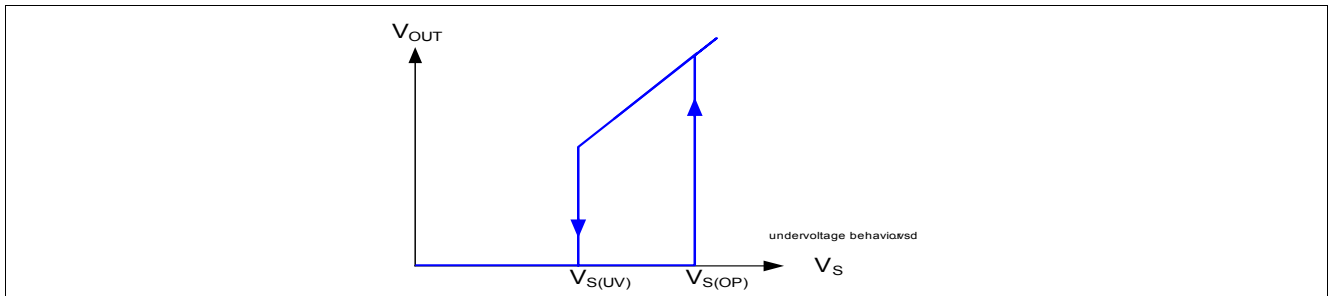


Figure 15 Undervoltage Behavior

### 6.3 Overvoltage Protection

There is an integrated clamp mechanism for overvoltage protection ( $Z_{D(AZ)}$ ). To guarantee this mechanism operates properly in the application, the current in the Zener diode has to be limited by a ground resistor. **Figure 16** shows a typical application to withstand overvoltage issues. In case of supply voltage higher than  $V_{S(AZ)}$ , the power transistor switches ON and the voltage across the logic section is clamped. As a result, the internal ground potential rises to  $V_S - V_{S(AZ)}$ . Due to the ESD Zener diodes, the potential at pin INx, DSEL and DEN rises almost to that potential, depending on the impedance of the connected circuitry. In the case the device was ON, prior to overvoltage, the BTS5120-2EKA remains ON. In the case the BTS5120-2EKA was OFF, prior to overvoltage, the power transistor can be activated. In the case the supply voltage is in above  $V_{BAT(SC)}$  and below  $V_{DS(AZ)}$ , the output transistor is still operational and follows the input. If at least one channel is in the ON state, parameters are no longer guaranteed and lifetime is reduced compared to the nominal supply voltage range. This especially impacts the short circuit robustness, as well as the maximum energy  $E_{AS}$  capability.  $Z_{GND}$  as a resistor (150  $\Omega$ ) will offer superior results compared to a diode and resistor (1 k $\Omega$ ).

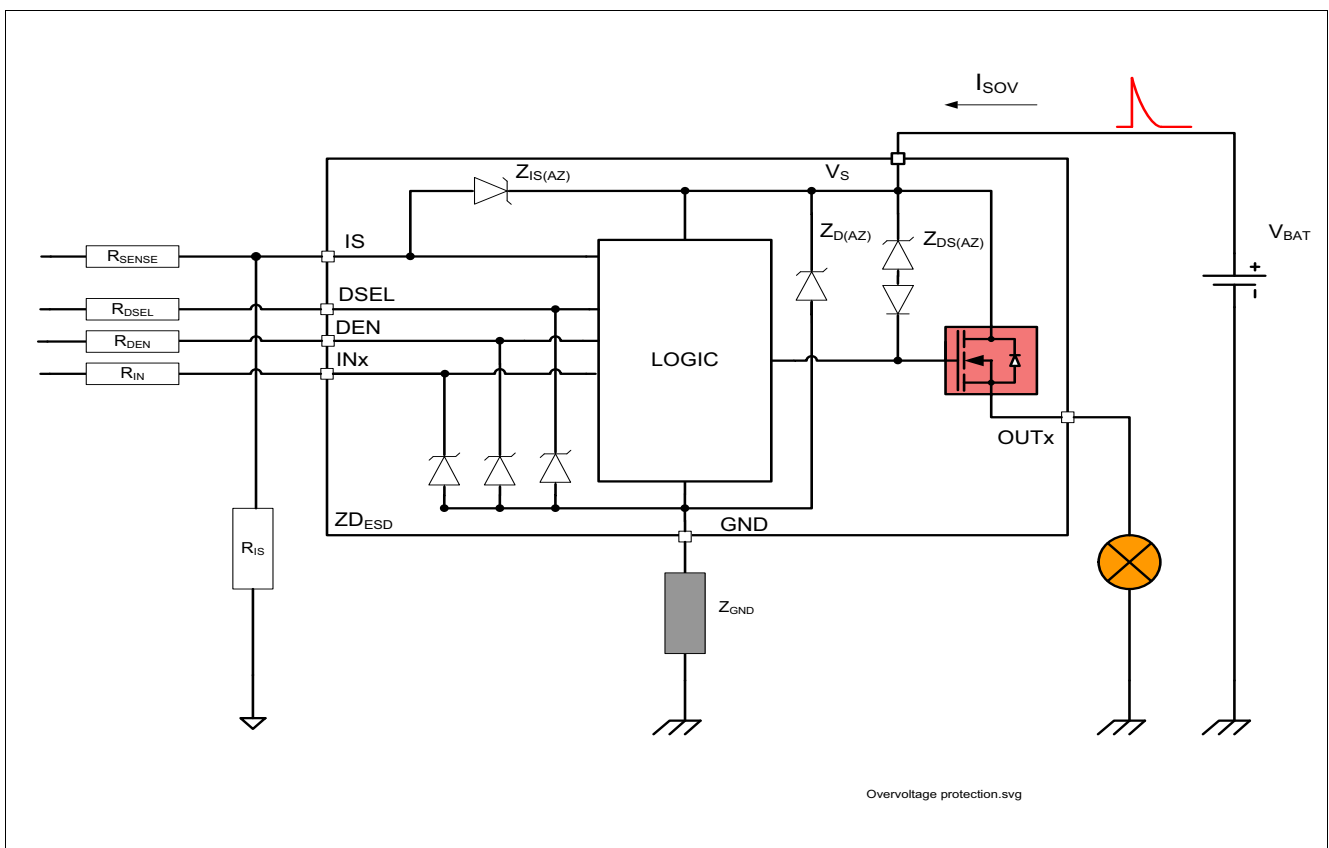


Figure 16 Overvoltage Protection with External Components

### 6.4 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diodes of the power DMOS causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Additionally, the current into the ground path and the logic pins has to be limited to the maximum current described in Chapter 4.1 with an external resistor. Figure 17 shows a typical application.  $R_{GND}$  resistor is used to limit the current in the Zener protection of the device. Resistors  $R_{DSEL}$ ,  $R_{DEN}$ , and  $R_{IN}$  are used to limit the current in the logic of the device and in the ESD protection stage.  $R_{SENSE}$  is used to limit the current in the sense transistor which behaves as a diode. The recommended value for  $R_{DEN} = R_{DSEL} = R_{IN} = R_{SENSE} = 4.7\text{ k}\Omega$ .  $Z_{GND}$  can be either a  $150\ \Omega$  resistor or Schottky diode with  $1\text{ k}\Omega$  resistor in parallel.

In case the overvoltage is not considered in the application,  $R_{GND}$  can be replaced by a Schottky diode and  $1\text{ k}\Omega$  resistor in parallel. Optionally a capacitor in parallel is recommended for EMC reasons.

During reverse polarity, no protection functions are available.

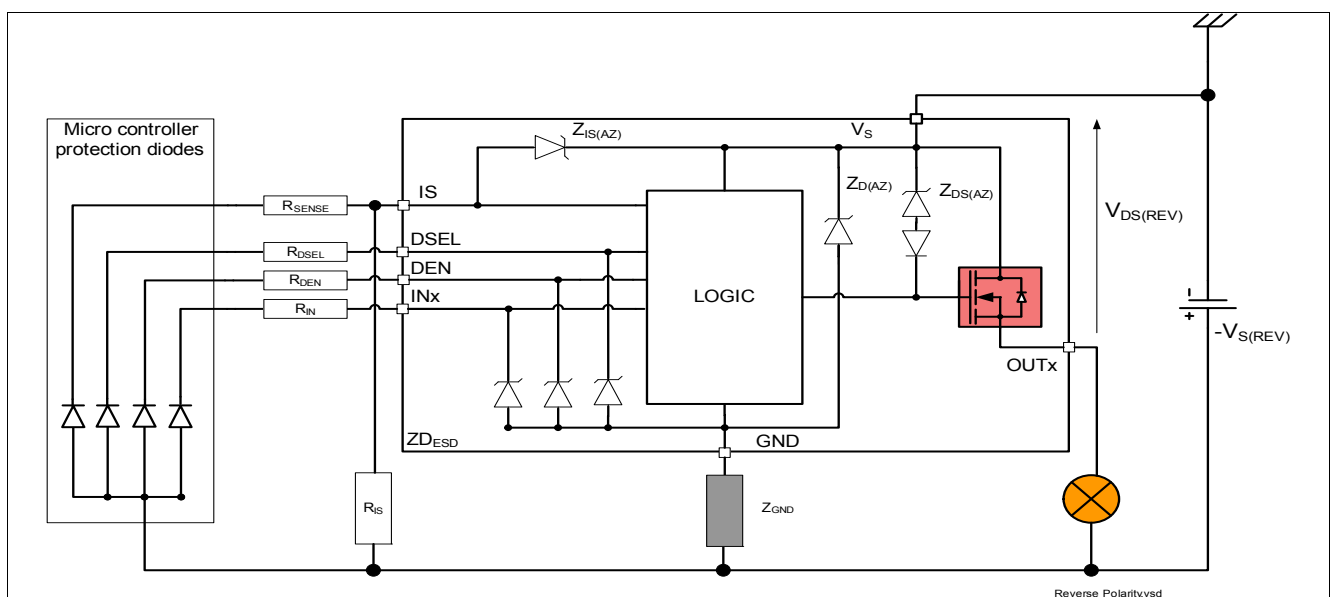


Figure 17 Reverse Polarity Protection with External Components

### 6.5 Overload Protection

In case of overload, such as high inrush of cold lamp filament, or short circuit to ground, the BTS5120-2EKA offers several protection mechanisms.

#### 6.5.1 Current Limitation

At first step, the instantaneous power in the switch is maintained at a safe value by limiting the current to the maximum current allowed in the switch  $I_{L(SC)}$ . During this time, the DMOS temperature is increasing, which affects the current flowing in the DMOS. The current limitation value is  $V_{DS}$  dependent. Figure 18 shows the behavior of the current limitation as a function of the drain to source voltage.



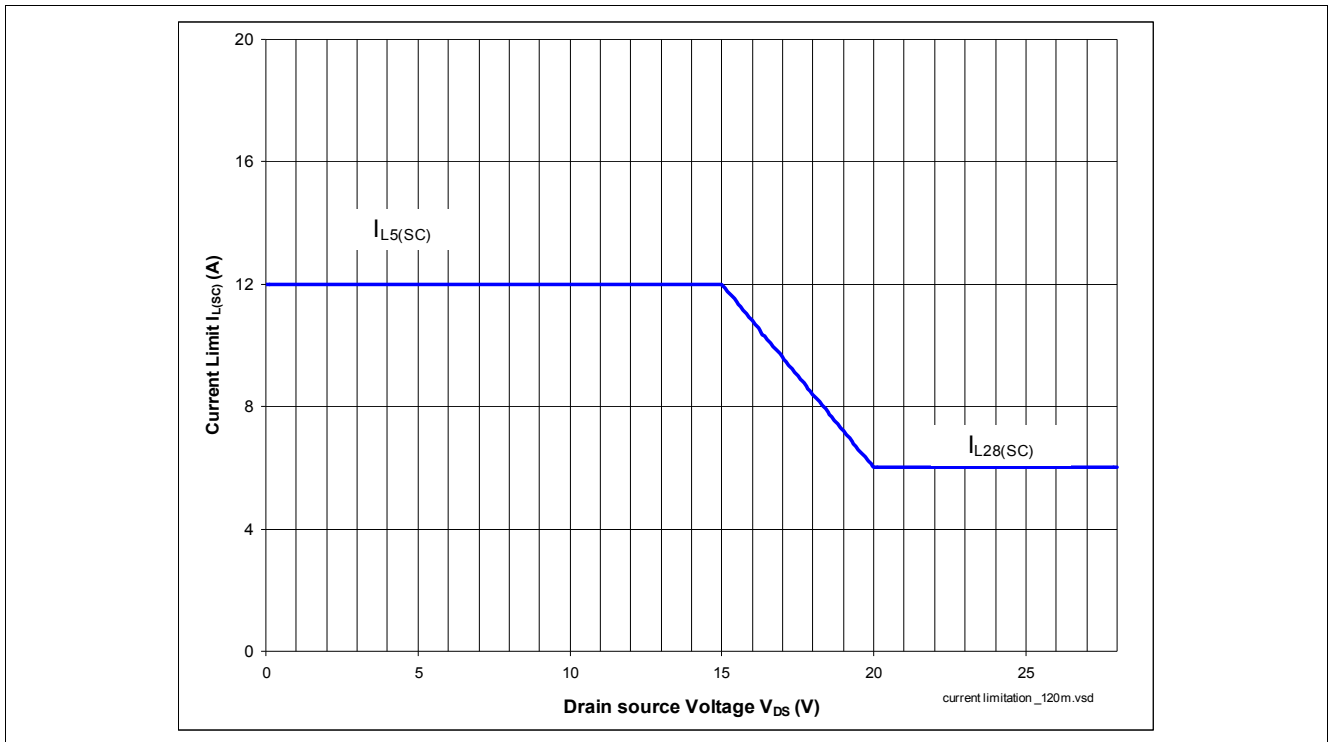
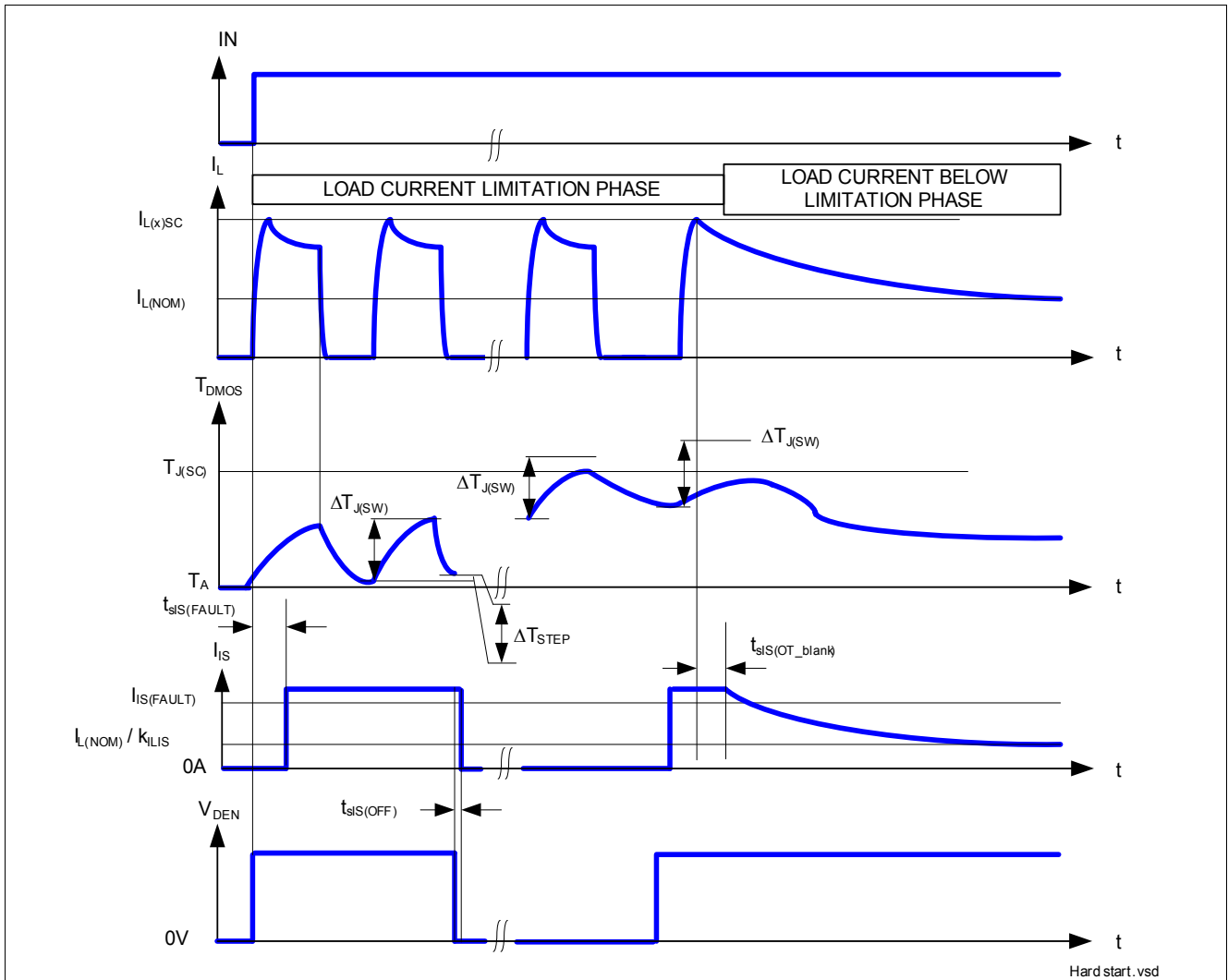


Figure 18 Current Limitation (typical behavior)

### 6.5.2 Temperature Limitation in the Power DMOS

Each channel incorporates both an absolute ( $T_{J(SC)}$ ) and a dynamic ( $T_{J(SW)}$ ) temperature sensor. Activation of either sensor will cause an overheated channel to switch OFF to prevent destruction. Any protective switch OFF latches the output until the temperature has reached an acceptable value. **Figure 19** gives a sketch of the situation. The  $\Delta T_{STEP}$  describes the device's warming, due to the overcurrent in the channel.

A retry strategy is implemented such that when the DMOS temperature has cooled down enough, the switch is switched ON again, if the IN pin signal is still high (restart behavior).



**Figure 19 Overload Protection**

*Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.*

### 6.5.3 Short Circuit Appearance with Channel in Parallel

The two channels are not synchronized in the restart event. When the two channels are in temperature limitation, the channel which has cooled down the fastest doesn't wait for the second one to be cooled down as well to restart. Thus, it is not recommended to use the device with channels in parallel.