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PROFET™+ 12V

BTS5200-4EKA

Smart High-Side Power Switch
Quad Channel, 200mΩ

Data Sheet

PROFET™+ 12V
Rev. 1.0, 2014-02-06

Automotive Power

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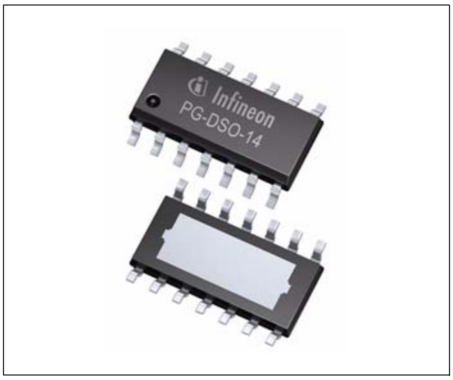
Smart High-Side Power Switch

BTS5200-4EKA

1 Overview



PG-DSO-14-48-EP

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps

Basic Features

- Quad channel device
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Logic ground independent from load ground
- Very low power DMOS leakage current in OFF state
- Green product (RoHS compliant)
- AEC qualified

Description

The BTS5200-4EKA is a 200 mΩ quad channel Smart High-Side Power Switch, embedded in a PG-DSO-14-48-EP, Exposed Pad package, providing protective functions and diagnosis. The power transistor is built by an N-channel vertical power MOSFET with charge pump. The device is integrated in Smart6 technology. It is specially designed to drive lamps up to R5W, as well as LEDs in the harsh automotive environment.

Table 1 Product Summary

Parameter	Symbol	Value
Operating voltage range	$V_{S(OP)}$	5 V ... 28 V
Maximum supply voltage	$V_{S(LD)}$	41 V
Maximum ON state resistance at TJ = 150 °C per channel	$R_{DS(ON)}$	400 mΩ
Nominal load current (one channel active)	$I_{L(NOM)1}$	1 A
Nominal load current (all channels active)	$I_{L(NOM)2}$	0.8 A
Typical current sense ratio	k_{ILIS}	300
Minimum current limitation	$I_{L5(SC)}$	5.6 A
Maximum standby current with load at T_J = 25 °C	$I_{S(OFF)}$	500 nA

Type	Package	Marking
BTS5200-4EKA	PG-DSO-14-48-EP	BTS5200-4EKA

Diagnostic Functions

- Proportional load current sense multiplexed for the 4 channels
- Open load detection in ON and OFF
- Short circuit to battery and ground indication
- Overtemperature switch off detection
- Stable diagnostic signal during short circuit
- Enhanced k_{ILIS} dependency with temperature and load current

Protection Functions

- Stable behavior during undervoltage
- Reverse polarity protection with external components
- Secure load turn-off during logic ground disconnection with external components
- Overtemperature protection with restart
- Overvoltage protection with external components
- Enhanced short circuit operation
- Voltage dependent current limitation

2 Block Diagram

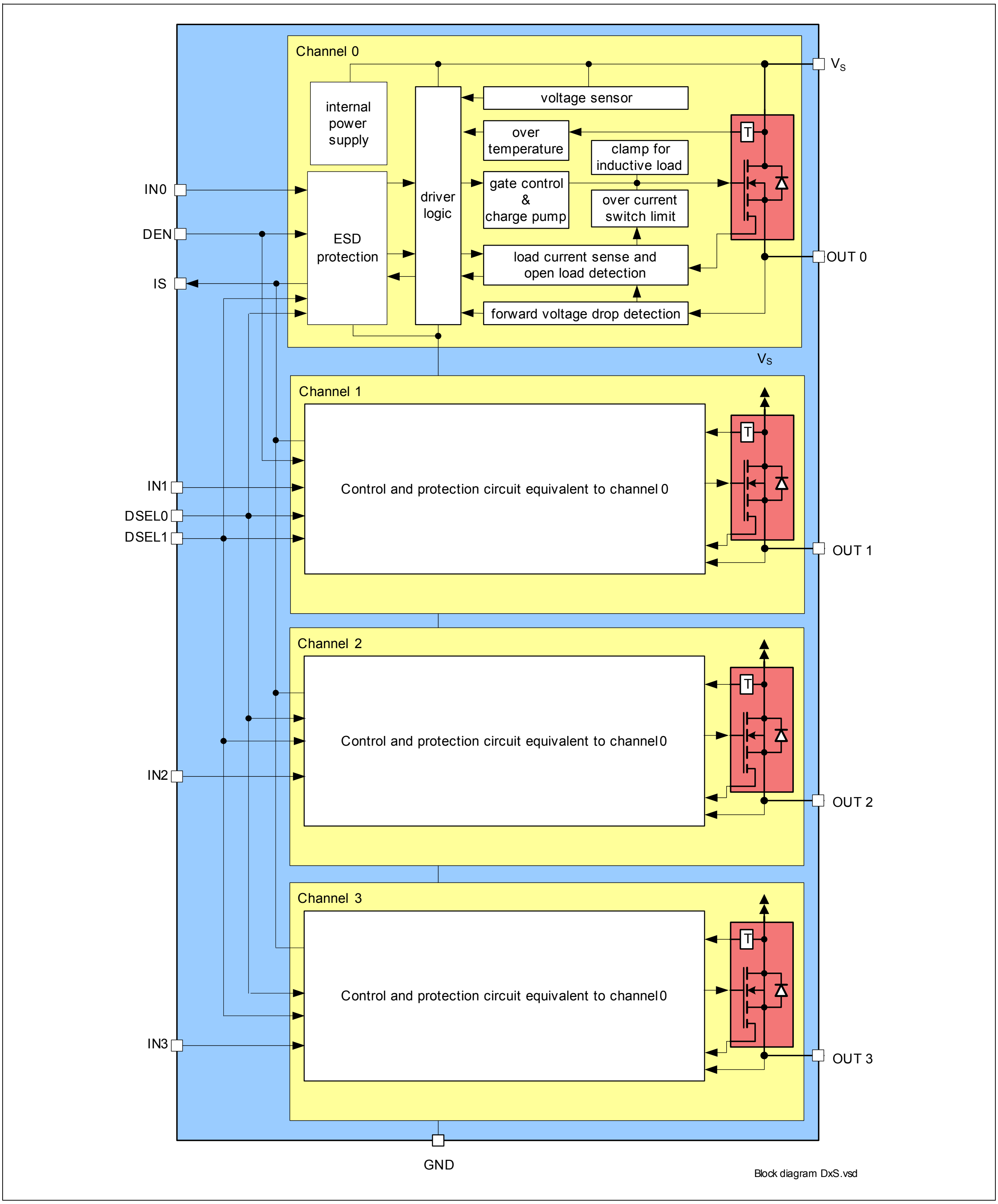


Figure 1 Block Diagram for the BTS5200-4EKA

3 Pin Configuration

3.1 Pin Assignment

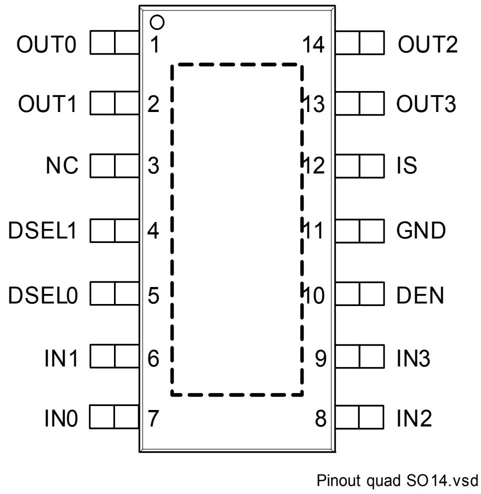


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	OUT0	**OUTput 0;** Protected high side power output channel 0[1)]
2	OUT1	**OUTput 1;** Protected high side power output channel 1 [1)]
3	NC	**Not Connected;** No internal connection to the chip
4	DSEL1	**Diagnostic SELection;** Digital signal to select the channel to be diagnosed
5	DSEL0	**Diagnostic SELection;** Digital signal to select the channel to be diagnosed
6	IN1	**INput channel 1;** Input signal for channel 1 activation
7	IN0	**INput channel 0;** Input signal for channel 0 activation
8	IN2	**INput channel 2;** Input signal for channel 2 activation
9	IN3	**INput channel 3;** Input signal for channel 3 activation
10	DEN	**Diagnostic ENable;** Digital signal to enable/disable the diagnosis of the device
11	GND	**GrouND;** Ground connection
12	IS	**Sense;** Sense current of the selected channel
13	OUT3	**OUTput 3;** Protected high side power output channel 3 [1)]
14	OUT2	**OUTput 2;** Protected high side power output channel 2 [1)]
Cooling Tab	V_S	**Voltage Supply;** Battery voltage

1) All PCB traces that are connected to the ouput pin have to be designed to withstand the maximum current which can flow.

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

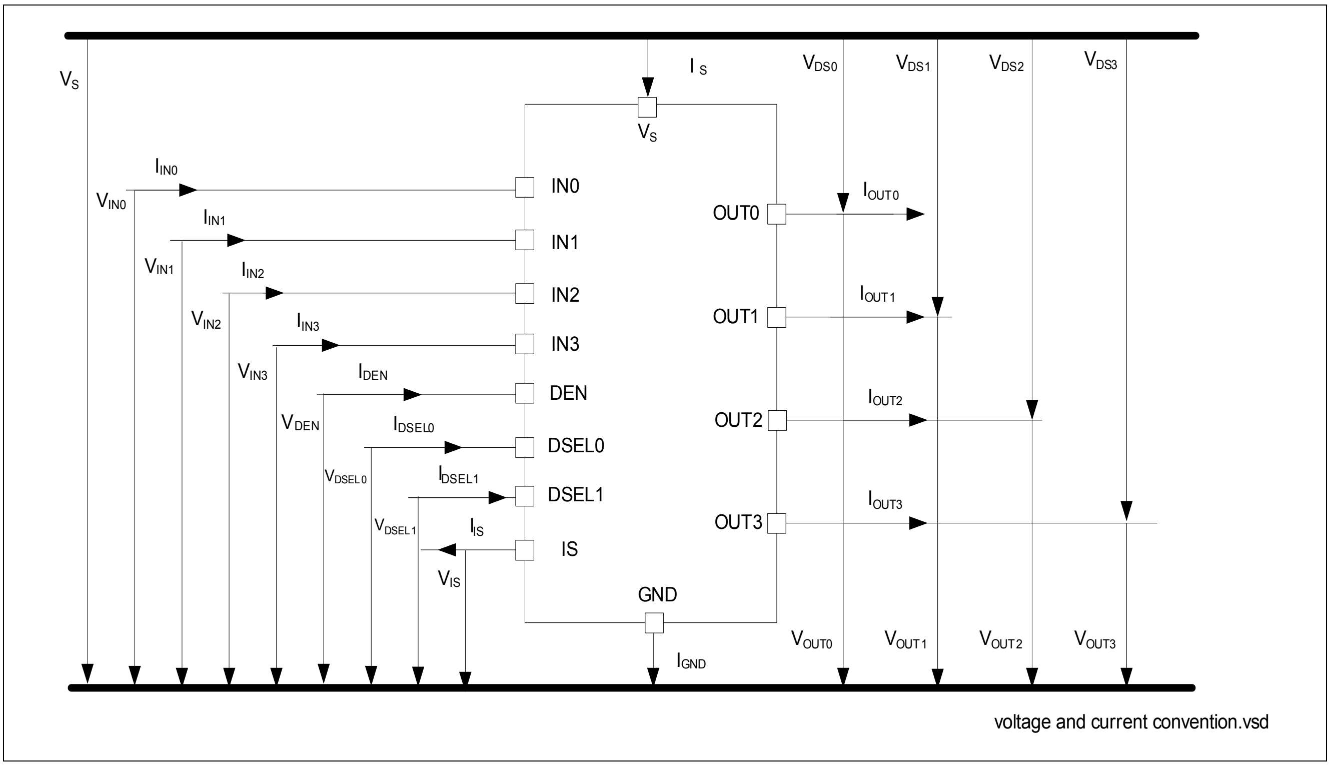


Figure 3 Voltage and Current Definition

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_J = -40°C to 150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply voltage	V_S	-0.3	–	28	V	–	P_4.1.1
Reverse polarity voltage	$-V_{S(REV)}$	0	–	16	V	t < 2 min T_A = 25 °C R_L ≥ 25 Ω R_{GND} = 150 Ω	P_4.1.2
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0	–	24	V	[2)] R_{ECU} = 20 mΩ R_{Cable} = 16 mΩ/m L_{Cable} = 1 µH/m, l = 0 or 5 m See **Chapter 6** and **Figure 28**	P_4.1.3
Supply voltage for Load dump protection	$V_{S(LD)}$	–	–	41	V	[3)] R_I = 2 Ω R_L = 25 Ω	P_4.1.12
Short Circuit Capability							
Permanent short circuit IN pin toggles	n_{RSC1}	–	–	100	k cycles	[4)] t_{ON} = 300ms	P_4.1.4
Input Pins							
Voltage at INPUT pins	V_{IN}	-0.3 –	–	6 7	V	– t < 2 min	P_4.1.13
Current through INPUT pins	I_{IN}	-2	–	2	mA	–	P_4.1.14
Voltage at DEN pin	V_{DEN}	-0.3 –	–	6 7	V	– t < 2 min	P_4.1.15
Current through DEN pin	I_{DEN}	-2	–	2	mA	–	P_4.1.16
Voltage at DSEL pin	V_{DSEL}	-0.3 –	–	6 7	V	– t < 2 min	P_4.1.17
Current through DSEL pin	I_{DSEL}	-2	–	2	mA	–	P_4.1.18
Sense Pin							
Voltage at IS pin	V_{IS}	-0.3	–	V_S	V	–	P_4.1.19
Current through IS pin	I_{IS}	-25	–	50	mA	–	P_4.1.20
Power Stage							
Load current	$\|I_L\|$	–	–	$I_{L(LIM)}$	A	–	P_4.1.21
Power dissipation (DC)	P_{TOT}	–	–	1.4	W	T_A = 85 °C T_J < 150 °C	P_4.1.22

Table 2 Absolute Maximum Ratings (cont'd)[1]

T_J = -40°C to 150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Maximum energy dissipation Single pulse (one channel)	E_{AS}	–	–	50	mJ	$I_{L(0)}$ = 0.5 A $T_{J(0)}$ = 150 °C V_S = 13.5 V	P_4.1.23
Maximum Energy dissipation repetitive pulse	E_{AR}	–	–	20	mJ	1Mio cycles T_A < 105 °C V_S = 13.5 V $I_{L(0)}$ = 350 mA	P_4.1.25
Voltage at power transistor	V_{DS}	–	–	41	V	–	P_4.1.26
Currents							
Current through ground pin	I_{GND}	-10 -150	–	10 20	mA	– t < 2 min	P_4.1.27
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	P_4.1.28
Storage temperature	T_{STG}	-55	–	150	°C	–	P_4.1.30
ESD Susceptibility							
ESD susceptibility (all pins)	V_{ESD}	-2	–	2	kV	[5] HBM	P_4.1.31
ESD susceptibility OUT Pin vs. GND and V_S connected	V_{ESD}	-4	–	4	kV	[5] HBM	P_4.1.32
ESD susceptibility	V_{ESD}	-500	–	500	V	[6] CDM	P_4.1.33
ESD susceptibility pin (corner pins)	V_{ESD}	-750	–	750	V	[6] CDM	P_4.1.34

1) Not subject to production test. Specified by design.
2) Hardware set-up in accordance to AEC Q100-012 and AEC Q101-006.
3) $V_{S(LD)}$ is setup without the DUT connected to the generator per ISO 7637-1.
4) EOL tests according to AECQ100-012. Threshold limit for short circuit failures: 100 ppm. Please refer to the legal disclaimer for short-circuit capability at the end of this document.
5) ESD susceptibility HBM according to ANSI/ESDA/JEDEC JS-001
6) "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 3 Functional Range T_J = -40°C to 150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	V_{NOM}	8	13.5	18	V	–	P_4.2.1
Extended operating voltage	$V_{S(OP)}$	5	–	28	V	2) V_{IN} = 4.5 V R_L = 25 Ω V_{DS} < 0.5 V	P_4.2.2
Minimum functional supply voltage	$V_{S(OP)\_MIN}$	3.5	4.3	5	V	1) V_{IN} = 4.5 V R_L = 25 Ω From I_{OUT} = 0 A to V_{DS} < 0.5 V;	P_4.2.3
Undervoltage shutdown	$V_{S(UV)}$	2.6	3.5	4.1	V	1) V_{IN} = 4.5 V V_{DEN} = 0 V R_L = 25 Ω From V_{DS} < 1 V; to IOUT = 0 A See Chapter 9.1	P_4.2.4
Undervoltage shutdown hysteresis	$V_{S(UV)\_HYS}$	–	850	–	mV	2) –	P_4.2.13
Operating current All channels active	I_{GND_4}	–	4	11	mA	V_{IN} = 5.5 V V_{DEN} = 5.5 V Device in $R_{DS(ON)}$ V_S = 18 V See Chapter 9.1	P_4.2.6
Standby current for whole device with load (ambiente)	$I_{S(OFF)}$	–	0.1	0.5	µA	1) V_S = 18 V V_{OUT} = 0 V V_{IN} floating V_{DEN} floating $T_J \leq$ 85 °C	P_4.2.7
Maximum standby current for whole device with load	$I_{S(OFF)\_150}$	–	–	10	µA	V_S = 18 V V_{OUT} = 0 V V_{IN} floating V_{DEN} floating T_J = 150 °C	P_4.2.10
Standby current for whole device with load, diagnostic active	$I_{S(OFF\_DEN)}$	–	1.2	–	mA	2) V_S = 18 V V_{OUT} = 0 V V_{IN} floating V_{DEN} = 5.5 V	P_4.2.8

1) Test at T_J = -40°C only
2) Not subject to production test. Specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to soldering point	R_{thJS}	–	5	–	K/W	[1]	P_4.3.1
Junction to ambient All channels active	R_{thJA}	–	40	–	K/W	[1][2]	P_4.3.2

1) Not subject to production test. Specified by design.

2) Specified R_{thja} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacts the first inner copper layer. Please refer to **Figure 4**.

4.3.1 PCB set up

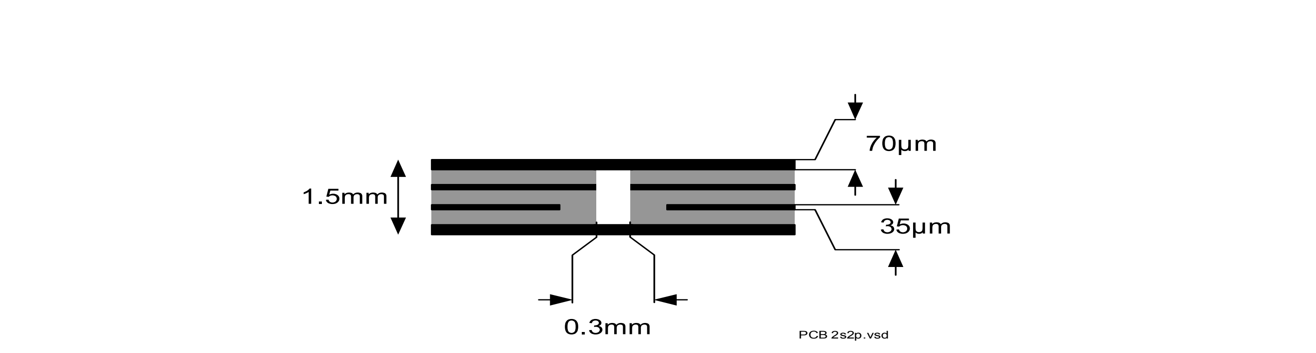


Figure 4 2s2p PCB Cross Section

4.3.2 Thermal Impedence

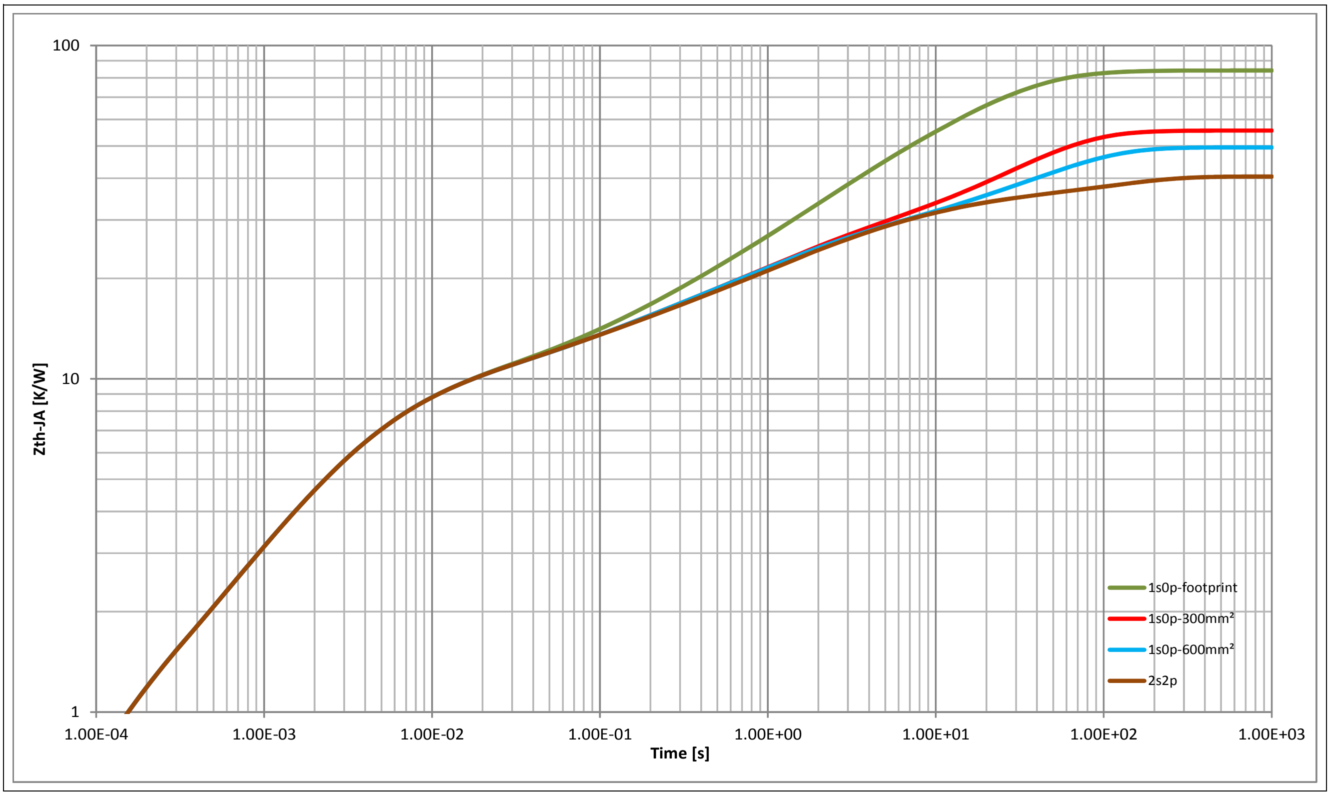


Figure 5 Typical Thermal Impedance. 2s2p PCB set up according Figure 4

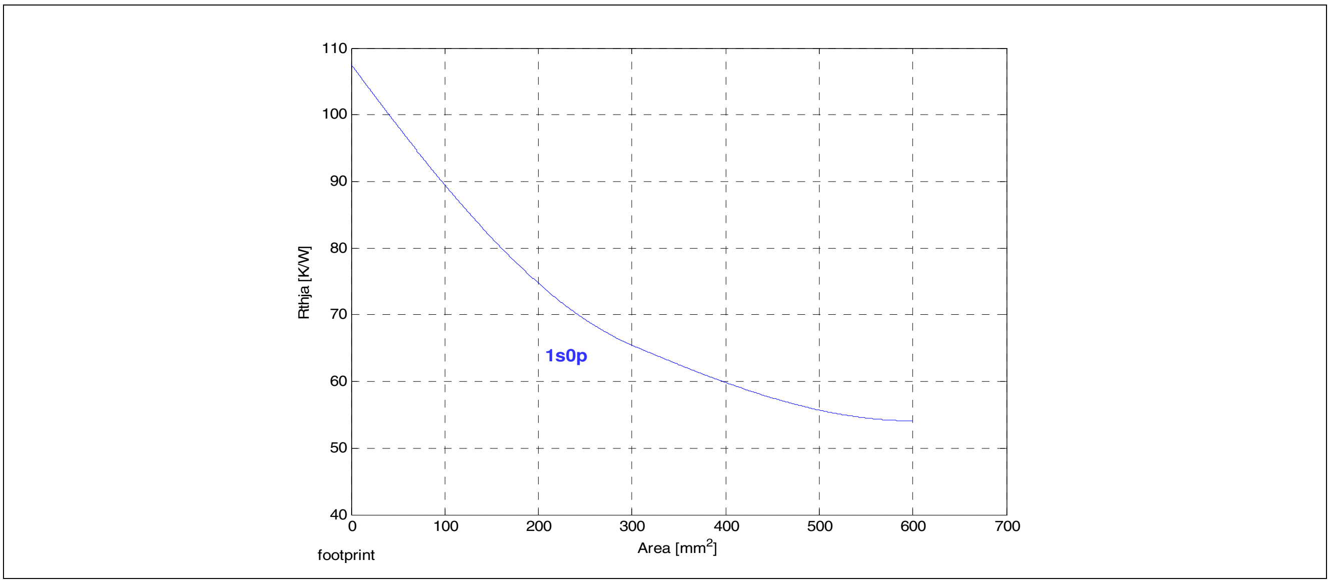


Figure 6 Typical Thermal Resistance. PCB set-up 1s0p

5 Power Stage

The power stages are built using an N-channel vertical power MOSFET (DMOS) with charge pump.

5.1 Output ON-state Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J. **Figure 7** shows the dependencies in terms of temperature and supply voltage for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 6.4**.

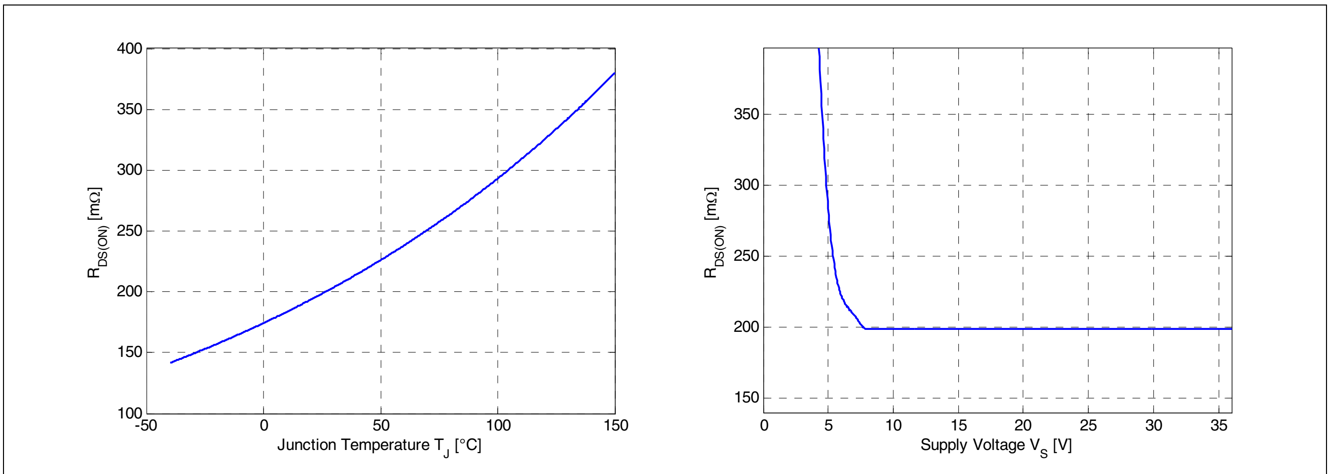


Figure 7 Typical ON-state Resistance

A high signal at the input pin (see **Chapter 8**) causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.2 Turn ON/OFF Characteristics with Resistive Load

Figure 8 shows the typical timing when switching a resistive load.

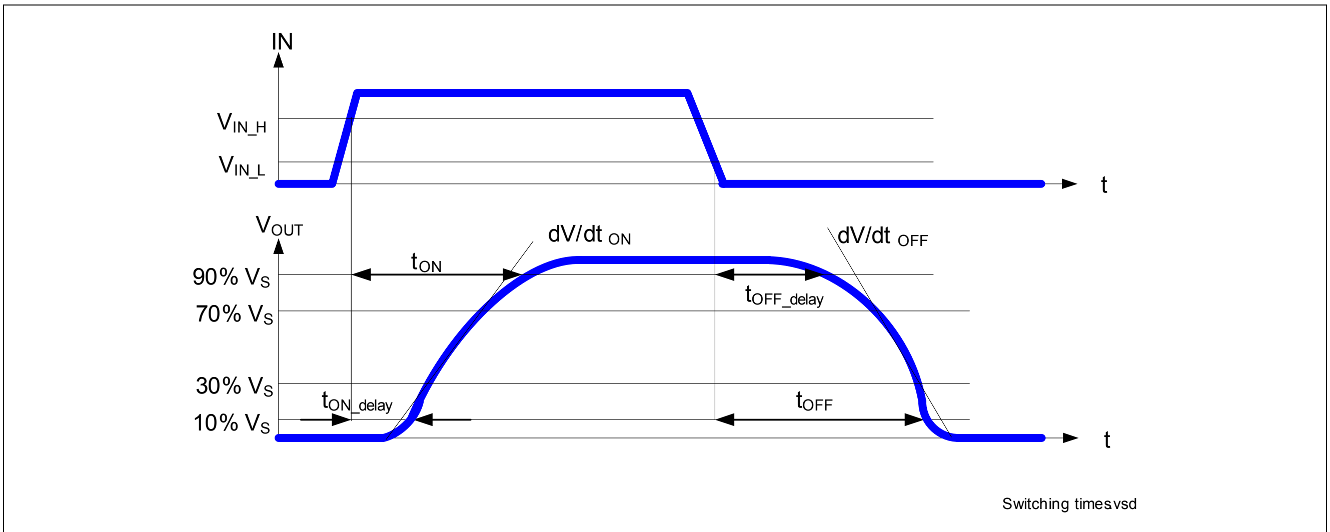


Figure 8 Switching a Resistive Load Timing

5.3 Inductive Load

5.3.1 Output Clamping

When switching OFF inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltages, there is a voltage clamp mechanism $Z_{DS(AZ)}$ implemented that limits negative output voltage to a certain level (V_S - $V_{DS(AZ)}$). Please refer to **Figure 9** and **Figure 10** for details. Nevertheless, the maximum allowed load inductance is limited.

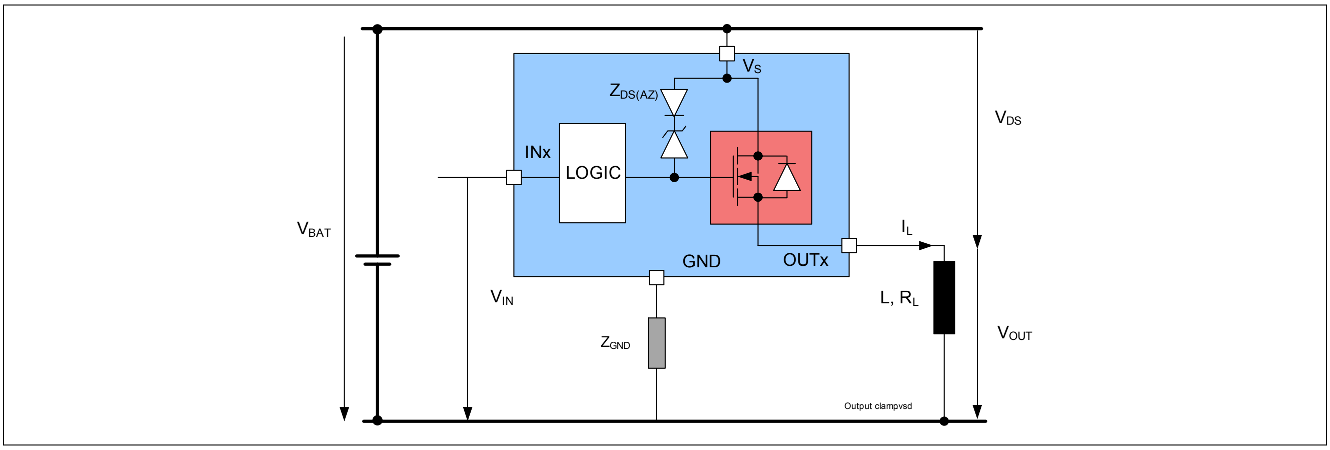


Figure 9 Output Clamp

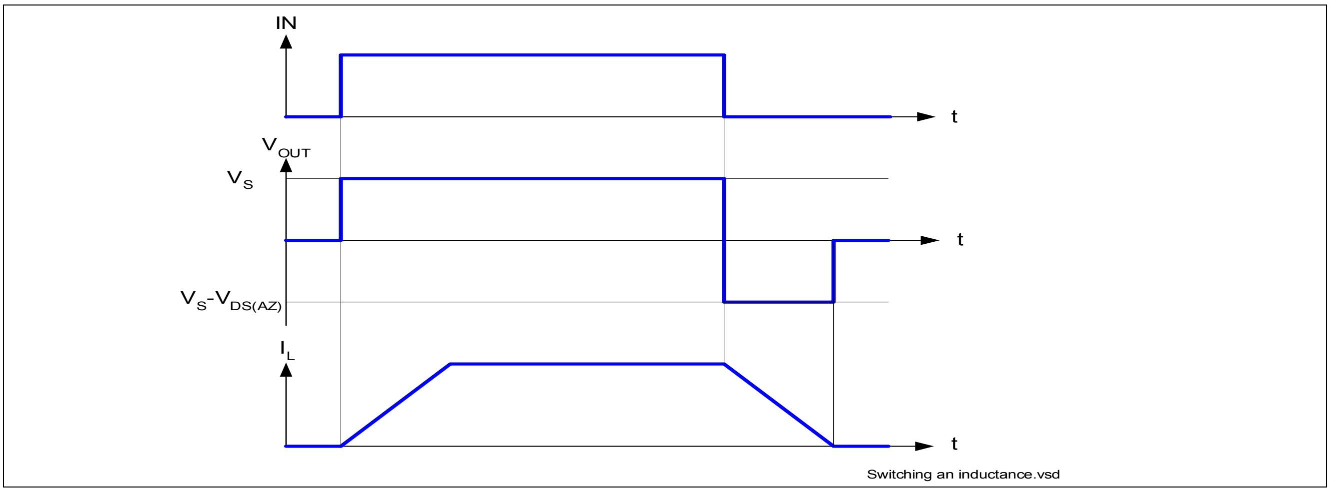


Figure 10 Switching an Inductive Load Timing

5.3.2 Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the BTS5200-4EKA. This energy can be calculated with following equation:

$$E = V_{DS(AZ)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{DS(AZ)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(AZ)}}\right) + I_L\right] \quad (1)$$

Following equation simplifies under the assumption of R_L = 0 Ω.

$$E = \frac{1}{2} \times L \times I^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(AZ)}}\right) \tag{2}$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 11** for the maximum allowed energy dissipation as a function of the load current.

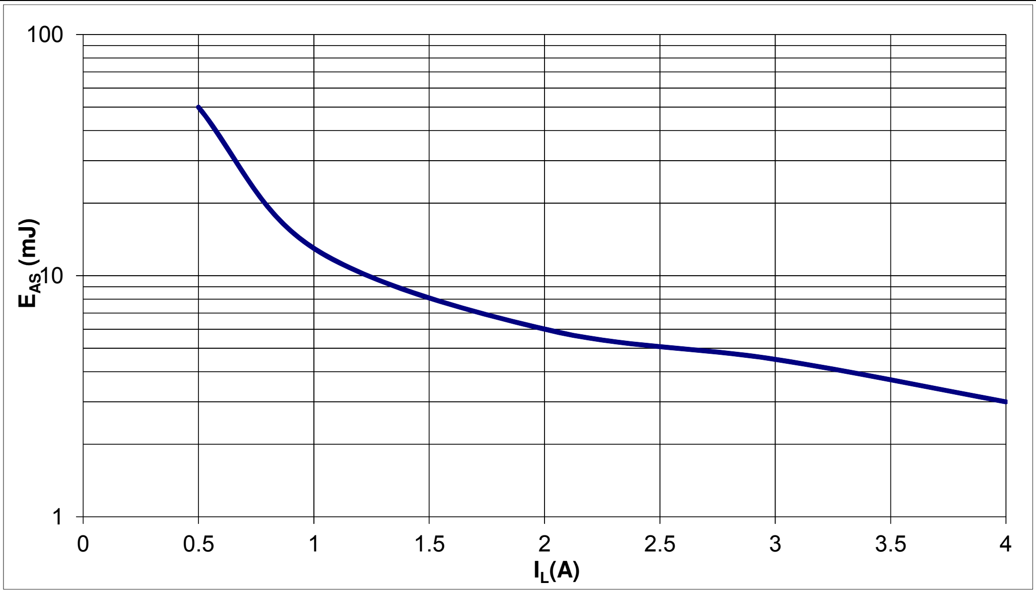


Figure 11 Maximum Energy Dissipation Single Pulse, T_{J_START} = 150 °C; V_S = 13.5V

5.4 Inverse Current Capability

In case of inverse current, meaning a voltage V_{INV} at the OUTput higher than the supply voltage V_S, a current I_{INV} will flow from output to V_S pin via the body diode of the power transistor (please refer to **Figure 12**). The output stage follows the state of the IN pin, except if the IN pin goes from OFF to ON during inverse. In that particular case, the output stage is kept OFF until the inverse current disappears. Nevertheless, the current I_{INV} should not be higher than $I_{L(INV)}$. If the channel is OFF, the diagnostic will detect an open load at OFF. If the affected channel is ON, the diagnostic will detect open load at ON (the overtemperature signal is inhibited). At the appearance of V_{INV}, a parasitic diagnostic can be observed. After, the diagnosis is valid and reflects the output state. At V_{INV} vanishing, the diagnosis is valid and reflects the output state. During inverse current, no protection functions are available.

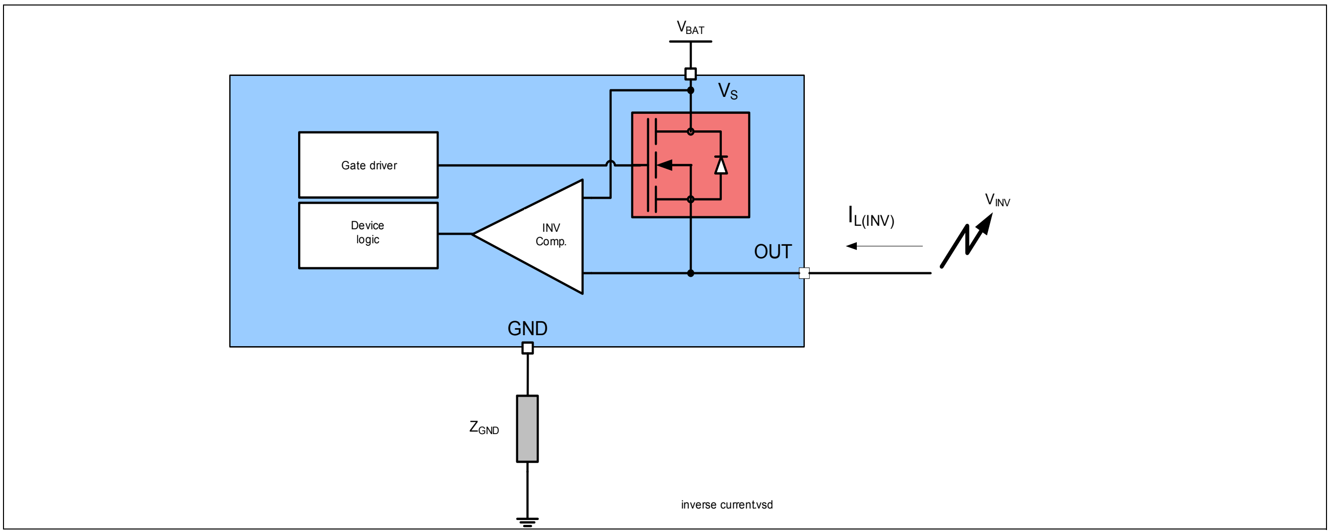


Figure 12 Inverse Current Circuitry

5.5 Electrical Characteristics Power Stage

Table 5 Electrical Characteristics: Power Stage

V_S = 8 V to 18 V, T_J = -40°C to 150°C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
ON-state resistance per channel	$R_{DS(ON)\_150}$	300	360	400	mΩ	$I_L = I_{L4}$ = 0.5 A V_{IN} = 4.5 V T_J = 150 °C See **Figure 7**	P_5.5.1
ON-state resistance per channel	$R_{DS(ON)\_25}$	–	200	–	mΩ	[1] T_J = 25 °C	P_5.5.21
Nominal load current One channel active	$I_{L(NOM)1}$	–	1	–	A	[1] T_A=85 °C T_J < 150 °C	P_5.5.2
Nominal load current All channels active	$I_{L(NOM)2}$	–	0.8	–	A		P_5.5.3
Output voltage drop limitation at small load currents	$V_{DS(NL)}$	–	10	25	mV	$I_L = I_{L0}$ = 25 mA See **Chapter 9.3**	P_5.5.4
Drain to source clamping voltage $V_{DS(AZ)} = [V_S - V_{OUT}]$	$V_{DS(AZ)}$	41	47	53	V	I_{DS} = 20 mA See **Figure 10** See **Chapter 9.1**	P_5.5.5
Output leakage current $T_J \leq$ 85 °C per channel	$I_{L(OFF)}$	–	0.1	0.5	µA	[2] V_{IN} floating V_{OUT} = 0 V $T_J \leq$ 85 °C	P_5.5.6
Output leakage current T_J = 150 °C per channel	$I_{L(OFF)\_150}$	–	–	2.5	µA	V_{IN} floating V_{OUT} = 0 V T_J = 150 °C	P_5.5.8
Inverse current capability	$I_{L(NV)}$	–	0.8	–	A	[1] $V_S < V_{OUTX}$	P_5.5.9
Slew rate 30% to 70% V_S	dV/dt_{ON}	0.1	0.25	0.5	V/µs	R_L = 25 Ω V_S = 13.5 V See **Figure 8** See **Chapter 9.1**	P_5.5.11
Slew rate 70% to 30% V_S	$-dV/dt_{OFF}$	0.1	0.25	0.5	V/µs		P_5.5.12
Slew rate matching $dV/dt_{ON} - dV/dt_{OFF}$	$\Delta dV/dt$	-0.15	0	0.15	V/µs		P_5.5.13
Turn-ON time to V_{OUT} = 90% V_S	t_{ON}	30	90	230	µs		P_5.5.14
Turn-OFF time to V_{OUT} = 10% V_S	t_{OFF}	30	90	230	µs		P_5.5.15
Turn-ON / OFF matching $t_{OFF} - t_{ON}$	Δt_{SW}	-50	5	50	µs		P_5.5.16
Turn-ON time to V_{OUT} = 10% V_S	t_{ON_delay}	10	35	100	µs		P_5.5.17
Turn-OFF time to V_{OUT} = 90% V_S	t_{OFF_delay}	10	35	100	µs		P_5.5.18

Table 5 Electrical Characteristics: Power Stage (cont'd)

V_S = 8 V to 18 V, T_J = -40°C to 150°C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Switch ON energy	E_{ON}	–	210	–	µJ	[1] R_L = 25 Ω V_{OUT} = 90% V_S V_S = 18 V See **Chapter 9.1**	P_5.5.19
Switch OFF energy	E_{OFF}	–	140	–	µJ	[1] R_L = 25 Ω V_{OUT} = 10% V_S V_S = 18 V See **Chapter 9.1**	P_5.5.20

1) Not subject to production test, specified by design.
2) Test at TJ = -40°C only

6 Protection Functions

The device provides integrated protection functions. These functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

6.1 Loss of Ground Protection

In case of loss of the module ground and the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pins.

In case of loss of device ground, it’s recommended to use input resistors between the microcontroller and the BTS5200-4EKA to ensure switching OFF of channels.

In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS. **Figure 13** sketches the situation.

Z_{GND} is recommended to be a diode in parallel to a resistor (1 kΩ).

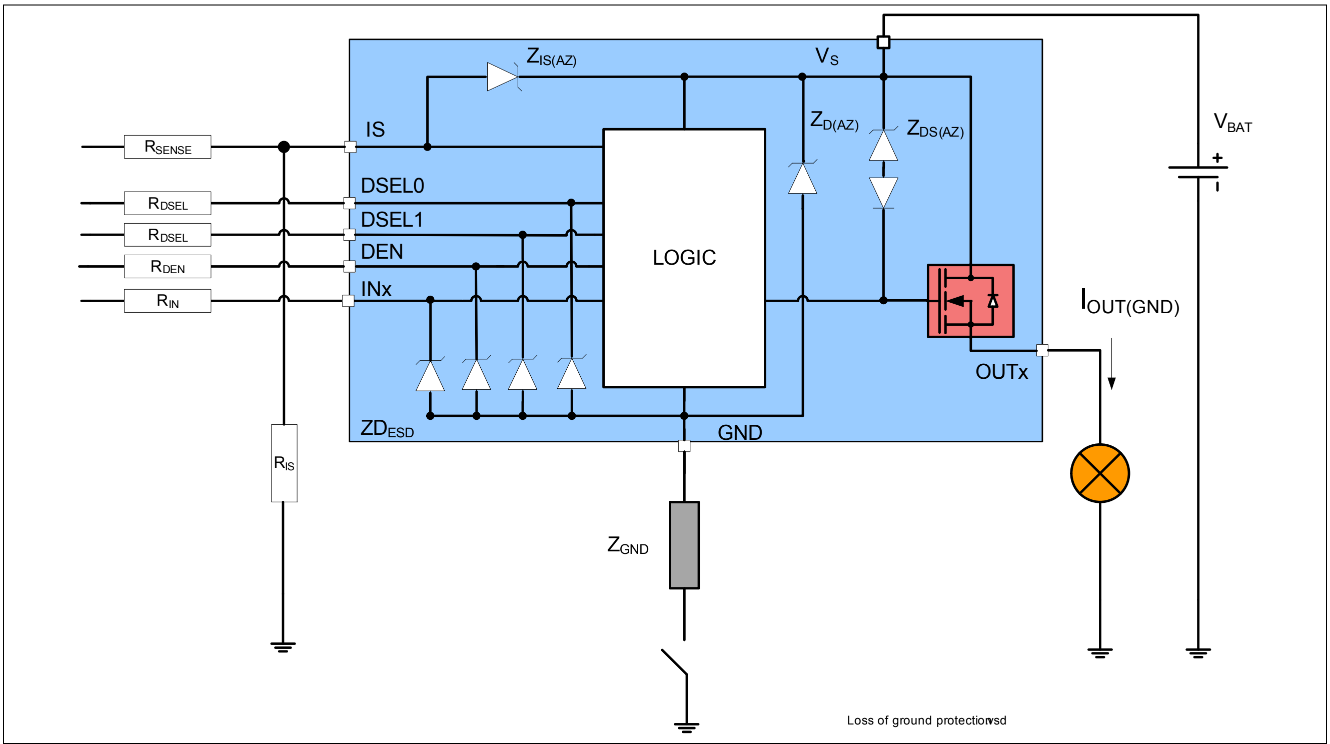


Figure 13 Loss of Ground Protection with External Components

6.2 Undervoltage Protection

Between $V_{S(UV)}$ and $V_{S(OP)}$, the undervoltage mechanism is triggered. $V_{S(OP)}$ represents the minimum voltage where the switching ON and OFF can takes place. $V_{S(UV)}$ represents the minimum voltage the switch can hold ON. If the supply voltage is below the undervoltage mechanism $V_{S(UV)}$, the device is OFF (turns OFF). As soon as the supply voltage is above the undervoltage mechanism $V_{S(OP)}$, then the device can be switched ON. When the switch is ON, protection functions are operational. Nevertheless, the diagnosis is not guaranteed until V_S is in the V_{NOM} range. **Figure 14** sketches the undervoltage mechanism.

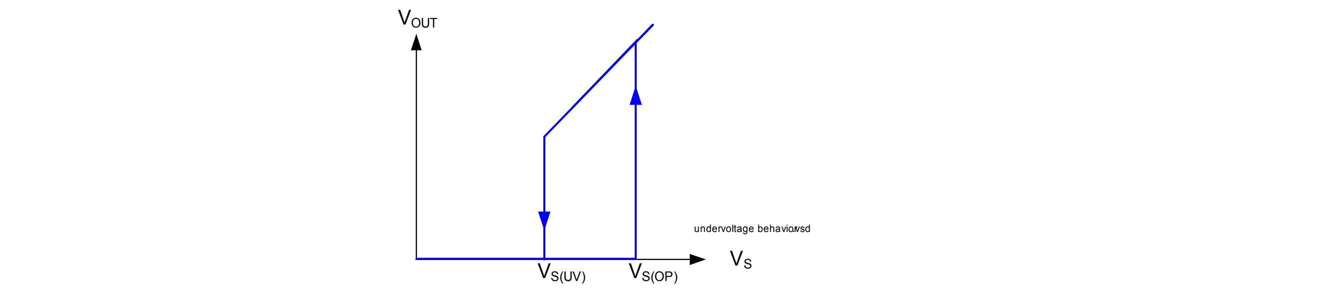


Figure 14 Undervoltage Behavior

6.3 Overvoltage Protection

There is an integrated clamp mechanism for overvoltage protection ($Z_{D(AZ)}$). To guarantee this mechanism operates properly in the application, the current in the Zener diode has to be limited by a ground resistor. **Figure 15** shows a typical application to withstand overvoltage issues. In case of supply voltage higher than $V_{S(AZ)}$, the power transistor switches ON and the voltage across the logic section is clamped. As a result, the internal ground potential rises to V_S - $V_{S(AZ)}$. Due to the ESD Zener diodes, the potential at pin INx, DSELx, and DEN rises almost to that potential, depending on the impedance of the connected circuitry. In the case the device was ON, prior to overvoltage, the BTS5200-4EKA remains ON. In the case the BTS5200-4EKA was OFF, prior to overvoltage, the power transistor can be activated. In the case the supply voltage is in above $V_{BAT(SC)}$ and below $V_{DS(AZ)}$, the output transistor is still operational and follows the input. If at least one channel is in the ON state, parameters are no longer guaranteed and lifetime is reduced compared to the nominal supply voltage range. This especially impacts the short circuit robustness, as well as the maximum energy E_{AS} capability. Z_{GND} with a resistor (27 Ω) in series to the diode will offer better results.

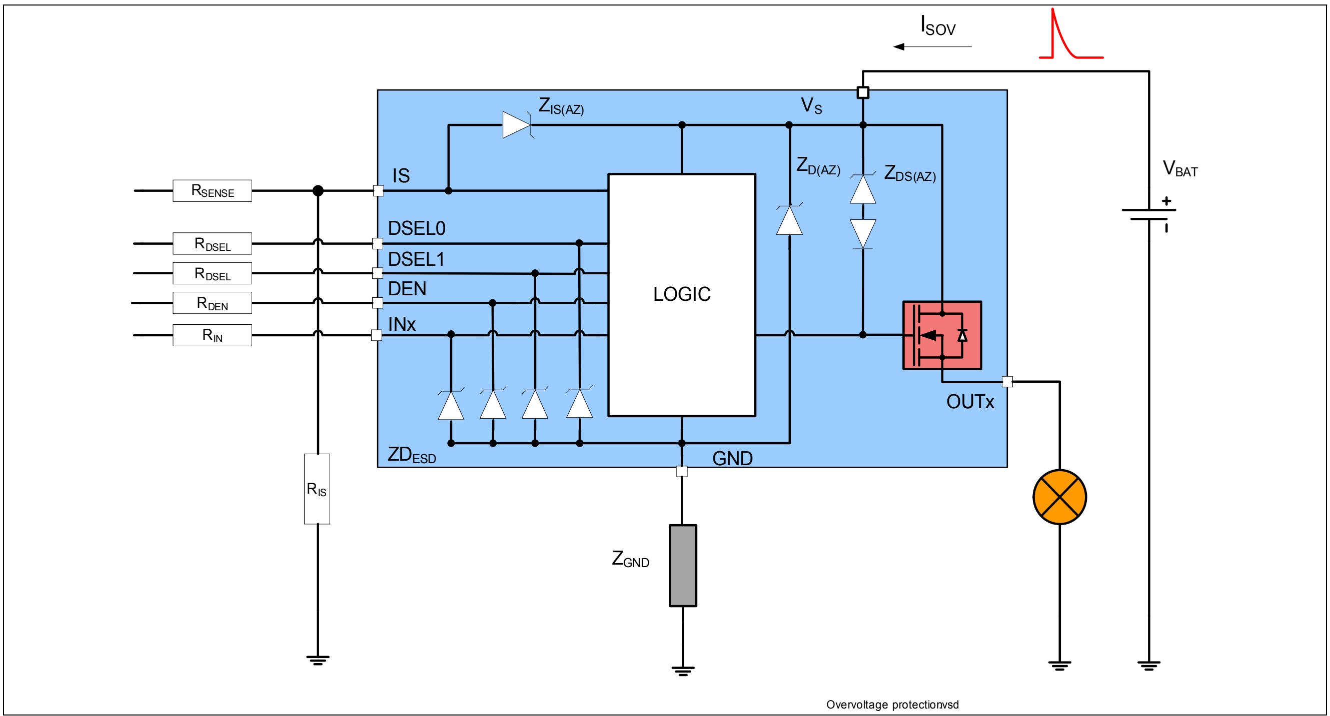


Figure 15 Overvoltage Protection with External Components

6.4 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diodes of the power DMOS causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Additionally, the current into the ground path and the logic pins has to be limited to the maximum current described in **Chapter 4.1** with an external resistor. **Figure 16** shows a typical application. R_{GND} resistor is used to limit the current in the Zener protection of the device. Resistors R_{DSEL}, R_{DEN}, and R_{IN} are used to limit the current in the logic of the device and in the ESD protection stage. R_{SENSE} is used to limit the current in the sense transistor which behaves as a diode. The recommended value for R_{DEN} = R_{DSEL} = R_{IN} = R_{SENSE} = 4.7 kΩ. Z_{GND} is recommended to be a 1 kΩ resistor in parallel to a diode.

During reverse polarity, no protection functions are available.

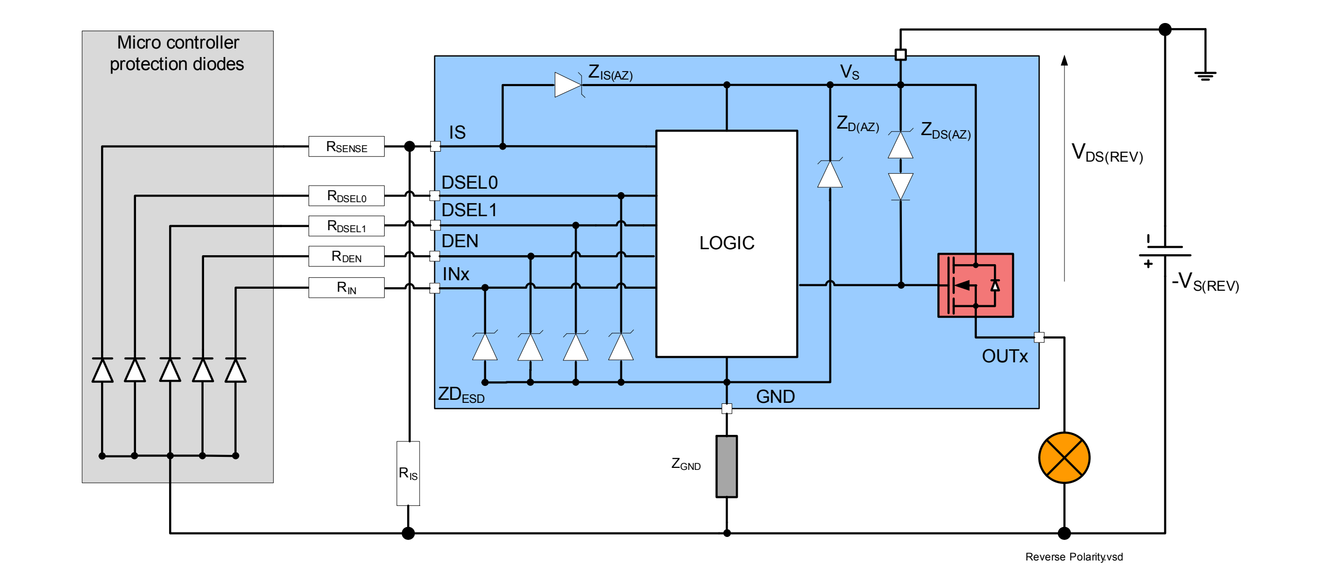


Figure 16 Reverse Polarity Protection with External Components

6.5 Overload Protection

In case of overload, such as high inrush of cold lamp filament, or short circuit to ground, the BTS5200-4EKA offers several protection mechanisms.

6.5.1 Current Limitation

At first step, the instantaneous power in the switch is maintained at a safe value by limiting the current to the maximum current allowed in the switch $I_{L(SC)}$. During this time, the DMOS temperature is increasing, which affects the current flowing in the DMOS. The current limitation value is V_{DS} dependent. **Figure 17** shows the behavior of the current limitation as a function of the drain to source voltage.

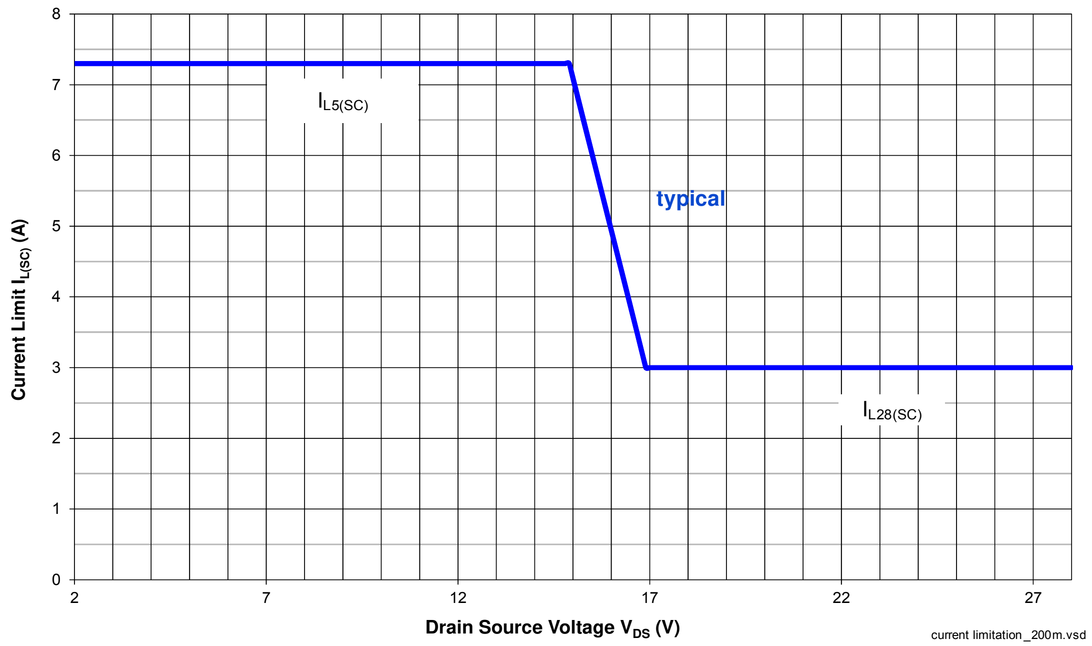


Figure 17 Current Limitation (typical behavior)

6.5.2 Temperature Limitation in the Power DMOS

Each channel incorporates an absolute ($T_{J(SC)}$) temperature sensor and a switch OFF timer that is started by an overcurrent event. The activation of these protection mechanisms will cause an overheated channel to switch OFF to prevent destruction. A temperature limitation switch OFF latches the output until the temperature has reached an acceptable value. **Figure 18** gives a sketch of the situation.

A retry strategy is implemented such that when the DMOS temperature has cooled down enough, the switch is switched ON again, if the IN pin signal is still high (restart behavior).

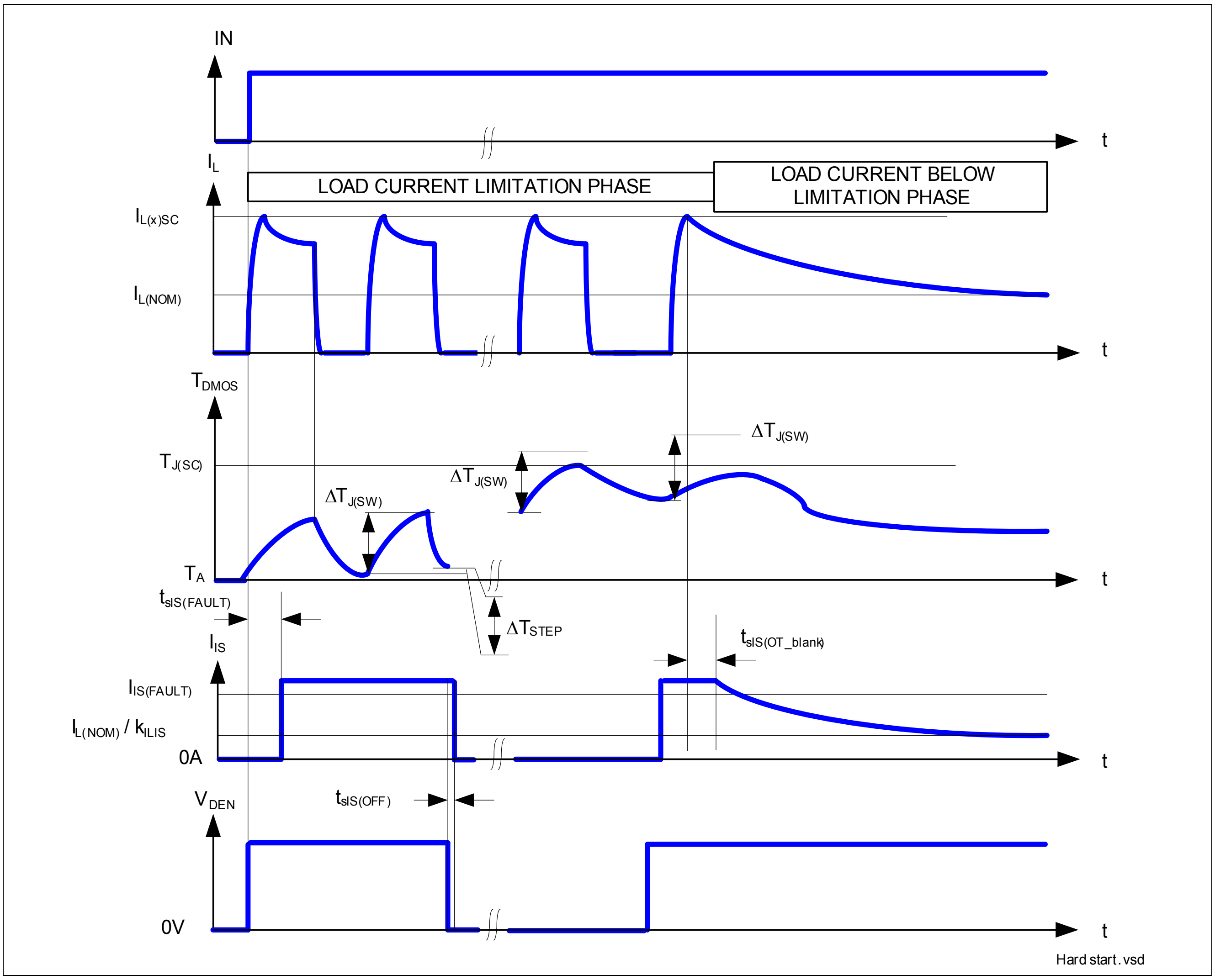


Figure 18 Overload Protection

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

6.5.3 Short Circuit Appearance with Channels in Parallel

The four channels are not synchronised in the restart event. When the channels are in temperature limitation, the channel which has cooled down the fastest doesn’t wait for the other to be cooled down as well to restart. Thus, it is not recommended to use the device with channels in parallel.

6.6 Electrical Characteristics for the Protection Functions

Table 6 Electrical Characteristics: Protection

V_S = 8 V to 18 V, T_J = -40°C to 150°C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Loss of Ground							
Output leakage current while GND disconnected	$I_{OUT(GND)}$	–	0.1	–	mA	[1][2] V_S = 28 V See **Figure 13**	P_6.6.1
Reverse Polarity							
Drain source diode voltage during reverse polarity	$V_{DS(REV)}$	200	650	700	mV	[3] I_L = - 0.5 A T_J = 150 °C See **Figure 16**	P_6.6.2
Overvoltage							
Overvoltage protection	$V_{S(AZ)}$	41	47	53	V	I_{SOV} = 5 mA See **Figure 15**	P_6.6.3
Overload Condition							
Load current limitation	$I_{L5(SC)}$	5.6	7.3	9	A	[4] V_{DS} = 5 V See **Figure 17** and **Chapter 9.3**	P_6.6.4
Load current limitation	$I_{L28(SC)}$	–	3	–	A	[2] V_{DS} = 28 V See **Figure 17** and **Chapter 9.3**	P_6.6.7
Short circuit average current after several minutes of thermal toggling	$I_{L(RMS)}$	–	1	–	A	[2] V_{IN} = 4.5 V R_{SHORT} = 100 mΩ L_{SHORT} = 5 µH	P_6.6.12
Thermal shutdown temperature	$T_{J(SC)}$	150	170	200	°C	[3] [5] See **Figure 18**	P_6.6.10
Thermal shutdown hysteresis	$\Delta T_{J(SC)}$	–	20	–	K	[2] See **Figure 18**	P_6.6.11

1) All pins are disconnected except V_S and OUT.
2) Not Subject to production test, specified by design
3) Test at TJ = +150°C only
4) Test at TJ = -40°C only
5) Functional test only