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# SPOC™+ 12V

# BTS54040-LBA

SPI Power Controller

## Data Sheet

Rev. 2.2, 2016-10-10

Automotive

| Revision History | |
|---|---|
| **Page or Item** | **Subjects (major changes since previous revision)** |
| **Rev. 2.2, 2016-10-10** | |
| All | Package name changed<br>General: Typos corrected and wording improved<br>**Table 1**: Channel description improved<br>**Table 4**: Footnote added<br>**Table 5**: Updated and Footnote added<br>**Chapter 5.1.3**: Updated<br>**Chapter 5.1.6**: Note added<br>**Chapter 5.2**: Updated<br>**Chapter 6.3**: Updated<br>**Chapter 7.2**: Updated<br>**Figure 28** updated |

| Revision History | |
|---|---|
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| All | General: Numbering of Figures and Tables changed<br>**Table 1** updated<br>**Chapter 4.2.1** added<br>**Chapter 4.2.2** added<br>Parameter P_4.1.4: number changed to P_4.1.5 and max. value improved<br>Parameter P_4.1.11: Max. Value improved<br>Parameter P_4.1.28: Max. Value improved<br>Parameter P_4.1.31: Max. Value improved<br>Parameter P_4.1.34: Max. Value improved<br>Parameter P_4.1.37: Max. Value improved<br>Parameter P_4.1.39: Min. Value improved<br>Parameter P_4.1.42: Max. Value improved<br>**Chapter 5** rewritten (content improved)<br>Parameter P_5.3.7: Max. Value improved<br>Parameter P_5.3.8: Test Condition updated and Max. Value improved<br>Parameter P_5.3.10: Max. Value improved<br>Parameter P_5.3.13: Test Condition updated<br>Parameter P_5.3.14: Max. Value improved<br>Parameter P_5.3.16: Typ. and Max. value improved<br>Parameter P_5.3.17: Typ. and Min. Value improved<br>Parameter P_5.3.23: Max. Value improved<br>**Chapter 6.1**: $R_{DS(ON)}$ graphs removed<br>**Chapter 6.1**: $R_{DS(ON)}$ variation factor added<br>**Chapter 6.4**: Description improved<br>**Figure 16**: Content updated<br>**Chapter 6.4.4**: Note added<br>**Chapter 7.1**: Content improved<br>**Chapter 7.1**: $I_{L(LIM)}$ graphs removed<br>**Chapter 7.1**: $I_{L(LIM)}$ variation factor added<br>**Chapter 7.2**: Content improved<br>**Figure 18**: Content updated<br>**Figure 19**: Content and Title updated<br>**Figure 20**: added<br>Undervoltage Behavior shifted from Chapter 7.4 to **Chapter 5.2.1**<br>**Figure 21**: Content updated<br>**Chapter 8.1**: Content improved<br>**Figure 22**: Content updated<br>**Figure 23**: Content updated<br>**Chapter 8.2.3** added<br>**Chapter 8.4**: Content improved<br>Parameter P_8.5.118 added |

| Revision History | |
|---|---|
| **Page or Item** | **Subjects (major changes since previous revision)** |
| | Parameter P_9.4.19: Test Condition updated<br>Parameter P_9.4.20: Test Condition updated<br>Parameter P_9.4.22: Max. Value improved<br>Parameter P_9.4.24: Min. Value improved<br>Parameter P_9.4.26: Min. Value improved<br>Parameter P_9.4.28: Min. Value improved<br>Parameter P_9.4.30: Min. Value improved<br>Parameter P_9.4.32: Min. Value improved<br>Parameter P_9.4.34: Test Condition updated and Max. Value improved<br>**Chapter 9.5**: Content improved<br>**Figure 33**: Content updated<br>**Figure 34**: Content updated<br>**Chapter 9.6**: Content improved<br>**Chapter 9.6.3** added<br>**Chapter 9.7**: Content improved<br>**Chapter 9.7.8**: Descriptions improved and Footnote added<br>Chapter 9.8 removed. Redundant information<br>**Figure 35**: Content updated<br>**Table 15** updated |
| BTS54040-LBA | Parameter P_5.3.26: Max. Value improved<br>Parameter P_5.3.27: Max. Value improved<br>Parameter P_6.6.26: Max. Value improved<br>**Table 10** split into different tables<br>**Table 10** to **Table 11**: Unit of $k_{ILIS}$ updated<br>Parameter P_8.5.95: Max. Value improved<br>Parameter P_8.5.96: Max. Value improved |
| **Rev. 1.0, 2013-03-24** | |
| All | Data Sheet released |

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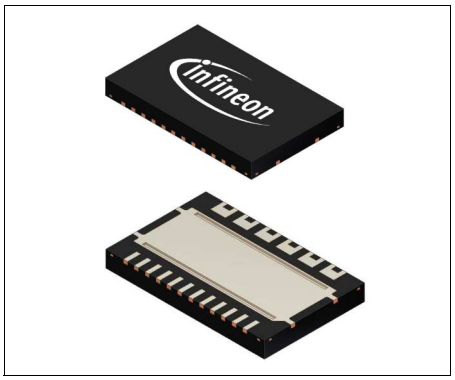
# 1 Overview



TSON-24-8

### Features

- 8-bit serial peripheral interface (daisy chain capable SPI) for control and diagnosis
- CMOS compatible parallel input pins for four channels
- Selectable AND- / OR-combination for parallel inputs (PWM control)
- Load type configuration via SPI (bulbs or LEDs) for optimized load control
- Very low stand-by current
- Device ground independent from load ground
- Green Product (RoHS-Compliant)
- AEC Qualified

### Description

The BTS54040-LBA is a four channel high-side smart power switch in TSON-24-8 package providing embedded protective functions. It is specially designed to control standard exterior lighting in automotive applications. In order to use the same hardware, the device can be configured to bulb or LED mode. As a result, both load types are optimized in terms of switching and diagnosis behavior.

It is designed to drive exterior lamps up to 27 W or the equivalent LED light.

**Table 1 Product Summary**

| | | |
|---|---|---|
| Operating Voltage Power Switch | $V_S$ | 5.5 … 28 V |
| Logic Supply Voltage | $V_{DD}$ | 3.8 … 5.5 V |
| Over Voltage Protection | $V_{S(AZ,min)}$ | 42 V |
| Maximum Stand-By Current at 25 °C | $I_{VS(STB)}$ | 1 µA |
| Maximum ON State Resistance at $T_j$ = 150 °C<br>39 mΩ channels (Channel 1, 2, 3, 4) | $R_{DS(ON,max)}$ | 78 mΩ |
| SPI Access Frequency | $f_{SCLK(max)}$ | 3 MHz |

Configuration and status diagnosis are done via SPI. An 8-bit serial peripheral interface (SPI) is used. The SPI is daisy chain capable.

| Type | Package | Marking |
|---|---|---|
| BTS54040-LBA | TSON-24-8 | BTS54040-LBA |

The device provides a current sense signal per channel that is multiplexed to the diagnosis pin IS. It can be enabled and disabled via SPI commands. An over temperature flag per output is provided in the SPI diagnosis word. A multiplexed switch bypass monitor provides short-circuit to $V_S$ diagnosis.

39 mΩ channels can be configured to bulb or LED mode for maximum flexibility.

The BTS54040-LBA provides a fail-safe feature via a Limp Home Input (LHI) pin and direct Input pins.

The power transistors are built by N-channel vertical power MOSFETs with charge pumps. The device is monolithically integrated in SMART technology.

### Applications

- High-side power switch for 12 V in automotive or industrial applications such as lighting, heating, motor driving, energy and power distribution
- Especially designed for standard exterior lighting like position light, tail light, brake light, parking light, license plate light, indicators and equivalent in the LED technology
- Replaces electromechanical relays, fuses and discrete circuits

### Protective Functions

- Reverse battery protection with external components
- Short circuit to ground protection
- Stable behavior at under voltage
- Current limitation
- Absolute and dynamic temperature sensor
- Thermal shutdown with latch after a limited amount of retries
- Overvoltage protection
- Loss of ground protection
- Electrostatic discharge protection (ESD)

### Diagnostic Functions

- Multiplexed proportional load current sense signal (IS)
- Enable function for current sense signal configurable via SPI
- High accuracy of current sense signal at wide load current range
- Current sense ratio ($k_{ILIS}$) configurable for LEDs or bulbs
- Very fast diagnosis in LED mode
- Feedback on over temperature via SPI
- Short circuit to $V_S$ detection
- Monitoring of Input pins status

### Application Specific Functions

- Fail-safe activation via LHI pin and control via input pins
- Enhanced electromagnetic compatibility (EMC) for bulbs as well as LEDs
- LED mode selection available
- SPI with daisy chain capability
- Switch bypass monitoring for detecting short circuit to $V_S$

# 2 Block Diagram

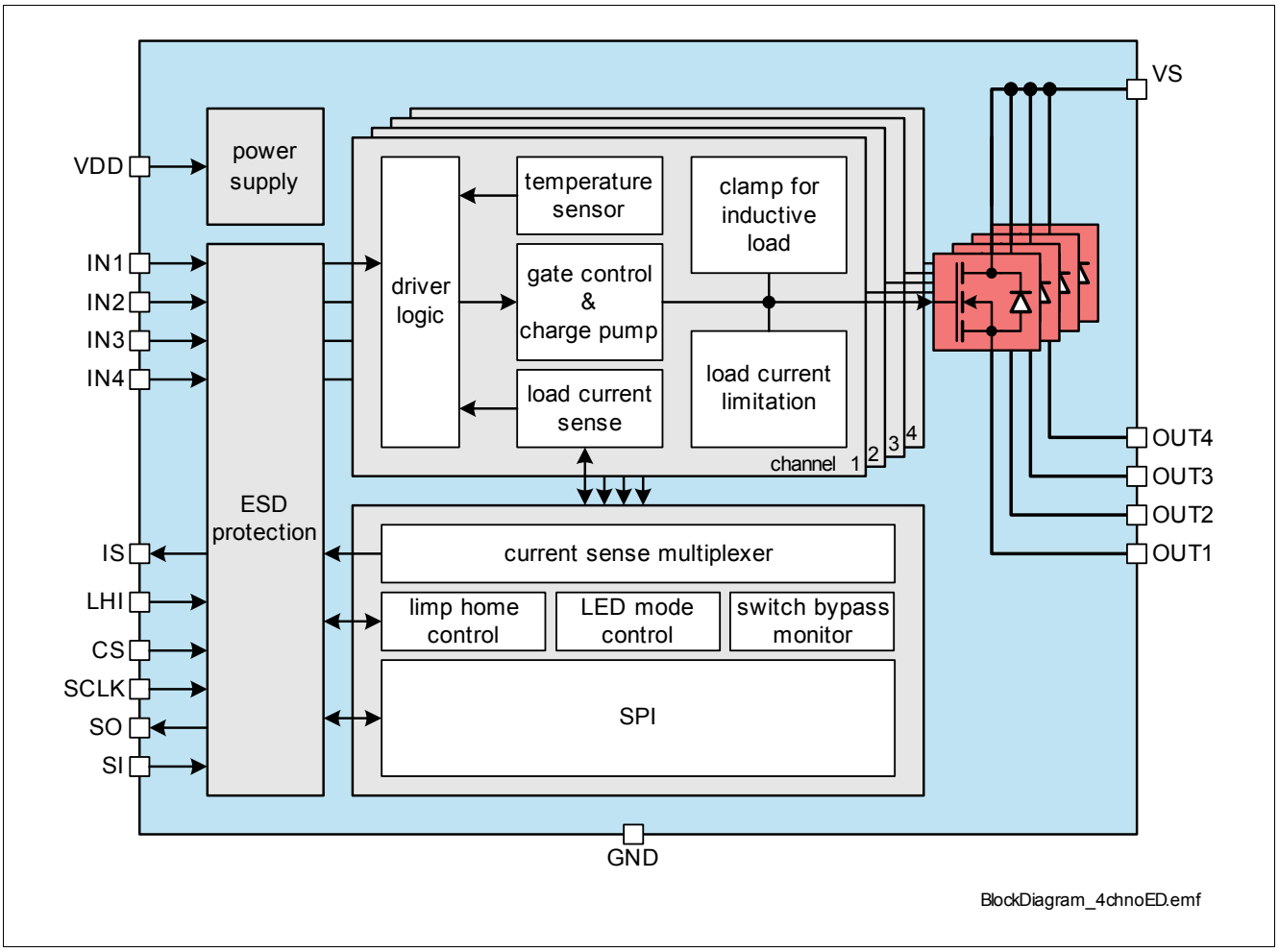



**Figure 1 Block Diagram BTS54040-LBA**

## 2.1 Terms

Figure 2 shows all terms used in this data sheet, with associated convention for positive values.

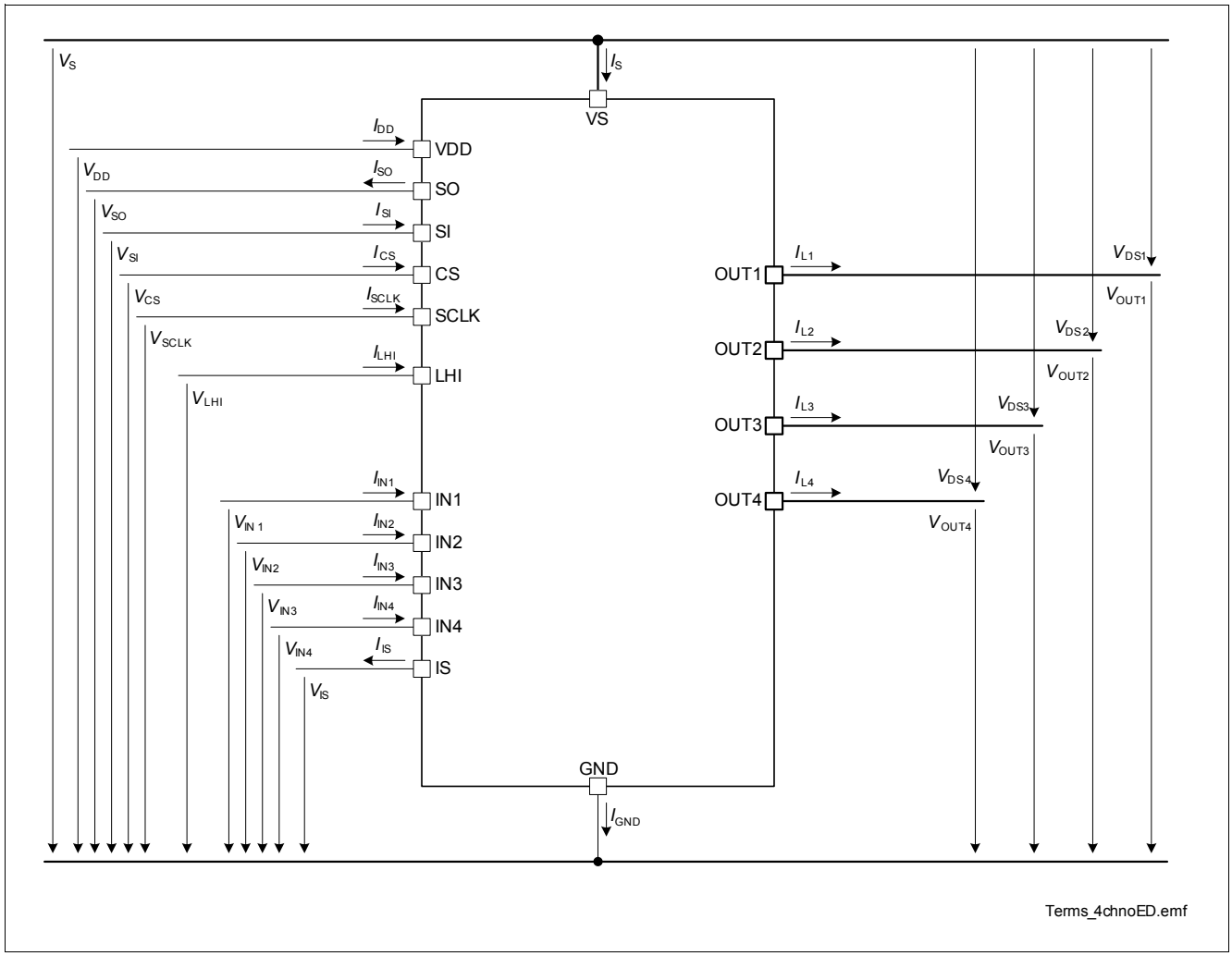



**Figure 2 Voltage and Current Definition**

In all tables of electrical characteristics, symbols related to channels without channel number are valid for each channel separately (e.g. $V_{DS}$ specification is valid for $V_{DS1}$ ... $V_{DS4}$).

All SPI register bits are marked as follows: `ADDR.PARAMETER` (e.g. **`HWCR.STB`**) with the exception of the bits in the Diagnosis frames which are marked only with `PARAMETER` (e.g. **`VSMON`**).

# 3 Pin Configuration

## 3.1 Pin Assignment BTS54040-LBA

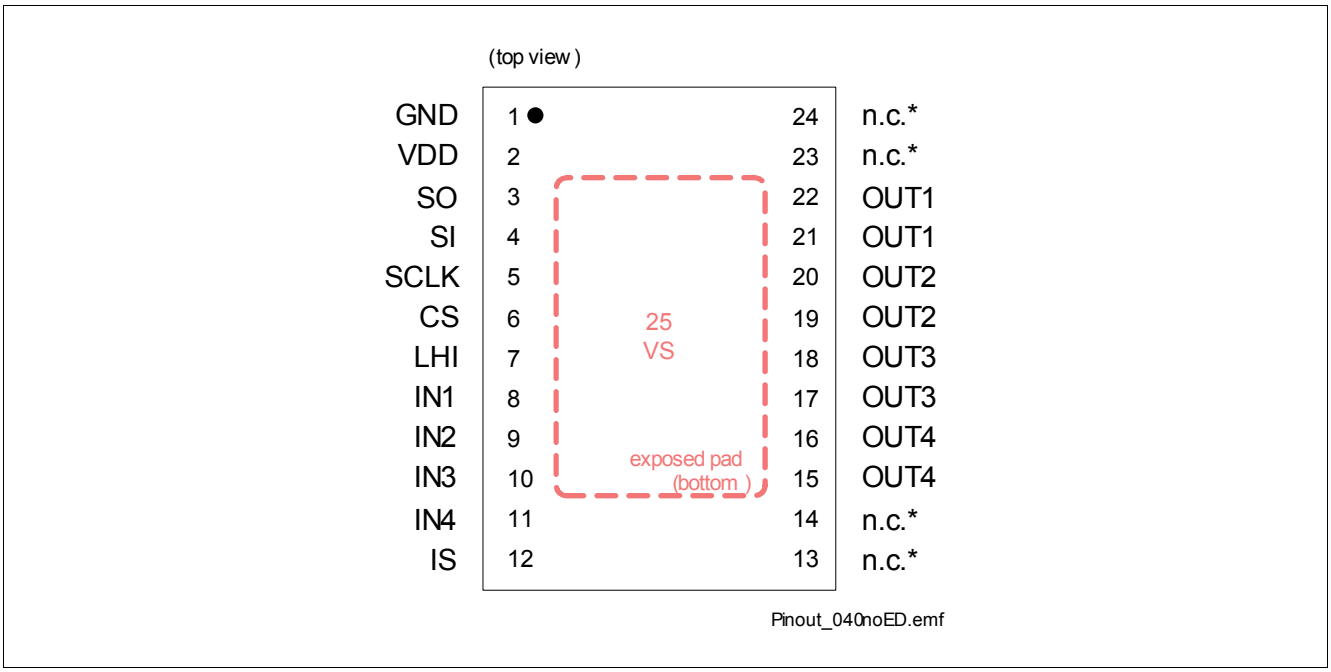



**Figure 3 Pin Configuration TSON-24-8**

## 3.2 Pin Definitions and Functions

| Pin | Symbol | I/O | Function |
|---|---|---|---|
| **Power Supply Pins** | | | |
| 25 | VS | – | Positive power supply for high-side power switch |
| 1 | GND | – | Ground connection |
| 2 | VDD | – | Logic supply (5 V) |
| **SPI & Diagnosis Pins** | | | |
| 3 | SO | O | Serial output of SPI interface |
| 4 | SI | I | Serial input of SPI interface (“high” active) |
| 5 | SCLK | I | Serial clock of SPI interface (“high” active) |
| 6 | CS | I | Chip select of SPI interface (“low” active); Integrated pull up to VDD |
| 12 | IS | O | Current sense output signal |
| **Limp Home Input Pin (integrated pull-down, leave unused Limp Home Input pin unconnected)** | | | |
| 7 | LHI | I | Limp home activation signal (“high” active) |
| **Parallel Input Pins (integrated pull-down, leave unused pins unconnected)** | | | |
| 8 | IN1 | I | Input signal of channel 1 (“high” active) |
| 9 | IN2 | I | Input signal of channel 2 (“high” active) |
| 10 | IN3 | I | Input signal of channel 3 (“high” active) |
| 11 | IN4 | I | Input signal of channel 4 (“high” active) |
| **Power Output Pins** | | | |
| 21, 22 [1)] | OUT1 | O | Protected high-side power output of channel 1 |
| 19, 20 [1)] | OUT2 | O | Protected high-side power output of channel 2 |
| 17, 18 [1)] | OUT3 | O | Protected high-side power output of channel 3 |
| 15, 16 [1)] | OUT4 | O | Protected high-side power output of channel 4 |
| **Not connected Pins** | | | |
| 13, 14 | n.c.* | – | Not connected, internally not bonded, shorted together |
| 23, 24 | n.c.* | – | Not connected, internally not bonded, shorted together |

1) All outputs pins of each channel must be connected together on the PCB. All pins of an output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

# 4 Electrical Characteristics

## 4.1 Absolute Maximum Ratings

$T_j$ = -40 to +150 °C; all voltages with respect to ground

Typical resistive loads connected to the outputs (unless otherwise specified):

39 mΩ channels: $R_L$ = 6.8 Ω (33 Ω when `LGCR.LEDn` = “1”)

**Table 2 Absolute Maximum Ratings[1)]**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Supply Voltage** | | | | | | | |
| Power supply voltage | $V_S$ | -0.3 | | 28 | V | – | P_4.1.1 |
| Logic supply voltage | $V_{DD}$ | -0.3 | | 5.5 | V | – | P_4.1.2 |
| Reverse polarity voltage | $-V_{S(rev)}$ | – | | 16 | V | 2)<br>$T_{jStart}$ = 25 °C<br>$t$ ≤ 2 min.<br>See **Chapter 10** for setup | P_4.1.3 |
| Supply voltage for short circuit protection (single pulse) | $V_{S(SC)}$ | 0 | | 28 | V | 3)<br>$R_{ECU}$ = 20 mΩ<br>$l$ = 0 or 5 m<br>$R_{Cable}$ = 16 mΩ/m<br>$L_{Cable}$ = 1 µH/m | P_4.1.5 |
| Permanent short circuit number channel activations<br>All channels | $n_{RSC1}$ | - | | 100 | k | 3)<br>$V_{DD}$ = 5 V<br>$t_{ON}$ = 300 ms | P_4.1.6 |
| Voltage at power transistor | $V_{DS}$ | – | | 42 | V | – | P_4.1.8 |
| Supply voltage for load dump protection | $V_{S(LD)}$ | – | | 42 | V | 4)<br>$R_I$ = 2 Ω<br>$t$ = 400 ms | P_4.1.9 |
| Current through ground pin | $I_{GND}$ | -100 | | 25 | mA | $t$ ≤ 2 min. | P_4.1.10 |
| Current through VDD pin | $I_{DD}$ | -25 | | 30 | mA | $t$ ≤ 2 min. | P_4.1.11 |
| **Power Stages** | | | | | | | |
| Load current | $\|I_L\|$ | – | | $I_{L(LIM)}$ | A | 5) | P_4.1.12 |
| Maximum energy dissipation single pulse -<br>39 mΩ ch. | $E_{AS}$ | – | | 45 | mJ | 6)<br>$T_{j(0)}$ = 150 °C<br>$I_{L(0)}$ = $I_{L(nom)}$ = P_6.6.17 | P_4.1.15 |
| **Diagnosis Pin** | | | | | | | |
| Voltage at sense pin IS | $V_{IS}$ | -0.3 | | $V_S$ | V | – | P_4.1.24 |
| Current through sense pin IS | $I_{IS}$ | -10 | | 40 | mA | $t$ ≤ 2 min. | P_4.1.25 |
| **Input Pins** | | | | | | | |

**Table 2 Absolute Maximum Ratings[1)]** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Voltage at input pins | $V_{IN}$ | -0.3 | | 6.0 | V | – | P_4.1.26 |
| Current through input pins | $I_{IN}$ | -0.75 | | 0.75 | mA | – | P_4.1.27 |
| Current through input pins | $I_{IN}$ | -2.0 | | 10 | mA | $t \leq 2$ min. | P_4.1.28 |
| **SPI Pins** | | | | | | | |
| Voltage at chip select pin | $V_{CS}$ | -0.3 | | 6.0 | V | – | P_4.1.29 |
| Current through chip select pin | $I_{CS}$ | -0.75 | | 0.75 | mA | – | P_4.1.30 |
| Current through chip select pin | $I_{CS}$ | -2.0 | | 10 | mA | $t \leq 2$ min. | P_4.1.31 |
| Voltage at serial input pin | $V_{SI}$ | -0.3 | | 6.0 | V | – | P_4.1.32 |
| Current through serial input pin | $I_{SI}$ | -0.75 | | 0.75 | mA | – | P_4.1.33 |
| Current through serial input pin | $I_{SI}$ | -2.0 | | 10 | mA | $t \leq 2$ min. | P_4.1.34 |
| Voltage at serial clock pin | $V_{SCLK}$ | -0.3 | | 6.0 | V | – | P_4.1.35 |
| Current through serial clock pin | $I_{SCLK}$ | -0.75 | | 0.75 | mA | – | P_4.1.36 |
| Current through serial clock pin | $I_{SCLK}$ | -2.0 | | 10 | mA | $t \leq 2$ min. | P_4.1.37 |
| Current through serial output pin SO | $I_{SO}$ | -0.75 | | 0.75 | mA | – | P_4.1.38 |
| Current through serial output pin SO | $I_{SO}$ | -10 | | 2.0 | mA | $t \leq 2$ min. | P_4.1.39 |
| **Limp Home Input Pin** | | | | | | | |
| Voltage at Limp Home Input pin | $V_{LHI}$ | -0.3 | | 6.0 | V | – | P_4.1.40 |
| Current through Limp Home Input pin | $I_{LHI}$ | -0.75 | | 0.75 | mA | – | P_4.1.41 |
| Current through Limp Home Input pin | $I_{LHI}$ | -2.0 | | 10 | mA | $t \leq 2$ min. | P_4.1.42 |
| **Temperatures** | | | | | | | |
| Junction temperature | $T_j$ | -40 | | 150 | °C | – | P_4.1.45 |
| Dynamic temperature increase while switching | $\Delta T_j$ | – | | 60 | K | – | P_4.1.46 |
| Storage temperature | $T_{stg}$ | -55 | | 150 | °C | – | P_4.1.47 |
| **ESD Susceptibility** | | | | | | | |
| ESD susceptibility HBM OUT pins vs. VS | $V_{ESD}$ | -4 | | 4 | kV | 7) HBM | P_4.1.48 |
| ESD susceptibility HBM all pins vs. VDD | $V_{ESD}$ | -1.5 | | 1.5 | kV | 7) HBM | P_4.1.54 |
| ESD susceptibility HBM other pins vs. GND incl. OUT pins vs. GND | $V_{ESD}$ | -2 | | 2 | kV | 7) HBM | P_4.1.49 |
| ESD Resistivity to GND | $V_{ESD}$ | -500 | | 500 | V | 8) CDM | P_4.1.51 |
| ESD Resistivity Pin 1, 12, 13, 24 (corner pins) to GND | $V_{ESD1, 12, 13, 24}$ | -750 | | 750 | V | 8) CDM | P_4.1.52 |

1) Not subject to production test, specified by design.

2) Device is mounted on an FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; The product (chip and package) was simulated on a 76.4 * 114.3 * 1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

3) EOL tests according to AECQ100-012. Threshold limit for short circuit failures: 100 ppm. Please refer to the legal disclaimer for short-circuit capability at the end of this document.
4) $R_I$ is the internal resistance of the load dump pulse generator.
5) Current limitation is a protection feature. Protection features are not designed for continuous repetitive operation.
6) Pulse shape represents inductive switch OFF: $I_{D(t)} = I_D(0) \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$
7) ESD resistivity, HBM according to ANSI/ESDA/JEDEC JS-001-2010
8) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1

**Notes**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

**Table 3 Thermal Resistance**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to Soldering Point | $R_{thJSP}$ | – | 2 | – | K/W | 1) $T_{j(0)}$ = 105 °C measured to pin 25 | P_4.2.1 |
| Junction to Ambient | $R_{thJA}$ | – | 21 | – | K/W | 1)2) $T_{j(0)}$ = 105 °C | P_4.2.2 |

1) Not subject to production test, specified by design.

2) Specified $R_{thJA}$ values is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip and package) was simulated on a 76.4 * 114.3 * 1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

### 4.2.1 PCB Setup

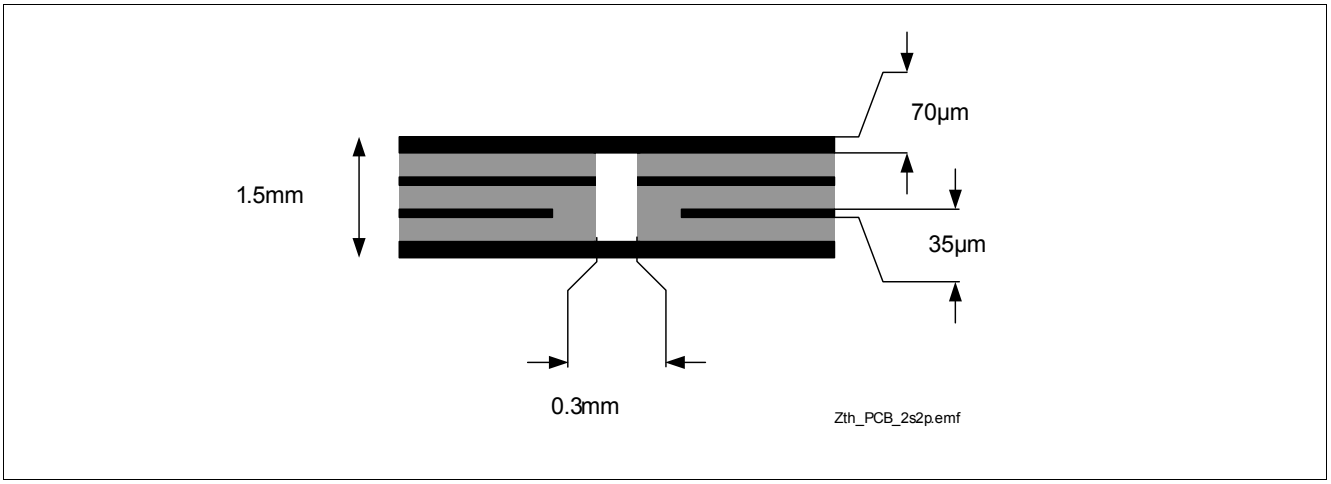



**Figure 4 2s2p PCB Cross Section**

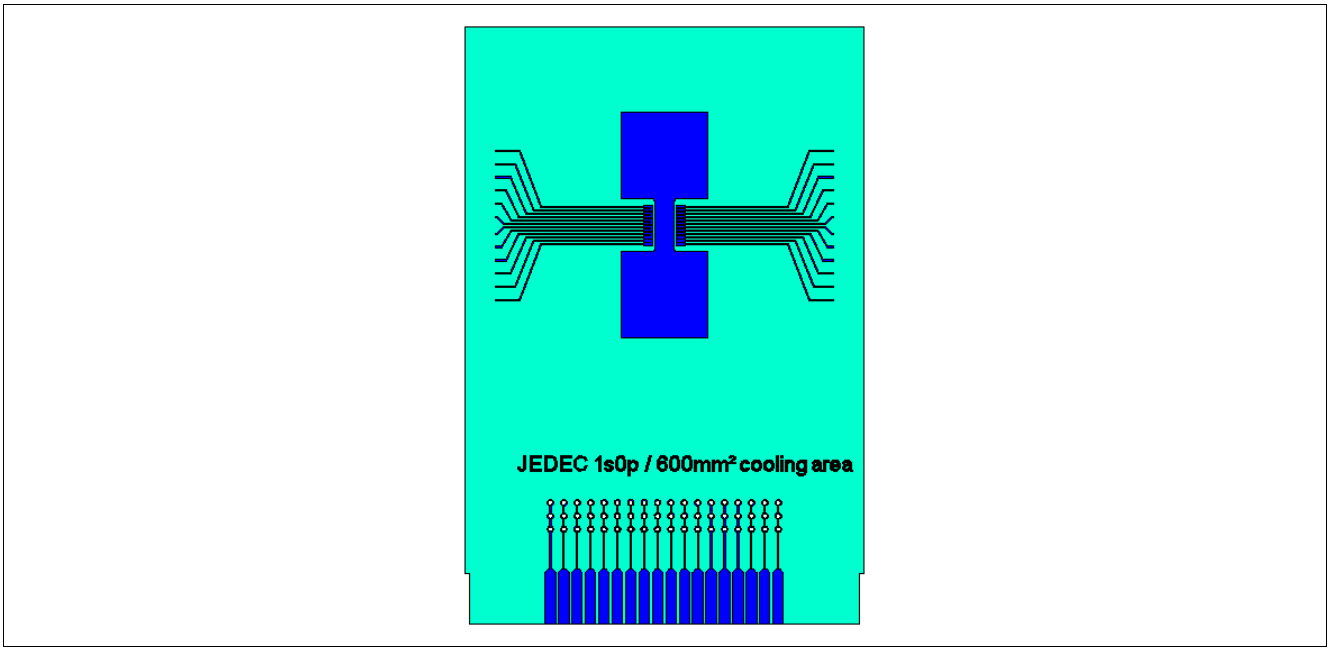



**Figure 5 PC Board for Thermal Simulation with 600 mm² Cooling Area**

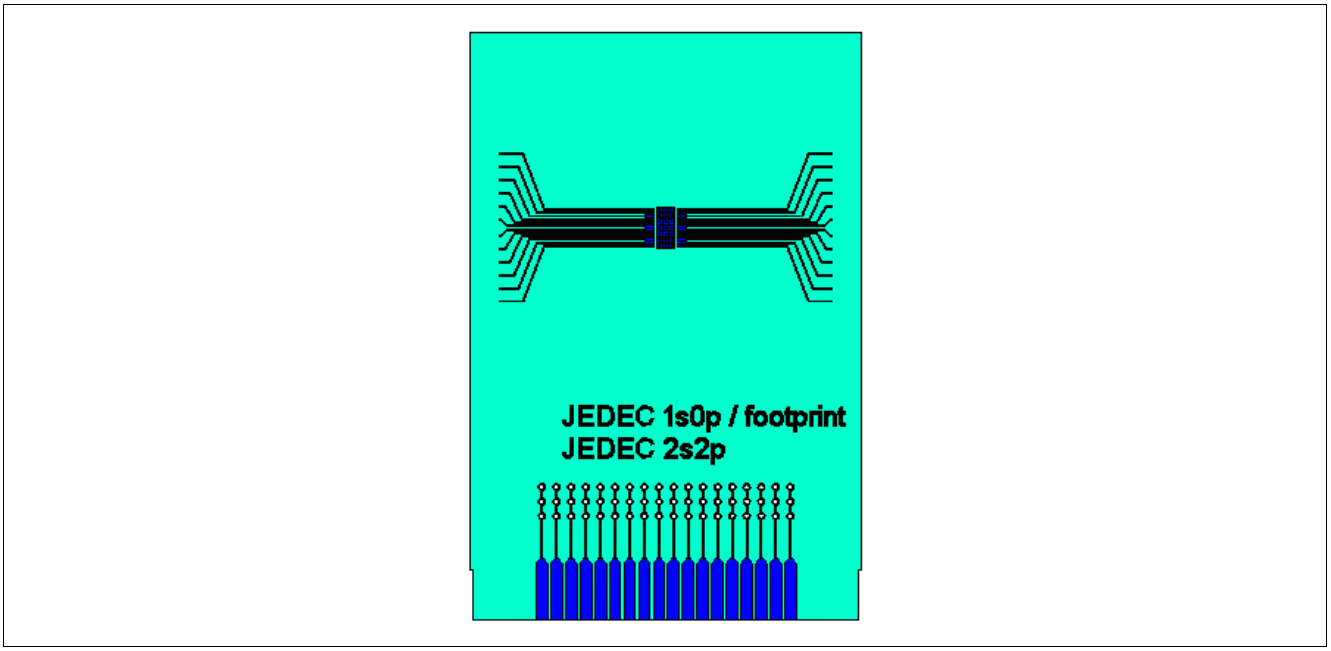



**Figure 6 PC Board for Thermal Simulation with 2s2p Cooling Area**

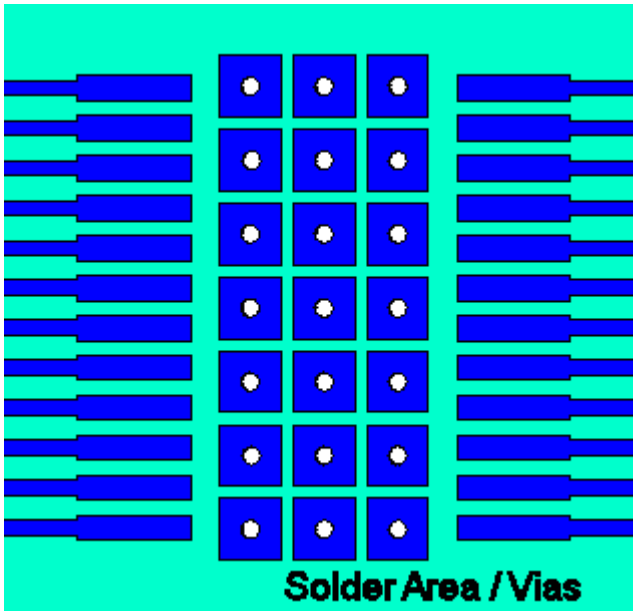



**Figure 7 Solder Area / Vias**

### 4.2.2 Thermal Impedance

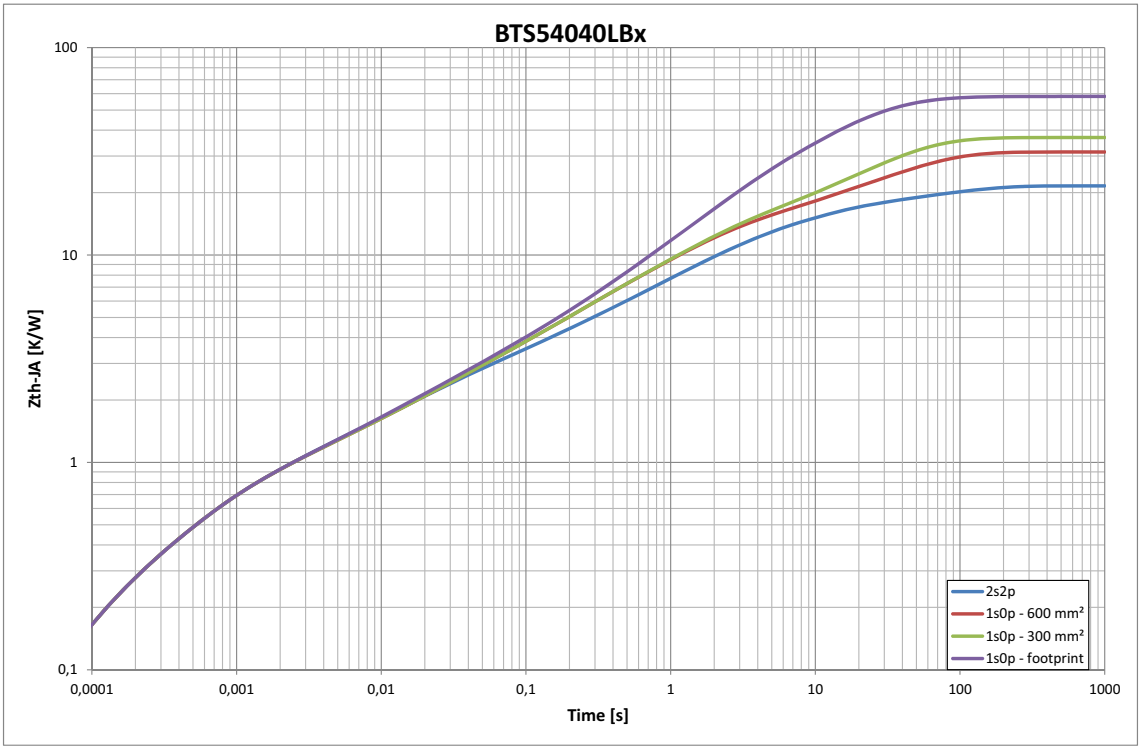



**Figure 8 Typical Thermal Impedance. PCB setup according Figure 6**

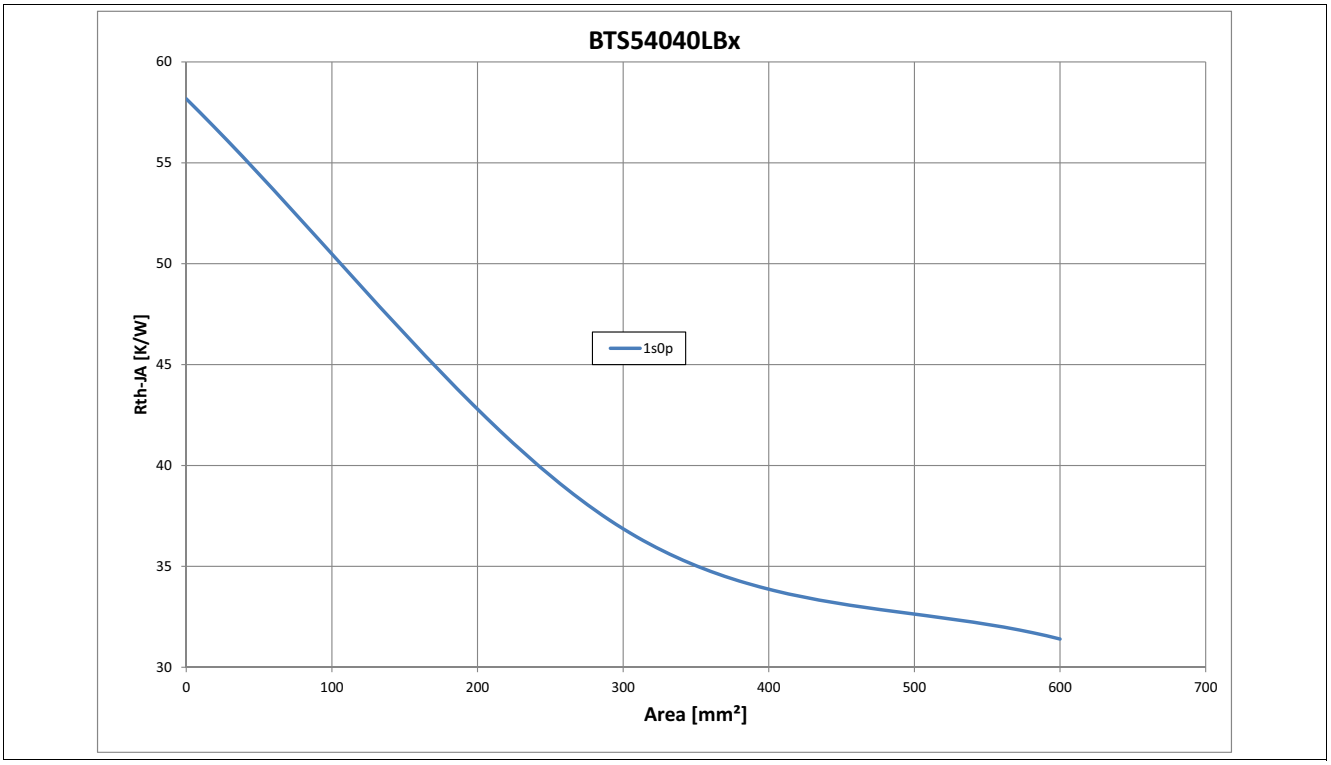



**Figure 9 Typical Thermal Resistance. PCB setup 1s0p**

# 5 Power Supply

The BTS54040-LBA is supplied by two voltage sources:

- $V_S$ (analog supply voltage)
- $V_{DD}$ (digital supply voltage)

The $V_S$ supply line is connected to a battery feed and used for the driving circuitry of the power stages, while $V_{DD}$ is used for the SPI logic and for driving SO pin.

$V_S$ and $V_{DD}$ supply voltages have an undervoltage detection circuit, which prevents the activation of the associated function in case the measured voltage is below the undervoltage threshold. More in detail:

- An undervoltage on $V_{DD}$ supply prevents SPI communication. SPI registers are reset to default values. The retry counters used to protect the channels are reset therefore the channels are in “unlimited restart” mode.
- An undervoltage on $V_S$ supply switches OFF all channels, even in Limp Home mode. The channels are enabled again as soon as $V_S = V_{S(OP)}$.

The voltage at pin VS is also monitored. In case of a negative voltage transient resulting in $V_S < V_{SMON}$ with **DCR.MUX** ≠ “$111_B$”, any SPI command sent by the micro-controller is not accepted (see **Chapter 9.5** for further details).

An overview of channel behavior according to different $V_S$ and $V_{DD}$ supply voltages is shown in **Table 4** (the table is valid after a successful supply voltage ramp-up).

**Table 4 Device capability as function of $V_S$ and $V_{DD}$**

| | $V_{DD} \le V_{DD(PO)}$ ($V_{DD(PO)}$ = P_5.3.17) | $V_{DD} > V_{DD(PO)}$ |
|---|---|---|
| $V_S \le V_{SMON}$ ($V_{SMON}$ = P_5.3.12) | Channels are OFF | Channels are OFF |
| | SPI registers reset | SPI registers protected[1] |
| | SPI communication not available ($f_{SCLK}$ = 0 MHz) | SPI communication available[2] ($f_{SCLK}$ = 3 MHz) |
| | Limp Home mode not available | Limp Home mode not available |
| $V_{SMON} < V_S \le V_{S(UV)}$ ($V_{S(UV)}$ = P_5.3.2) | Channels are OFF | Channels are OFF |
| | SPI registers reset | SPI registers available |
| | SPI communication not available ($f_{SCLK}$ = 0 MHz) | SPI communication available ($f_{SCLK}$ = 3 MHz) |
| | Limp Home mode available (channels are OFF) | Limp Home mode available (channels are OFF) |
| $V_S > V_{S(UV)}$[3] | Channels cannot be controlled by SPI | Channels can be switched ON and OFF |
| | SPI registers reset | SPI registers available |
| | SPI communication not available ($f_{SCLK}$ = 0 MHz) | SPI communication available ($f_{SCLK}$ = 3 MHz) |
| | Limp Home mode available | Limp Home mode available |

1) If **DCR.MUX** ≠ $111_B$, otherwise SPI registers are available.
2) SPI response depends on **DCR.MUX** value. See **Chapter 9.5** for further details.
3) The undervoltage condition on $V_S$ supply must be considered. See **Chapter 5.2.1** for further details.

## 5.1 Operation modes

BTS54040-LBA has the following operation modes:

- Stand-by mode
- Idle mode
- Ready mode
- Operative mode
- Limp Home mode

The transition between operation modes is determined according to these variables:

- logic level at LHI pin
- logic level at INn pins
- **DCR.MUX** bits state
- **OUT.OUTn** bits state

The state diagram including the possible transitions is shown in **Figure 10**. The behavior of BTS54040-LBA as well as some parameters may change in dependence from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors $V_S$ and $V_{DD}$ supply voltages, some changes within the same operation mode can be seen accordingly.

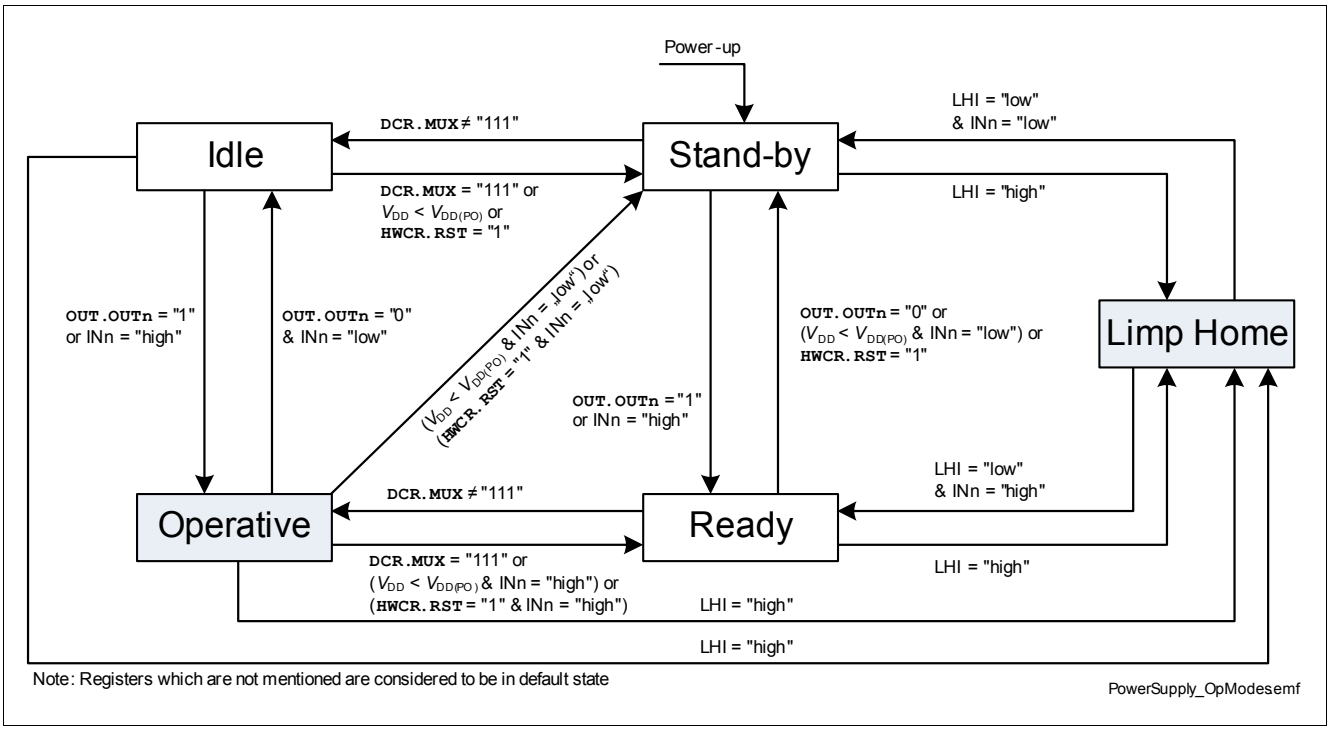



**Figure 10 Operation Mode state diagram**

There are three parameters describing the behavior of BTS54040-LBA:

- status of output channels
- status of SPI registers
- status of SPI communication

It is necessary to set **DCR.MUX** to a value different from $111_B$ to command a switch ON of one or more channels. In alternative it is necessary to set the LHI to “high” - in this case the logic state of the Input pins is reflected to the outputs (if there is no undervoltage condition on $V_S$ supply).

Table 5 shows the correlation between device operation modes, $V_S$ and $V_{DD}$ supply voltages, and the state of the most important functions (channel status, SPI communication and SPI registers).

**Table 5 Device function in relation to operation modes, $V_S$ and $V_{DD}$ voltages**

| Operation Mode | Function | $V_S \leq V_{SMON}$ | $V_{SMON} > V_S \leq V_{S(UV)}$ | $V_S > V_{S(UV)}$ |
|---|---|---|---|---|
| Stand-by | Channels | OFF | OFF | OFF |
| | SPI comm. | available[1)] | available[1)] | available[1)] |
| | SPI registers | available[1)] | available[1)] | available[1)] |
| Idle | Channels | OFF | OFF | OFF |
| | SPI comm. | all commands rejected[1)] | available[1)] | available[1)] |
| | SPI registers | available[1)] | available[1)] | available[1)] |
| Ready | Channels | OFF | OFF | OFF |
| | SPI comm. | available[1)] | available[1)] | available[1)] |
| | SPI registers | available[1)] | available[1)] | available[1)] |
| Operative | Channels | OFF | OFF | follow `OUT.OUTn` and/or Input pins |
| | SPI comm. | all commands rejected[1)] | available[1)] | available[1)] |
| | SPI registers | available[1)] | available[1)] | available[1)] |
| Limp Home | Channels | OFF | OFF | follow Input pins |
| | SPI comm. | available (read-only)[1)2)] | available (read-only)[1)2)] | available (read-only)[1)2)] |
| | SPI registers | reset | reset | reset |

1) If $V_{DD} > V_{DD(PO)}$, otherwise not available or in reset.

2) `HWCR.CTC` and `HWCR.RST` commands are accepted.

### 5.1.1 Power-up

The Power-up condition is entered when one of the supply voltages ($V_S$ or $V_{DD}$) is applied to the device. Both supplies are rising until they are above the undervoltage thresholds $V_{S(OP)}$ and $V_{DD(PO)}$ therefore the internal power-on signals are set.

### 5.1.2 Stand-by mode

When BTS54040-LBA is in Stand-by mode, all outputs are OFF. The SPI registers can be programmed if $V_{DD} > V_{DD(PO)}$. The current consumption is minimum (see parameter $I_{VS(STB)}$). The circuitry that monitors $V_S$ versus the threshold $V_{SMON}$ is disabled, allowing the programming of the registers. Even if one Input pin is set to “high” or if one `OUT.OUTn` bit is set to “1”, all outputs stay switched OFF.

### 5.1.3 Idle mode

In Idle mode, the internal supply circuitry is working and the device current consumption is increased. All channels are OFF and a command to switch ON one or more outputs (either via SPI or via Input pins) is accepted and executed, bringing the device into Operative mode.